BT258-500R

Logic level thyristor

Rev.03 - 26 August 2022

Product data sheet

1. General description

Passivated, sensitive gate thyristors in a plastic envelope, intended for use in general purpose switching and phase control applications. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

2. Features and benefits

- Sensitive gate
- Planar passivated for voltage ruggedness and reliability
- Direct triggering from low power drivers and logic ICs
- Surface mountable package

3. Applications

- General purpose switching and phase control
- Ignition circuits, CDI for 2- and 3-wheelers
- Motor control - e.g. small kitchen appliances

4. Quick reference data

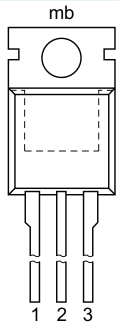
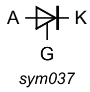
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage			-	-	500	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_{mb} \leq 111$ °C; Fig. 1		-	-	5	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{mb} \leq 111$ °C; Fig. 2; Fig. 3		-	-	8	A
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(init)} = 25$ °C; $t_p = 10$ ms; Fig. 4; Fig. 5		-	-	75	A
		half sine wave; $T_{j(init)} = 25$ °C; $t_p = 8.3$ ms		-	-	82	A
T_j	junction temperature		[1]	-	-	125	°C
Static characteristics							
I_{GT}	gate trigger current	$V_D = 12$ V; $I_T = 0.1$ A; $T_j = 25$ °C; Fig. 7		-	50	200	µA
Dynamic characteristics							
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 335$ V; $T_j = 125$ °C; $R_{GK} = 100$ Ω; (V_{DM} = 67% of V_{DRM}); exponential waveform; Fig. 12		50	100	-	V/µs

[1] Operation above 110°C may require the use of a gate to cathode resistor of 1kΩ or less.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K	cathode		
2	A	anode		
3	G	gate		
mb	A	mounting base; connected to anode		

6. Ordering information

Table 3. Ordering information

Type number	Package name	Orderable part number	Packing method	Small packing quantity	Package version	Package issue date
BT258-500R	TO220	BT258-500R,127	Tube	50	SOT78	13-Jun-2008

7. Marking

Table 4. Marking codes

Type number	Marking codes	
	Assembly factory: d	Assembly factory: A
BT258-500R	BT258 500R PJdxxxx xx	BT258 500R PJAxxxx xx

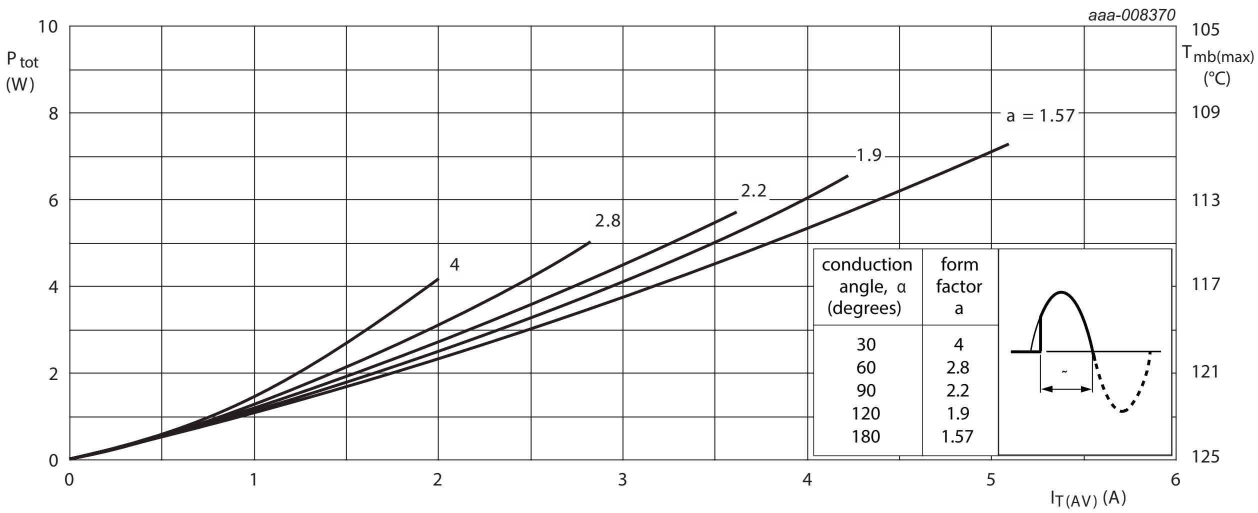
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage			-	500	V
V_{RRM}	repetitive peak reverse voltage			-	500	V
$I_{T(AV)}$	average on-state current	half sine wave; T_{mb} ≤ 111 °C; Fig. 1		-	5	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; T_{mb} ≤ 111 °C; Fig. 2; Fig. 3		-	8	A
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(init)}$ = 25 °C; t_p = 10 ms; Fig. 4; Fig. 5		-	75	A
		half sine wave; $T_{j(init)}$ = 25 °C; t_p = 8.3 ms		-	82	A
I^2t	I^2t for fusing	t_p = 10 ms; SIN		-	28	A^2s
dI_T/dt	rate of rise of on-state current	I_T = 10 A; I_G = 50 mA; dI_G/dt = 50 mA/µs		-	50	A/µs
I_{GM}	peak gate current			-	2	A
V_{RGM}	peak reverse gate voltage			-	5	V
P_{GM}	peak gate power			-	5	W
$P_{G(AV)}$	average gate power	over any 20 ms period		-	0.5	W
T_{stg}	storage temperature			-40	150	°C
T_j	junction temperature		[1]	-	125	°C

[1] Operation above 110°C may require the use of a gate to cathode resistor of 1kΩ or less.



α = conduction angle

a = form factor = $I_{T(RMS)}$ / $I_{T(AV)}$

Fig. 1. Total power dissipation as a function of average on-state current; maximum values

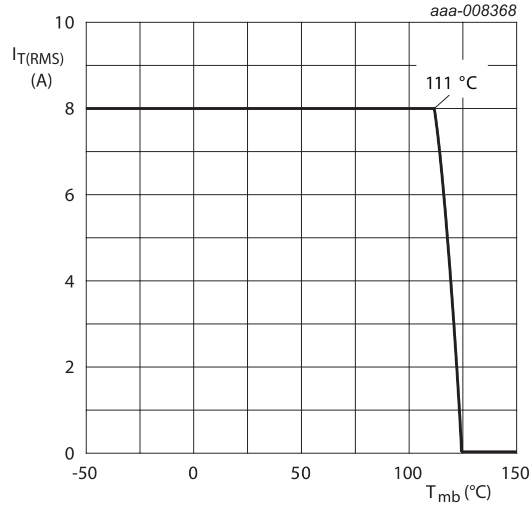
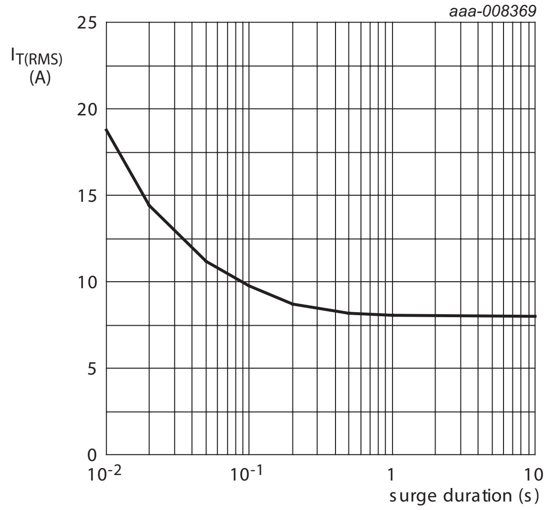
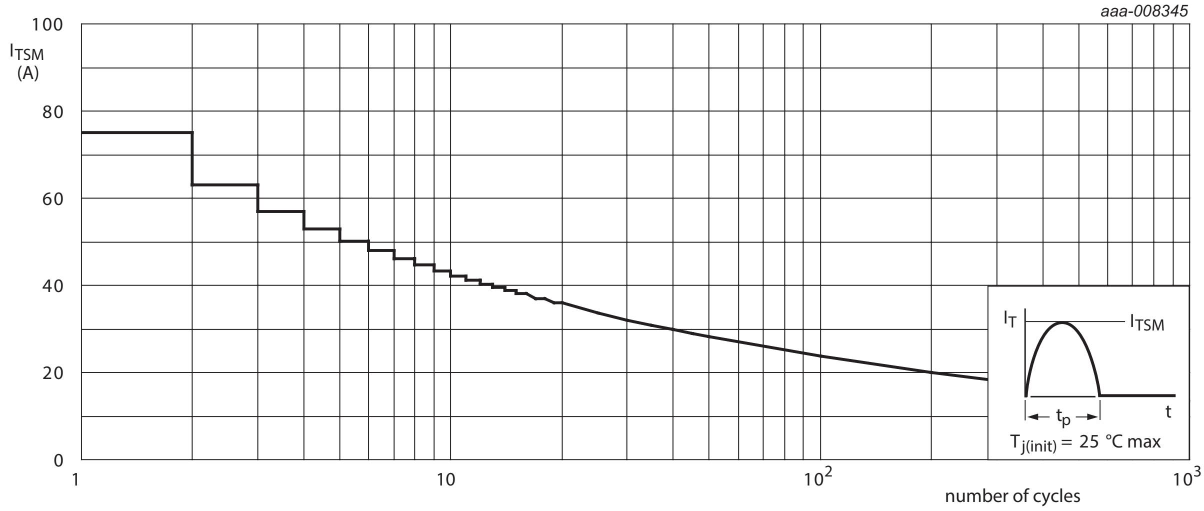


Fig. 2. RMS on-state current as a function of mounting base temperature; maximum values



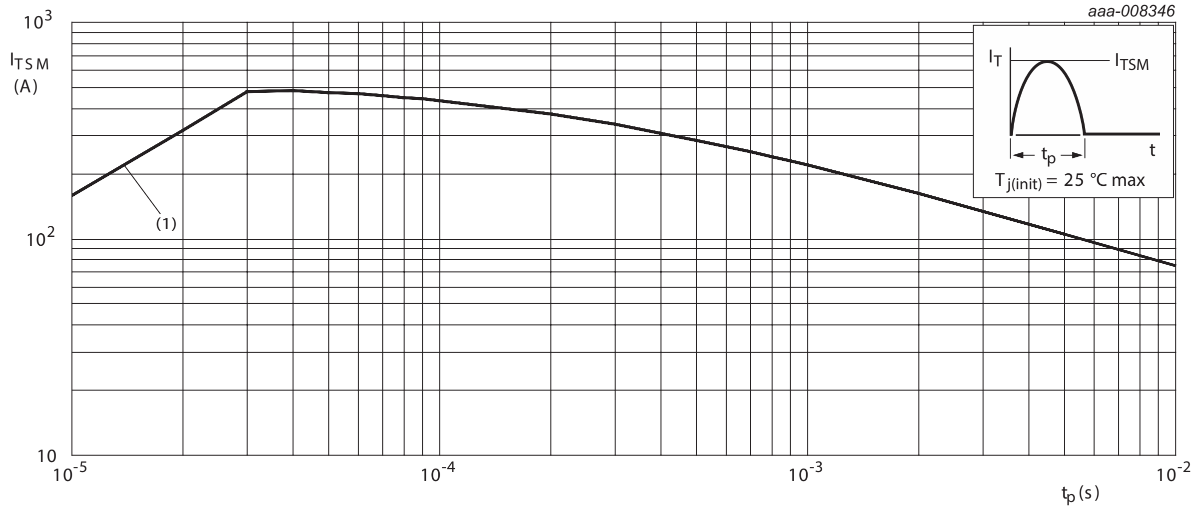
f = 50 Hz; T_{mb} = 111 °C

Fig. 3. RMS on-state current as a function of surge duration; maximum values



f = 50 Hz

Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



$t_p \leq 10$ ms

(1) dI_T/dt limit

Fig. 5. Non-repetitive peak on-state current as a function of pulse width for sinusoidal currents; maximum values

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 6		-	-	2	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient free air	in free air		-	60	-	K/W

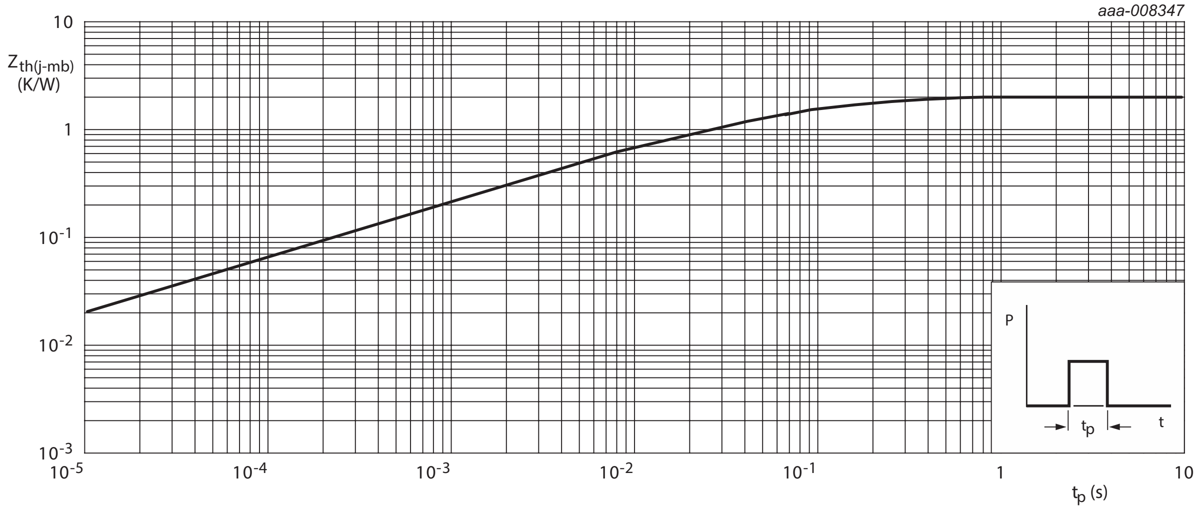


Fig. 6. Transient thermal impedance from junction to mounting base as a function of pulse width

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I_{GT}	gate trigger current	V_D = 12 V; I_T = 0.1 A; T_j = 25 °C; Fig. 7		-	50	200	µA
I_L	latching current	V_D = 12 V; I_G = 0.1 A; T_j = 25 °C; Fig. 8		-	0.4	10	mA
I_H	holding current	V_D = 12 V; T_j = 25 °C; Fig. 9		-	0.4	6	mA
V_T	on-state voltage	I_T = 16 A; T_j = 25 °C; Fig. 10		-	1.3	1.6	V
V_{GT}	gate trigger voltage	V_D = 12 V; I_T = 0.1 A;T_j = 25 °C; Fig. 11		-	0.4	1	V
		V_D = 500V; I_T = 0.1 A;T_j = 110 °C		0.1	0.2	-	V
I_D	off-state current	V_D = 500 V; T_j = 125 °C		-	0.1	0.5	mA
I_R	reverse current	V_R = 500 V; T_j = 125 °C		-	0.1	0.5	mA
Dynamic characteristics							
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 335 V; T_j = 125 °C; R_{GK} = 100 Ω; (V_{DM} = 67% of V_{DRM}); exponential waveform; Fig. 12		50	100	-	V/µs
t_{gt}	gate-controlled turn-on time	I_{TM} = 10 A; V_D = 500 V; I_G = 5 mA; dI_G/dt = 0.2 A/µs; T_j = 25 °C		-	2	-	µs
t_q	commutated turn-off time	V_{DM} = 335 V; T_j = 125 °C; I_{TM} = 12 A; V_R = 24 V; $(dI_T/dt)_M$ = 10 A/µs; dV_D/dt = 2 V/µs; $R_{GK(ext)}$ = 1 kΩ; (V_{DM} = 67% of V_{DRM})		-	100	-	µs

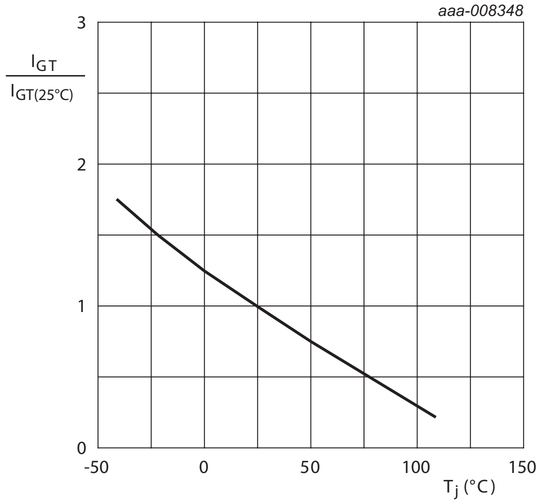


Fig. 7. Normalized gate trigger current as a function of junction temperature

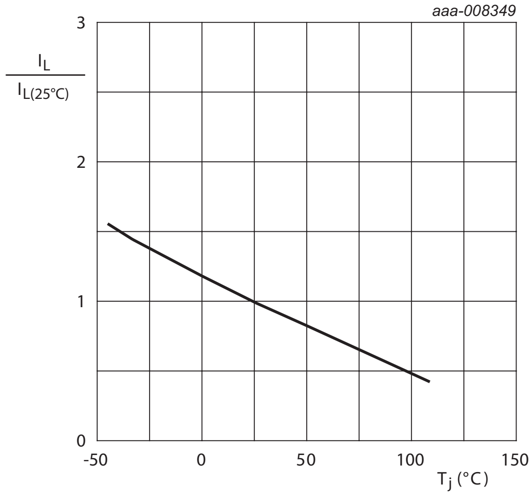


Fig. 8. Normalized latching current as a function of junction temperature

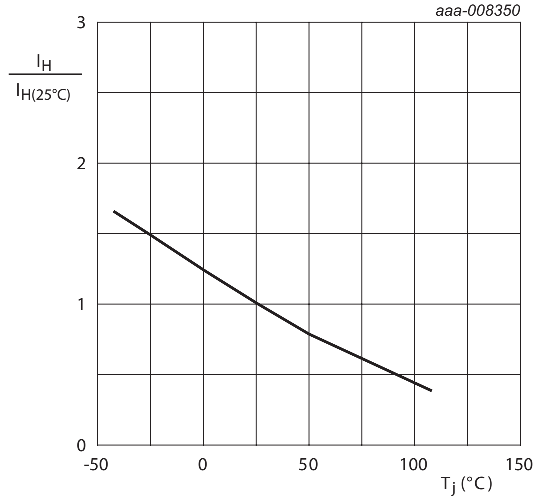
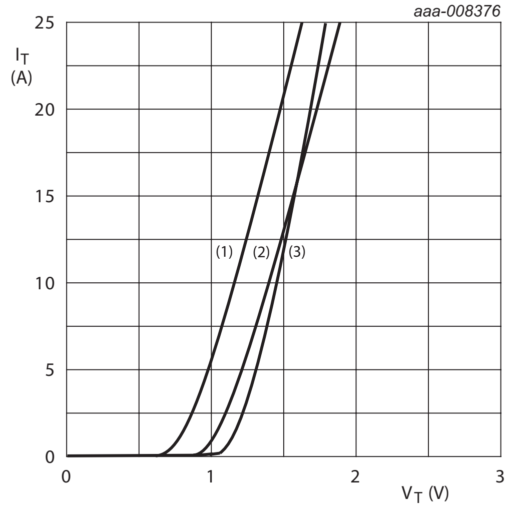


Fig. 9. Normalized holding current as a function of junction temperature



V_0 = 1.0 V; R_s = 0.04 Ω
(1) T_j = 125 °C; typical values
(2) T_j = 125 °C; maximum values
(3) T_j = 25 °C; maximum values

Fig. 10. On-state current as a function of on-state voltage

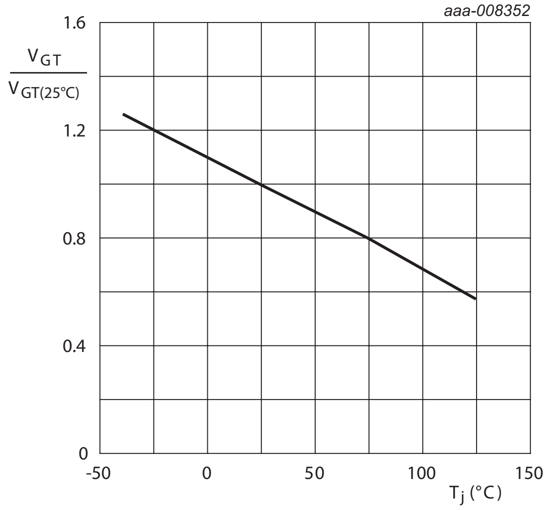
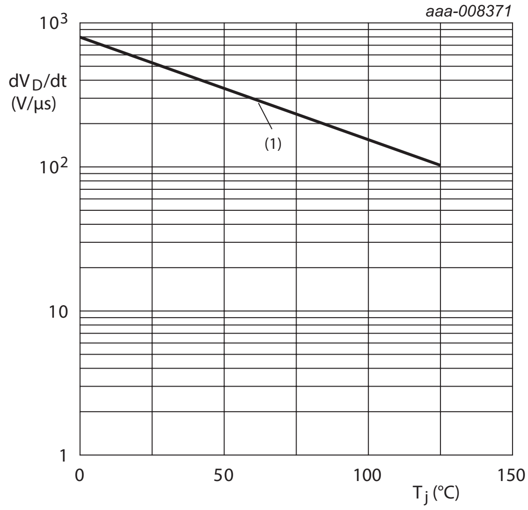


Fig. 11. Normalized gate trigger voltage as a function of junction temperature



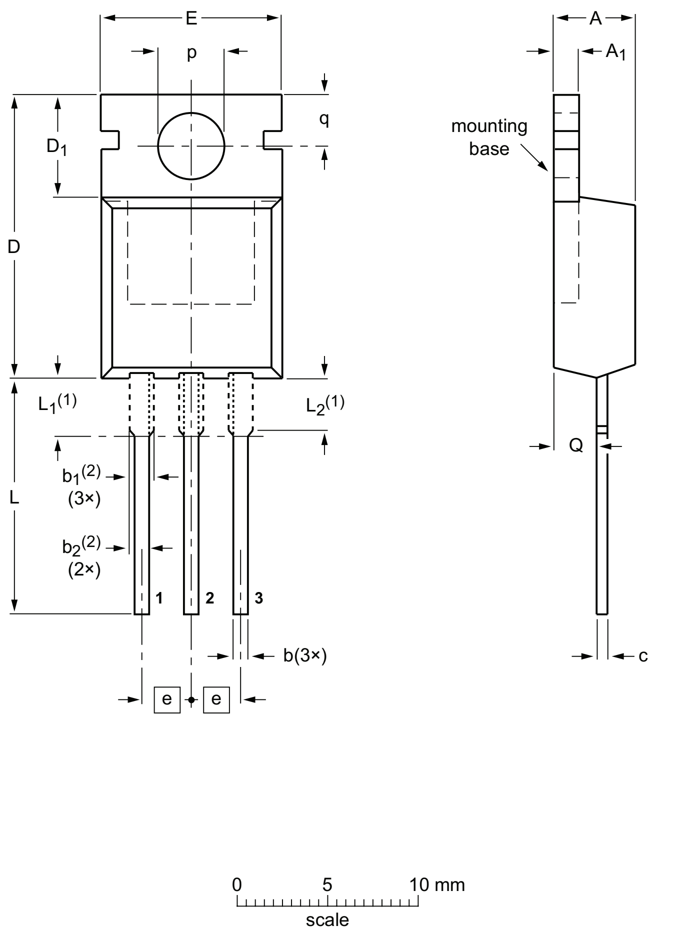
(1) R_{GK} = 100 Ω

Fig. 12. Critical rate of rise of off-state voltage as a function of junction temperature; typical values

11. Package outline

Assembly factory: d & A

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB **SOT78**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	b_1(2)	b_2(2)	c	D	D_1	E	e	L	L_1(1)	L_2(1) max.	p	q	Q
mm	4.7 4.1	1.40 1.25	0.9 0.6	1.6 1.0	1.3 1.0	0.7 0.4	16.0 15.2	6.6 5.9	10.3 9.7	2.54	15.0 12.8	3.30 2.79	3.0	3.8 3.5	3.0 2.7	2.6 2.2

Notes

1. Lead shoulder designs may vary.
2. Dimension includes excess dambar.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT78		3-lead TO-220AB	SC-46			~~08-04-23~~ 08-06-13

12. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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