ACTT4X-800C

AC Thyristor Triac power switch

Rev.03 - 25 September 2024 — Product data sheet

1. General description

Planar passivated AC Thyristor Triac power switch in a TO220F "full pack" plastic package with self-protective capabilities against low and high energy transients.

2. Features and benefits

- Clamping structure ensuring safe high over-voltage withstand capability
- Direct interfacing with low power drivers and microcontrollers
- Full cycle AC conduction
- Isolated mounting base package
- Less sensitive gate for high noise immunity
- Over-voltage withstand capability to IEC 61000-4-5
- Pin compatible with standard triacs
- Planar passivated for voltage ruggedness and reliability
- Safe clamping capability for low energy over-voltage transients
- Self-protective turn-on during high energy voltage transients
- Triggering in three quadrants only
- Very high immunity to false turn-on by dV/dt

3. Applications

- AC fan, pump and compressor controls
- Highly inductive, resistive and safety loads
- Large and small appliances (White Goods)
- Reversing induction motor controls

4. Quick reference data

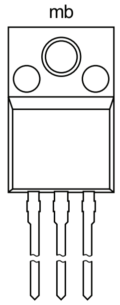
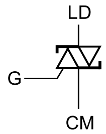
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage			-	-	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_h \leq 94$ °C; Fig. 1; Fig. 2; Fig. 3		-	-	4	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(init)} = 25$ °C; $t_p = 20$ ms; Fig. 4; Fig. 5		-	-	35	A
		full sine wave; $T_{j(init)} = 25$ °C; $t_p = 16.7$ ms		-	-	39	A
T_j	junction temperature			-	-	125	°C
V_{PP}	peak pulse voltage	$T_j = 25$ °C; non-repetitive, off-state; Fig. 6		-	-	2	kV
Static characteristics							
I_{GT}	gate trigger current	$V_D = 12$ V; $I_T = 100$ mA; LD+ G+; $T_j = 25$ °C; Fig. 8		-	-	35	mA
		$V_D = 12$ V; $I_T = 100$ mA; LD+ G-; $T_j = 25$ °C; Fig. 8		-	-	35	mA
		$V_D = 12$ V; $I_T = 100$ mA; LD- G-; $T_j = 25$ °C; Fig. 8		-	-	35	mA
I_H	holding current	$V_D = 12$ V; $T_j = 25$ °C; Fig. 10		-	-	35	mA
V_T	on-state voltage	$I_T = 6$ A; $T_j = 25$ °C; Fig. 11		-	-	1.7	V
V_{CL}	clamping voltage	$I_{CL} = 0.1$ mA; $t_p = 1$ ms; $T_j = 25$ °C		850	-	-	V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Dynamic characteristics							
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 536 V; T_j = 125 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit; Fig. 13		1000	-	-	V/µs
dI_{com}/dt	rate of change of commutating current	V_D = 400 V; T_j = 125 °C; $I_{T(RMS)}$ = 4 A; dV_{com}/dt = 20 V/µs; (snubberless condition); gate open circuit; Fig. 14; Fig. 15		8	-	-	A/ms
		V_D = 400 V; T_j = 125 °C; $I_{T(RMS)}$ = 4 A; dV_{com}/dt = 10 V/µs; gate open circuit; Fig. 14; Fig. 15		10	-	-	A/ms
		V_D = 400 V; T_j = 125 °C; $I_{T(RMS)}$ = 4 A; dV_{com}/dt = 1 V/µs; gate open circuit; Fig. 14; Fig. 15		15	-	-	A/ms

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	CM	common		 003aaf296
2	LD	load		
3	G	gate		
mb	n.c.	mounting base; isolated		

6. Ordering information

Table 3. Ordering information

Type number	Package Name	Orderable part number	Packing method	Small packing quantity	Package version	Package issue date
ACTT4X-800C	TO220F	ACTT4X-800C,127	Tube	50	SOT186A	14-Nov-2013
ACTT4X-800C/DG		ACTT4X-800C/DGQ	Tube	50	SOT186A (Halogen free)	14-Nov-2013

7. Marking

Table 4. Marking codes

Type number	Marking codes	
	Assembly factory: d	Assembly factory: A
ACTT4X-800C	ACTT4X 800C PJdxxxx xx	ACTT4X 800C PJAxxxx xx
ACTT4X-800C/DG	ACTT4X 800CDG PJdxxxx xx	ACTT4X 800CDG PJAxxxx xx

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage			-	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_h \leq 94$ °C; Fig. 1; Fig. 2; Fig. 3		-	4	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(init)} = 25$ °C; $t_p = 20$ ms; Fig 4; Fig 5		-	35	A
		full sine wave; $T_{j(init)} = 25$ °C; $t_p = 16.7$ ms		-	39	A
I^2t	I^2t for fusing	$t_p = 10$ ms; sine-wave pulse		-	6	A^2s
dI_T/dt	rate of rise of on-state current	$I_G = 20$ mA		-	100	A/µs
I_{GM}	peak gate current	$t_p = 20$ µs		-	2	A
P_{GM}	peak gate power			-	5	W
$P_{G(AV)}$	average gate power	over any 20 ms period		-	0.5	W
T_j	junction temperature			-	125	°C
V_{pp}	peak pulse voltage	$T_j = 25$ °C; non-repetitive, off-state; Fig 6		-	2	kV

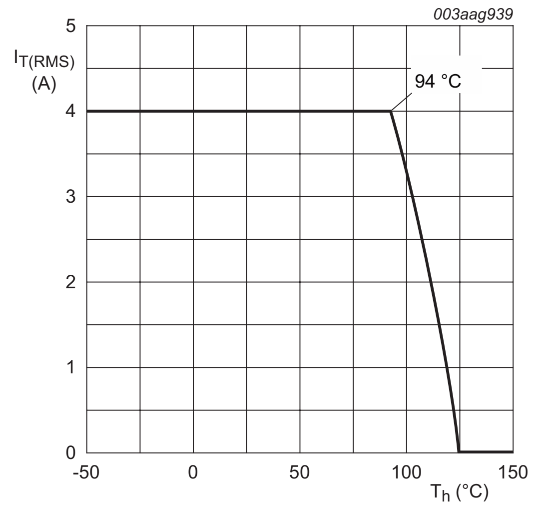
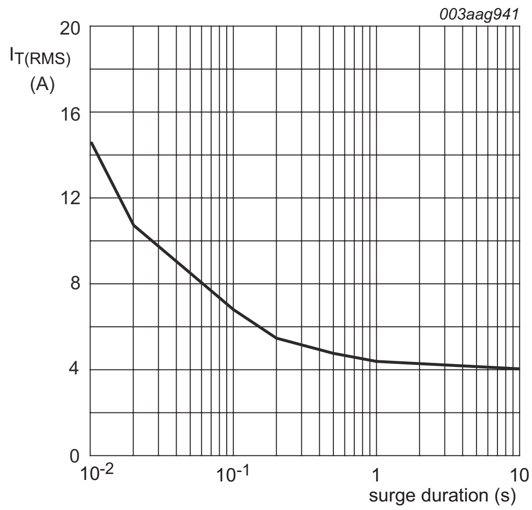
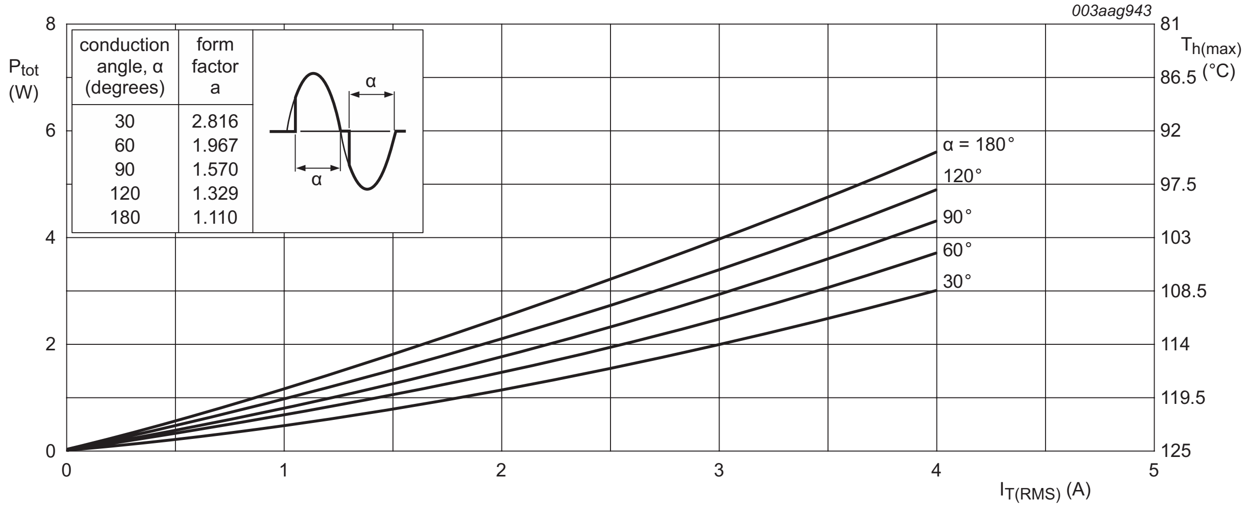


Fig. 1. RMS on-state current as a function of heatsink temperature; maximum values



f = 50 Hz; $T_h = 94$ °C

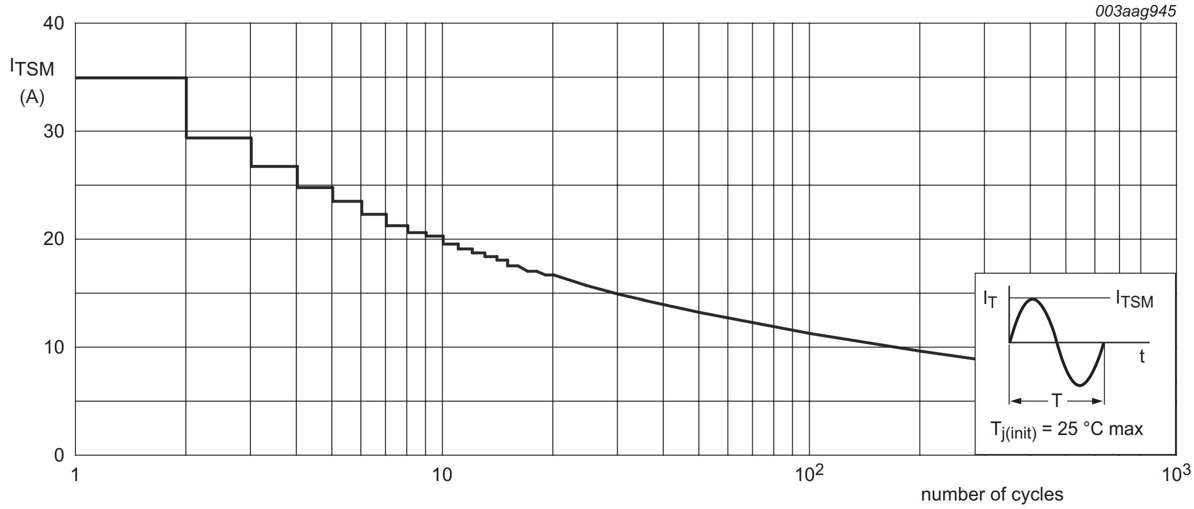
Fig. 2. RMS on-state current as a function of surge duration; maximum values



α = conduction angle

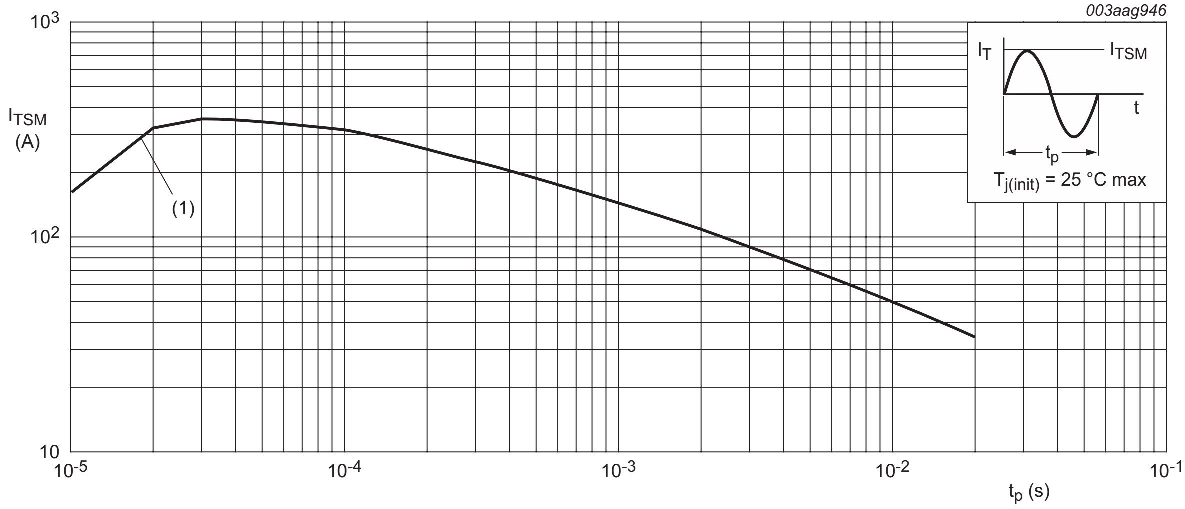
a = form factor = $I_{T(RMS)}$ / $I_{T(AV)}$

Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values



f = 50 Hz

Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



$t_p \leq 20$ ms

(1) dI_T/dt limit

Fig. 5. Non-repetitive peak on-state current as a function of pulse width; maximum values

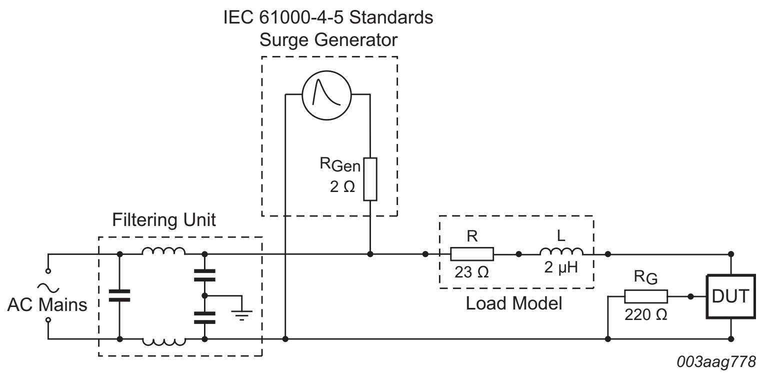
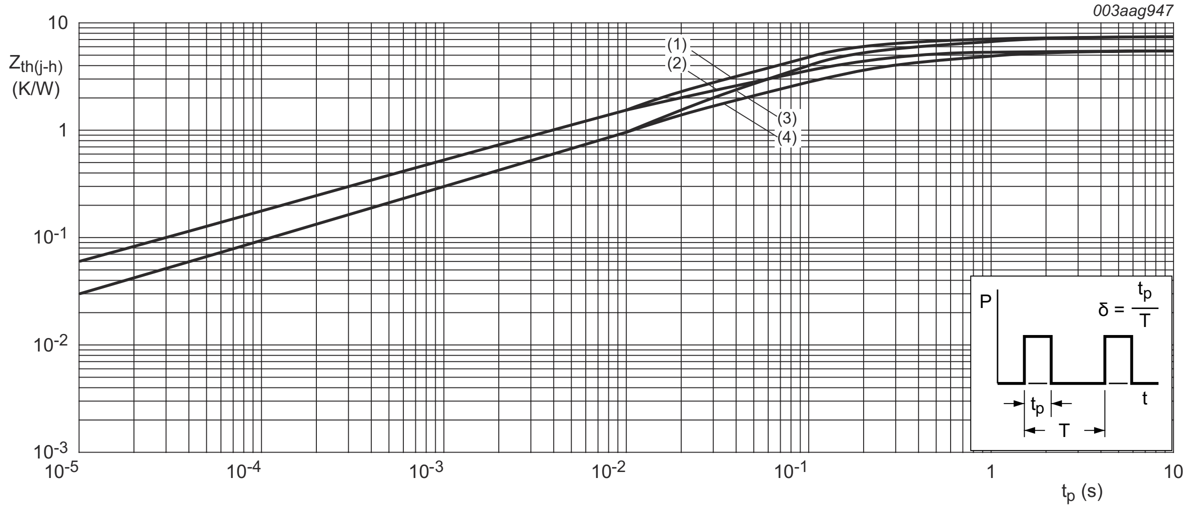


Fig. 6. Test circuit for inductive and resistive loads with conditions equivalent to IEC 61000-4-5

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-h)}$	thermal resistance from junction to heatsink	full cycle or half cycle with heatsink compound; Fig. 7		-	-	5.5	K/W
		full cycle or half cycle without heatsink compound; Fig. 7		-	-	7.2	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient free air	in free air		-	55	-	K/W



(1) Unidirectional (half cycle) without heatsink compound
(2) Unidirectional (half cycle) with heatsink compound
(3) Bidirectional (full cycle) without heatsink compound
(4) Bidirectional (full cycle) with heatsink compound

Fig. 7. Transient thermal impedance from junction to heatsink as a function of pulse width

10. Isolation characteristics

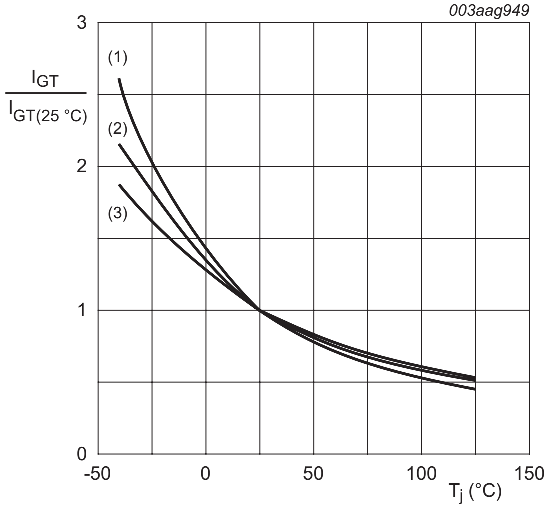
Table 7. Isolation characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{isol(RMS)}$	RMS isolation voltage	sinusoidal waveform; from all pins to external heatsink; clean and dust free; 50 Hz ≤ f ≤ 60 Hz; RH ≤ 65 %; T_h = 25 °C		-	-	2500	V
C_{isol}	isolation capacitance	from LD pin to external heatsink; f = 1 MHz; T_h = 25 °C		-	10	-	pF

11. Characteristics

Table 8. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I_{GT}	gate trigger current	V_D = 12 V; I_T = 100 mA; LD+ G+; T_j = 25 °C; Fig. 8		-	-	35	mA
		V_D = 12 V; I_T = 100 mA; LD+ G-; T_j = 25 °C; Fig. 8		-	-	35	mA
		V_D = 12 V; I_T = 100 mA; LD- G-; T_j = 25 °C; Fig. 8		-	-	35	mA
I_L	latching current	V_D = 12 V; I_G = 100 mA; LD+ G+; T_j = 25 °C; Fig. 9		-	-	50	mA
		V_D = 12 V; I_G = 100 mA; LD+ G-; T_j = 25 °C; Fig. 9		-	-	60	mA
		V_D = 12 V; I_G = 100 mA; LD- G-; T_j = 25 °C; Fig. 9		-	-	50	mA
I_H	holding current	V_D = 12 V; T_j = 25 °C; Fig. 10		-	-	35	mA
V_T	on-state voltage	I_T = 6 A; T_j = 25 °C; Fig. 11		-	-	1.7	V
V_{GT}	gate trigger voltage	V_D = 12V; I_T = 100 mA;T_j = 25 °C; Fig. 12		-	0.8	1	V
		V_D = 400V; I_T = 100 mA;T_j = 125 °C		0.2	0.45	-	V
I_D	off-state current	V_D = 800 V; T_j = 25 °C		-	-	10	µA
		V_D = 800 V; T_j = 125 °C		-	-	0.5	mA
V_{CL}	clamping voltage	I_{CL} = 0.1 mA; t_p = 1 ms; T_j = 25 °C		850	-	-	V
Dynamic characteristics							
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 536 V; T_j = 125 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit; Fig. 13		1000	-	-	V/µs
dI_{com}/dt	rate of change of commutating current	V_D = 400 V; T_j = 125 °C; $I_{T(RMS)}$ = 4 A; dV_{com}/dt = 20 V/µs; (snubberless condition); gate open circuit; Fig. 14; Fig. 15		8	-	-	A/ms
		V_D = 400 V; T_j = 125 °C; $I_{T(RMS)}$ = 4 A; dV_{com}/dt = 10 V/µs; gate open circuit; Fig. 14; Fig. 15		10	-	-	A/ms
		V_D = 400 V; T_j = 125 °C; $I_{T(RMS)}$ = 4 A; dV_{com}/dt = 1 V/µs; gate open circuit; Fig. 14; Fig. 15		15	-	-	A/ms



(1) LD- G-
(2) LD+ G+
(3) LD+ G-

Fig. 8. Normalized gate trigger current as a function of junction temperature

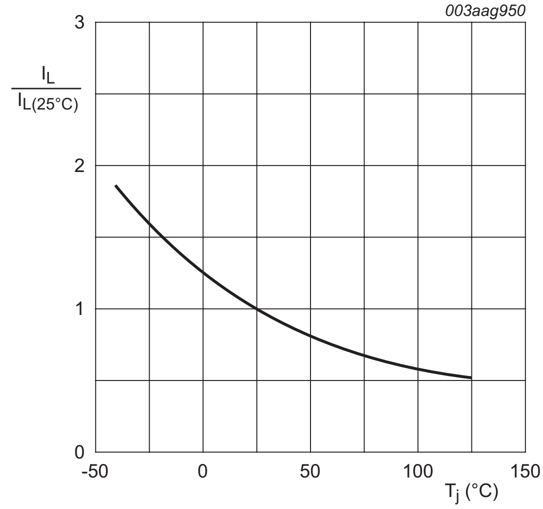


Fig. 9. Normalized latching current as a function of junction temperature

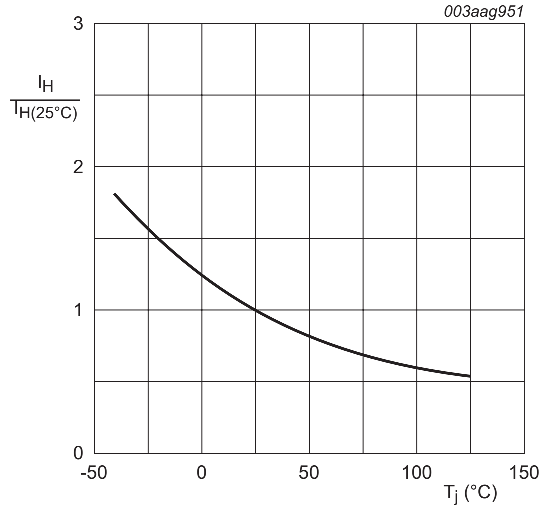
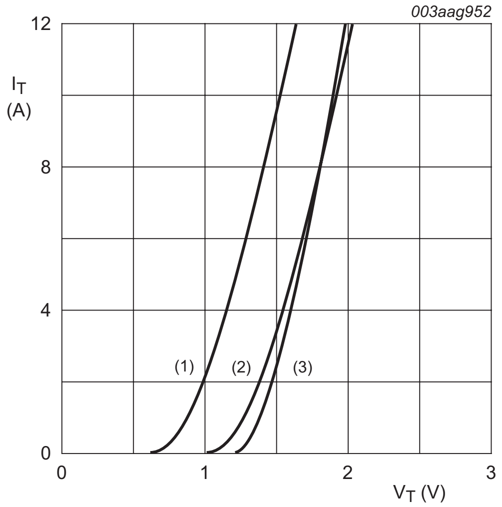


Fig. 10. Normalized holding current as a function of junction temperature



V_o = 1.242 V; R_s = 0.074 Ω
(1) T_j = 125 °C; typical values
(2) T_j = 125 °C; maximum values
(3) T_j = 25 °C; maximum values

Fig. 11. On-state current as a function of on-state voltage

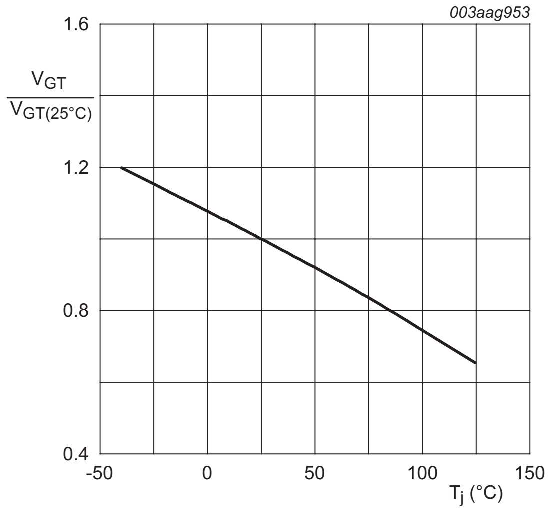
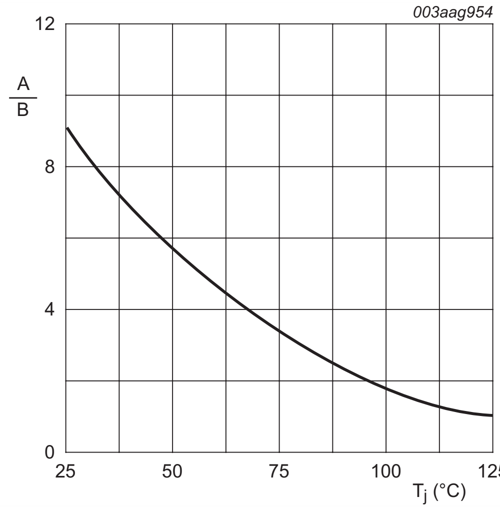
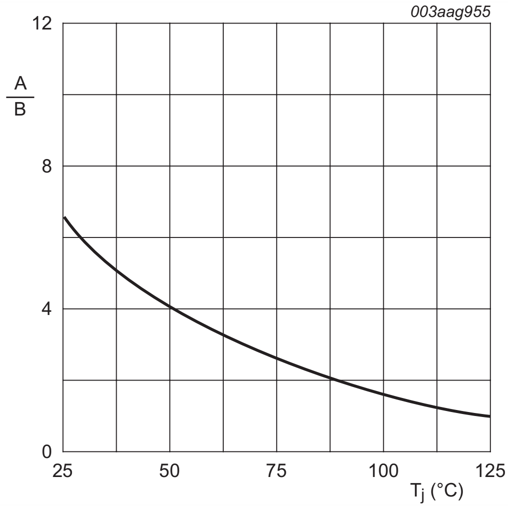


Fig. 12. Normalized gate trigger voltage as a function of junction temperature



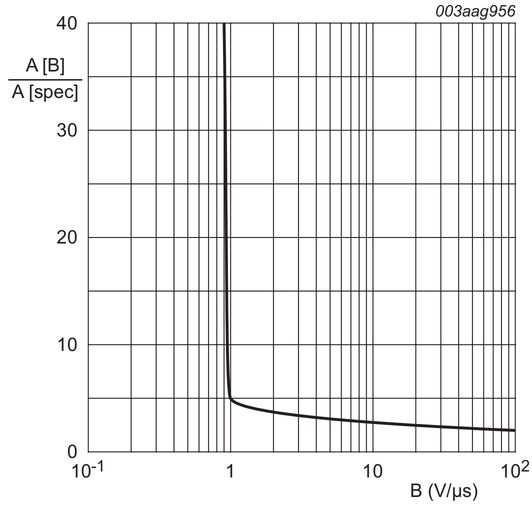
A = dV_D/dt at condition T_j °C
B = dV_D/dt at condition T_j [125] °C

Fig. 13. Normalized rate of rise of off-state voltage as a function of junction temperature



A = dI_{com}/dt at condition T_j °C
B = dI_{com}/dt at condition T_j [125] °C
V_D = 400 V

Fig. 14. Normalized critical rate of rise of commutating current as a function of junction temperature



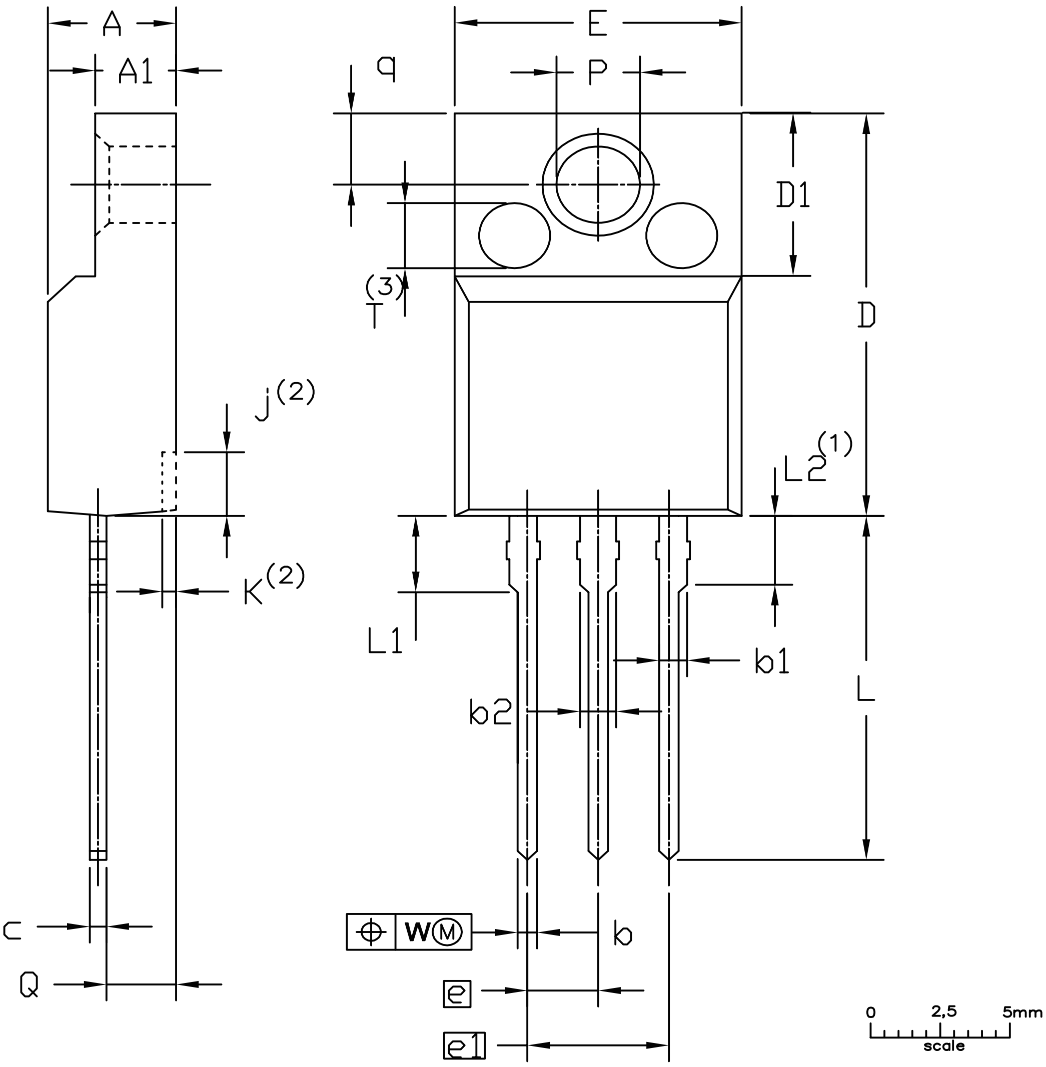
A [B] = dI_{com}/dt at condition B, dV_{com}/dt
A [spec] is the specified data sheet value for dI_{com}/dt
turn-off time < 20 ms

Fig. 15. Normalized critical rate of change of commutating current as a function of critical rate of change of commutating voltage; minimum values

12. Package outline

Assembly factory: d & A

Plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220 "full pack" SOT186A



UNIT	A	A_1	b	b_1	b_2	c	D	D_1	E	e	e_1	j(2)	K(2)	L	L_1	L_2(1) max.	P	Q	q	W	T(3)
mm	4.6	2.9	0.9	1.1	1.4	0.7	15.8	6.5	10.3	2.54	5.08	2.7	0.6	14.4	3.30	3	3.2	2.6	3.0	0.4	2.5
	4.0	2.5	0.7	0.9	1.0	0.4	15.2	6.3	9.7			1.7	0.4	13.5	2.79		3.0	2.3	2.6		

Notes
1. Terminal dimensions within this zone are uncotrolled
2. Dot lines area designs may vary
3. Eject pin mark is for reference only

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT186A		3 LEADS TO220F				2013-11-14

13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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