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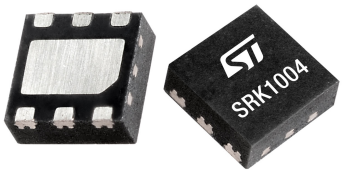
SRK1004

Datasheet

Synchronous rectifier controller for non-complementary active clamp flyback converter



DFN 6L 2x2mm

Features

- Secondary-side synchronous rectification controller optimized for Non-Complementary Actively Clamped Flyback converter (NC-ACF).
- Able to operate in both low-side and high-side configuration
- Supporting logic level (A and B) and standard level (C and D) MOSFETs
- Two different turn-off delays available to cover a wide range of MOSFETs
- Wide range supply voltage: 4 to 36 V
- Very low operating current (580 µA) and quiescent current (230 µA)
- High-voltage sensing input for SR MOSFET drain-source voltage (190 V AMR)
- Operating frequency up to 500 kHz
- Fast short-circuit detector
- Tiny DFN 6L 2x2 mm package

Applications

- High-power-density USB-PD adapters/chargers
- USB-PD wall-plugs
- In-wall smart outlets

Product status link

SRK1004

Product label

SUSTAINABLE TECHNOLOGY

Description

SRK1004 controller is intended for secondary side synchronous rectification (SR) in Non-Complementary Actively Clamped Flyback, Resonant Flyback, and Quasi-Resonant Flyback converters.

It provides a gate-drive output suitable for N-channel logic-level or standard level power MOSFETs.

The control scheme of this device is such that the SR MOSFET is switched on as soon as current starts flowing through its body diode and it is then switched off as current approaches zero.

The device can be supplied directly from the converter's output voltage when operated in low-side configuration. When used in high-side configuration, it is recommended to power the IC from a dedicated auxiliary winding.

When operated in high-side configuration, a special function enables a quick detection of short-circuit conditions to inhibit its operation as if the IC were powered directly from the output voltage.

1 Block diagrams

Figure 1. **Internal block diagram**

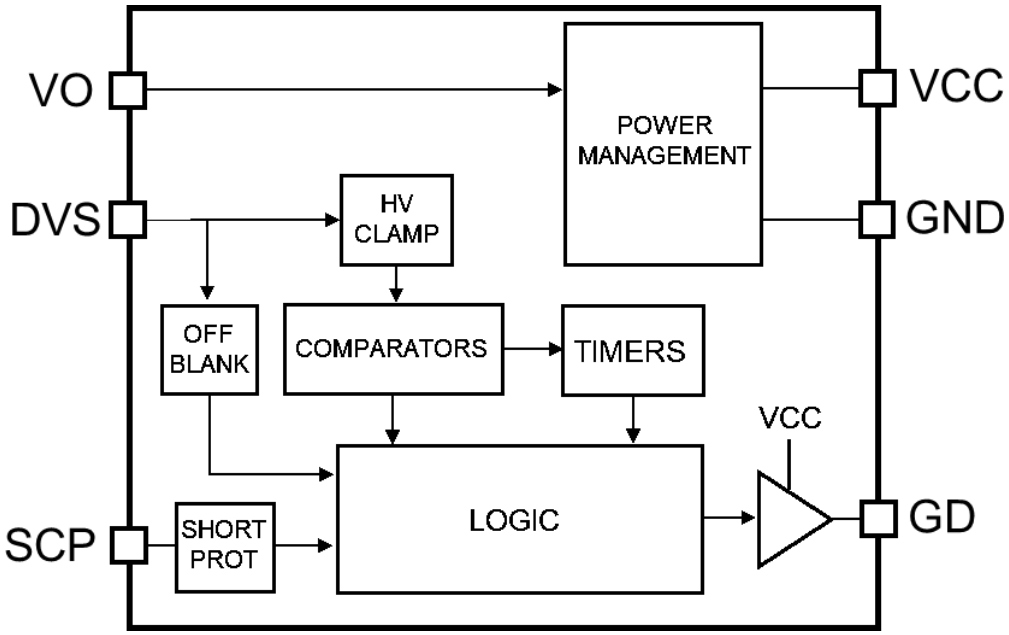


Table 1. **Device information**

Order code	VCC [V]	Typ. turn-off delay [ns]	Package marking
SRK1004ATR	5.5	25	S4A
SRK1004BTR	5.5	150	S4B
SRK1004CTR	9.0	25	S4C
SRK1004DTR	9.0	150	S4D

2 Pin connections and functions

Figure 2. **Pin connections (top view)**

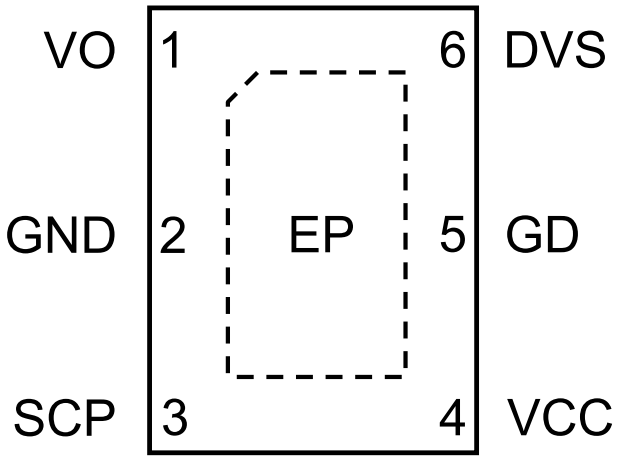


Table 2. **Pin functions**

No.	Name	Function
1	VO	Supply voltage of the device. This pin, able to accept voltages as high as 36 V, is powered directly from the converter's output voltage in case the IC is used in low-side configuration or from a floating auxiliary winding (plus a rectifying diode and a buffer capacitor) in case the IC is used in high-side configuration. Internally, this pin is the input of the linear regulator that supplies the internal circuits of the IC as well as the gate driver, and whose output is available on pin 4 (VCC)
2	GND	Return of the device bias current and return of the gate drive current. Route this pin close to the source terminal of the synchronous rectifier MOSFET
3	SCP	Short-circuit protection for HS configuration. This pin, providing a 1 V reference voltage and an external resistor connected from the pin to the secondary ground of the converter, sets the output voltage, around 3 V, below which the IC stops operating the SR MOSFET. In case of LS configuration, the protection on the SCP pin cannot be used and must be disabled. The protection can be disabled connecting a resistor of 22 kΩ to GND. In this configuration the protection is implemented through the UVLO function on the VO pin: VO < VO_{OFF} → SRK1004 is disabled
4	VCC	Internally regulated supply voltage of the device. A bypass capacitor, C_{VCC}, to GND, located as close to IC's pins as possible, helps to obtain a clean supply voltage for the internal control circuitry, and acts as an effective energy buffer for the pulsed gate drive current
5	GD	Gate driver output. The totem-pole output stage intended to drive N-channel power MOSFETs is powered from the regulated supply voltage available on pin 4 (VCC). The pin is to be connected directly to the SR MOSFET gate terminal
6	DVS	Drain voltage sensing. This pin must be connected to the drain terminal of the synchronous rectifier MOSFET through a series resistor of 390 Ω
	EP	Exposed pad. Thermal dissipation purpose. Connect to GND network at PCB level

3 Electrical data

3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Pin	Parameter	Value	Unit
V_{CC}	1	Internally regulated IC supply voltage (output pin)	-0.3 to 11	V
I_{VCC}	1	VCC output current	30	mA
SCP	3	SCP pin current rating	-0.7 to 1.7	mA
VO	4	External unregulated IC supply voltage (input pin)	-0.3 to 65	V
GD	5	GD pin voltage rating	-0.3 to VCC	V
DVS	6	Drain sense voltage referred to GND	-1 to 190	V
T_j	-	Junction temperature	-40 to 125	°C
T_{stg}	-	Storage temperature	-55 to 125	°C

Stressing the device above the ratings listed in the above table may cause permanent damage to the device.
Exposure to absolute maximum rated conditions may affect device reliability

3.2 Recommended operating conditions

Table 4. Recommended operating conditions

Symbol	Pin	Parameter	Value	Unit
I_{VCC} (1)	1	VCC output current	0 to 25	mA
VO	4	External unregulated IC supply voltage (input pin)	-0.3 to 36	V
DVS	6	Drain sense voltage referred to GND	-1 to 160	V

1. *25 mA is the max. operating output current of the internal regulator at 500 kHz / 5 nF*

If the device is operated within the "recommended operating conditions", its performance and electrical parameter degradation are guaranteed to remain within device specification.
These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions.
Unless otherwise specified, these conditions are intended to be continuously applied.

3.3 ESD immunity levels

Table 5. ESD immunity levels

Symbol	Pin	Parameter	Reference specification	Value	Unit
HBM	2 to 6, EP	Human Body Model	According to JS001	± 2	kV
HBM	1	Human Body Model	According to JS001	± 1.5	kV
CDM	All	Charge Device Model	According to JES002	± 500	V

3.4 Thermal data

Table 6. Thermal data

Symbol	Parameter	Value	Unit
R_{thJ-A}	Junction-to-ambient thermal resistance (1)	68	°C/W
R_{thJ-TC}	Junction-to-top-case thermal resistance (2)	106	°C/W
R_{thJ-BC}	Junction-to-bottom-case thermal resistance (2)	19	°C/W
P_{tot}	Power dissipation at T_{amb} = 50 °C	0.5	W

1. *2s2p board according to Jedec, JESD51-7, board size 114.3 x 76.2 x 1.6 [mm], natural convection*
2. *According to Jedec best practice guidelines, JESD51-12*

Note: Typical maximum VO in application is 20 V, while the internally regulated VCC is typically 5.5 V or 9 V. The power related to the regulation process is about (VO – VCC) by the average flowing current that depends on the frequency and the gate charge of the SR MOSFET. In some cases, it could be necessary to dissipate part of such power outside the IC by means, for instance, of a series resistor on VO.

4 Typical application schematic

Figure 3. Typical application schematic, low-side configuration

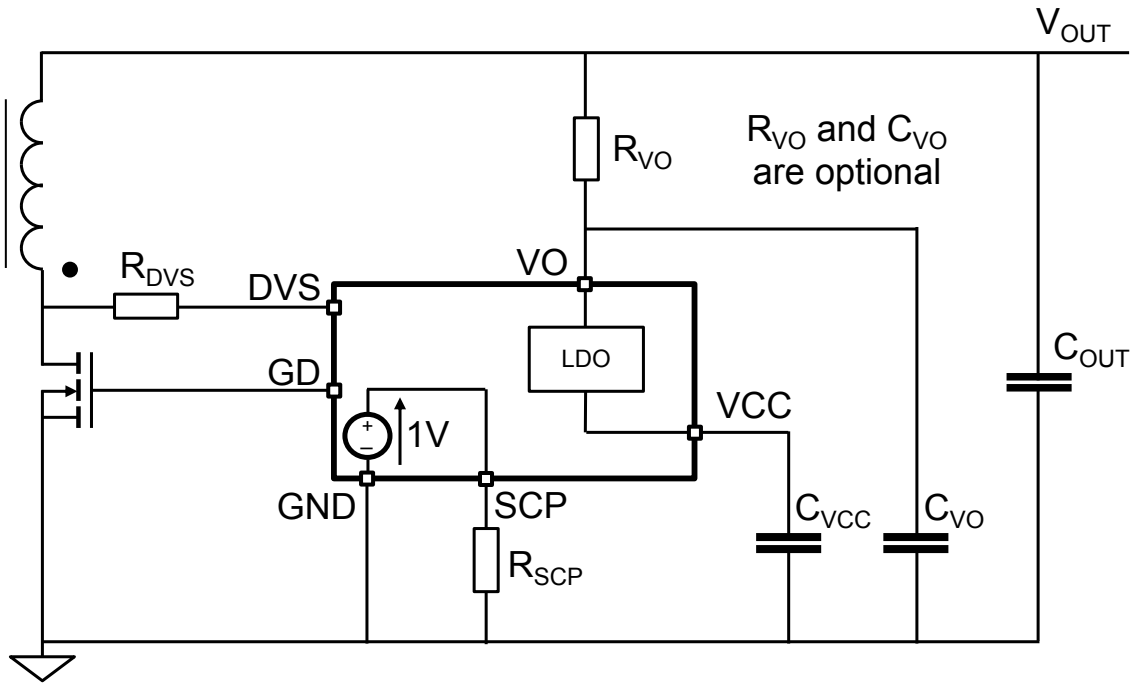
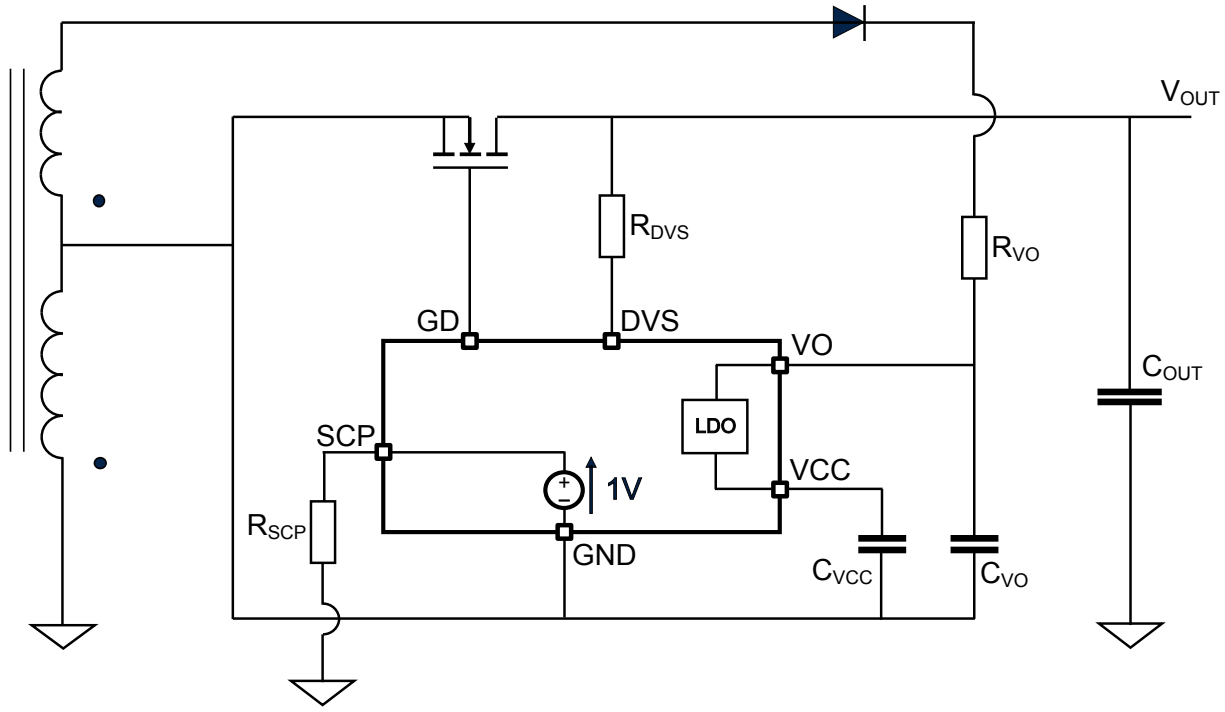


Figure 4. Typical application schematic, high-side configuration



5 Electrical characteristics

Table 7. Electrical characteristics

(T_j = -40 to 125 °C, VO = 20 V, C_{GD} = 4.7 nF; unless otherwise specified, typical values refer to T_j = 25 °C).

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Supply section						
VO	VO operating voltage	After turn-on	4.12		36	V
VO_{On}	Turn-on voltage	Voltage rising (1)	4.38	4.5	4.67	V
VO_{Off}	Turn-off voltage	Voltage falling (1)	3.88	4.0	4.12	V
I_{q_run}	Operating current	f_{sw} = 100 kHz, C_{GD} = 0		580	700	µA
I_q	Quiescent current	Idle during burst mode operation		230	290	µA
VCC linear regulator						
V_{CC}	V_{CC} regulation setpoint	I_{VCC} = 0 , 25 mA, SRK1004A, B	5	5.5	6	V
		I_{VCC} = 0 , 25 mA, SRK1004C, D	8.2	9	9.8	V
VO-V_{CC}	Max. dropout voltage	I_{VCC} = 10 mA @ 85 °C			0.25	V
Drain-source sensing input and Synch functions						
V_{VDS}	DVS operating voltage	Pulsed voltage			160	V
V_{TH_ON}	ON comparator threshold		-430	-330	-230	mV
V_{TH_OFF}	OFF comparator threshold		-3.5	0	1	mV
T_{D_OFF}	Turn-off delay			65	85	ns
T_{D_On}	Turn-on delay		55	85	105	ns
Dynamic characteristics						
T_{ON_MIN}	Minimum turn-on time		430	530	630	ns
T_{OFF_MIN}	Blanking time after turn-off	V_{DVS} > 2 V	200	270	340	ns
T_{ON_ENW}	Turn-on enable window	From V_{DVS} falling below 90% of its high level to V_{TH_ON} crossing	100	125	150	ns
Short-circuit detection						
V_{SCP}	Reference voltage	Forced voltage on SCP pin. An external resistor (200 kΩ) is connected to converter GND. This resistor is used to set the threshold for VOUT short circuit protection. When VOUT is lower than 3 V the SR MOSFET is turned-off. The SR MOSFET is turned-on again once VOUT > 3.7 V. When I_{SCP} = 20 µA	0.85	1	1.15	V
I_{SCP_TH}	Detection threshold	GD = high	15	20	25	µA
I_{SCP}	Max. source/sink current		-0.5		1.5	mA
Primary-side burst mode operation detection (low consumption mode)						
T_{stop}	Detection time. Switching stop time interval detection to enter low consumption mode (primary controller burst mode)	DVS > 1.4 V	48	65	82	µs
Gate driver						
I_{source_pk}	Output source peak current	SRK1004A, B		0.5		A

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{source_pk}	Output source peak current	SRK1004C, D		0.6		A
I_{sink_pk}	Output sink peak current	SRK1004A, B		1.5		A
		SRK1004C, D		1.7		A
t_r(2)	Rise time	V_{CC} in regulation, C_{GD} = 4.7 nF, SRK1004A, B		60		ns
		V_{CC} in regulation, C_{GD} = 4.7 nF, SRK1004C, D		80		
t_f(2)	Fall time	V_{CC} in regulation, C_{GD} = 4.7 nF, SRK1004A, B		15		ns
		V_{CC} in regulation, C_{GD} = 4.7 nF, SRK1004C, D		20		
V_{GDLow}	Low level voltage	I_{GD} = 100 mA		100	170	mV
V_{GDHigh}	Drive clamp voltage @ 0 load	Clamped to V_{CC}		V_{CC}		V

1. *Parameters tracking each other*
2. *Parameter guaranteed by design*

6 Application information

6.1 Non-complementary active clamp flyback and synchronous rectification

The SRK1004 is a controller specifically designed for synchronous rectification in non-complementary active clamp flyback (NC-ACF) converters. By their nature, NC-ACF converters are operated either close to the boundary between Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM) or in DCM. Normally, they work close to the CCM-DCM boundary at heavy load, and in DCM at light load. Burst mode is generally used at very light or no load to optimize efficiency in those conditions and minimize standby consumption.

As shown in the timing diagrams of Figure 5 and Figure 6, in NC-ACF converters, during the off phase of the main primary switch, that is the low-side MOSFET, depending on the load condition, two or three temporal windows can be observed: the transformer de-magnetization time, T_{DEM}, an idle time, T_{wait}, with no current at both primary and secondary, expected of DCM operation, and the reverse current build-up time, T_{REV}. T_{DEM}, the transformer de-magnetization time is from the low-side MOSFET turn-off, driven by the PWM control loop, to the complete transformer de-magnetization, occurring when the secondary current reaches zero.

In the first part of T_{DEM}, the energy stored in the magnetizing inductance is released to the secondary, while the energy stored in the leakage inductance is delivered to the clamp capacitor. So, on the one hand, the secondary current builds up, reaching the peak when the primary current is zeroed, and, on the other hand, the drain voltage of the low-side MOSFET is clamped.

In the second part of T_{DEM}, the secondary current linearly decays from peak to zero, that is, the transformer is de-magnetized, while the energy that was in the leakage inductance is maintained into the clamp capacitor. Once T_{DEM} has elapsed, the auxiliary primary switch, that is the high-side MOSFET, can be turned on; however, the actual turn-on of the high-side MOSFET depends on the load condition.

At heavy loads, the converter works at CCM-DCM boundary, T_{DEM} and T_{REV} are contiguous and the high-side MOSFET is turned on right after the transformer de-magnetization (see Figure 5). The idle time, T_{wait}, is zero.

As the load is reduced, the converter starts operating in DCM: the idle time, T_{wait}, appears between T_{DEM} and T_{REV}, getting longer and longer as the load becomes smaller and smaller (see Figure 6. NC-ACF converter: DCM key waveforms (light load conditions)).

Depending on the load level, the high-side MOSFET is turned on at a peak of the low-side MOSFET drain voltage ringing, as far as the ringing is detectable, that is, at moderate loads, or after a certain timeout, when the drain ringing is no longer detectable, that is, at light loads. In the former case, the high-side MOSFET is turned on when the low-side drain voltage is higher than the input voltage and the high-side MOSFET turn-on losses are minimized. In the latter case, the low-side drain voltage is practically equal to the input voltage and the high-side MOSFET can be turned anywhere with no impact on its turn-on losses.

In both cases, CCM-DCM boundary and DCM operations, during T_{REV}, when the high-side MOSFET is on, the primary current and the secondary current flow, at the same time, in a forward mode fashion: at primary, it is reverse current, from the clamp capacitor to the transformer, that, at secondary, becomes a ‘useful’ current bump delivered to the output.

Figure 5. NC-ACF converter: CCM-DCM boundary key waveforms (full load conditions)

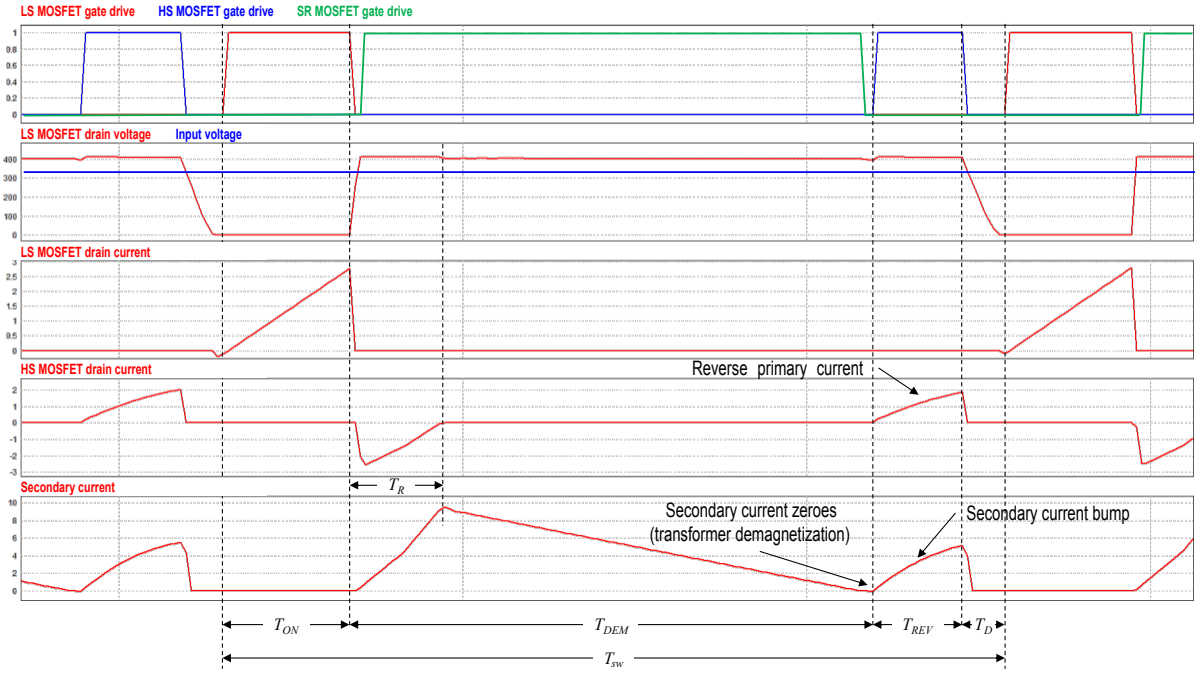
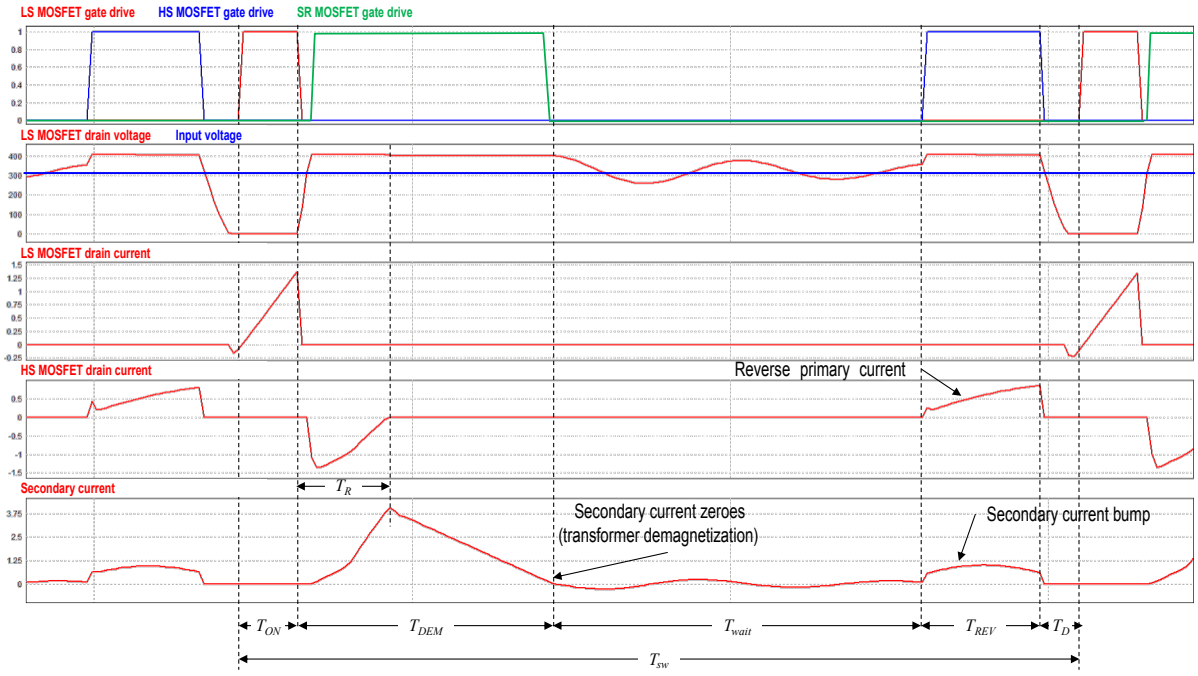


Figure 6. NC-ACF converter: DCM key waveforms (light load conditions)



The current bump during T_{REV} has typically a low amplitude and duration. For this reason, if the synchronous rectification is used during T_{REV}, MOSFET driving and switching losses may be higher than the saved conduction losses. Therefore, the synchronous rectifier (SR) MOSFET must be on during the first secondary side conduction interval only, which is during T_{DEM}, and must be off during the second secondary side conduction, which is during T_{REV}.

Consequently, the control algorithm implemented in the SR controller must be able to distinguish the two secondary conduction phases to properly drive the SR MOSFET. The required operation is shown in the following Figure 7 and Figure 8, for CCM-DCM boundary and DCM operations.

Figure 7. **NC-ACF converter: secondary side CCM-DCM boundary key waveforms and SR control**

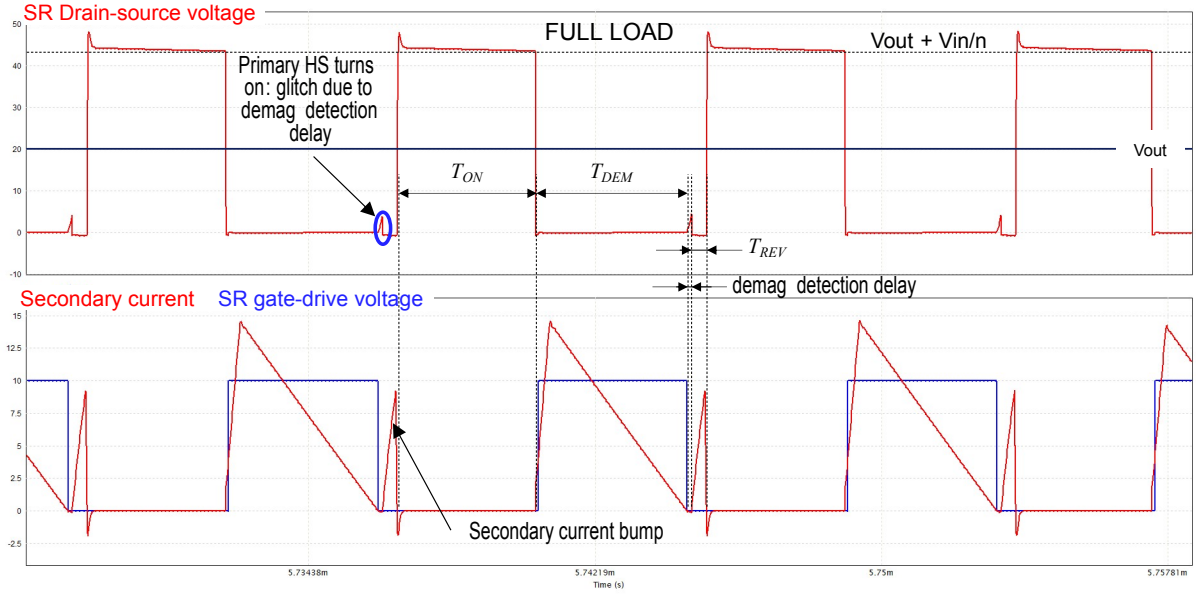
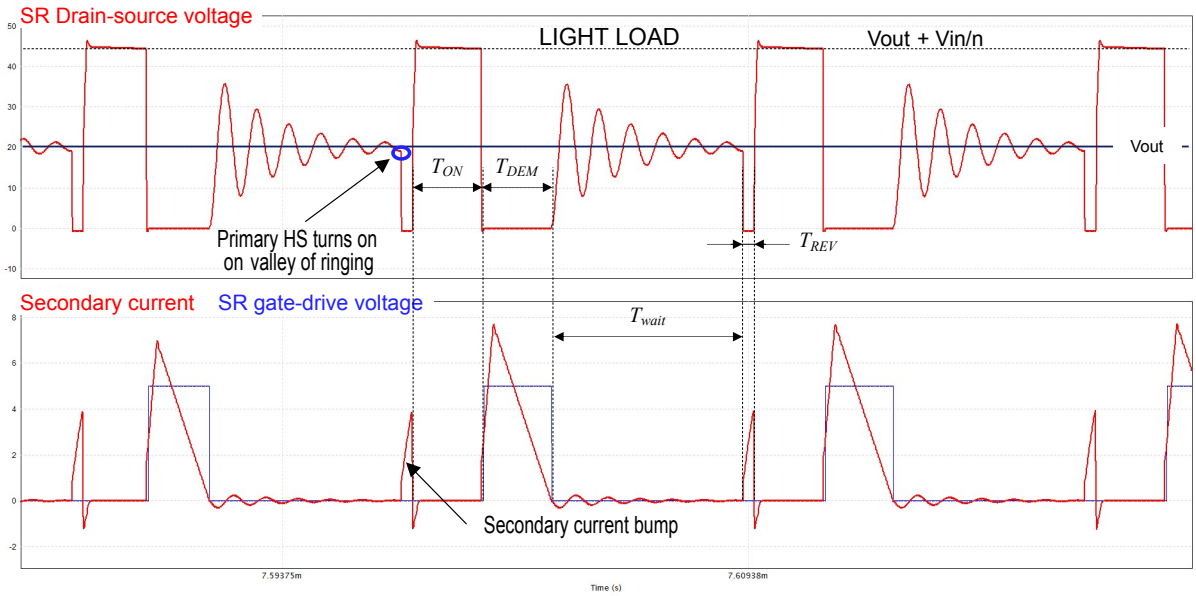


Figure 8. **NC-ACF converter: secondary side DCM key waveforms and SR control**



6.2 Operating principle of SRK1004

The SRK1004 operates by sensing the drain-to-source voltage V_{DS_SR} of the SR MOSFET. This is done through the DVS pin: this is a high voltage pin and needs to be properly routed to the MOSFET drain, through a resistor of at least 390 Ω (to limit dynamic current injection into the pin in any condition).

In case of turn-on with output in short-circuit, the series resistor on the DVS pin could be stressed by pulse train. Considering the DVS signal amplitude, to have a good margin on the voltage rating, a 0805 resistor is recommended or, even better from the viewpoint of power dissipation, two 0603 resistors.

6.2.1 SR MOSFET turn-on and premature turn-off protection

During the on-time of the low-side primary switch, the drain-to-source voltage, V_{DS_SR}, of the SR MOSFET is flat at 'V_{OUT} + V_{IN}/n' (V_{IN} and V_{OUT} are the input and the output voltage of the converter respectively, and n the primary-to-secondary turns ratio).

As the low-side primary switch turns off, the drain-to-source voltage of the SR MOSFET quickly reverses and goes negative until it is clamped, at '-V_F', by the body diode of the SR MOSFET itself, allowing the secondary current to flow. This determines the turn-on of the SR MOSFET, after a short delay, T_{D_On}, by means of a comparator triggered by V_{DS_SR} falling below a slightly negative threshold (V_{TH_ON} > '-V_F').

After turn-on, the sensed DVS signal goes from '-V_F' to the *I·R* drop across the SR MOSFET channel resistance (R_{DS_ON}). This small negative voltage is generally affected by some amount of noise, associated to the flyback transformer leakage inductance and to the stray inductance of the gate-drive path: a premature turn-off of the SR MOSFET could be triggered by such noise and must be avoided. The SR MOSFET premature turn-off is prevented by an internally fixed blanking time, implemented in SRK1004, which then sets a minimum on-time of the SR MOSFET as well (T_{ON_min}).

The SR MOSFET stays on during all the whole T_{DEM} interval.

6.2.2 SR MOSFET turn-off and unwanted turn-on protection

As the secondary current decays to zero and T_{DEM} ends, the drain-to-source voltage of the SR MOSFET, V_{DS_SR}, approaches zero almost linearly and a fast comparator, referred to a threshold $V_{TH\_OFF} \approx 0$, turns the SR MOSFET off. As a result, the V_{DS_SR} voltage reverses again and tends to go up. Before going up, V_{DS_SR} might go below ground at '-V_F' for a short while when the SR MOSFET is turned off with a secondary current still greater than zero, so that its body diode conducts the final part. This might cause an improper turn-on of the SR MOSFET: to avoid this event the turn-on mechanism is blanked for an internally fixed time, which then sets a minimum off-time of the SR MOSFET as well (T_{OFF_min}).

Once the secondary current has zeroed, if the converter is working on the CCM-DCM boundary, the V_{DS_SR} voltage experiences just a small positive glitch because the primary control turns on the high-side primary switch immediately ($T_{wait} \approx 0$), which again forward biases the body diode of the SR MOSFET and makes V_{DS_SR} drop at '-V_F' again (see Figure 7). The SR MOSFET, however, is not turned on.

If the converter is working in DCM, since the primary control does not immediately turn on the HS switch (T_{wait} > 0), the V_{DS_SR} voltage naturally evolves as a damped oscillation around V_{OUT} (see Figure 8). The amplitude of this ringing is theoretically smaller than V_{OUT} because of the damping but may be larger if the SR MOSFET has been turned off a bit too late, so that its current is slightly negative (flowing from drain-to-source). Consequently, the first valley of the ringing (and sometimes even the second one) may take V_{DS_SR} below the turn-on threshold V_{TH_ON}. Should this occur, the SR MOSFET is not turned on.

Eventually, after T_{wait} has elapsed, the primary control turns on the high-side primary switch and V_{DS} quickly drops at '-V_F' again and, again, the SR MOSFET is not turned on.

6.2.2.1 *SR MOSFET stray inductance compensation*

The parasitic inductance of the drain terminal of the SR MOSFET introduces a timing advance on the zero crossing detection: the zero crossing on the voltage signal occurs in advance with respect to the zero crossing of the rectified current and the time lead is given by the ratio L_{stray} / R_{DSON}. The consequence is a premature turn-off that means a larger residual diode conduction time, that is, an efficiency degradation.

To optimize the application, SRK1004 is characterized by an extra turn-off delay. Typical extra turn-off delays are as highlighted in Table 8.

Table 8. SRK1004 - Internal extra turn-off delay

	Typ. extra turn-off delay [ns]
SRK1004A, SRK1004C	25
SRK1004B, SRK1004D	150

SRK1004 is offered with two different extra turn-off delays. This allows compensating anticipation generated by a wide range of MOSFET part numbers.

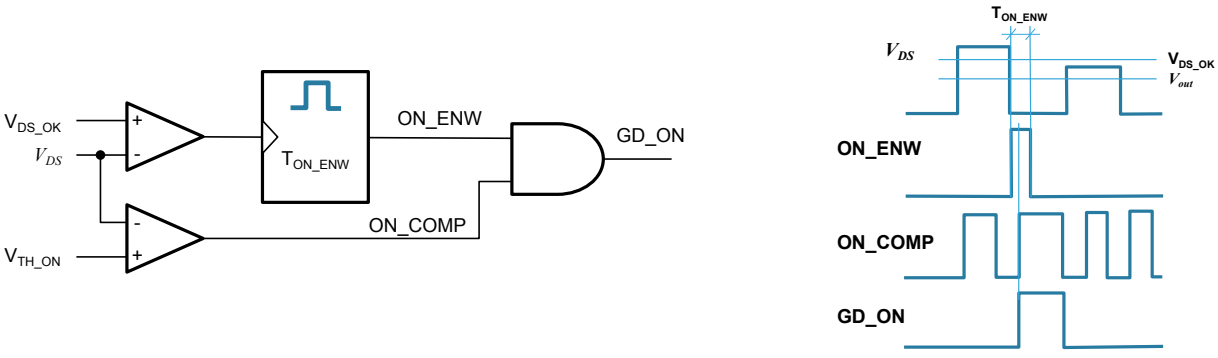
6.2.3 SR MOSFET improper turn-on avoidance

In addition to the T_{OFF_min} blanking, the SRK1004 is provided with a mechanism that prevents the SR MOSFET from improperly turning on, by defining a “turn-on enable window”, when the high-side primary switch is turned on or in case V_{DS_SR} is ringing below ground in DCM. It is based on these observations:

- The negative-going edges of V_{DS_SR} corresponding to the T_{DEM} interval, where the SR MOSFET is to be turned on, are steep (few ten ns) and start from 'V_{OUT} + V_{IN}/n', then from a voltage higher than V_{OUT}.
- The negative-going edges of V_{DS_SR} corresponding to the turn-on of the high-side primary switch are as steep but start from a value close to zero when the converter works on the CCM-DCM boundary and from a value lower than or equal to V_{OUT} when the converter works in DCM (the peaks of the drain-source voltage of the low-side primary switch are the valleys of V_{DS_SR}).
- The negative-going edges of V_{DS_SR} corresponding to its ringing during T_{wait}, even if falling below the turn-on threshold V_{TH_ON} starting from above V_{OUT}, are much easier, so that it takes much longer for V_{DS_SR} to go, in case, from the peak to V_{TH_ON}. This time is approximately half the ringing period of V_{DS_SR} (= 1 / $2\pi\sqrt{L_pC_D}$), which is in the hundred nanoseconds, at least one order of magnitude longer than the duration of the steep edges due to the turn-off of low-side MOSFET or the turn-on of high-side MOSFET.

The principle of the circuit that generates the “turn-on enable window”, based on the previous observations is shown in the following Figure 9.

Figure 9. Circuit that generates the “turn-on enable window” (a) and related timing (b)



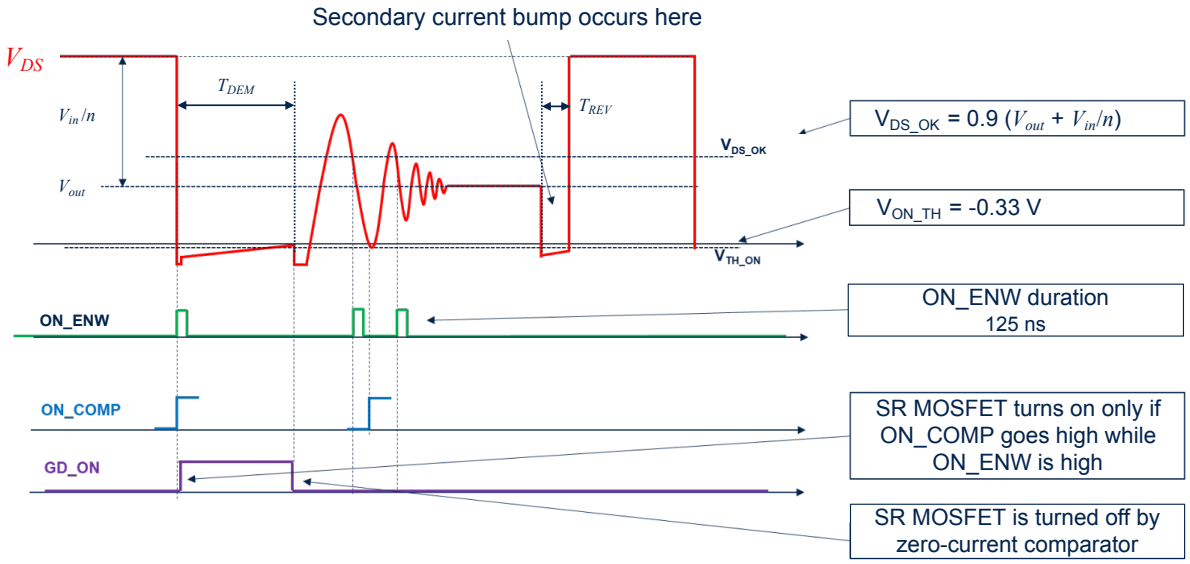
As shown in Figure 9 (a), the SRK1004 embeds a reference voltage V_{DS_OK} > V_{OUT} (actually, V_{DS_OK} is proportional to 'V_{OUT} + V_{IN}/n' cycle-by-cycle) and a comparator that compares V_{DS_SR} against V_{DS_OK}. This comparator outputs a low logic level when V_{DS_SR} > V_{DS_OK} and a high logic level when V_{DS_SR} < V_{DS_OK}. The positive-going edge of this comparator’s output triggers a monostable flip-flop that delivers a pulse ON_ENW whose internally fixed width T_{ON_ENW} defines a “turn-on enable window”.

As shown in Figure 9 (b), if V_{DS_SR} falls below V_{TH_ON} (that is, ON_COMP goes high) within the “turn-on enable window” then the GD_ON signal goes high as well (being the logical AND between the signals ON_ENW and ON_COMP), and the SR MOSFET turns on; otherwise, it does not.

In this way, as illustrated in Figure 10, especially for the DCM operation case:

- The SR MOSFET is enabled to turn on after the low-side primary switch turns off because the fall time of V_{DS_SR} is << T_{ON_ENW} (the time V_{DS_SR} takes to fall from V_{DS_OK} to V_{TH_ON} is even shorter): the turn-on enable window is generated as well as the ON_COMP signal being asserted.
- The SR MOSFET is prevented from turning on as the high-side primary switch turns on when the converter works on the CCM-DCM boundary because V_{DS_SR} remains close to zero and then does not even go above V_{DS_OK}, so that the turn-on enable window is not generated.
- The SR MOSFET is prevented from turning on as the high-side primary switch turns on when the converter works in DCM because this occurs on the valley of the V_{DS_SR} ringing, when V_{DS_SR} < V_{OUT}. This is obviously true when the high-side primary switch is turned on after some ringing cycles as shown in the previous Figure 8, because V_{DS_SR} rings stay below V_{DS_OK} and no turn-on enable time window is generated. Furthermore, it is true when the turn-on of the high-side primary switch occurs on the first valley of V_{DS_SR} ringing as well: the time from V_{DS_SR} falling below V_{DS_OK} to the valley is >> T_{ON_ENW}, so that the steep edge falling below V_{TH_ON} is outside the turn-on enable window.
- The SR MOSFET is prevented from turning on by the natural V_{DS_SR} ringing falling below V_{TH_ON} when the converter works in DCM for the same reason: even if V_{DS_SR} exceeds V_{DS_OK} while ringing, the time from V_{DS_SR} falling below V_{DS_OK} to the valley is >> T_{ON_ENW}, so that the V_{TH_ON} crossing is outside the turn-on enable window.

Figure 10. NC-ACF converter: secondary side DCM boundary key waveforms and SR control



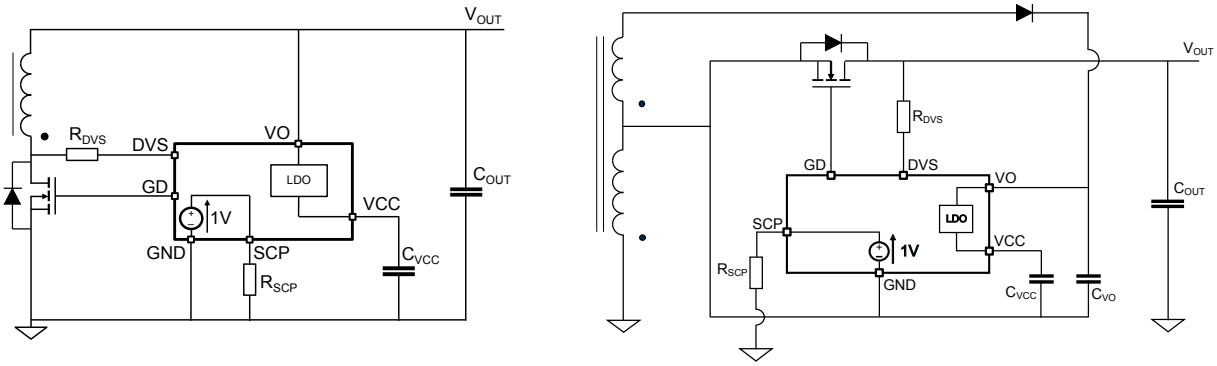
6.3 Short circuit protection – SCP

The SRK1004 can be used with the SR MOSFET placed both low-side (with the drain terminal connected to the secondary winding and the source to the return of the output voltage, that is, the secondary ground, Figure 11 left-hand side) or high-side (with the drain terminal connected to the output voltage bus and the source to the secondary winding of the transformer, Figure 11 right-hand side).

On the one hand, in case of low-side configuration of the SR MOSFET, the VO pin of the IC, whose ground, that is, the GND pin, must be connected to the source terminal of the SR MOSFET, can be supplied by the output voltage bus. The schematic of this ‘traditional’ configuration is shown in Figure 11 on the left-hand side.

On the other hand, in case of high-side configuration, the source terminal of the SR MOSFET and the ground of the IC, are connected to the swinging node of the secondary winding, so the IC is typically supplied by an auxiliary winding with a rectifier diode and a buffer capacitor connected, as shown in Figure 11 on the right-hand side.

Figure 11. Low-side and high-side configuration of SR MOSFET and SRK1004



Low-side configuration

High-side configuration

With the low-side configuration (that is, VO = V_{OUT}), in case of short-circuit on converter's output, as the VO voltage falls below the UVLO threshold (VO_{Off}), the SRK1004 shuts down and stops driving the SR MOSFET. Secondary current conduction through the body diode of the SR MOSFET ensures that, on the primary side, the ACF controller is still able to correctly detect transformer demagnetization and ensure proper operation of the converter during a short-circuit. See hereinafter, how to choose R_{SCP} in case of low-side configuration.

With the high-side configuration, in case of short-circuit on converter's output, VO and V_{OUT} differently evolve in time: V_{OUT} drops quickly with a time constant depending on the output capacitance C_{OUT} and the short-circuit impedance (there may be also a negative step-change due to the ESR of C_{OUT}), whereas VO decays with a rate determined by the VO buffer capacitance and the consumption of the IC. In some extreme cases VO might not even go below the UVLO threshold, leaving the SRK1004 always operating during a short-circuit (until a protection in the primary ACF controller is triggered). However, even in case VO eventually goes below the UVLO threshold, as far as the SR MOSFET is driven, the ACF primary controller might not be able to correctly detect transformer demagnetization, thus causing the controller to operate the primary switches improperly and increasing the already high stress of all power components.

To handle this condition, that is, the output short-circuit on high-side configuration of the SR MOSFET, the SRK1004 implements a short-circuit protection that prevents the SR MOSFET from being driven when the converter output is shorted. This function uses an external pin (SCP) that provides a reference voltage V_{SCP} = 1 V referred to the IC ground, able to both sink and source current. A resistor R_{SCP} (in the hundred kΩ range) is connected from the pin to the secondary ground.

When current is flowing on the secondary side, the IC ground is at a potential essentially equal to V_{OUT} with respect to the secondary ground and the current flowing through this resistor is:

$$I_{SCP} = \frac{V_{OUT} + 1}{R_{SCP}} \quad (1)$$

If this current falls below a reference current I_{SCP_TH} = 20 µA, a short-circuit condition is assumed, the SRK1004 turns off the SR MOSFET and inhibits its turn-on in the next switching cycle. Note that, when the SRK1004 skips a turn-on cycle of the SR MOSFET, the IC is keeping the gate drive output low, but the internal signals are unaffected. Thus, from the instant the short-circuit is detected, turn-on skipping is confirmed cycle-by-cycle and no gate driving occurs until the SRK1004 is shut down by VO falling below the UVLO threshold or a protection on the ACF primary controller stops the converter, whichever comes first.

Detailed short-circuit protection mechanism

The output voltage corresponding to SCP detection is in the range 2.5 V – 3.5 V. The upper limit is from the minimum operating voltage, 5 V, including ripple and margin. The lower limit is selected to guarantee the operation of the primary controller, at reduced output voltage.

SCP is active during de-magnetization phase only (SCP pin forced to 1 V and current flowing in the resistor is compared with a 20 µA, typ, internal reference). On the other hand, during primary conduction phase, SCP pin is clamped to a maximum voltage of 2 V.

When an SCP event is triggered, the SR MOSFET is turned off: consequently, the output voltage has a positive variation corresponding to 'V_{FWD} - R_{DSon}· I_{OUT}' (the difference between body diode forward voltage and MOSFET channel voltage drop). A 1 V hysteresis is added onto the comparator to hold the protection state despite the output voltage variation. The SCP pin is then forced to the GND pin voltage.

From Equation 1, if V_{OUTSC} is the output voltage below which the SRK1004 is required to stop switching, the R_{SCP} resistor is selected as:

$$R_{SCP} = \frac{V_{OUT_{SC}} + 1}{I_{SCP\_TH}} \quad (2)$$

Note that there is a lower limit to R_{SCP}: during the time interval when the low-side primary switch is on, the ground of the IC is at '-V_{IN}/n' with respect to the secondary ground. Therefore, a current equal to $(V_{IN}/n - 1)/R_{SCP}$ enters the SCP pin and this current must not exceed the sink current capability of the pin (1.5 mA).

In case of low-side configuration, the function needs to be disabled, thus the R_{SCP} resistor is selected in the range:

$$2.2\text{k}\Omega < R_{SCP} < 36\text{k}\Omega \quad (3)$$

A value R_{SCP} = 22 kΩ is typically recommended.

6.4 Light load condition: burst mode operation

The SRK1004 recognizes the primary side operation in burst mode looking at the time the DVS signal stays above a certain threshold. If DVS > 1.4 V for a time larger than T_{STOP} (65 µs, typ.), then the primary burst mode operation is recognized: the SR MOSFET is no longer turned on and off and the SRK1004 enters in low power mode.

The minimum value of T_{STOP} (48 µs) has been taken larger than the maximum switching period of the primary controller, during light load operation. In this way, the SRK1004 cannot enter in burst mode when the primary is not in such operating condition.

The SRK1004 exits from the low power mode at the first DVS edge triggering the turn-on threshold by falling below V_{TH_ON} (-330 mV, typ.).

When the load is reduced at light levels and the on-time is pushed to the minimum value (250 ns, typ.), the SRK1004 no longer turns on the SR MOSFET.

When the switching activity of primary starts or restarts, up to two switching cycles are necessary before the SRK1004 begins or resumes the SR MOSFET turn-on/off activity.

7 Layout guidelines

In this section, the layout guidelines for both low-side driving configuration and high-side driving configuration are summarized.

Common guidelines:

- C_{VCC} and C_{VO} near IC with short connections to VCC pin and GND pin.
- A small resistor, 10 Ω for instance, could be useful to build an RC filter on VO pin.
- Minimize the area of circuit done by GD pin, SR MOSFET and DVS pin.
- Short trace from DRAIN of SR MOSFET to DVS pin.
- Exposed pad: connect to GND pin/net.

SCP pin:

- No special care in the case of low-side driving since the resistor can be easily connected between SCP pin and GND pin of the IC.
- In the case of high-side driving (see Figure 11), minimize the area of the circuit done by R1, SCP/GND pins and secondary winding.
- Furthermore, keep R1 = R_{SCP} near the in SCP to minimize the parasitic capacitance from the pin to the ground.

Output current circuit:

- In the low-side driving configuration, minimize the connection between the source of the SR MOSFET and the negative terminal of the output electrolytic capacitor.
- In the high-side driving configuration, minimize the connection between the negative terminals of the secondary winding and the output electrolytic capacitor.

8 Ordering information

Table 9. Device summary

Order code	VCC [V]	Typ. turn-off delay [ns]	Package marking	Package	Packaging
SRK1004ATR	5.5	25	S4A	DFN 6L	Tape and Reel
SRK1004BTR	5.5	150	S4B	DFN 6L	Tape and Reel
SRK1004CTR	9.0	25	S4C	DFN 6L	Tape and Reel
SRK1004DTR	9.0	150	S4D	DFN 6L	Tape and Reel

9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

9.1 DFN 2 x 2 x 0.75, 6L (EP), pitch 0.65 mm package information

Table 10. DFN 2 x 2 x 0.75 package dimensions

Symbol	Dimensions (mm)		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0.00		0.05
A3	0.200 REF		
b	0.25	0.30	0.35
D	1.95	2.00	2.05
D1	1.50	1.60	1.70
e	0.65 BSC		
e2	0.25 REF		
E	1.95	2.00	2.05
E1	0.90	1.00	1.10
K		0.25	
L	0.20	0.25	0.30

Figure 12. **DFN 2 x 2 x 0.75 package drawing: bottom and top view**

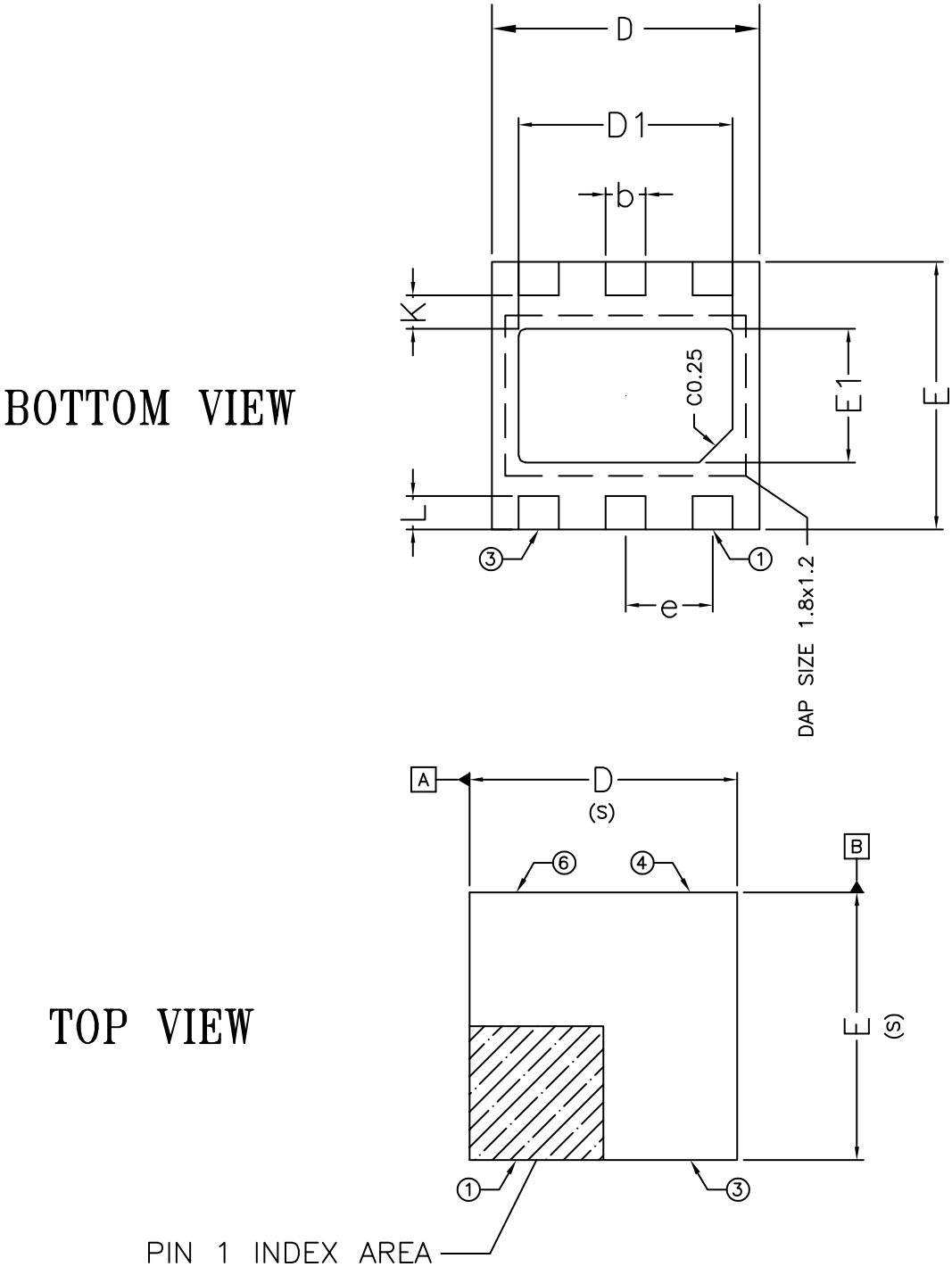
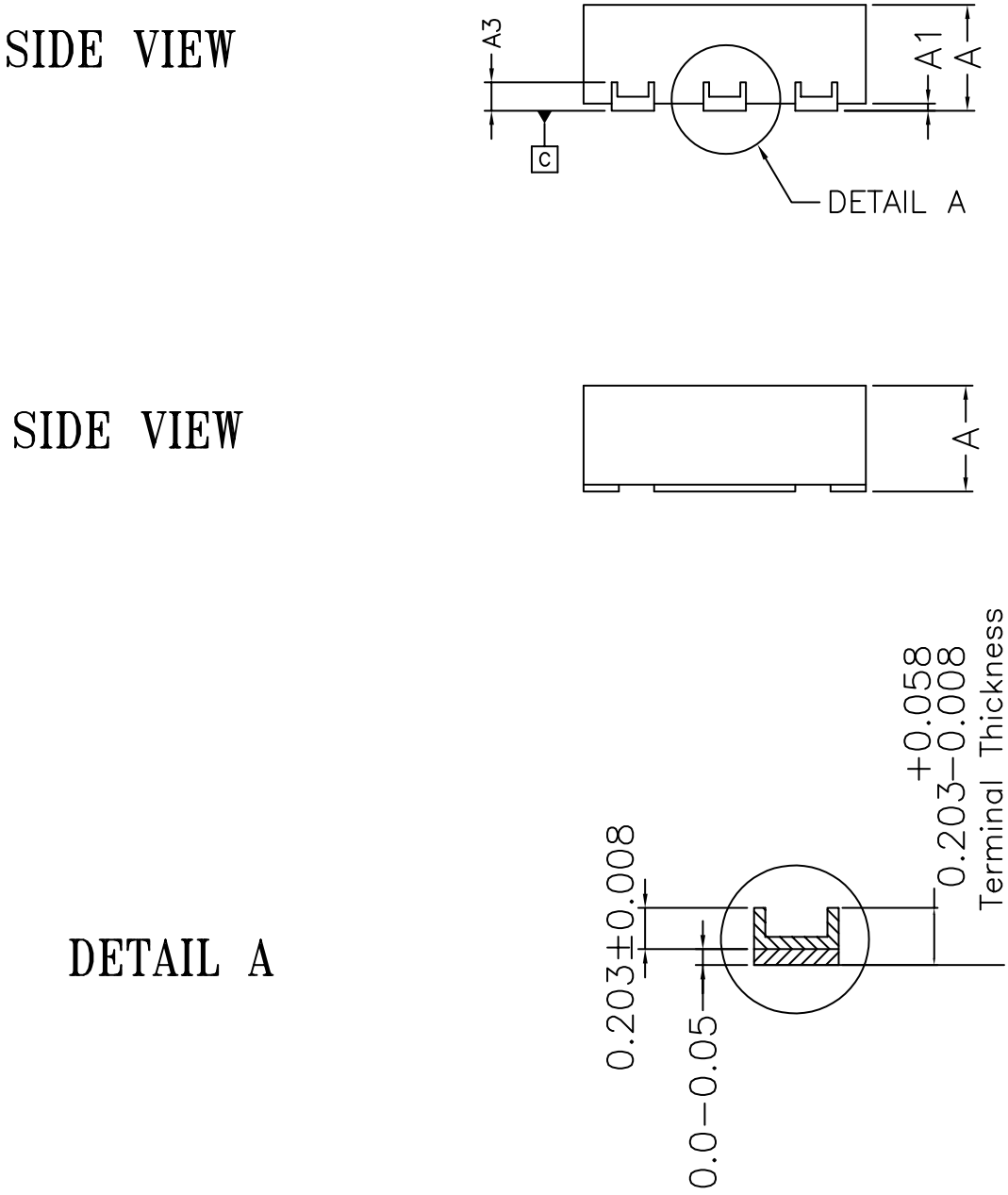


Figure 13. **DFN 2 x 2 x 0.75 package drawing: side views**



Revision history

Table 11. **Document revision history**

Date	Version	Changes
16-Aug-2023	1	Initial release.
08-Jan-2024	2	Updated order codes in Table 1 and Table 9, updated GD value in Table 3

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