ST-ONEHP

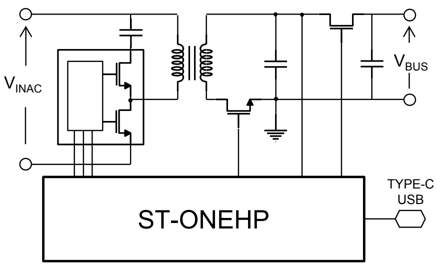
Datasheet

Fully integrated controller for EPR USB-PD power supplies

Product status link
ST-ONEHP

Product label
SUSTAINABLE TECHNOLOGY

Figure 1. Typical system block diagram



Features

- ZVS non-complementary active clamp flyback controller with synchronous rectification and USB-PD 3.1 EPR and AVS interface
- ARM® 32-bit Cortex®-M0+ MCU with 64 kB flash memory for digital power control and USB protocol
  - FW programmable secondary side MCU controls both synchronous rectifier and ZVS active clamp flyback on the primary side to improve system efficiency in every condition
  - High switching frequency operations in companion with MasterGaN power stage allow to use small size magnetic components, including planar transformers
- Reinforced galvanically isolated dual communication channel compliant with IEC 62368-1:
  - 4 kV pk transient voltage
  - 9.6 kV pk 1min hipot type testing
  - 6.4 kV pk 1s hipot production testing
- 800 V high voltage startup with integrated input voltage sensing and Brown-in/out functions
- Active input filter capacitor discharge circuitry for reduced standby power compliant with IEC 62368-1
- Fully Integrated USB-PD PHY with 24 V tolerant protection, and integrated load switch driver

Application

- USB-PD 3.1 EPR chargers and adapters over 100 W for smartphones, tablets, laptops and other equipment

Description

The ST-ONEHP is part of the ST-ONE® family, the world’s first digital controllers embedding ARM Cortex M0+ core, an offline programmable controller with synchronous rectification, and USB PD PHY in a single package. Such a system is specifically designed to control ZVS non-complementary active clamp flyback converters to create high power density chargers and adapters with EPR compliant USB-PD interface.

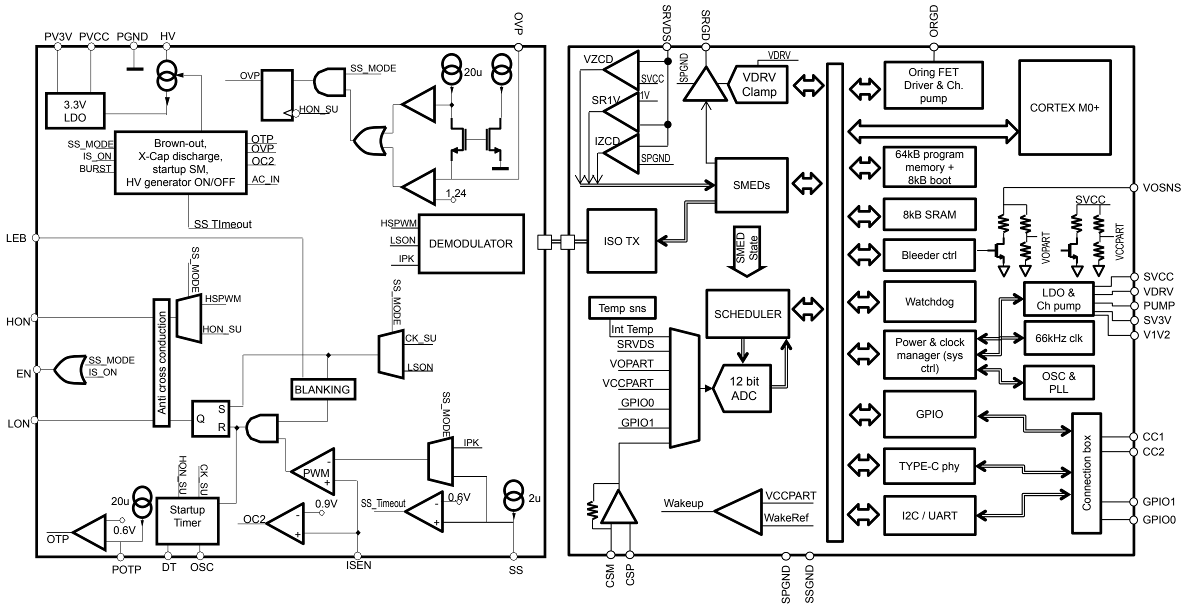
The device includes an active clamp flyback controller and its HV startup on the primary side, a microcontroller and all the peripherals required to control the conversion and the USB-PD communication on the secondary side. The two sides are connected through an embedded galvanically isolated dual communication channel. By using a novel non-complementary control technique and specifically designed power modes the device allows to reach both high efficiency and low no load power consumption

The device is delivered with a pre-loaded firmware which handles both the power conversion and the communication protocols for EPR USB-PD including AVS and electronically marked cable management.

A dedicated memory stores a default device configuration during factory process. The user can change or adapt this memory area to fit the final product specifications.

1 ST-ONEHP block diagram

Figure 2. ST-ONEHP block diagram



2 Pin connections and description

Figure 3. Pin connection (top view)

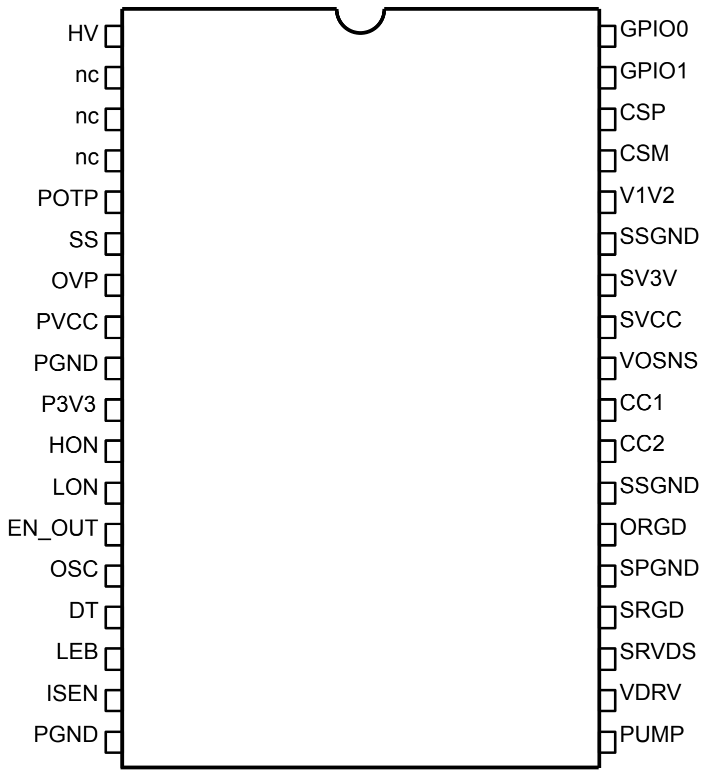


Table 1. Pin functions

Pin	Name	Function
1	HV	High voltage start-up generator / ac voltage sensing input. The pin, able to withstand 800 V, must be connected to the ac side of the input bridge via a pair of diodes to sense the ac input voltage. When the voltage on the pin is higher than $V_{HVStart}$, an internal pull-up circuit charges the capacitor connected between the pin PVCC and PGND. The pin is used also to sense the ac voltage, which is used by ac brown-out and X-cap discharge functions.
2,3,4	nc	High voltage spacer. The pin is not connected internally to increase spacing between the high-voltage pin and the other pins.
5	POTP	Primary side overtemperature protection. Pulling this pin below V_{POVTH} shuts down the IC.
6	SS	Soft-start setting. Connect a capacitor to PGND to set the soft-start duration.
7	OVP	Aux winding sense for overvoltage protection.
8	PVCC	Primary side supply voltage pin. The internal high voltage generator allows to charge an external capacitor connected between this pin and PGND before the converter starts up. A small bypass capacitor (0.1 µF typ.) to PGND must be placed close to the pins to get a clean bias voltage.
9	PGND	Primary side ground. Reference for I/Os.
10	P3V3	Primary side internal supply regulator bypass capacitor.
11	HON	High-side gate-drive control signal.
12	LON	Low-side gate-drive control signal.
13	EN_OUT	Enable signal for an external driver. Improves efficiency during bursts in case the driver supports this functionality.

Pin	Name	Function
14	OSC	Oscillator pin. A resistor from the pin to PGND defines the switching frequency during the initial soft-start.
15	DT	Deadtime programming. A resistor from this pin to PGND sets the deadtime during soft-start and minimum deadtime during functional mode.
16	LEB	Leading edge blanking time programming. A resistor from this pin to ground sets the leading edge blanking time for the ISEN comparator.
17	ISEN	Current sense (PWM comparator) input. The voltage on this pin is compared with an internal reference to turn off LON.
18	PGND	Primary side signal ground. Reference for analog signals.
19	PUMP	Charge pump pin 1. Used to power the VDRV when SVCC drops below a programmable threshold.
20	VDRV	Driver supply.
21	SRVDS	Output winding voltage sense. Connect to sync FET drain through a clamping MOSFET.
22	SRGD	Synchronous rectifier gate driver.
23	SPGND	Secondary side power ground. Current return for the sync FET gate-drive current.
24	ORGD	Load switch gate drive. The pin is pulled to 5V above VOSNS to control an external circuit to drive a load switch.
25	SSGND	Secondary side signal ground.
26	CC2	USB Type-C CC2 pin. Used for USB-PD compliant communication or alternate function as DN / GPIO3 / I2C-SCL / UART-TX.[(1)]
27	CC1	USB Type-C CC1 pin. Used for USB-PD compliant communication or alternate function as DP / GPIO2 / I2C-SDA / UART-RX.[(1)]
28	VOSNS	This pin provides a path for the output voltage bleeder. Connect to the USB connector VBUS through a clamping circuit.
29	SVCC	Secondary side VCC. The device senses and controls the converter output through this pin for output voltage lower than 15V.
30	SV3V	3.3 V Regulated supply for the IC. Connect a 1μF capacitor from this pin to SSGND.
31	SSGND	Secondary side signal ground.
32	V1V2	1.2 V regulated supply for the IC. Connect a 4.7μF capacitor from this pin to SSGND.
33	CSM	Output current sense pin. Connect to the negative side of sense resistor on the ground path.
34	CSP	Output current sense pin. Connect to the positive side of sense resistor on the ground path to sense the current drawn by the load.
35	GPIO1	General purpose digital I/O, used as output voltage sense through a resistor divider when the programmed output voltage is above a 15V (see SVCC pin).
36	GPIO0	General purpose digital I/O, digital interface or analog input, not used with the pre-loaded firmware. The pin is also used to enter in programming/boot mode at IC startup. Connect a 100kΩ pullup to SV3V to avoid unwanted entry in boot mode at startup, unless this function is configured as disabled.

1. *The firmware loaded on ST-ONEHP configures the pins as either USB-PD or programming interface, depending on parameter setup. The default configuration is programming interface*

3 Electrical ratings

Stresses above the absolute maximum ratings listed in Table 2. Absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute maximum ratings

Symbol	Pin	Parameter	Value	Unit
V_{HV}	HV	Voltage range (referenced to PGND)	-1 to 800	V
V_{PVCC}	PVCC	Primary side supply voltage	-0.3 to 18	V
V_{PV3V}	P3V3	3.3 V supply range	-0.3 to 3.6	V
I_{OVP}	OVP	Maximum clamp source/sink current on OVP	-200 to 200	µA
V_{HON}, V_{LON}, V_{EN_OUT}	HON, LON, EN_OUT	Voltage range	-0.3 to 5.5	V
V_{AMRPri}	Other primary side pins	Primary side analog Inputs & Outputs	-0.3 to 3.6	V
Secondary side voltages, referred to SSGND				
V_{CC1}, V_{CC2}	CC1, CC2	USB connector IOs	-0.3 to 24	V
V_{VOSNS}, V_{SVCC}	VOSNS, SVCC	Output voltage sense & VCC	-0.3 to 24	V
V_{PUMP}	PUMP	Charge pump pin, referred to SPGND	-0.3 to 15	V
V_{ORGD}	ORGD	Oring FET gate driver voltage range	-0.3 to 29	V
V_{CSP}, V_{CSM}	CSP,CSM	Current sense voltage range	-0.3 to 3.6	V
V_{SV3V}	SV3V	3 V supply voltage range	-0.3 to 3.6	V
V_{V1V2}	V1V2	1.2 V supply voltage range	-0.3 to 2	V
V_{VDRV}	VDRV	Secondary side driver voltage	-0.3 to 24	V
V_{SRGD}	SRGD	Sync FET gate driver voltage range	-0.3 to 18	V
V_{SRVDS}	SRVDS	Drain sense voltage range	-2 to 28	V
V_{GPIO}	GPIO0,GPIO1	GPIO voltage	-0.3 to 3.6	V
V_{SPGND}	SPGND	Power ground vs. signal ground	-1 to 1	V

Table 3. Maximum operating conditions

Symbol	Pin	Parameter	Value	Unit
V_{HV}	HV	Voltage range (referenced to PGND)	-1 to 450	V
V_{PVCC}	PVCC	Primary side supply voltage	-0.3 to 16	V
C_{IO}	HON, LON, EN_OUT	Capacitive load on primary side digital outputs	0 to 10	pF
V_{CSP}, V_{CSM}	CSP,CSM	Current sense voltage range	-0.3 to 1	V
V_{SVCC} , V_{VOSNS}, V_{VDRV}	SVCC, VOSNS, VDRV	Secondary side voltage range	-0.3 to 22.5	V

4 ESD immunity levels

Table 4. **ESD immunity levels**

Mode	Pin	Reference specification	Value	Unit
HBM	All	According to JS-001	+/- 2	kV
CDM	All	According to JS-002	+/- 500	V

5 Thermal data

Table 5. Thermal data

Symbol	Parameter	Max. value	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance, Junction-to-ambient[(1)]	65	°C/W
T_J	Junction Temperature Range	-40 to 125	°C
T_{STG}	Storage Temperature	-55 to 150	°C

1. *Simulated, device mounted on 1s1p board*

6 Safety data

Table 6. Insulation safety data according to IEC 62368

Parameter	Value
Insulation type	Reinforced
Transient voltage	4 kV
Electric strength test (type test)	9.6 kV / 1 min
Electric strength test (routine test)	6.4k V / 1 sec
Clearance	8 mm
Creepage	8 mm

Table 7. Insulation safety data according to UL 1577

Parameter	Value
Isolation Voltage	3770 Vrms
Transmitter maximum current	11 mA
Receiver maximum current	91 mA
Transmitter maximum power	1100 mW
Receiver maximum current	130 mW
Maximum operating ambient temperature	85 °C
Maximum junction temperature	125 °C
Maximum storage temperature	150 °C
Maximum data rate	1 MHz

Table 8. X-Cap discharge safety data according to IEC 62368

Parameter	Value
Maximum line voltage	240 Vrms + 10%
Overvoltage category	II
External capacitor value	47 nF – 2.2 µF
Series resistor value	330 Ω – 4700 Ω

7 Electrical data

T_J = -40 to 125 °C, V_{PVCC} = 12 V, V_{SVCC} = 5 V , unless otherwise specified.

Table 9. **Electrical characteristics**

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Primary side						
Supply voltage						
V_{PVCCOn}	Turn-on threshold		13	14	15	V
$V_{PVCCOff}$	UVLO / Restart threshold		6	6.5	7	V
V_{P3V3}	Primary side 3V3 regulator voltage	Iload < 4 mA	3.1	3.3	3.5	V
Supply current						
I_{pq}	Quiescent current	Before turn-on			0.55	mA
I_{cc}	Operating supply current	Fsw=300 kHz, R_{DT}=R_{LEB}=12 kohm, C_{EN}=C_{LON}=C_{HON}=10 pF		2.8		mA
I_{burst}	Current during burst mode				1.1	mA
I_{qdis}	Shutdown quiescent current	Device latched			0.57	mA
High voltage start-up generator						
V_{HV}	HV breakdown voltage	I_{HV} < 100 µA	800			V
$V_{HVStart}$	HV pin start-up voltage			30		V
V_{PVCC_SO}	Switchover threshold			1		V
I_{HVON}	ON-state current	$V_{HV} > V_{HVStart}$ $V_{PVCC} > V_{PVCC\_SO}$		7		mA
		$V_{HV} > V_{HVStart}$ $V_{PVCC} < V_{PVCC\_SO}$		1		mA
I_{HVOFF}	Leakage current (Off-state)	V_{HV} = 400 V		20		µA
X-cap discharge						
T_{XCDDET}	Detection time			64		ms
V_{HVmin}	Peak residual voltage	$I_{HV,DIS}$ > 4.2 mA			45	V
I_{HVDIS}	Discharge current	V_{HV} > 45 V	5			mA
$V_{PVCCClamp}$	PVCC clamp voltage during X-cap			7		V
AC brown-in/out						
V_{HVpk_BO}	Brown-out threshold	Peak voltage	94	100	106	V
V_{HVpk_BI}	Brown-in threshold	Peak voltage	108	115	122	V
V_{HVpk_BI}	Brown-in/out hysteresis	Peak voltage		15		V
T_{BODG}	Brown-out deglitch time		48	60	72	ms
T_{DB_BI}	Brown-in deglitch time			500		µs
Overtemperature protection						
V_{POVTH}	Overtemperature threshold	Pin falling (temperature rising)	0.57	0.6	0.63	V

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{POVTH}	Overtemperature threshold	Pin rising (temperature falling)	1.12	1.24	1.36	
I_{POTP}	POTP pull-up current	V_{POTP} = 0.6 V	18	20	22	µA
Soft-start						
I_{SS}	Soft start current	V_{SS} = 0.25 V	1.7	2	2.3	µA
T_{DT_SS}	Deadtime duration during soft-start	R_{DT} = 100 kΩ	240	300	360	ns
		R_{DT} = 12.1 kΩ	32	40	48	ns
T_{OFFSS}	Off-time duration during soft-start	R_{OSC} = 470 kΩ	8	10	12	µs
		R_{OSC} = 47 kΩ	0.8	1	1.2	µs
V_{SSEND}	Soft-start timeout voltage		0.55	0.6	0.65	V
Overvoltage protection						
V_{OVTH}	Overvoltage threshold (for flyback aux winding)		1.12	1.24	1.36	V
I_{OVTH}	Overvoltage threshold (for forward aux winding)		17	20	23	µA
$V_{OVCLAMP}$	Clamping voltage on OVP pin	OVP sourcing 20 uA	-0.1	0	0.1	V
		OVP sinking 20 uA	3.1	3.3	3.5	V
T_{OVFILT}	OVP time filtering		2	4	6	µs
Overcurrent protection						
V_{OCTH}	Overcurrent threshold		0.8	0.9	1.0	V
Burst mode						
T_{TO}	IsoPWM absence time to trigger sleep mode entry	From PWM falling edge		60		µs
Current mode unit						
G_{TV}	Time to voltage conversion gain	IsoPWM Ton = 380 ns	0.59	0.66	0.73	V/µs
$V_{IPKCLAMP}$	Maximum threshold		0.5	0.525	0.55	V
T_{LEB}	Blanking time (from LON rising edge)	R_{LEB} = 100 kOhm	240	300	360	ns
		R_{LEB} = 12.1 kΩ	33	41	49	ns
T_{CSDEL}	Total time between CS crossing and LON turn-off	Including driver delay. dV/dt = 2 V/us. Time to 50%			25	ns
V_{PCSOFF}	CS comparator offset		-22	0	22	mV
T_{DT}	LS to HS deadtime duration during normal mode	R_{DT} = 100 kΩ	120	150	190	ns
		R_{DT} = 12.1 kΩ	15	22	30	ns
R_{LEB} OPEN protection (ROP)						
R_{LEB_OPEN}	Maximum R_{LEB} resistance to trigger the protection		0.8	1.0	1.25	MΩ
IO electrical data						
V_{OH}	LON/HON high voltage	Pin sourcing 4 mA	4			V
V_{OL}	LON/HON low voltage	Pin sinking 4 mA			0.4	V
Secondary side						
Supply voltage						
V_{SVCCOP}	Secondary side operative range		3.05		22.5	V
V_{SVCCON}	Secondary side turn-on threshold		3.3	3.5	3.7	V

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{SUVLO}	Secondary side UVLO threshold			3	3.05	V
V_{SV3V}	Secondary side 3 V regulator voltage	Iload [1]< I_{SV3V} (2 mA) V_{SVCC} > 3.3	3.1	3.2	3.3	V
I_{SV3V}	Maximum current capability from SV3V for external circuitry		2			mA
V_{CPON}	Charge pump turn-on threshold (hysteretic mode)	In burst mode		8		V
V_{CPOFF}	Charge pump turn-off threshold (hysteretic mode)	In burst mode		8.4		V
Supply current						
I_{SVCC}	Operating supply current			18		mA
I_{sleep}	Deep sleep mode supply current	SVCC=5 V		1.4		mA
SR gate driver						
V_{SRON}	SR driving voltage	SRDRVCONF[2] = 11		5		V
		SRDRVCONF[2] = 10		7		V
		SRDRVCONF[2] = 01		9		V
		SRDRVCONF[2] = 00		11		V
T_{SRPROP}	Driver propagation delay	Turn-on, time to 10%			20	ns
		Turn-off, time to 90%		15	20	ns
T_{SRRISE}	Driver rise time	10% to 90%, 1 nF load		40	65	ns
T_{SRFALL}	Driver fall time	90% to 10%, 1 nF load		20	40	ns
I_{DRVSRC}	Driver source current			0.45		A
I_{DRVSNK}	Driver sink current			0.6		A
Load switch gate driver						
I_{ORON}	Load switch turn-on current			10		µA
V_{ORON}	Load switch-on voltage	Referred to SVCC SVCC < 12 V	4	5	7	V
		Referred to SVCC SVCC >= 12 V	4	5	6.5	V
Current sense						
V_{CSM}	CSM input range[3]		0		50	mV
V_{SCSOFF}	Current sense input offset	Including ADC accuracy Input signal > 4 mV	-0.5		0.5	mV
V_{CSFSR}	Current sense full scale range	CSP – CSM voltage		25		mV
CMRR	Common mode rejection	100 kHz – 1 MHz, 10 mV signal[4]	50			dB
Voltage sense						
V_{FSR}	Full scale range for SVCC & VOSNS reading	VSET[5] = 00		6		V
		VSET[5] = 01		12		V
		VSET[5] = 10		24		V
	Gain error	Including ADC contribution T_j = 0 to 125 °C.	-1		1	%

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
	Offset	Including ADC contribution T_j = 0 to 125 °C	-0.2% * V_{FSR}		0.2% * V_{FSR}	V
Adc						
N_{bit}	Number of bits			12		
INL	Integral non linearity	3% V_{REF} < V_{IN} < 95% V_{REF}(4)	-3		3	LSB
DNL	Differential non linearity	3% V_{REF} < V_{IN} < 95% V_{REF}(4)	-2		2	LSB
Wake-up comparator						
V_{WUP}	Wake-up threshold	DAC(2) = 0000, FSR(5) = 6 V		4.9		V
		DAC(2) = 0001, FSR(5) = 6 V		4.95		V
		DAC(2) = 0010, FSR(5) = 6 V		5		V
		DAC(2) = 0011, FSR(5) = 6 V		5.05		V
		DAC(2) = 0100, FSR(5) = 12 V		8.82		V
		DAC(2) = 0101, FSR(5) = 12 V		8.91		V
		DAC(2) = 0110, FSR(5) = 12 V		9		V
		DAC(2) = 0111, FSR(5) = 12 V		9.09		V
		DAC(2) = 1100, FSR(5) = 24 V		11.76		V
		DAC(2) = 1101, FSR(5) = 24 V		11.88		V
		DAC(2) = 1110, FSR(5) = 24 V		12		V
		DAC(2) = 1111, FSR(5) = 24 V		12.12		V
		DAC(2) = 1000, FSR(5) = 24 V		14.7		V
		DAC(2) = 1001, FSR(5) = 24 V		14.85		V
		DAC(2) = 1010, FSR(5) = 24 V		15		V
		DAC(2) = 1010, FSR(5) = 24 V		15.15		V
		DAC(2) = 0000, FSR(5) = 24 V		19.6		V
		DAC(2) = 0001, FSR(5) = 24 V		19.8		V
		DAC(2) = 0010, FSR(5) = 24 V		20		V
		DAC(2) = 0011, FSR(5) = 24 V		20.2		V
V_{WUPACC}	Wake-up threshold accuracy		-0.9%		0.9%	
$V_{WUPHYSY}$	Hysteresis	HYST(2) = 00, FSR(5) = 6 V		13.5		mV
		HYST(2) = 01, FSR(5) = 6 V		18		mV
		HYST(2) = 10, FSR(5) = 6 V		24		mV
		HYST(2) = 11, FSR(5) = 6 V		34.5		mV
SR comparators						
V_{THSR1V}	SR1V comparator threshold		0.7	1	1.3	V
T_{DSR1V}	SR1V comparator delay	DVS falling @ 0.2 V/ns		20	30	ns
V_{THIZCD}	IZCD threshold		-5	0	2	mV
T_{DIZCD}	IZCD comparator delay	DVS rising @ 0.1 V/µs		50	80	ns
V_{DYNZCD}	VZCD dynamic comparator threshold	Negative step starting from SVCC – 1 V		1		V
Bleeding resistor						
I_{BLEED}	SVCC / VOSNS Bleeding current	ISET(6) = 0, V > 0.8 V	7	10		mA
		ISET(6) = 1, V > 0.8 V	14	20		mA

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
R_{CCBLD}	CC Bleeder resistance	V > 0.8 V		2500	4000	Ω
Clock						
F_{CK}	Master clock frequency	T_j = 0 – 125 °C	126.7	132	136.3	MHz
		T_j = -40 – 125 °C	126.7	132	137.3	MHz
F_{CKLF}	Low frequency clock		60	66	72	kHz
Internal temperature sense						
T_{ACC}	Temperature reading accuracy	ADC reading(4)	-10		10	K
GPIO electrical data						
V_{OHGPIO}	GPIO0/1 high voltage	Pin sourcing 8 mA, digital mode	2.4			V
V_{OLGPIO}	GPIO0/1 low voltage	Pin sinking 8 mA, digital mode			0.4	V
V_{IHGPIO}	GPIO0/1 input high voltage	Digital mode	2			V
V_{ILGPIO}	GPIO0/1 input low voltage	Digital mode			0.8	V
VCONN						
R_{VCONN}	Vconn switch resistance to SVCC	SVCC = 5 V		20		Ω
CC cable connection wakeup						
$V_{THCCWUP}$	CC wake-up threshold		2.5	2.6	2.7	V
CC Communication Wakeup						
	CC communication threshold	Rising		0.85		V
	CC communication threshold	Falling		0.25		V
CC OVP						
V_{CCOVP}	CC OVP threshold		5.5	6		V
CC pullup						
$I_{CCPUVMAX}$	CC Pull-up current at $V_{CCPUMAX}$	V_{CC} = $V_{CCPUMAX}$ = 2.75 V	30			µA
I_{CCPU}	CC Pull-up current	ICCSET(7) = 01 V_{CC1} = V_{CC2}= 2.7 V	64	80	96	µA
		ICCSET(7) = 10 V_{CC1} = V_{CC2}= 2.7 V	166	180	195	µA
		ICCSET(7) = 11 V_{CC1} = V_{CC2}= 2.7 V	303	330	360	µA

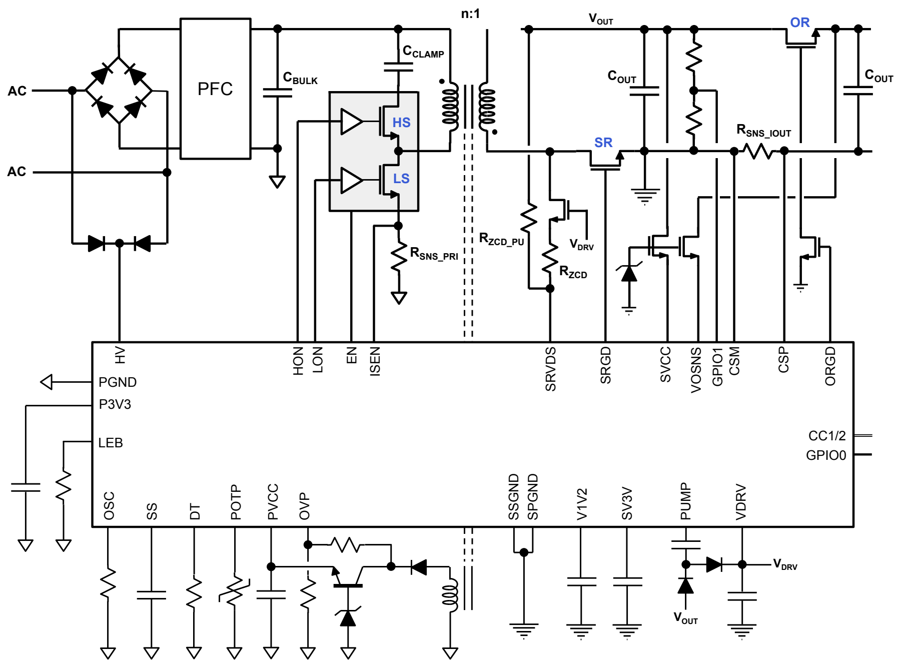
1. *Iload is the current drawn by external circuits connected to SV3V pin.*
2. *This internal peripheral register is managed by the firmware according to the parameter configuration. See Device setup and User personalization*
3. *Current sense accuracy is not guaranteed if CSM pin voltage is beyond this range*
4. *Guaranteed by design.*
5. *This internal peripheral register is managed by the firmware depending on the output voltage setpoint. See Voltage sensing*
6. *This internal peripheral register is managed by the firmware. See Bleeding*
7. *This internal peripheral register is managed by the USB-PD protocol FW according to the standard*

8 Device operation

8.1 Typical application schematic

The following image is a simplified schematic for the typical application

Figure 4. **Typical configuration**



The ST-ONEHP is a very intergrated IC, which needs a few external components to build a complete system. On the primary side:

- An AC full wave power rectifier connected to a bulk capacitor, or a PFC if high power factor is required.
- Two rectifier diodes to provide HV voltage to ST-ONE IC both for high voltage startup and AC brownout and disconnection detection.
- An integrated half bridge power stage (e.g ST MasterGaN) or Gate driver + FETs connected to the transformer primary winding.
- A clamp capacitor to store the residual energy in the transformer leakage inductance.
- An auxiliary winding power supply for the IC PVCC, also used to perform overvoltage function during the soft-start.

On the secondary side:

- A synchronous rectifier FET is connected to the SRGD pin.
- A cascode FET connected to the SRVDS pin to provide synchronous rectifier drain voltage sense while limiting the voltage on the pin below its AMR.
- A circuit connected to ORGD pin to drive a load switch to disconnect the output voltage as required by USB-PD power supplies.
- A sense resistor is connected to CSM/CSP pins to read the output current.
- A capacitor and two diodes connected to the PUMP pin to implement a charge pump providing the driving voltage to the synchronous rectifier.
- A clamp FET to limit the voltage on the SVCC to a value which must be below its maximum rating and above 15V
- A resistor divider to read the output voltage above 15V
- A clamp circuit to limit the voltage on VOSNS below its maximum rating

8.2 External component selection

8.2.1 Symbols used in this section

I_{pk} peak magnetizing current
L_p primary side inductance
L_k primary side leakage inductance
V_i converter input voltage
V_o converter output voltage
n transformer turns ratio
T_{sw} switching period
f_{sw} switching frequency
P_o converter output power
D duty cycle
C_{ph} phase (switching) node total capacitance (typically, switch C_{OSS} + transformer input capacitance)
C_{clamp} clamp capacitor value
V_{priPk} peak primary side voltage
f_{samp} control loop sampling frequency
C_{out} output capacitor value
V_{drop} voltage drop during step load transient
I_{step} load transient current step

8.2.2 Transformer design

8.2.2.1 *Turns ratio*

The ideal operating condition for a flyback is with duty cycle around 50%. The turns ratio is anyway limited by the voltage capability of the primary side switches.

As a first approximation, the turns ratio can be selected considering the maximum input and output voltage and selecting the highest value for which the voltage stress on the primary side switches is acceptable.

The voltage stress can be calculated as

$$V_{priPk} = V_i + nV_o + I_{pk}\sqrt{\frac{L_k}{C_{clamp}}} \tag{1}$$

The last term in the equation can be ignored for a first approximation, then considered after component selection.

Typical turns ratio value for a 140W, 28V output USB-PD EPR application is around 4 to 4.5.

8.2.2.2 *Primary side inductance – switching frequency*

The ST-ONE Non complementary active clamp operates in a similar way as a quasi-resonant flyback, so as a first approximation the relation between the switching frequency and the primary side inductance can be calculated as

$$L_p = \left(\frac{V_i nV_o}{V_i - nV_o}\right)^2 \frac{1}{2f_{sw}P_o} \tag{2}$$

For a more accurate calculation the clamping time and the deadtimes must be considered, especially for high frequency converters. The following equation can be used to calculate the switching frequency when the system operates in ZVS:

$$T_{sw} = \frac{2L_p(V_i + V_{or})\left(\frac{P_i(V_i + nV_o)}{V_i nV_o} + \sqrt{\frac{C_{ph}\left(V_i^2 - n^2V_o^2\right)}{L_p}}\right)}{V_i nV_o} + \frac{\pi\sqrt{L_pC_{ph}}}{2} \tag{3}$$

8.2.3 Clamp capacitor selection

The clamp capacitor value determines the resonance period between the capacitor and the transformer leakage inductance during phase 5 of the switching cycle (see Normal switching mode).

It is suggested to choose the clamp capacitor value so that the phase 5 lasts approximately 15% of the switching cycle in high line, high output voltage conditions, so

$$C_{clamp} \approx \frac{(0.15T_{sw})^2}{\pi^2 L_k} \quad (4)$$

8.2.4 Secondary side drain sensing

The SRVDS pin is used for sensing the synchronous rectifier drain voltage to control turn-on and turn-off of the synchronous rectifier MOSFET and to sense the drain oscillations to operate in valley switching. The first function is performed by comparing SRVDS voltage with a 1 V and a 0 V internal threshold, while the second function is implemented by comparing the SRVDS voltage with SVCC.

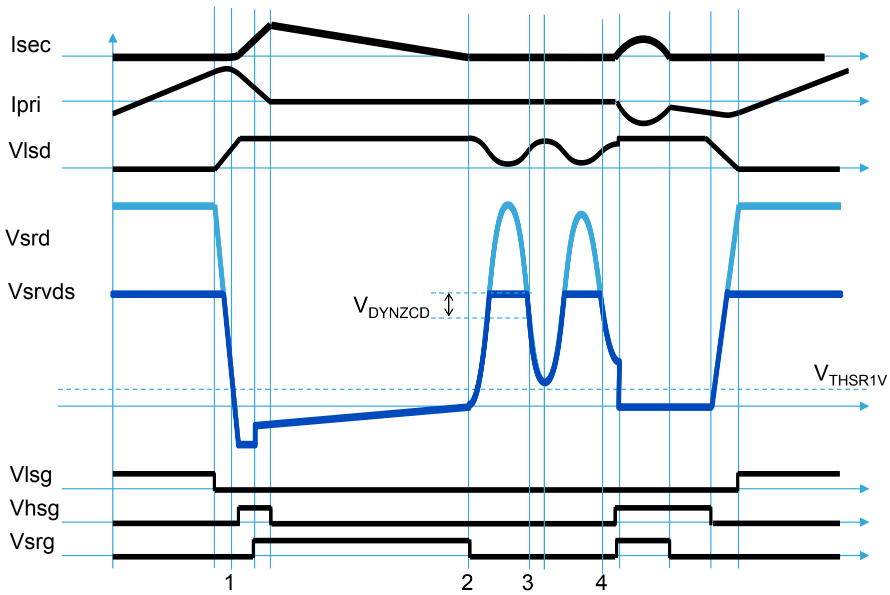
A proper external clamp circuit is required to limit the voltage on the pin below its operative range while being able to correctly sense the MOSFET drain voltage from 0 V up to SVCC. A signal mosfet with gate tied to VDRV as shown the typical configuration schematic (see Figure 4) is the suggested solution. The resistors R_{ZCD} and R_{ZCDPU} in the schematic can be added to offset the signal and anticipate the IZCD comparator triggering.

8.2.4.1 SRVDS comparators

The SRVDS pin has three comparators connected to it which are used to control the switching cycle.

The following figure shows the waveforms associated to the SRVDS comparators when the system is operating in valley skipping mode. The SR drain voltage is drawn as a light blue line, the clamped voltage on the SRVDS pin is shown in dark blue.

Figure 5. SRVDS sensing waveforms



VZCD: This comparator is used to count the switching node oscillations in valley skipping mode and to obtain valley turn-on. The comparator has a dynamic threshold, detecting when the voltage on SRVDS drops more than V_{DYNZCD} below the last peak reached. Referring to Figure 5, the comparator is triggered in instant 3 and 4

IZCD: This comparator compares SRVDS with SSGND. It is used to detect the zero crossing of the current during SR mos conduction phase. Referring to Figure 5, the comparator is triggered in instant 2.

SR1V: This comparator compares SRVDS with a 1 V threshold. It is used to detect when the primary side low side FET is turned off, making the voltage across the SR MOS drop. This comparator commands the turn-on of the SR mos. Referring to Figure 5, the comparator is triggered in instant 1.

8.2.5 Secondary side current sense resistor

The secondary side current sense has a full-scale range V_{CSFSR} equal to 25 mV. The current sense is chosen according to the formula:

$$R_{senseSec} < \frac{V_{CSFSR}}{I_{MAX}} \quad (5)$$

8.2.6 Voltage sense resistor divider

The secondary side voltage is read through an external resistor divider connected on the GPIO 1 pin whenever the voltage exceeds 15 V. The resistor divider ratio can be chosen by the user, the value shall be programmed in the device parameters to obtain the correct output voltage regulation.

The default value for the resistor divider is 14.96:1, which can be obtained using 127 kΩ and 9.1 kΩ resistors. This value is suggested for applications which provide up to 28 V on the output.

8.3 High voltage startup

The ST-ONE is equipped with internal HV start-up circuitry dedicated to supplying the IC during the initial start-up phase, before the self-supply winding is operating. An external capacitor connected to the PVCC pin is charged by the HV start-up circuitry, connected to the HV pin.

When the power is applied to the circuit and the voltage on the input is high enough, the HV generator is sufficiently biased to start operating, thus it draws the current I_{HVON} through the HV pin and charges the capacitor connected between PVCC pin and ground. This charging current is limited at 1 mA in case the voltage on PVCC is lower than V_{PVCC_SO}, in order to prevent excessive IC dissipation if the pin is accidentally shorted to ground.

As the PVCC voltage reaches the start-up threshold (V_{PVCCOn}) the chip starts operating, and the control logic disables the HV generator.

The IC is powered by the energy stored in the PVCC capacitor until the auxiliary winding develops a voltage high enough to sustain the operation.

8.4 Soft-start

As soon as the proper conditions for startup are met, the primary side controller performs a soft-start autonomously until the secondary side is powered and able to take control of the switching.

During soft-start the IC operates in constant off-time, peak current mode. The user can set the off-time by connecting a resistor from the OSC pin to ground.

The peak current during soft-start is determined by comparing the SS pin and ISEN pin voltages. Connecting a capacitor to the SS sets the soft-start duration.

The primary side controlled soft-start ends as the secondary side takes control of the conversion.

During the soft-start the high-side is controlled in complementary mode, with deadtimes determined by a resistor connected between DT and ground. Note that during soft-start both the deadtimes are equal to T_{DT_SS} which is approximately double the value used in normal mode for LS to HS.

As the voltage on the secondary side reaches V_{SVCCON} the secondary side IC boots up, takes control of the conversion and the converter starts to operate in normal mode as described in Section 8.5.1. The secondary side controller continues the soft-start operating in closed loop and ramping the SVCC voltage to 5 V, then the soft-start ends.

Figure 6. Soft-start waveforms : primary side controlled soft-start phase

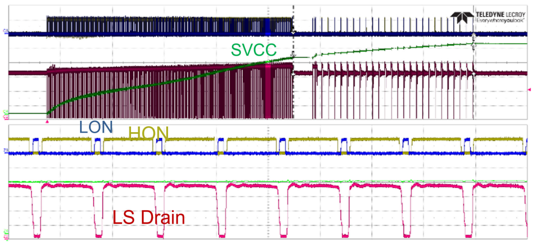
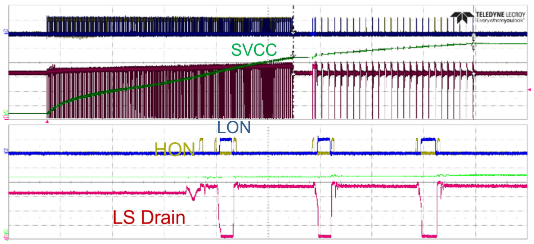


Figure 7. Soft-start waveforms: switch to secondary side control



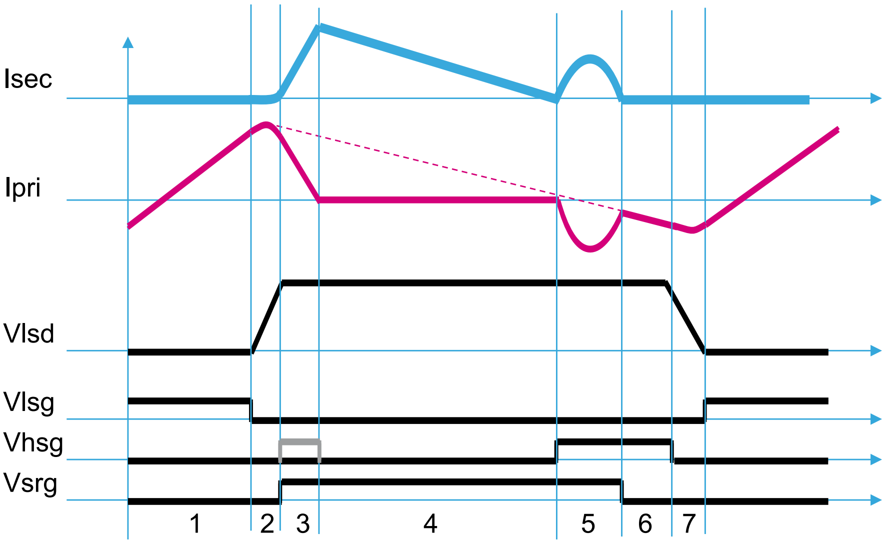
8.5 Switching modes

The following sections describe the switching modes which are used by the device depending on the output power to be delivered.

8.5.1 Normal switching mode

The controller operates a non-complementary active clamp converter. The main waveforms are shown in Figure 8.

Figure 8. Normal operation waveforms



The converter operation is similar to a traditional QR flyback, with the addition of a clamp switch to recover the energy in the transformer leakage inductance at low-side turn-off and uses the energy to obtain soft switching at low-side turn-on. In particular, the high-side is turned on for a time proportional to the input/output conversion ratio in order to limit the circulating current to what is required to obtain soft switching at low-side turn-on. The synchronous rectifier is kept on after high-side turn-on to obtain zero secondary side current before the high-side is turned off and a new cycle is started through a resonance between the leakage inductance and the clamp capacitor.

The phases are as follows:

1. LS turn-on. The on timing and peak current are defined by the secondary side controller. The phase terminates when the primary side peak current comparator is triggered.
2. Deadtime. A deadtime is inserted between LS turn-on and HS / SR turn-on.
3. SR turn-on / first HS turn-on. When the secondary side ZCD12 comparator is triggered, the secondary side commands the turn-on of both SR and HS switches. During this phase the current in the primary side leakage inductance drops to 0, while the energy is stored in the clamp capacitor. The HS switch turn-on is not strictly required but improves the efficiency of the system by avoiding conduction through the HS body diode. The duration of the first HS pulse can be controlled by the configuration parameters.
4. During phase 4 current flows on the secondary side through the SR FET. The phase terminates when the IZCD comparator is triggered (current on the secondary side reached 0).
5. HS is turned on to recover the energy stored in the clamp capacitor in phase 3 and to store energy in the primary side inductance to force a soft switching. During this phase the leakage inductance resonates with the clamp capacitor, creating a bump on the output current. When the current reaches 0 the SR is turned off. The duration of this phase is configured through programmable parameters.
6. Extra HS turn-on time may be added to increase the energy stored in the magnetizing inductor, in particular at low output and high input voltage. The firmware calculates the duration of this phase based on parameters.
7. Deadtime. The deadtime between HS and LS is controlled by the secondary side through the parameter DT_HVG_LVG.

8.5.1.1 Deadtime

Deadtime between LS on and HS on is set by connecting a resistor between DT pin and ground, according to the following formula:

$$t_{DT\_LS\_HS} = 3.88\text{ns} + 1.46\frac{\text{ns}}{\text{k}\Omega} \cdot R_{DT} \quad (6)$$

Deadtime between HS and LS is instead controlled by the controller parameter DT_HVG_LVG according to the formula:

$$t_{DT\_HS\_LS} = \frac{DT\_HVG\_LVG}{F_{CK}} \quad (7)$$

Where F_{CK} is the IC clock frequency of 132 MHz.

8.5.1.2 *Synchronous rectification voltage*

The synchronous rectifier turn-on voltage is clamped to a programmable value. The user can choose the driving voltage which yields the best application performance.

The driver is powered from the VDRV pin.

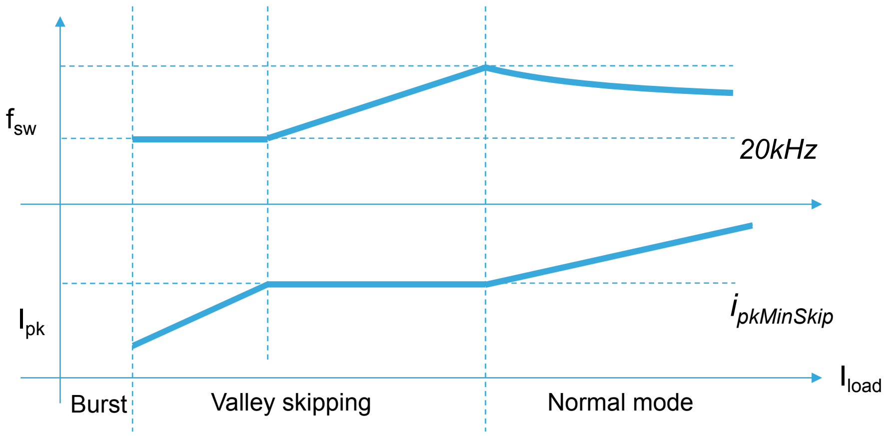
8.5.2 Skip mode

In order to improve the efficiency at medium load, the controller enters in valley skipping mode when the peak current falls below a programmable value.

While in skip mode the controller keeps the peak current approximately constant at the skipping mode entry point.

If the frequency falls below approximately 20 kHz, the controller starts dropping the peak current while keeping the frequency limited between 20 kHz and a programmable value (typ. 50 kHz).

Figure 9. Transition between normal mode, skip mode and burst mode



8.5.3 Burst mode

While in skip mode, if the frequency drops below F_{CK}/6500 (approximately 20 kHz) the system enters burst mode.

While in burst mode the controller generates bursts of pulses with a programmable peak current. The number of pulses generated depends on the output voltage and can be programmed through the parameters.

The system exits burst mode and comes back to normal operation when the average time between bursts drops below a programmable time.

8.5.3.1 *Deep burst*

When the regulated output voltage is 5 V or 9 V, all the IC functions are shut down between the bursts, leaving only a dedicated comparator to wake up the system when a new burst is required. In this condition, the consumption of the secondary side IC drops to I_{sleep}. For any other regulation voltage, the burst is controlled by the firmware and ADC readings, so the IC consumption between bursts is close to the normal mode operating current.

8.5.4 Special modes for voltage transitions

Protocols like USB-PD require to change the output voltage while the converter is operating following specific timing requirements. ST-ONEHP provides special operating modes to Manage negative transition while the applied load to the converter is very low.

8.5.4.1 *Bleeding*

The device integrates bleeding current sinks to discharge the output during negative voltage transitions which may happen at light load.

Bleeding current I_{BLEED} is initially set to 10 mA, then increased to 20 mA.

8.5.4.2 *Forced burst*

In order to maintain the primary side PVCC powered, the IC forces bursts at regular intervals to recharge the primary side through its auxiliary winding.

8.5.4.3 *Active bleeding mode*

The IC can be configured to operate in a reverse flyback mode transferring energy from the output capacitor to the input bulk capacitor by switching the SR MOSFET.

This function is useful when the 20 mA bleeding current is not enough to meet the negative transition timing specifications, for example in applications with a big SVCC capacitor.

8.6 Control loop

The controller includes a peak current mode regulation loop to control the output voltage.

8.6.1 Voltage sensing

The IC senses the output voltage through a programmable resistor divider connected to the internal 12 bit ADC when the target voltage is below 15 V, otherwise the output voltage is sensed through an external resistor divider on pin GPIO0.

The internal resistor divider rescales the SVCC voltage so that the full scale can be configured as 6 V, 12 V or 24 V. The IC selects the scale depending on the target output voltage.

The thresholds for switching then internal scales are 5.8 V and 11.8 V, while the threshold to switch to the external divider is 15V.

During output voltage transitions, the greater scale between the initial and final voltages is used. At the end of the transition the scale is changed according to the final voltage.

For example in a transition from 5 V to 9 V the scale is initially switched to 12 V, at the end of the transition it is kept at 12 V scale. For a transition 9 V to 5 V, the scale is kept at 12 V and at the end of transition is changed to 6 V scale.

8.6.2 Peak current mode unit

The primary side low-side switch is controlled in peak current mode.

At every switching cycle LON stays high for the blanking time T_{LEB}. After the blanking time is expired, the LON is turned off when the CS comparator is triggered.

8.6.2.1 *Reference generator*

During normal operation the reference for the peak current mode control is provided by the secondary side through the galvanic isolation communication channel.

The primary side IC converts the duration of pulses received by the secondary side in a voltage reference for the peak current comparator according to the equation

$$v_{pk} = G_{TV} t_{pulse} \tag{8}$$

The reference voltage is limited by a hardware clamp to $V_{IPKCLAMP}$.

The pulses are generated by the secondary side SMEDs.

8.6.3 Voltage loop

The voltage loop is managed by a digital PI (Type2) controller.

The device parameters control the proportional and integral gain of the controller. If sampling effects are ignored, the controller gain can be expressed as follows:

$$\frac{I_{peak}}{V_{err}} = \frac{G_{TV}}{R_{sense}} \frac{8}{F_{ck} V_{fsrMax}} \left(PID\_Pgain + \frac{1}{sT_{samp}} PID\_Igain \right) \tag{9}$$

Where R_{sense} is the primary side current sense resistor value, Fck is the clock frequency (132 MHz typ.), V_{fsrMax} is the ADC full scale range at the highest scale (24 V), G_{TV} is the time-voltage converter gain and T_{samp} is the control loop sampling period (30 us).

Considering the primary side peak current to average output current relation, the equation can be written as:

$$\frac{I_{sec}}{V_{err}} = \frac{nV_{in}}{nV_{out} + V_{in}} \frac{G_{TV}}{R_{sense}} \frac{4}{F_{ck}V_{fsrMax}}\left(PID\_Pgain + \frac{1}{sT_{samp}}PID\_Igain\right) \tag{10}$$

Where n is the turns ratio (primary to secondary) and I_{sec} is the transformer secondary side average current.

8.6.3.1 *Setting the voltage loop parameters*

The loop cutoff frequency is dominated by the proportional part of the controller, and can be approximated as:

$$f_t \approx \frac{1}{2\pi} \frac{G_{TV}}{R_{sense}} \frac{8}{F_{ck}V_{fsrMax}} PID\_Pgain \frac{nV_{in}}{nV_{out} + V_{in}} \frac{1}{C_{out}} \tag{11}$$

The proportional gain can be set as:

$$PID\_Pgain = f_t \frac{\pi R_{sense} F_{ck} V_{fsrMax}}{4G_{TV}} \frac{n\frac{V_{out}}{V_{in}} + 1}{n} C_{out} \tag{12}$$

It is advisable to keep the cutoff frequency at least below 1/5 of the loop sampling frequency, i.e. below 8 kHz. If no need for fast transient response is required, a lower bandwidth helps in limiting the control noise.

The integral gain determines the loop zero frequency as:

$$PID\_Igain = PID\_Pgain \cdot 2\pi f_z T_{samp} \tag{13}$$

8.7 Fault management

The IC includes many protections to avoid damage to the converter or to the load in abnormal or failure conditions.

8.7.1 Fault modes

The faults can be either managed as auto-restart, latched, or conditioned restart. The behavior of each fault is described in Fault summary.

8.7.1.1 *Auto-restart mode*

In auto-restart mode, once the protection is tripped, the switching activity is stopped, and the condition is maintained until V_{PVCC} goes below the $V_{PVCCOff}$ restart voltage and then rises again to V_{PVCCOn} for six times. Ultimately, this results in a low frequency intermittent operation (Hiccup-mode operation).

8.7.1.2 *Latched mode*

In latched mode the protection is maintained until the input main is removed. During this time the HV generator is activated periodically to cycle the supply voltage between V_{PVCCOn} and $V_{PVCCOff}$. The condition is indefinitely maintained until the AC mains is removed triggering a brown-out or an X-Cap discharge fault which clears all fault conditions.

8.7.1.3 *Conditioned restart mode*

Faults like the overtemperature or the brown-out, require the fault condition to disappear before the system can restart. When the fault condition is no longer present the system restarts after V_{PVCC} goes below $V_{PVCCOff}$ restart voltage and then rises again to V_{PVCCOn}.

8.7.2 Soft-start timeout

As a protection from secondary side failures, the IC stops switching if no signal is received from the secondary side before the SS pin voltage reaches V_{SSEND}.

This fault is managed as auto-restart.

8.7.3 Soft-start overvoltage protection

The primary side IC includes a detection circuit to avoid generating overvoltage on the output when the secondary side is not active. The OV function operates only during primary side soft-start: as the secondary side takes control, the protection is managed by the secondary side.

The overvoltage function of the ST-ONEHP device monitors the voltage on the OVP pin during HS MOSFET's on-time, when the voltage generated by the auxiliary winding tracks converter's output voltage.

The overvoltage protection is adapted for both flyback and forward mode auxiliary windings. In flyback mode, the auxiliary winding is coupled with the same polarity as the output winding, so when the voltage is positive it reflects the output voltage. In forward mode, the auxiliary winding has a reversed polarity, so when the voltage is positive it reflects the input voltage. This option can be advantageous when the output voltage range is very wide. Both protections for flyback and forward mode OV are active at the same time. The application circuit is designed to allow only the proper protection to be triggered.

To reduce sensitivity to noise and prevent the protection from being erroneously activated, the OVP comparator must be asserted for a time longer than T_{OVFILT} for the protection to be triggered.

8.7.3.1 *Flyback aux winding*

For flyback windings the OVP condition is detected by comparing the voltage on OVP pin with the V_{OVTH} threshold.

8.7.3.2 *Forward winding*

The OVP pin is clamped at $V_{OVCLAMP}$ when sourcing current, avoiding it reaching negative voltages. The current sourced by the clamp is measured and compared with I_{OVTH} to detect the OV condition.

8.7.3.2.1 OV pin clamping

The OV pin is protected from overvoltage by an internal clamp at 3.3 V, able to sink up to 200 uA.

8.7.3.3 *Soft-start OV Threshold selection*

Since the primary side OV is active only during the primary side soft-start, it is suggested to set the threshold to a value which lies between the secondary side turn-on threshold and the maximum secondary side voltage.

Values between 10 V and 15 V are typically good for many applications: the higher voltages are reached only when the secondary side is controlling the conversion and the primary side is disabled.

8.7.4 Ac brown-out protection

The ST-ONE device is equipped with brown-out protection to prevent the operation at too low ac input voltage. Power conversion starts only when the voltage on HV becomes higher than V_{HVPk_BI}.

If the voltage on HV remains below V_{HVPk_BO} for more than T_{BODG} the power conversion is turned off until the voltage goes back above V_{HVPk_BI}. The T_{BODG} masking avoids unexpected turn-offs due to disturbances or line dips.

8.7.5 Primary side overcurrent protection (OCP)

The primary side device includes protections to avoid uncontrolled current rise in the transformer.

8.7.5.1 *First level overcurrent protection*

The first protection level is provided by a clamp on the primary side current mode unit comparator which guarantees that, after the blanking time is expired, the LON signal is turned off if the voltage on the ISEN pin bypasses $V_{IPKCLAMP}$. Even if this limit is reached, the device keeps operating unless other faults are triggered, for example if the current limitation causes an unvervoltage on the output voltage.

8.7.5.2 *Second level overcurrent protection (OCP)*

The device is protected against short-circuit of the secondary rectifier, short-circuit on the secondary winding or a hard-saturated transformer. A comparator monitors continuously the voltage on the CS pin and activates a protection circuitry if this voltage exceeds V_{OCTH}.

To distinguish an actual malfunction from a disturbance (e.g. induced during ESD tests), the first time the comparator is tripped the protection circuit enters a “warning state”. If in the subsequent switching cycle the comparator is not tripped, a temporary disturbance is assumed, and the protection logic is reset in its idle state; if the comparator is tripped again a real malfunction is assumed and the device is stopped.

The fault is managed in auto-restart mode.

8.7.6 Primary side overtemperature protection

The primary side device can be protected from excess temperature by connecting a thermistor to the POTP pin.

When the voltage on POTP drops below V_{POVTH} the conversion is stopped and the device enters fault.

The fault is managed as conditioned-restart.

8.7.7 Primary side undervoltage lockout

In case the voltage on PVCC drops below $V_{PVCCOff}$ the IC enters auto-restart fault mode.

8.7.8 Fault summary

The following table summarizes the faults and their effect.

Table 10. Faults table

Fault	Side	Effect	Comment
UVLO	Primary	Auto-restart	
OVP	Primary	Enter burst	Primary side stops and enters burst. In case the secondary side gives no signal, the system enters UVLO.
OCP	Primary	Auto-restart	Second level OC may happen in case of output short. The effect is a shutdown.
SSTO	Primary	Auto-restart	Soft-start timeout (SS pin reached V_{SSEND}).
POTP	Primary	Conditioned-restart	Overtemperature protection.
BO	Primary	Conditioned-restart	In case of brown-out, switching is stopped. Primary side stops until the BO condition disappears. All fault conditions are cleared.
XCD	Primary	Conditioned-restart	X-Cap discharge is managed in the same way as brown-out.
OCP	Secondary	Load switch Turn off	If load switch is not present, protection is performed by primary side OCP.
OVP	Secondary	Enter burst	If OVP is triggered secondary side stops and waits the voltage drop under safe condition.
UVP	Secondary	Auto-restart	If UVP last for 6.6ms the system stops switching waiting for primary side restart.
UVLO	Secondary	Auto-restart	If secondary side hits UVLO, the system stops switching waiting for primary side restart.
SOTP	Secondary	Auto-restart	The secondary overtemperature value is programmable and is considered also a warning temperature (if enabled) before the SOTP. The fault does not stop switching, but turns off the load switch and sends a hard reset command on the USB-PD.

8.8 X-cap discharge

Safety regulations such as IEC 62368-1 require that the capacitors directly connected to the input plug (so called “X-Caps”) are discharged when the converter mains connector is removed from the outlet, in order to avoid the risk of electrical shock to the user.

Typically, this function is performed by means of a resistor in parallel, but this method cannot be applied in case the converter requires very low power consumption during light-load or no-load operation, because the losses of the X-cap discharging resistor would be too high.

The ST-ONEHP monitors the input voltage through the HV pin and discharges the X-capacitors through the HV pin T_{XCDDET} after a plug disconnection is detected.

The discharge continues until the voltage on HV falls below V_{HVmin} or the plug is connected again.

Note that a DC voltage on the HV pin is interpreted as a plug disconnection, so the device cannot operate with DC input voltage.

8.9 IC Supply

8.9.1 Primary side LDO

A 3.3 V regulator generates the voltage for internal circuitry and digital I/Os. The regulator requires an 100 nF capacitor connected from P3V3 to PPGND.

8.9.2 Secondary side Charge pump & LDO

An internal LDO provides the supply for the IC analog & digital circuits. The SV3V internal LDO can be used to supply external circuits up to 2 mA.

A voltage doubler charge pump provides the driving voltage for the synchronous rectifier. The voltage which can be obtained is approximately 2 * (SVCC – Vf), where Vf is the external diode forward voltage.

The charge pump is turned on when the regulation voltage is below a threshold set by the configuration parameters.

A second LDO provides the 1.2 V supply for the IC logic.

8.9.2.1 LDO decoupling

The 3V3 LDOs require a 1 uF ceramic capacitor to ground to decouple the supply voltage and guarantee stability.

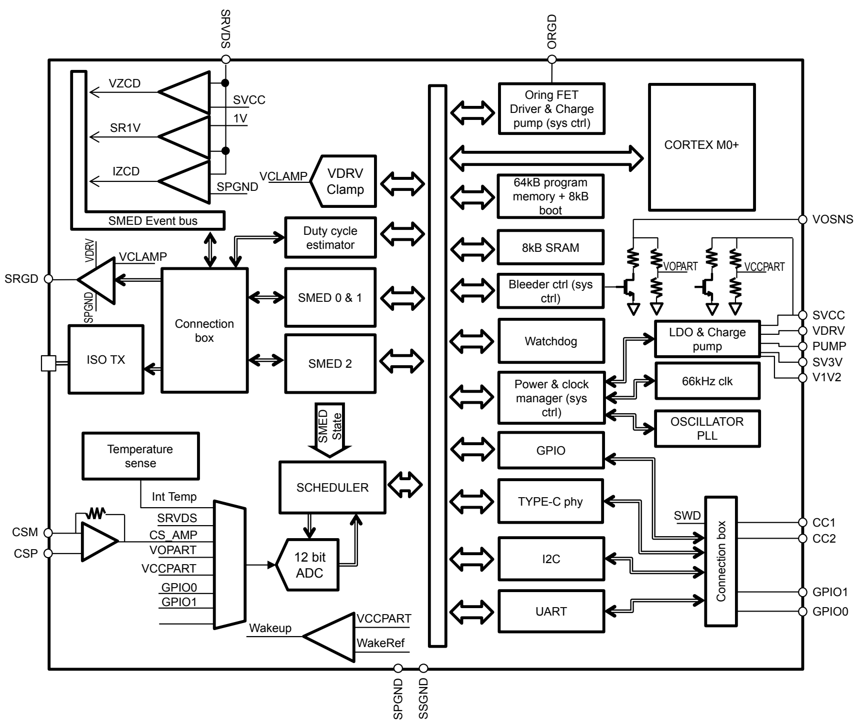
The V1V2 LDO requires a 4.7 uF ceramic capacitor to ground.

The capacitors should be located as near as possible to the device.

8.10 Secondary side controller

The secondary side includes a digital controller which is in charge of both the power conversion and the communication with the load through USB-PD.

Figure 10. Secondary side block diagram



8.10.1 Microcontroller core

The secondary side is controlled by a Cortex M0+ core clocked at $F_{CK}/2$, with 8 kB static RAM and 64 kB programmable flash code memory. The flash is loaded in production with a complete code managing both the voltage conversion of an active clamp flyback and the protocol for EPR USB-PD.

A dedicated 8 kB ROM area is reserved for the boot activity and trimming area.

8.10.1.1 *Parameter memory*

A section of the flash is dedicated to parameters which can be programmed by the user to tune the power conversion, set up the application functionality, choose the protocol and the PDOs or APDOs to be used.

8.10.2 SMED

A set of dedicated event driven state machines can generate complex PWMs. The transitions between the states can be controlled by either timings or external events, or a combination of the two.

The SMED configuration is fully managed by the IC firmware to implement the control modes described in Switching modes.

9 Communication interface

9.1 USB-PD protocol

The USB-PD module controls the USB Type-C™ connector signals and power delivery on Vbus line using USB-PD protocol.

The ST-ONEHP device can provide an output voltage between 3.3 V to 48 V. The PDOs or APDOs used in the application can be defined by the user (except for the mandatory 5 V).

The module provides the USB-PD Source layers over one power channel. This is the list of the USB-PD options available on the ST-ONEHP USB-PD firmware stack embedded on the device.

The USB-PD module supports:

- One USB-PD power SOURCE channel (DFP - AC adapter)
- USB-PD REV 3.1 specification
- EPR (Extended Power Range) with AVS (Adjustable Voltage Supply) support
- Vconn source with 100 mW output power used to identify Electronically Marked Cables
- Send Alert on OTP and OCP protections
- Send Source_Capability_Extended message

The USB-PD module does NOT support:

- PPS mode
- Communication via USB (D+/D- and or SSTx+/- and SSRx+/-)
- Fast Role Swap
- VDM message management apart from SVDM-SOP’ to manage the cable discovered
- Battery Supply PDO and Variable Supply PDO
- Power Sharing
- Unchunked message
- Type C authentication 1.0 extension
- Firmware update using 1.0 extension

9.1.1 USB-PD Physical layer

The device includes a complete physical layer for USB-PD applications.

The CC pins can withstand up to 24 V. An external clamp is required to manage accidental shorts to Vbus for applications providing a higher voltage.

9.1.1.1 CC Pins Vconn

The IC includes an internal switch between CC1/2 and SVCC which is used to provide the VCONN for electronically marked cable detection. The Vconn switch is current limited to avoid damaging the IC in case of short on CC pins.

As required by the USB-PD standard, the CC pins include an integrated bleeder resistor with value R_{CCBLD} which is turned on for 10 ms when the Vconn is removed.

The CC Vconn directly connects the CC1 or CC2 pin to the SVCC voltage, so it can be used only when the regulated voltage is 5 V, as during the Electronically Marked Cable detection.

9.1.1.2 CC OV comparator

The CC pins include a comparator to detect abnormal voltages on the pins caused, for example, by shorts to Vbus.

9.1.2 USB-PD PDO and APDO adaptation and protection

During the attach procedure, the Source and Sink verify the voltage and current, offered and requested. As defined by the USB-PD protocol, upon cable connection the device checks the cable capabilities; in case the cable used is not 5 A capable, the maximum current in all the PDOs and APDOs sent upon capability request is limited to 3 A.

In case of secondary side temperature protection, the capabilities are modified depending on the temperature level.

9.1.3 USB-PD alert management

The device implements protections such as UVP, OVP, OCP. Some, for this mode, are reported during the USB-PD message exchange between source and sink. In some cases of this alarm type, the VBUS is automatically disconnected and no message is sent.

The temperature is also verified and controlled. The corresponding bit into alert messages is managed.

9.1.4 Overcurrent management

The IC manages the OCP and turns off the load switch according to the USB-PD standard.

The OCP level and behavior depends on the PDO or APDO selected by sink.

- if a PPS APDO is selected, the current is limited in the CC mode if the Vout is more than PPS_Vout_min. If the output voltage drops below PPS_Vout_min, the power module disconnects the Vbus.
- otherwise (e.g. if an SPR PDO is selected), the OCP is set up adding the 5.5% of max. current defined on the PDO. If an OCP is detected, the load switch is turned off and Vbus is disconnected.

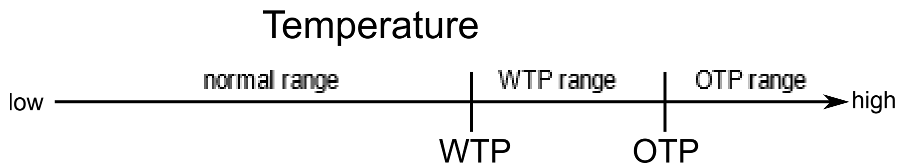
9.1.5 Temperature management

The ST-ONE device supports two temperature measurement points on the secondary side, one internal to the device and one external using an optional NTC.

- The internal temperature is relative to the device and, normally, the default limit is considered good for most applications. The internal temperature sense can read between 0 °C and +150 °C, with an accuracy of T_{ACC} (see Electrical data).
- The external temperature limit is defined by the user by connecting an external resistor divider using an NTC. The user can program the voltage thresholds for the overtemperature fault (OTP) and warning (WTP).

The device implements the secondary side Overtemperature Protection (SOTP) and Warning Temperature Protection (WTP). The temperature trip points are programmable, and separate thresholds can be set for internal and external temperature sense.

Figure 11. Temperature management



In case of overtemperature (temperature higher than OTP limit), the HARD_RESET message is sent out and the next capability proposed is only 5 V and 500 mA. In case the OTP is confirmed for 10 seconds, the Vbus voltage is switched off. The Vbus voltage is provided only when the secondary temperature returns below OTP-10 °C for the internal temperature or below OTP-Hysteresis in case of external temperature. In case the OTP is triggered, the charger functionality is restored if either:

- the AC line is removed, and the temperature returns into an acceptable range.
- the internal temperature returns below WTP range. In that case, the default contract is established automatically.

The WTP range is a range between the WTP point and the OTP point.

When the temperature enters the WTP range the device sends an Alarm message, and if the system is in EPR mode the device leaves EPR mode. In case of new capability request or new contract, the next capability message limits the current/power, depending on the setup on the configuration area.

When the temperature exits from the WTP range and enters into normal range the full capabilities and EPR mode are made available.

10 Device setup and User personalization

It is possible to set up device parameters to configure ST-ONEHP behavior. A dedicated GUI and a HW tool are available to change and tune the application behavior during development time. The ST-ONEHP devices are shipped with a pre-defined set-up, but the user can change it using the serial line.

The entire device setup is always modifiable using a dedicated tool. In case the write protection is enabled on the device, the user can only delete this memory area. The devices set-up area is divided into different zones, application set-up area, application parameter area, USB-PD area and power area.

The data area is protected by CRC32 reverse polynomial (ISO 3309 - 0xedb88320).

Please check the ST-ONEHP Parameter Configuration Manual document which specifies any detail regarding the User personalization.

The same tools can be used also to update the entire program file area with a new firmware version or a dedicated firmware. The program file area is protected by CRC32 reverse polynomial.

10.1 Application set-up area

This area stores all the values used to configure the application. This area is read by the Boot code during startup.

10.2 Application parameters area

The Application parameters area contains the secondary overtemperature protection levels (SOTP). The SOTP levels are divided into two zones, internal on ST-ONEHP and external.

- The internal temperature is provided by an internal sensor: the user defines the internal temperature trigger point.
- The external temperature requires a thermistor connected to a GPIO pin that is specified in the Application set-up field. The user provides the voltage levels at which SOTP is triggered, and the direction (rising or falling) depending on the external circuit used. External sense circuit is optional, if not connected this function is not available.

The programmability of the ST-ONEHP device also provides a warning temperature limit.

10.3 USB-PD area

The USB-PD area defines which PDOs and APDOs are provided by the USB-PD protocol.

This area contains also the maximum power provided by the ST-ONEHP application. The maximum power value is shared with the SINK during USB-PD messages.

10.4 Power area

The power parameters area stores the parameters required for the switching control, including loop compensation parameters, low power mode settings, etc.

10.5 Default configuration

The default configuration allows the user to set up and define all the parameters .

The default configuration selects the CC1 and CC2 pins as the serial line used to communicate, configure and program the IC through a serial interface. Please visit the product page on www.st.com to find the dedicated HW programmer and software.

11 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

11.1 SSOP36L package information

Figure 12. **SSOP36L package outline**

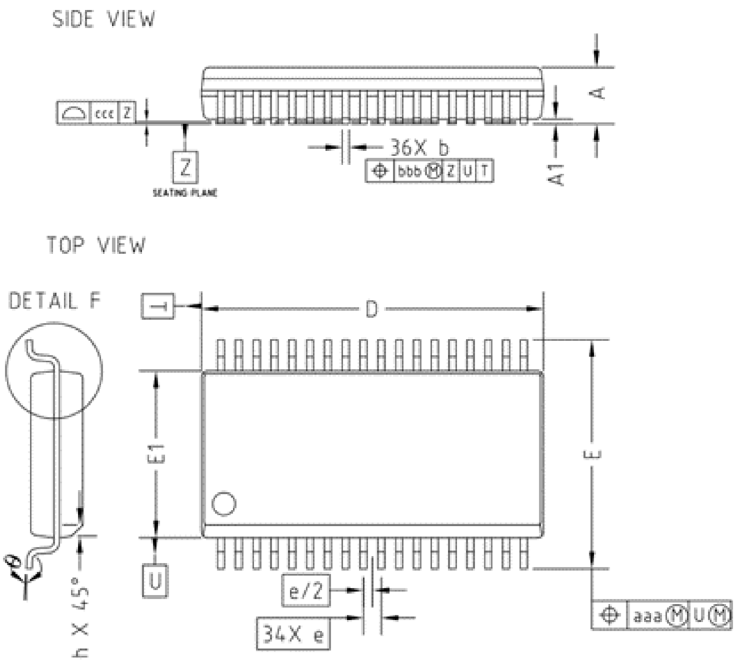


Table 11. **SSOP36L package mechanical data**

Symbol	Dimensions (mm)		
	Min.	Typ.	Max.
A	-	-	2.65
A1	0.10	-	0.30
b	0.25	-	0.35
c	0.20	-	0.33
D	15.20	-	15.60
E1	7.40	-	7.60
E	10.05	-	10.55
e	0.80 BSC		
L	0.61	-	0.91
h	0.25	-	0.75
θ	0°	-	8°

12 Ordering information

Table 12. Order codes

Order codes	Packing	Package
ST-ONEHP	Tube	SSOP 36L
ST-ONEHPTR	Tape & Reel	

Revision history

Table 13. Document revision history

Date	Version	Changes
20-Jun-2023	1	Initial release.

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