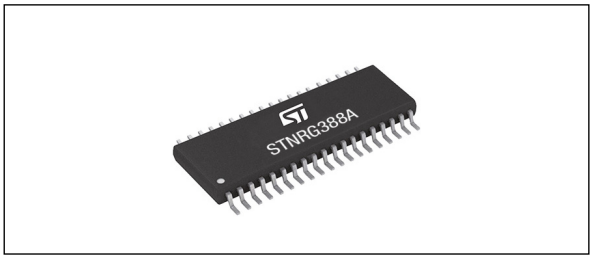
STNRG388A

Digital controller for power conversion applications with up to 6 programmable PWM generators, 96 MHz PLL

Datasheet - production data



Features

- Up to 6 programmable PWM generators (SMED - “State Machine Event Driven”)
  - 10 ns event detection and reaction
  - Max.1.3 ns PWM resolution
  - Single, coupled and two coupled operational modes
  - Up to 3 internal/external events per SMED
- 4 analog comparators
  - 4 internal 4-bit references
  - Up to 4 external references
  - Less than 50 ns propagation time
  - Continuous comparison cycle
  - Configurable hysteresis voltage levels
- ADCs (up to 8 channels)
  - 10-bit precision, with operational amplifier to extend resolution to 12-bit equivalent
  - Sequencer functionality
  - Input impedance: 1 MΩ
  - Configurable gain value: x1 and x4
- Integrated microcontroller
  - Advanced STM8® core with Harvard architecture and 3-stage pipeline
  - Max. f_{CPU}: 16 MHz
- Memories
  - Flash and E^2PROM with read while write (RWW) and error correction code (ECC)
  - Program memory: 32 Kbytes Flash; data retention 15 years at 85 °C after 10 kcycles at 25 °C
  - Data memory: 1 Kbyte true data E^2PROM; data retention:15 years at 85 °C after 100 kcycles at 85 °C
  - RAM: 6 Kbytes
- Clock management
  - Internal 96 MHz PLL
  - Low power oscillator circuit for external crystal resonator or direct clock input
  - Internal, user-trimmable 16 MHz RC and low power 153.6 kHz RC oscillators
  - Clock security system with clock monitor
- Basic peripherals
  - System, auxiliary and basic timers
  - IWDG/WWDG watchdog, AWU, ITC
- Reset and supply management
  - Multiple low power modes (wait, slow, auto-wakeup, Halt) with user definable clock gating
  - Low consumption power-on and power-down reset
- I/O
  - Multifunction bidirectional GPIO with highly robust design, immune against current injection
  - Fast digital input DIGIN, with configurable pull-up
- Communication interfaces
  - UART asynchronous with SW flow control and bootloader support
  - I^2C master/slave fast-slow speed rate
- Operating temperature: -40 °C up to 105 °C.

Table 1. Device summary

Part number	Package
STNRG388A	TSSOP38

Contents

List of tables

List of figures

1 Description

STNRG devices are a part of the STNRG family of STMicroelectronics® digital devices designed for advanced power conversion applications.

The STNRG improves the design of the successful STLUX™ family, now integrated in a wide range of LED driver architectures, to support industrial power conversion applications such as PFC+LLC, interleaved LC DC/DC, interleaved PFC for smart power supplies as well as the full bridge for pilot line drivers for electric vehicles.

2 STNRG family features list

All devices of the STNRG family provide the following features:

Table 2. STNR388A features list

Feature list		Device
		STNRG388A
Package		TSSOP38
Pin count		38
SMED numbers		6
SMED PWM output pins		6
Fast digital inputs pins		6
Positive comparator input pin		4
Negative comparator input pins		3(1)
Comparator hysteresis		Yes
Internal DACs		4
ADC input pins		8
ADC gain		x1 - x4
ADC hardware trigger		Yes
GPIO Port 0 pins		6
Communication	UART peripheral	Yes
	I^2C peripheral	Yes
	DALI peripheral	Yes
HSE function		Yes
Timers	System timer	1
	Auxiliary timer	1
	Basic timer	2
Auto-wakeup timer		1
Watchdog	Window watchdog timer	1
	Independent watchdog timer	1
Flash program memory		32 Kbytes
EEPROM data memory		1 Kbytes
RAM		6 Kbytes
SWIM pin		Mixed

1. Some CPM pin is shared with other signals.

3 Introducing SMED

The heart of the STNRG controller family is the SMED (state machine event driven) technology which allows the device to pilot six independently configurable PWM clocks with a maximum resolution of 1.3 ns. A SMED is a powerful autonomous state machine, which is programmed to react to both external and internal events and may evolve without any software intervention. The SMED reaction time can be as low as 10.4 ns, giving the STNRG the ability of operating in time critical applications. The SMEDs offer superior performances when compared to traditional, timer based, PWM generators.

Each SMED is configured via the STNRG internal microcontroller. The integrated controller extends the STNRG reliability and guarantees more than 15 years of both operating lifetime and memory data retention for program and data memory after cycling.

A set of dedicated peripherals complete the STNRG device:

- 4 analog comparators with configurable references and 50 ns max. propagation delay. It is ideal to implement zero current detection algorithms or detect current peaks.
- 10-bit ADC with configurable op amp and 8-channel sequencer.
- 96 MHz PLL for high output signal resolution.

Documentation

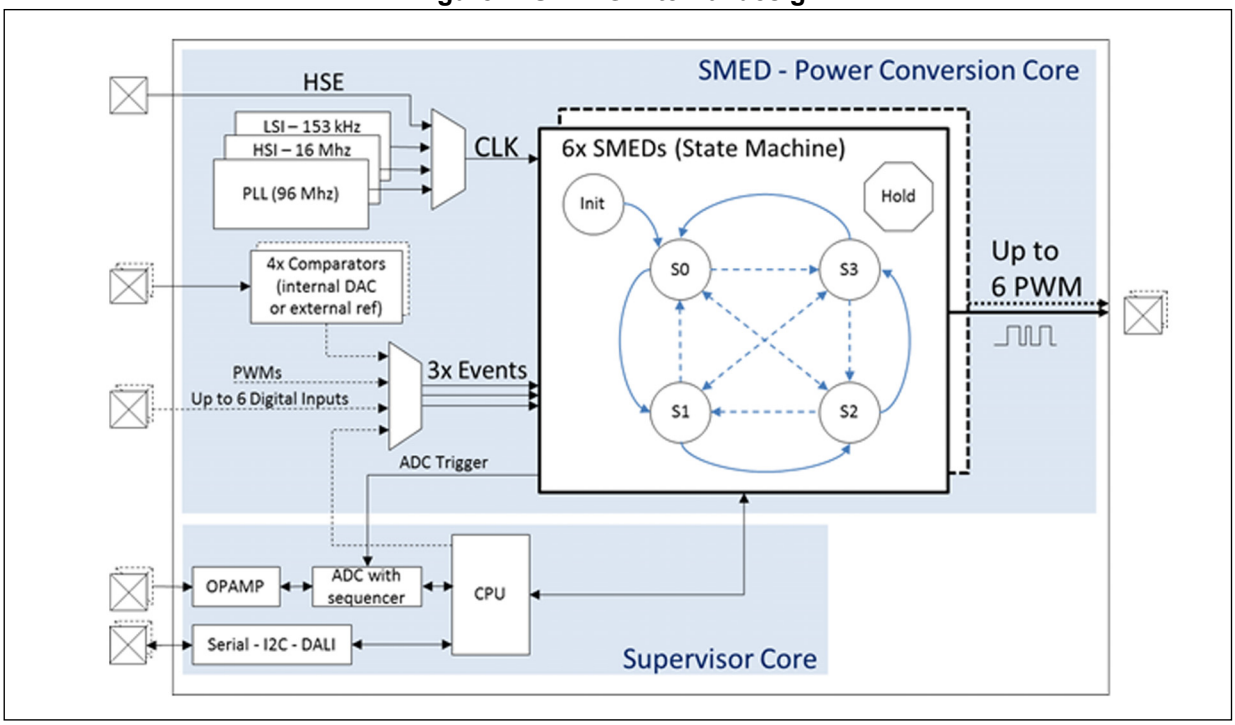
This datasheet contains the description of features, pinout, pin assignment, electrical characteristics, mechanical data and ordering information.

- For information on programming, erasing and protection of the internal Flash memory, please refer to the STM8S reference in the programming manual “How to program STM8S and STM8A Flash program memory and data EEPROM” (PM0051).
- For information on the debug and SWIM (single wire interface module) interface refer to the “STM8 SWIM communication protocol and debug module” user manual (UM0470).
- For information on the STM8 core, please refer to the “STM8 CPU programming manual” (PM0044).

4 System architecture

The STNRG device generates and controls PWM signals by means of a state machine, called SMED (state machine event driven). *Figure 1* gives an overview of the internal architecture.

Figure 1. STNRG internal design



The core of the device is the SMED unit: a hardware state machine driven by system events. The SMED includes 4 states (S0, S1, S2 and S3) available during running operations. A special HOLD state is provided as well. The SMED allows the user to configure, for every state, which system events will trigger a transaction to a new state. During a transaction from one state to the other, the PWM output signal level can be updated.

Once a SMED is configured and running, it becomes an autonomous unit, so no interaction is required since the SMED automatically reacts to system events.

Thanks to the SMED's 96 MHz operating frequency and their automatic dithering function, the PWM maximum resolution is 1.3 ns.

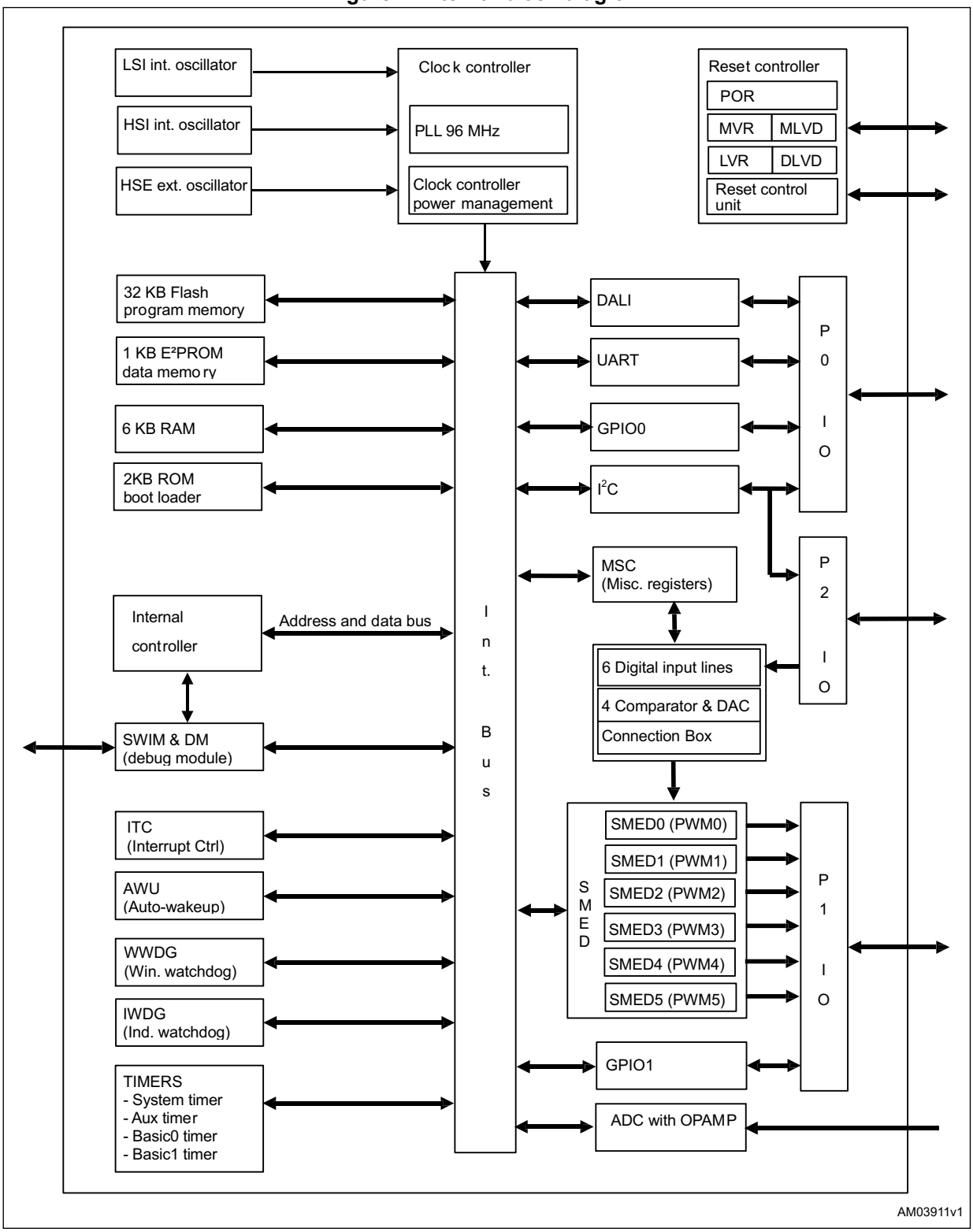
The STNRG family has 6 SMEDs available. Multiple SMEDs can operate independently from each other or they can be grouped together to form a more powerful state machine.

The STNRG also integrates a low power STM8 microcontroller which is used to configure and monitor the SMED activity and to supply external communication such as the UART, I^2C or DALI. The STM8 controller has full access to all the STNRG subsystems, including the SMEDs. The STNRG family also features a sequential ADC, which can be configured to continuously sample up to 8 channels.

Section : Block diagram illustrates the overall system block and shows how SMEDs have been implemented in the STNRG architecture.

Block diagram

Figure 2. Internal block diagram



5 Product overview

Section 5.1 describes the features implemented in the product device.

5.1 SMED (state machine event driven): configurable PWM generator

The SMED is an advanced programmable PWM generator signal. The SMED (state machine event driven) is a state machine device controllable by both external events (primary I/O signals) and internal events (counter timers), which generate an output signal (PWM) depending on the evolution of the internal state machine.

The PWM signal generated by the SMED is therefore shaped by external events and not only by a simple timer. This mechanism allows to generate controlled high frequency PWM signals.

The SMED is also autonomous: once it has been configured by the STNRG internal controller, the SMED can operate without any software interaction.

The STNRG family provides 6 SMED units. Multiple SMEDs can operate independently from each other or they can be grouped together to form a more powerful state machine.

The main features of a SMED are described here below:

- Configurable state machine generating a PWM signal
- More than 10.4 ns PWM native resolution
- Up to 1.3 ns PWM resolution when using SMED dithering
- 6 states available in each SMED: IDLE, S0, S1, S2, S3 plus a special HOLD state
- Transactions triggered by synchronous and asynchronous external events or an internal timer
- Each transaction can generate an interrupt
- Fifteen registers available to configure the state machine behavior
- Four 16-bit configurable time registers, one for each running state (T0, T1, T2, T3)
- Internal resources accessible through the processor interface
- Eight interrupt request lines
- Configurable ADC HW trigger request
- PWM pseudo open drain features configurable through GPIO1 registers

5.1.1 SMED coupling schemes

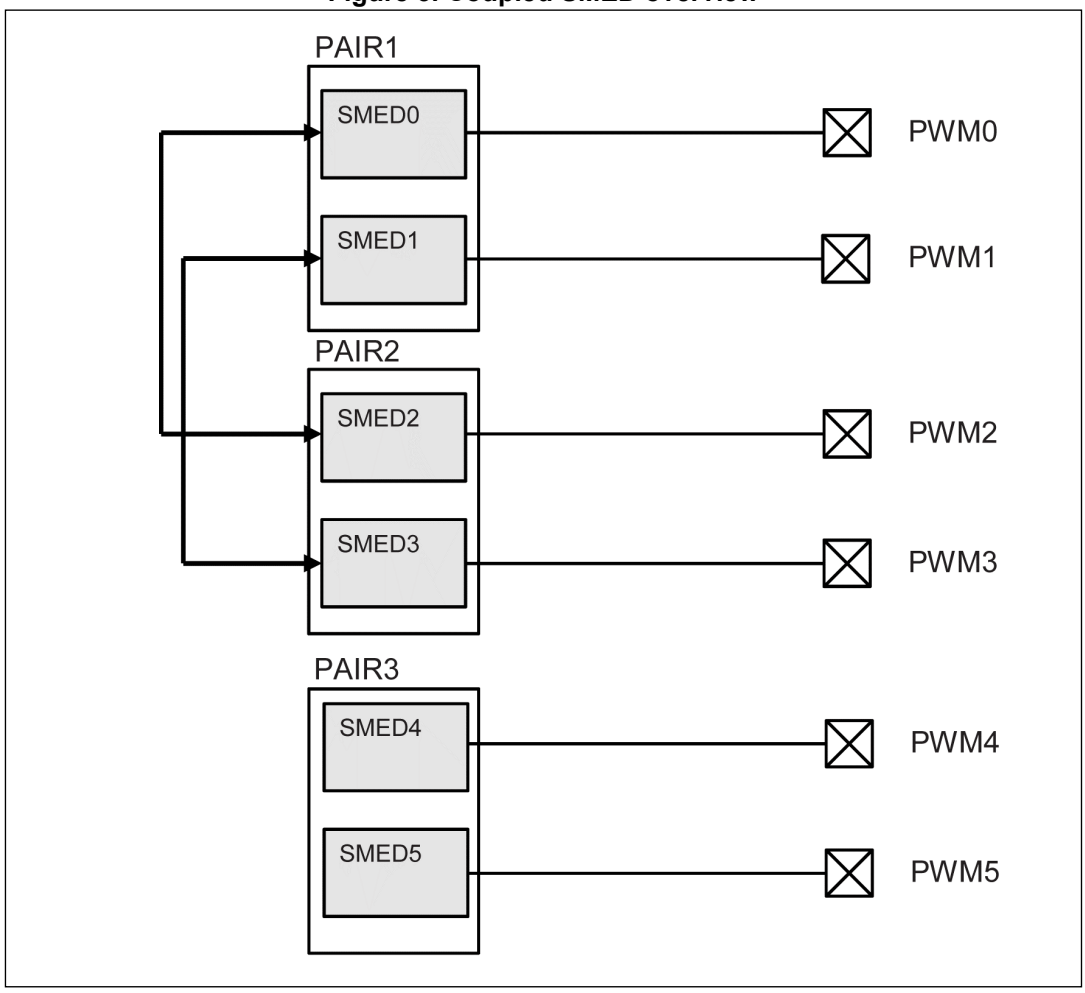
The SMED coupling extends the capability of the single SMED, preserving the independence of each “Finite State Machine” (FSM) programmed state evolution. The coupling scheme allows the SMED pulse signals to be interleaved on their own PWM or on a merged single PWM output. The STNRG supports the following coupled configuration schemes:

- Single SMED configuration
- Synchronous coupled SMED
- Asynchronous coupled SMED
- Synchronous two coupled SMEDs
- Asynchronous two coupled SMEDs
- External controlled SMED

The SMED units may be configured in different coupled schemes through the SMDx_GLBCONF and SMDx_DRVOUT bit fields of MSC_SMEDCFGxy registers.

An outline of the SMED subsystem is shown in *Figure 3*.

Figure 3. Coupled SMED overview



1. The PWM4 and PWM5 output pins are not present on all STNRG devices.

5.1.2 Connection matrix

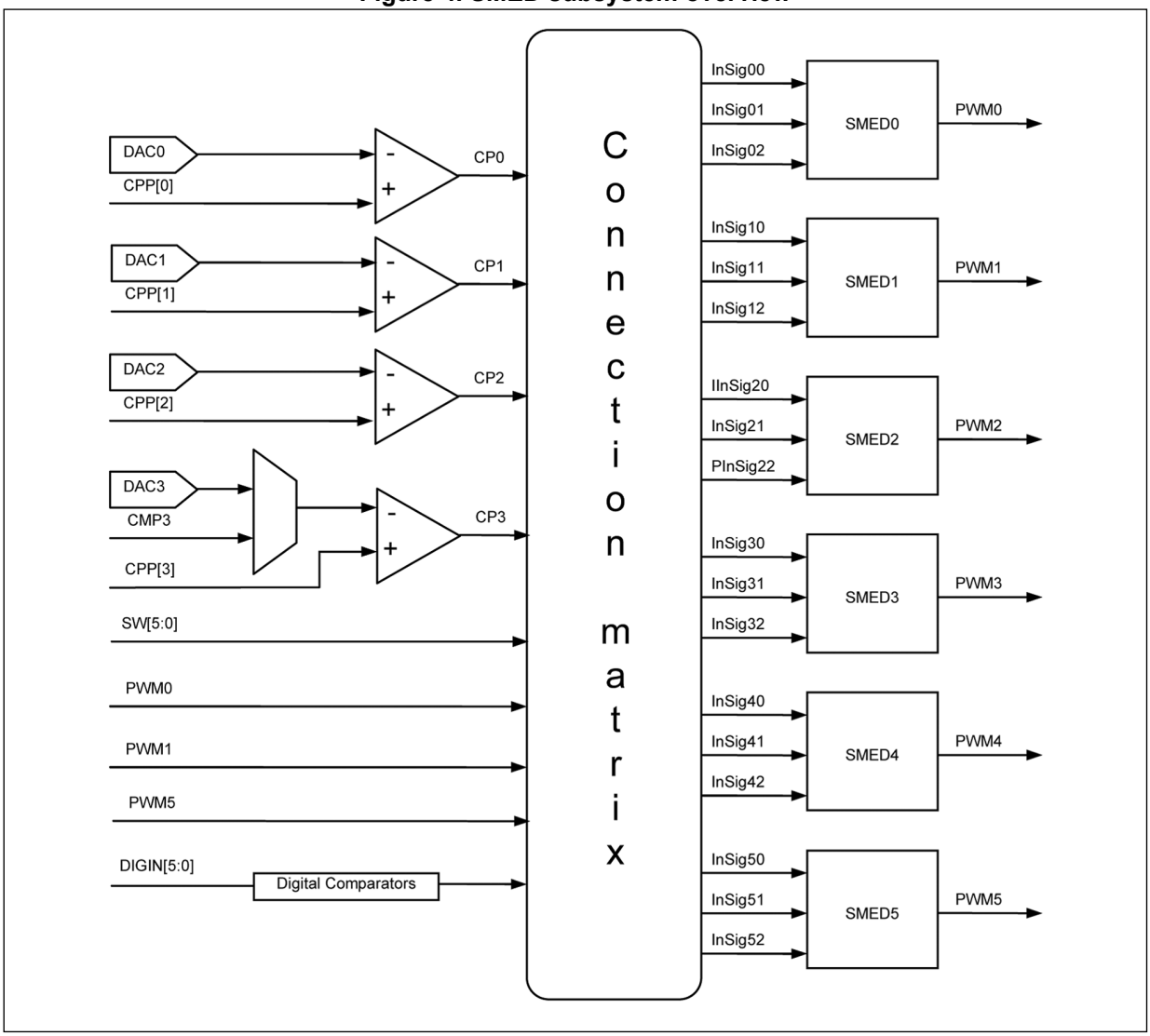
The connection matrix extends the input connectivity of each SMED unit so that a SMED can receive events from a wide range of sources. Through the matrix, it's possible to connect the SMED inputs to various signal families such as digital inputs, comparator output signals, SW events, and three PWM internal feedback signals as shown in *Figure 4*.

The list of the available event sources is the following:

- DIGIN [5:0] digital input lines
- CPM [3:0] analog comparator outputs
- PWM [5:0] output signals of SMEDs (only PWM 0, 1 and 5 are accessible)
- SW [5:0] software events

Figure 4 shows the connection matrix and signal interconnections as they are implemented in the STNRG family.

Figure 4. SMED subsystem overview



1. The CPP2 and CMP3 inputs are connected together in some STNRG devices.

Connection matrix interconnection

Every SMED unit has three input selection lines, one for each In_Sig input, configurable via the MSC_CBOXS (5:0) register. The selection lines choose the interconnection between one of possible four connection matrix signals for each SMED input event In_Sig (Y).

Table 3 shows the layout of the connection matrix interconnection signals as implemented in the STNRG family.

Table 3. Connection matrix interconnection

Conb_s(x)_(y)(z)					
SMED number	**SMED input**	**SMED input signal selection (z)**			
(x)	**(y)**	**00**	**01**	**10**	**11**
0	0	CP0	DIG0	DIG2	DIG5
	1	CP1	DIG0	DIG3	CP3
	2	CP2	DIG1	DIG4	SW0
1	0	CP1	DIG1	DIG3	DIG0
	1	CP2	DIG1	DIG4	CP3
	2	CP0	DIG2	DIG5	SW1
2	0	CP2	DIG2	DIG4	DIG1
	1	CP0	DIG2	DIG5	PWM0
	2	CP1	DIG3	DIG0	SW2
3	0	CP0	DIG3	DIG5	DIG2
	1	CP1	DIG3	DIG0	PWM1
	2	CP2	DIG4	DIG1	SW3
4	0	CP1	DIG4	DIG0	DIG3
	1	CP2	DIG4	DIG1	PWM5
	2	CP0	DIG5	DIG2	SW4
5	0	CP2	DIG5	DIG1	DIG4
	1	CP0	DIG5	DIG2	CP3
	2	CP1	DIG0	DIG3	SW5

Connection matrix legend:

- X represents the SMED [5:0] number
- Y represents the SMED input signal number (In_Sig [2:0])
- Z represents the In_Sig (Y) selection signal

Note: Each SMED input has independent connection matrix selection signals.

Internal controller (CPU)

The STNRG family integrates a programmable STM8 controller acting as a device supervisor. The STM8 is a modern CISC core and has been designed for code efficiency and performance. It contains 21 internal registers (six of them directly addressable in each

execution context), 20 addressing modes including indexed indirect and relative addressing and 80 instructions.

5.1.3 Architecture and registers

- Harvard architecture with 3-stage pipeline
- 32-bit wide program memory bus with single cycle fetching for most instructions
- X and Y 16-bit index registers, enabling indexed addressing modes with or without offset and read-modify-write type data manipulations
- 8-bit accumulator
- 24-bit program counter with 16 Mbyte linear memory space
- 16-bit stack pointer with access to a 64-Kbyte stack
- 8-bit condition code register with seven condition flags updated with the results of last executed instruction

5.1.4 Addressing

- 20 addressing modes
- Indexed indirect addressing mode for lookup tables located in the entire address space
- Stack pointer relative addressing mode for efficient implementation of local variables and parameter passing

5.1.5 Instruction set

- 80 instructions with 2-byte average instruction size
- Standard data movement and logic/arithmetic functions
- 8-bit by 8-bit multiplication
- 16-bit by 8-bit and 16-bit by 16-bit division
- Bit manipulation
- Data transfer between stack and accumulator (push/pop) with direct stack access
- Data transfer using the X and Y registers or direct memory-to-memory transfers

5.1.6 Single wire interface module (SWIM)

The single wire interface module (SWIM), together with the integrated debug module (DM), allows non-intrusive, real-time in-circuit debugging and fast memory programming. The interface can be activated in all device operation modes and can be connected to a running device (hot plugging).The maximum data transmission speed is 145 byte/ms.

The SWIM pin is a multifunction signal. For further details refer to *Table 7: Port P1 I/O multiplexing signal* in *Section 7.3 on page 38*.

5.1.7 Debug module

The non-intrusive debugging module is fully controllable through the external target emulator. Besides memory and peripheral operation, the CPU operation can also be monitored in real-time by means of shadow registers.

- R/W of RAM and peripheral registers in real-time
- R/W for all resources when the application is stopped
- Breakpoints on all program-memory instructions (software breakpoints), except for the interrupt vector table
- Two advanced breakpoints and 23 predefined breakpoint configurations

5.2 Basic peripherals

Section 5.2.1 and *Section 5.2.2* describe the basic peripherals accessed by the internal CPU controller.

5.2.1 Vectored interrupt controller

- Nested interrupts with three software priority levels
- 21 interrupt vectors with hardware priority
- Two vectors for 12 external maskable or un-maskable interrupt request lines
- Trap and reset interrupts

5.2.2 Timers

The STNRG family provides several timers which are used by software and do not interact directly with the SMED and the PWM generation.

System timers

The system timer consists of a 16-bit autoreload counter driven by a programmable prescaled clock and operating in one shoot or free running operating mode. The timer is used to provide the IC time base system clock, with an interrupt generation on timer overflow events.

Basic timers

The IC device includes two independent 6-bit timers programmable through the miscellaneous indirect register area. The time base frequency is configurable with different source clocks.

The timers have the following functionalities:

- Free running mode
- Timer prescaler 8-bits
- Counter register 6-bits
- Programmable time base clock (HSI, HSE, LSI, PLL)
- Interrupt timer capability:
  - Vectored interrupt
  - Interrupt IRQ/NMI or polling mode

Auxiliary timer

The auxiliary timer is a light timer with elementary functionality. The time base frequency is provided by the CCO clock logic (configurable with a different source clock and prescale division factors), while the interrupt functionality is supplied by an interrupt edge detection logic similarly to the solution adopted for the Port P0/P2.

The timer has the following main features:

- Free running mode
- Up counter
- Timer prescaler 8-bit
- Interrupt timer capability:
  - Vectored interrupt
  - Interrupt IRQ/NMI or Polling mode
- Timer pulse configurable as a clock output signal via the CCO primary pin

Thanks to the great configurability of the CCO frequency, the timer can cover a wide range of interval time to fit better the target application requirements.

Auto-wakeup timer

The AWU timer is used to cyclically wake-up the IC device from the active halt state. The AWU frequency time base f_{AWU} can be selected between the following clock sources: LSI (153.6 kHz) and the external clock HSE scaled down to 128 kHz clock.

By default the f_{AWU} clock is provided by the LSI internal source clock.

Watchdog timers

The watchdog system is based on two independent timers providing a high level of robustness to the applications. The watchdog timer activity is controlled by the application program or by suitable option bytes. Once the watchdog is activated, it cannot be disabled by the user program without going through reset.

Window watchdog timer

The window watchdog is used to detect the occurrence of a software fault, usually generated by external interferences or by unexpected logical conditions, which causes the application program to break the normal operating sequence.

The window function can be used to adjust the watchdog intervention period in order to match the application timing perfectly. The application software must refresh the counter before timeout and during a limited time window. If the counter is refreshed outside this time window, a reset is issued.

Independent watchdog timer

The independent watchdog peripheral can be used to solve malfunctions due to hardware or software failures.

It is clocked by the 153.6 kHz LSI internal RC clock source. By properly setting the hardware watchdog feature associated option bits, the watchdog is automatically enabled at power-on, and generates a reset unless the key register is written by software before the counter reaches the end of the count.

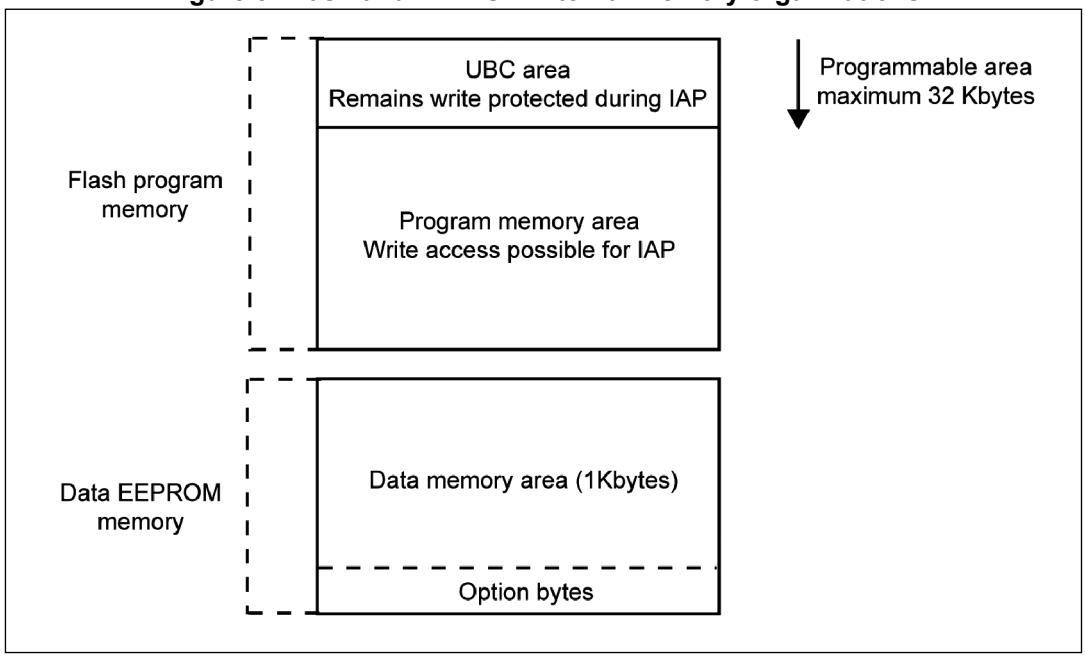
5.2.3 Flash program and data E^{2}PROM

Embedded Flash and E^{2}PROM with the memory ECC code correction and protection mechanism preventing embedded program hacking.

- 32 Kbyte of single voltage program Flash memory
- 1 Kbyte true (not emulated) data E^{2}PROM
- Read while write: writing in the data memory is possible while executing code program memory
- The device setup is stored in a user option area in the non-volatile memory.

5.2.4 Architecture

Figure 5. Flash and E^{2}PROM internal memory organizations



- The memory is organized in blocks of 128 bytes each
- Read granularity: 1 word = 4 bytes
- Write/erase granularity: 1 word (4 bytes) or 1 block (128 bytes) in parallel
- Writing, erasing, word and block management is handled automatically by the memory interface.

5.2.5 Write protection (WP)

Write protection in application mode is intended to avoid unintentional overwriting of the memory. The write protection can be removed temporarily by executing a specific sequence in the user software.

5.2.6 Protection of user boot code (UBC)

In STNRG devices a memory area of 32 Kbyte can be protected from overwriting at a user option level. In addition to the standard write protection, the UBC protection can be modified by the embedded program or via debug interface when the ROP protection is enabled.

The UBC memory area contains the reset and interrupt vectors and its size can be adjusted in increments of 512 bytes by programming the UBC and nUBC option bytes.

Note: If users choose to update the boot code in the application programming (IAP), this has to be protected so to prevent unwanted modification.

5.2.7 Read-out protection (ROP)

The STNRG family provides a read-out protection of the code and data memory which can be activated by an option byte setting.

The read-out protection prevents reading and writing program memory, data memory and option bytes via the debug module and SWIM interface. This protection is active in all device operation modes. Any attempt to remove the protection by overwriting the ROP option byte triggers a global erase of the program and data memory contents.

5.3 Clock controller

The clock controller distributes the system clock provided by different oscillators to the core and the peripherals. It also manages clock gating for low- power modes and ensures clock robustness.

The main clock controller features are:

- Clock sources
- Internal 16 MHz and 153.6 kHz RC oscillators
- External source clock:
  - Crystal/resonator oscillator
  - External clock input
- Internal PLL at 96 MHz (not used as the f_{MASTER} source clock)
- Reset: after the reset the microcontroller restarts by default with the HSI internal clock scaled at 2 MHz (16 MHz/8). The clock source and speed can be changed by the application program as soon as the code execution starts.
- Safe clock switching: clock sources can be changed safely on the fly in run mode through a configuration register. The clock signal is not switched until the new clock source is ready. The design guarantees glitch-free switching.
- Clock management: to reduce power consumption, the clock controller can stop the clock to the core or individual peripherals.
- Wakeup: In in case the device wakes up from low- power modes, the internal RC oscillator (16 MHz/8) is used for a quick startup. After a stabilization time, the device brings back the clock source that was selected before Halt mode was entered.
- Clock security system (CSS): the CSS permits monitoring of external clock sources and automatic switching to the internal RC (16 MHz/8) in case of a clock failure.
- Configurable main clock output (CCO): this feature permits to output an internal clock source signal for application usage.

5.3.1 Internal 16 MHz RC oscillator (HSI)

The high speed internal (HSI) clock is the default master clock line, generated by an internal RC oscillator and with nominal frequency of 16 MHz. It has the following major features:

- RC architecture
- Glitch-free oscillation
- 3-bit user calibration circuit.

5.3.2 Internal 153.6 kHz RC oscillator (LSI)

The low speed internal (LSI) clock is a low speed clock line provided by an internal RC circuit. It drives both the independent watchdog (IWDG) circuit and the auto-wakeup unit (AWU). It can also be used as a low power clock line for the master clock f_{MASTER}.

5.3.3 Internal 96 MHz PLL

The PLL provides a high frequency 96 MHz clock used to generate high frequency and accurate PWM waveforms. The input reference clock must be 16 MHz and may be sourced either by the internal HSI signal or by the external HSE auxiliary input crystal oscillator line.

The internal PLL prescaled clock cannot be selected as f_{MASTER}.

Note: When the application requires a PWM signal with a custom defined long term stability it is suggested to use an external clock source connected to the HSE auxiliary clock line as the PLL input reference clock. In this case, the external clock source accuracy determines the PWM output stability.

5.3.4 External clock input/crystal oscillator (HSE)

The high speed external clock (HSE) allows the connection of an external clock generated, for example, by a highly accurate crystal oscillator. The HSE is interconnected with the f_{MASTER} clock line and to several peripherals. It allows users to provide a custom clock characterized by a high level of precision and stability to meet the application requirements. The HSE supports two possible external clock sources with a maximum of 24 MHz:

- Crystal/ceramic resonator interconnected with the HseOscin/HseOscout signals
- Direct drive clock interconnected with the HseOscin signal

The HseOscin and HseOscout signals are multifunction pins configurable through the I/O multiplex mechanism; for further information refer to Section 6 on page 30.

Note: When the HSE is configured as the f_{MASTER} source clock, the HSE input frequency cannot be higher than 16 MHz.
When the HSE is the PLL input reference clock, then the HSE input frequency must be equal to 16 MHz.
If the HSE is the reference for the SMED or the ADC logic, the input frequency can be configured up to 24 MHz.

5.4 Power management

For efficient power management, the application can be put in one of four different low-power modes. Users can configure each mode to obtain the best compromise between the lowest power consumption, the fastest startup time and available wakeup sources.

- **Wait mode:** in this mode, the CPU is stopped, but peripherals are kept running. The wakeup is triggered by an internal or external interrupt or reset.
- **Active- halt mode with regulator on:** in this mode, the CPU and peripheral clocks are stopped. An internal wakeup is generated at programmable intervals by the auto-wakeup unit (AWU). The main voltage regulator is kept powered on, so current consumption is higher than in the active-halt mode with the regulator off, but the wakeup time is faster. The wakeup is triggered by the internal AWU interrupt, external interrupt or reset.
- **Active- halt mode with regulator off:** this mode is the same as active- halt with the regulator on, except that the main voltage regulator is powered off, so the wakeup time is slower.
- **Halt mode:** in this mode the microcontroller uses the least power. The CPU and peripheral clocks are stopped, while the main voltage regulator is switched in power-off. Wakeup is triggered by an external event or reset.

In all modes the CPU and peripherals remain permanently powered on, the system clock is applied only to selected modules. The RAM content is preserved and the brownout reset circuit remains enabled.

5.5 Communication interfaces

5.5.1 Universal asynchronous receiver/transmitter (UART)

UART is the asynchronous receiver/transmitter communication interface.

- SW flow control operating mode
- Full duplex, asynchronous communications
- High precision baud rate generator system
- Common programmable transmit and receive baud rates up to $f_{MASTER}/16$
- Programmable data word length (8 or 9-bit)
- Configurable stop bit - support for 1 or 2 stop bit
- Configurable parity control
- Separate enable bits for transmitter and receiver
- Interrupt sources:
  - Transmit events
  - Receive events
  - Error detection flags
- 2 interrupt vectors:
  - Transmitter interrupt
  - Receiver interrupt
- Reduced power consumption mode
- Wakeup from mute mode (by idle line detection or address mark detection)
- 2 receiver wakeup modes:
  - Address bit (MSB)
  - Idle line.

5.5.2 Inter-integrated circuit interface (I^2C)

The I^2C (inter-integrated circuit) bus interface serves as an interface between the microcontroller and the serial I^2C bus. It provides a multi-master capability, and controls all I^2C bus-specific sequencing, protocol, arbitration and timing. It supports standard and fast speed modes.

- Parallel-bus/I^2C protocol converter
- Multi-master capability: the same interface can act as master or slave
- I^2C master features:
  - Clock generation
  - Start and stop generation
- I^2C slave features:
  - Programmable I^2C address detection
  - Stop bit detection
- Generation and detection of 7-bit/10-bit addressing and general call
- Supports different communication speeds:
  - Standard speed (up to 100 kHz)
  - Fast speed (up to 400 kHz)

- Status flags:
  - Transmitter/receiver mode flag
  - End-of-byte transmission flag
  - I^2C busy flag
- Error flags:
  - Arbitration lost condition for master mode
  - Acknowledgment failure after address/ data transmission
  - Detection of misplaced start or stop condition
  - Overrun/underrun if clock stretching is disabled
- Interrupt sources:
  - Communication interrupt
  - Error condition interrupt
  - Wakeup from Halt interrupt
- Wakeup capability:
  - MCU wakes up from low power mode on address detection in slave mode.

5.5.3 Digital addressable lighting interface (DALI)

The DALI (digital addressable lighting interface), standardized as IEC 62386, is the new interface for lighting control solutions defined by the lighting industry.

The DALI protocol is generally implemented in a DALI communication module (DCM): a serial communication circuit designed for controllable electronic ballasts. The “ballast” is a device or circuit used to provide the required starting voltage and operating current for the LED, fluorescent, mercury or other electronic-discharge lamps.

The STNRG388A DALI interface has the following characteristics:

- Speed line: 1.2, 2.4 and 4.8 kHz transmission rate ±10%
- Forward message length: 16, 17, 18 or 24 bit
- Backward message length: 8 bit
- Bidirectional communications
- Monitor receiver line timeout 500 ms ± 10%
- Reversible polarity of DALI_rx, DALI_tx signal line
- Configurable noise rejection filter on DALI_rx input line
- Maskable interrupt request line
- DALI peripheral clock is slowed down to 153.6 kHz in low speed operating mode

DALI noise rejection filter

The DALI interface includes a noise rejection filter interconnected on the RX channel capable to remove any bounce, glitch or spurious pulse from the RX line. The filter can be configured via three registers:

- MSC_DALICKSEL: selects the source clock of filter timing
- MSC_DALICKDIV: configures the clock prescaler value
- MSC_DALICONF: configures the filter count and operating mode.

Further information about the noise rejection filter description is found in the STLUX and STNRG family reference manual (RM0380).

5.6 Analog-to-digital converter (ADC)

The STNRG family includes a 10-bit successive approximation ADC with 8 multiplexed input channels. The analog input signal can be amplified before conversion by a selectable gain of 1 or 4[a] times. The analog-to-digital converter can operate either in single or in continuous/circular modes. The ADC unit has the following main features:

- 8/6 ADC input channel[b]
- 10-bit resolution
- Single and continuous conversion mode
- Independent or fixed channel gain value x1 or x4 to extend dynamic range and resolution to 12-bit equivalent[a]
- Interrupt events:
  - EOC interrupt asserted on end of conversion cycle
  - EOS interrupt asserted on end of conversion sequences
  - SEQ_FULL_EN interrupt assert on sequencer buffer full
- ADC input voltage range dependent on selected gain value[a]
- Selectable conversion data alignment
- Individual registers for up to 8 successive conversions.
- Conversion start from SW command or HW trigger event
- Auto-reload conversion command parameters
- Auto-flush after single conversion mode
- Auto-flush after conversion mode program (single/circular)
- Abort/flush sequence improvement

5.7 Analog comparators

The STNRG family includes four independent fast analog comparator units (COMP3-0). Each comparator has an internal reference voltage. The COMP3 can be also configured to use an external reference voltage connected to the CPM3 input pin. On the STNRG388A each comparator has also the external reference voltage line pin.

a. The gain x 4 is available only on the STNRG388A type.

b. The numbers of ADC input channels depends on the STNRG device.

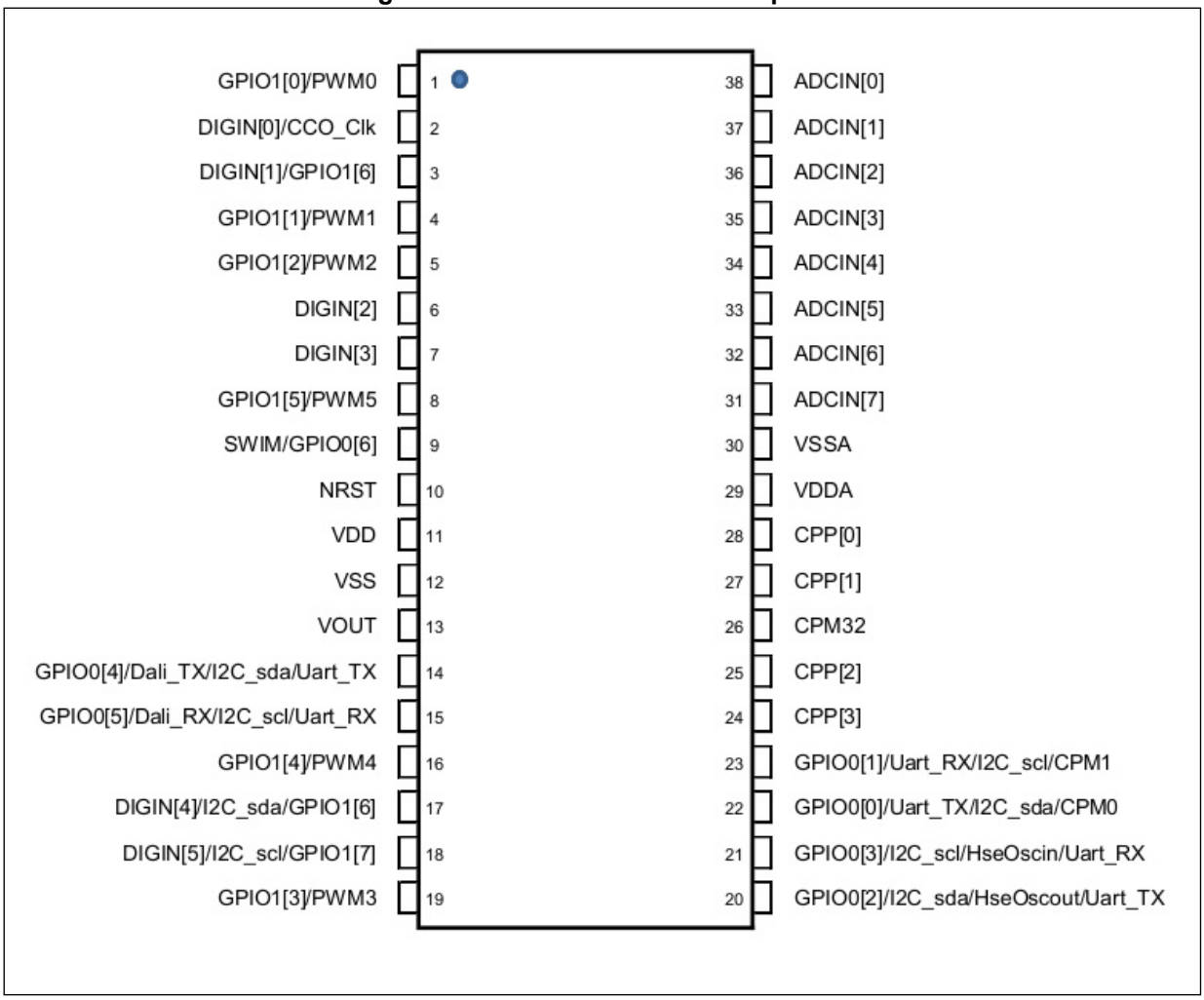
Each comparator internal reference voltage is generated by a dedicated internal-only 4-bit DAC unit. The main characteristics of the analog comparator unit (ACU) are the following:

- Each comparator has an internally/external configurable reference
- Internal reference voltages configurable in 16 steps with the 83 mV voltage gain from 0 V (VSSA) to 1.24 V (voltage reference)
- Two stage comparator architecture is used to reach a high gain
- Comparator output stage value accessible from processor interface
- Continuous fast cycle comparison time
- Configurable hysteresis voltage levels
- Configurable ADC HW trigger request
- Comparator outputs interrupt capability.

6 Pinout and pin description

6.1 Pinout

Figure 6. STNRG388A - TSSOP38 pinout



6.2 Pin description

Table 4. Pin description

Pin number TSSOP 38	Type	Pin name	Main function	Alternate function 1	Alternate function 2	Alternate function 3
1	I/O	GPIO1 [0]/PWM [0]	SMED PWM channel 0	General purpose I/O 10	-	-
2	I/O	DIGIN[0]/ CCO_clk	Digital input 0	Configurable clock output signal (CCO)	-	-
3	I	DIGIN[1]/ GPIO1 [6]	Digital input 1	General purpose I/O 16	-	-
4	I/O	GPIO1[1]/PWM[1]	SMED PWM channel 1	General purpose I/O 11	-	-
5	I/O	GPIO1 [2]/ PWM [2]	SMED PWM channel 2	General purpose I/O 12	-	-
6	I	DIGIN [2]	Digital input 2	-	-	-
7	I	DIGIN [3]	Digital input 3	-	-	-
8	I/O	GPIO1 [5]/ PWM[5]	SMED PWM channel 5	General purpose I/O 15	-	-
9	I/O	SWIM/GPIO0 [6]/ DIGIN [1]	SWIM data interface	General purpose I/O 06	Digital input 1 (3)	-
10	I/O	NRST	Reset	-	-	-
11	PS	VDD	Digital and I/O power supply	-	-	-
12	PS	VSS	Digital and I/O ground	-	-	-
13	PS	VOUT	1.8 V regulator capacitor	-	-	-
14	I/O	GPIO0[4]/Dali_TX/ I2C_sda/Uart_TX	General purpose I/O 04	DALI data transmit	I^2C data	UART data transmit
15	I/O	GPIO0[5]/Dali_RX/ I2C_scl/Uart_RX	General purpose I/O 05	DALI data receive	I^2C clock	UART data receive
16	I/O	GPIO1 [4]/PWM [4]	SMED PWM channel 4	General purpose I/O 14	-	-
17	I/O	DIGIN[4]/I2C_sda/ GPIO1[6]	Digital input 4	I^2C data	General purpose I/O 16	-
18	I/O	DIGIN[5]/I2C_scl/ GPIO1[7]	Digital input 5	I^2C clock	General purpose I/O 17	-
-	I/O	DIGIN54	Digital input 5,4	-	-	-
19	I/O	GPIO1 [3]/PWM [3]	SMED PWM channel 3	General purpose I/O 13	-	-

Table 4. Pin description (continued)

Pin number TSSOP 38	Type	Pin name	Main function	Alternate function 1	Alternate function 2	Alternate function 3
20	I/O	GPIO0 [2]/I2C_sda/ HseOscout/Uart_TX	General purpose I/O 02	I^2C data	Output crystal oscillator signal	UART data transmit
21	I/O	GPIO0[3]/I2C_scl/ HseOscin/Uart_RX	General purpose I/O 03	I^2C clock	Input crystal oscillator signal /input clock signal	UART data receive
22	I/O	GPIO0[0]/Uart_TX/ I2C_sda/CPM0	General purpose I/O 00	UART data transmit	I^2C data	Negative analog comparator input 0
23	I/O	GPIO0[1]/Uart_RX/ I2C_scl/CPM1	General purpose I/O 01	UART data receive	I^2C clock	Negative analog comparator input 1
24	I	CPP [3]	Positive analog comparator input 3	-	-	-
25	I	CPP [2]	Positive analog comparator input 2	-	-	-
26	I	CPM32	Negative analog comparator input 3, 2	-	-	-
-	I	CPM3	Negative analog comparator input 3	-	-	-
-	I	CPP2_CPM3	Positive analog comparator input 2 - Negative analog comparator input 3	-	-	-
27	I	CPP [1]	Positive analog comparator input 1	-	-	-
28	I	CPP [0]	Positive analog comparator input 0	-	-	-
29	PS	VDDA	Analog power supply	-	-	-
30	PS	VSSA	Analog ground	-	-	-

Table 4. Pin description (continued)

Pin number TSSOP 38	Type	Pin name	Main function	Alternate function 1	Alternate function 2	Alternate function 3
31	I	ADCIN [7]	Analog input 7	-	-	-
32	I	ADCIN [6]	Analog input 6	-	-	-
33	I	ADCIN [5]	Analog input 5	-	-	-
34	I	ADCIN [4]	Analog input 4	-	-	-
35	I	ADCIN [3]	Analog input 3	-	-	-
36	I	ADCIN [2]	Analog input 2	-	-	-
37	I	ADCIN [1]	Analog input 1	-	-	-
38	I	ADCIN [0]	Analog input 0	-	-	-

6.3 Input/output specifications

The STNRG family includes three different I/O types:

- Normal I/Os configurable either at 2 or 10 MHz maximum frequency
- Fast I/O operating up to 12 MHz.
- High speed I/O operating up to 32 MHz

The STNRG I/Os are designed to withstand current injection. For a negative injection current of 4 mA, the resulting leakage current in the adjacent input does not exceed 1 µA; further details are available in *Section 12 on page 81*.

7 I/O multifunction signal configuration

Several I/Os have multiple functionalities selectable through the configuration mechanism described from *Section 7.1* to *Section 7.5 on page 41*. The STNRG I/Os are grouped into four different configurable ports: P0, P1, P2 and P3.

7.1 Multifunction configuration policy

STNRG devices support either a cold or warm multifunction signal configuration policy according to the content of the EN_COLD_CFG bit field, a part of the GENCFG option byte register.

When the EN_COLD_CFG bit is set, the cold configuration is selected and the multifunction signals are configured according to the values stored in the option bytes; otherwise when the EN_COLD_CFG bit is cleared (default case), the warm configuration mode is chosen and the multifunction pin functionality is configured through the miscellaneous registers.

The configuration options and the proper configuration registers are detailed in *Table 5*.

Table 5. Multifunction configuration registers

EN_COLD_CFG	Configuration policy	Multifunction configuration registers
1	Cold	AFR_IOMXP0, AFR_IOMXP1 and AFR_IOMXP2
0 (default)	Warm	MSC_IOMXP0, MSC_IOMXP1 and MSC_IOMXP2

The warm configuration is volatile, thus not maintained after a device reset.

7.2 Port P0 I/O multifunction configuration signal

The Port P0 multiplexes several input/output functionalities, increasing the device flexibility. The P0 port pins can be independently assigned to general purpose I/Os or to internal peripherals. All communication peripherals and the external oscillator are hosted by the Port P0 pins.

In order to avoid electrical conflicts on the user application board, the P0 signals are configured at reset as GPIO0 inputs without pull-up resistors. Once reset is released, the firmware application must initialize the inputs with the proper configuration according to the application needs.

7.2.1 Alternate function P0 configuration signals

The multifunction pins can be configured via one of the following two registers, depending on the overall configuration policy (warm/cold):

- Cold configuration: AFR_IOMXP0 option byte registers (refer to *Section 10 on page 63*. After the reset the P0 signals are configured in line with AFR_IOMXP0 contents.
- Warm configuration: MSC_IOMXP0 miscellaneous register (refer to *Section 7.5 on page 41*). After the reset, the P0 signals are configured as GPIO input lines with the pull-up disabled.

Table 6 summarizes the Port P0 configuration scheme. Both registers MSC_IOMXP0 and AFR_IOMXP0 use the same register fields Sel_p054, Sel_p032 and Sel_p010 which respectively control the bits [5, 4], [3, 2] and [1, 0] of the Port P0.

Table 6. P0 internal multiplexing signals(1)

Port P0 multifunction configuration signal				
Port pins	**Multifunction signal**		**MUX SEL**	
			Selection fields	**Value (binary)**
P0 [1,0](2)	GPIO0 [1]	GPIO0 [0]	Sel_p010	00(3), (4)
	CPM1(3)	CPM0(4)		
	UART_rx	UART_tx		01
	I2C_scl	I2C_sda		10
	RFU reserved encoding			11
P0 [3, 2]	GPIO0 [3]	GPIO0 [2]	Sel_p032	00
	I2C_scl	I2C_sda		01
	HseOscin	HseOscout		10
	UART_rx	UART_tx		11
P0 [5, 4]	GPIO0 [5]	GPIO0 [4]	Sel_p054	00
	DALI_rx	DALI_tx		01
	I2C_scl	I2C_sda		10
	UART_rx	UART_tx		11

1. The Sel_p054, Sel_p032, Sel_p010 are register fields for both registers MSC_IOMXP0 and AFR_IOMXP0. The peripheral conflict (same resources selected on different pins at the same time) has to be prevented by SW configuration.
When the I^2C interface is selected either on the GPIO0 [5:4] or on the GPIO0 [3:2] signals the related I/O port speed has to be configured at 10 MHz by programming the GPIO0 internal peripheral.
2. Available only on STNRG388A.
3. The CPM1 (external COMP1 reference voltage) selection line requires the following configurations: GPIO0 [1] programmed as input Hiz and the bit field DAC1_EN = '0' and CP1_EN_ERef = '1 of MSC_DACCTR (available only on the STNRG388A).
4. The CPM0 (external COMP0 reference voltage) selection line requires the following configurations: GPIO0 [0] programmed as input Hiz (input high impedance with pull-up disable) and the bit field DAC0_EN = '0' and CP0_EN_ERef = '1 of MSC_DACCTR (available only on the STNRG388A).

7.2.2 Port P0 diagnostic signals

The primary I/Os can be used to trace the SMED's state evolution. This feature allows the debug of the complex SMED configurations. The trace selection can be enabled or disabled via register MSC_IOMXSMD. The diagnostic signal selection through MSC_IOMXSMD register overrides the functional configuration of MSC_IOMXP0 register.

The Port P0 [5:3] or P0 [2:0] can be configured to output one or two different SMEDs' current states.

The SMEDs FSM state signals (coded on three bits) may be multiplexed either on port bits P0 [5:3] or P0 [2:0]; alternatively two different SMEDs signal states can be traced

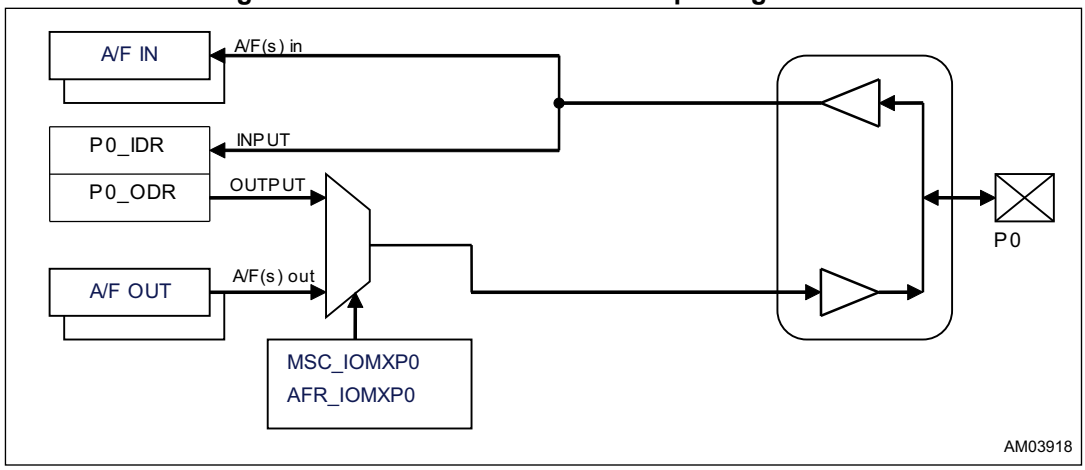
simultaneously on the same port bits. The SMED trace configuration is forbidden on the Port P [2:0] when the external comparator reference voltage is programmed on the Port P0 [1, 0].

Port 0 I/O signal availability depends on the STNRG device.

7.2.3 Port P0 I/O functional multiplexing signal

Figure 7 shows an outline view of the Port P0 multifunction multiplexing scheme.

Figure 7. Port P0 I/O functional multiplexing scheme



1. Where “A/F(s) in” and “A/F(s) out” signals are defined in Section 5.2 on page 28.
   Verify pinout availability in device pin table X?
   The P0 [6] is a multifunction signal configurable through the MSC_IOMXP2 [7] and AFR_IOMXP2 [7] register bits. For further details refer to Section-6.4.
   The Port P0 [6] signal is controlled by P0_ODR [6] and P0_IDR [6] GPIO0 registers.

7.2.4 P0 interrupt capability

Port P0 signals may be configured to generate maskable (IRQ) and un-maskable (NMI) interrupts by programming the MSC_CFGP0<n> and the MSC_STSP0 registers (n = index port signal).

The interrupt request may be configured to wake-up the IC device from the WFI (wait for interrupt), AHalt (active Halt) and Halt power saving state.

7.2.5 P0 programmable pull-up and speed feature

The I/O speed and pad pull-up resistance (47 kΩ) of the port P0 may be configured through the GPIO0 internal registers.

The pull-up resistance of the multifunction signal P0 [6] is always enabled.

7.3 Port P1 I/O multifunction configuration signal

The Port P1 I/O multifunction pins, similarly to the Port P0, can be individually configured through the following set of registers based on the selected device configuration policy:

- Cold configuration: AFR_IOMXP1 option byte register (refer to *Section 10 on page 63*). After reset the P1 signals are configured in line with AFR_IOMXP1 contents.
- Warm configuration: MSC_IOMXP1 miscellaneous register (refer to *Section 7.5*). After reset the P1 signals are configured as PWM output lines.

Every Port1 I/O can be configured to operate as a PWM output pin or a GPIO. Differently from the port P0s, the pins are configured as PWM output signals by default after reset.

Table 7 summarizes the Port P1 configurations as selected by the register fields Sel_p15 … Sel_p10 which respectively control the bits [5] … [0] of the Port P1 (verify resources availability on *Table 4: Pin description on page 32*).

Table 7. Port P1 I/O multiplexing signal(1)

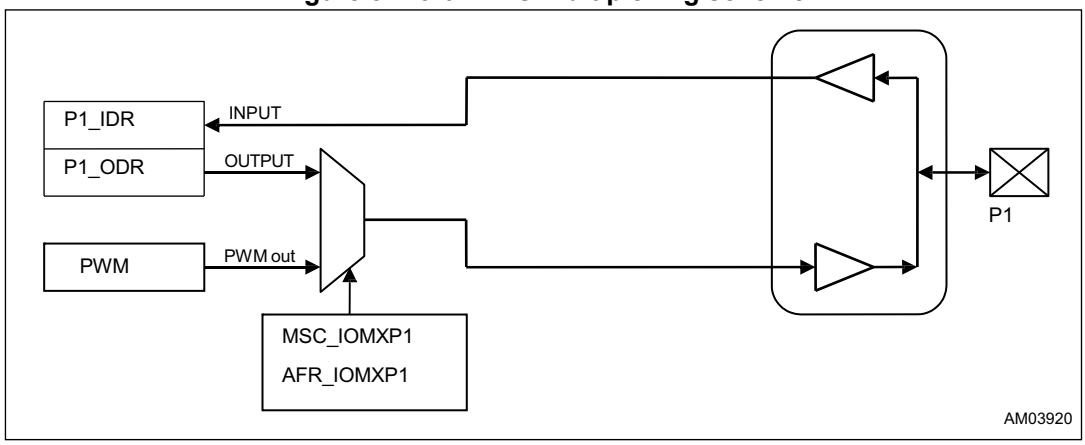
Port P1 multifunction configuration signal			
Output signal	Multi- function signal	MUX selection	
		Selection bits	Value (binary)
P1 [0]	PWM [0]	Sel_p10	1
	GPIO1 [0]		0
P1 [1]	PWM [1]	Sel_p11	1
	GPIO1 [1]		0
P1 [2]	PWM [2]	Sel_p12	1
	GPIO1 [2]		0
P1 [3]	PWM [3]	Sel_p13	1
	GPIO1 [3]		0
P1 [4]	PWM [4]	Sel_p14	1
	GPIO1 [4]		0
P1 [5]	PWM [5]	Sel_p15	1
	GPIO1 [5]		0

1. The Sel_p15…Sel_p10 are common register fields of both registers MSC_IOMXP1 and AFR_IOMXP1. In cold configuration the P1x are configured as defined by the AFR_IOMXP1 option byte. The PWM default polarity level is configured by the register option byte GENCFG. Verify pin out availability in *Table 4: Pin description on page 32*.

7.3.1 Port P1 I/O multiplexing signal

Figure 8 shows an outline view of the port P1 signal multiplexing scheme.

Figure 8. Port P1 I/O multiplexing scheme



1. The P1 [5:0] output signals may be read back from the P1_IDR register only when the pins are configured as GPIO out or PWM signals.
The PWM internal signal is read- back also by its own SMED through the SMD<n>_FSM_STS register.
P1_ODR [7:6] and P1_IDR [7:6] registers control the GPIO1 [7:6] alternate function signals, for further details refer to*Section 7.4*.
Check device feature availability.

7.3.2 P1 interrupt capability

Port P1 signals may be configured to generate maskable (IRQ) and un-maskable (NMI) interrupts by configuring the MSC_CFGP1<n> and the MSC_STSP1 registers (n = index port signal 4- 0). This functionality is applicable to the bit port P1 [4:0].

The interrupt request may be configured to wake-up the IC device from the WFI (wait for interrupt), AHalt (active Halt) and Halt power saving state.

7.3.3 P1 programmable pull-up feature

The pad pull-up resistances (47 kΩ) of the Port1 may be configured through the GPIO1 internal register.

The PWM output pseudo open drain functionality is controllable by the GPIO1 registers.

7.4 Port P2 I/O multifunction configuration signal

The Port2 I/O multifunction pins, similarly to the Port0 and Port2, can be individually configured through the following set of registers based on the selected device configuration policy:

- Cold configuration: AFR_IOMXP2 option byte registers (refer to *Section 10 on page 63*. After reset the P2 signals are configured in line with AFR_IOMXP2 contents.
- Warm configuration: MSC_IOMXP2 miscellaneous register (refer to *Section 7.5*). After reset the P2 signals are configured as DIGIN input lines with pull-up enabled.

Table 8 summarizes the port P2 configurations selected by the register fields Sel_p25 … Sel_p20 which respectively control the bits [5]… [0] of the port P2. The P2 [0] is configured by the CCOEN bit field of the register CKC_CCOR. The SWIM alternate function signal

(when available) is controlled by the Sel_SWIM bit field provided by registers AFR_IOMXP2 [7] and MSC_IOMXP2 [7].

Table 8. Port P2 I/O multiplexing signal(1)

Port P2 multifunction configuration signal				
Output signal	Multi-function signal		MUX SEL	
			Selection bits	Value (binary)
P2 [0]	DIGIN [0]		CCOEN	0(2)
	CCO			1
P2 [1]	GPIO1 [6]		Sel_P21	0
	DIGIN [1]			1(2)
P2 [3]	GPIO0 [7]		Sel_P23	0
	DIGIN [3]			1(2)
P2 [5, 4]	GPIO1 [7]	GPIO1 [6]	Sel_P2 [5, 4]	00
	GPIO1 [7]	DIGIN [4]		01
	I2C_scl	I2C_sda		10
	DIGIN [5]	DIGIN [4]		11(2)
SWIM	SWIM		Sel_SWIM	X(3)
	GPIO0 [6]			0(4)
	DIGIN1 (3)			1

1. The Sel_P2 [5, 4, 3, 1] is a common register field of both registers MSC_IOMXP2 and AFR_IOMXP2. The peripheral conflict (same resources selected on different pins at the same time) has to be prevented by SW configuration.
After reset by default P2 [3, 1, 0] are configured as DIGIN [3, 1, 0] signals.
The option byte AFR_IOMXP2, before user configuration, by default selects the I^2C alternative functionality.
The signal ports P2 [3:1] are exclusively interconnected with DIGIN [3:1] primary pins. When the I^2C i/f is selected on DIGIN [5:4] signals the I/O speed is auto-configured at 10 MHz and the internal pull-up functionality is controlled by the MSC_INPP2AUX1 register.
After reset by default the P2 [0] is configured as the DIGIN [0] signal.
GPIO1 [7:6] signals are controlled by P1_ODR [7:6] and P1_IDR [7:6] GPIO1 registers.
2. Default configuration after reset if the option byte is at the manufactory value.
Verify pin out availability in device pin table X.
3. SWIM pin: SWIM signal function is selected when CFG_GCR [0] = '0'.
4. SWIM pin: The GPIO0 [6] signal is selected when both Sel_SWIM = '0' and CFG_GCR [0] = '1'.

7.4.1 P2 ADC hardware trigger

The DIGIN [0, 3] signals may be configured to generate a HW trigger request to start the ADC conversion.

7.4.2 P2 interrupt capability

Port P2 signals may be configured to generate maskable (IRQ) and un-maskable (NMI) interrupts by configuring the MSC_CFGP2<n> and the MSC_STSP2 registers (n = index port signal 0 - 5).

The interrupt functionality is available on the port P2 [5:4] also in case these signals are configured as GPIO1 [7:6].

The interrupt request may be configured to wake-up the IC device from the WFI (wait for interrupt), AHalt (active Halt) and Halt power saving state.

7.4.3 P2 programmable pull-up feature

The pad pull-up resistances (47 kΩ) of Port2 signals are individually controllable by the MSC_INPP2AUX1 register.

7.5 Port P3 analog signal

The port P3 is an analog signal port based on the comparator input signals CPP [3:0]. Differently than the digital ports, the P3 is a single function port with fixed signal assignment.

7.5.1 P3 ADC conversion request

The CMP [0, 3] internal output signals may be configured to generate a HW trigger request to start the ADC conversion.

7.5.2 P3 interrupt capability

The comparator output signals of the port P3 (CMP [3:0]) may be configured to generate maskable interrupts by programming the MSC_CFGP3<n> and the MSC_STSP3 registers (n = index port signal 0-3).

The interrupt request may be configured to wake-up the IC device from the WFI (wait for interrupt), AHalt (active Halt) and Halt power saving state.

7.6 Multifunction port configuration registers

MSC_IOMXP0 (Port P1 I/O MUX control register)

Table 9. MSC_IOMXP0 (Port P1 I/O MUX control register)

Offset: 0x2A							
Default value: 0x00							
7	6	5	4	3	2	1	0
RFU		Sel_P054 [1:0]		Sel_P032 [1:0]		Sel_P010 [1:0]	
r		r/w		r/w		r/w	

The Port0 I/O multifunction signal configurations register (for functionality description refer to *Section 7.2 on page 35*).

Check device feature availability.

Bit 1 - 0:

Sel_P010 [1:0] Port0 [1:0] I/O multiplexing scheme:

00: Port0 [1:0] the bit port may be configured individually as GPIO [1:0] or as CPM [1:0] (comparator [1:0] external reference voltage):

GPIO0 [1:0] signals are controlled by the GPIO0 internal registers.

CPM [1, 0]: comparator external reference voltage requires that following configurations:

- GPIO0 [x] configured as input Hiz (where x = 1,0)
- DAC<x>_EN = '0' and CP<x>_EN_ERef = '1 of MSC_DACCTR available only on the STNRG388A register.

01: Port0 [1:0] are interconnected to UART_rx and UART_tx signals

10: Port0 [1:0] are interconnected to I^2C_scl and I^2C_sda signals

11: RFU

Bit 3 - 2:

Sel_P032 [1:0] Port0 [3:2] I/O multiplexing scheme:

00: Port0 [3:2] are interconnected to GPIO0 [3:2] signals

01: Port0 [3:2] are interconnected to I2C_scl and I2C_sda signals

10: Port0 [3:2] are interconnected to HseOscin and HseOscout analog signals

11: Port0 [3:2] are interconnected to UART_rx and UART_tx signals

Bit 5 - 4:

Sel_P054 [1:0] Port0 [5:4] I/O multiplexing scheme:

00: Port0 [5:4] are interconnected to GPIO0 [5:4] signals

01: Port0 [5:4] are interconnected to DALI_rx and DALI_tx signals

10: Port0 [5:4] are interconnected to I2C_scl and I2C_sda signals

11: Port0 [5:4] are interconnected to UART_rx and UART_tx signals

Bit 7 - 6:

RFU reserved; in order to guarantee future compatibility, the bits are kept or set to 0 during register write operations.

MSC_IOMXP1 (Port P1 I/O MUX control register)

Table 10. MSC_IOMXP1 (Port P1 I/O MUX control register)

Offset: 0x2B							
Default value: 0x3F							
7	6	5	4	3	2	1	0
RFU		Sel_P15	Sel_P14	Sel_P13	Sel_P12	Sel_P11	Sel_P10
r		r/w					

The Port1 I/O multifunction signal configuration register (for functionality description refer to *Section 7.3 on page 38*).

Check device feature availability.

Bit 0:

Sel_P10 Port1 [0] I/O multiplexing scheme:

0: Port1 [0] is interconnected to GPIO1 [0] signal

1: Port1 [0] is interconnected to PWM [0] signal

Bit 1:

Sel_P11 Port1 [1] I/O multiplexing scheme:

0: Port1 [1] is interconnected to GPIO1 [1] signal

1: Port1 [1] is interconnected to PWM [1] signal

Bit 2:

Sel_P12 Port1 [2] I/O multiplexing scheme:

0: Port1 [2] is interconnected to GPIO1 [2] signal

1: Port1 [2] is interconnected to PWM [2] signal

Bit 3:

Sel_P13 Port1 [3] I/O multiplexing scheme:

0: Port1 [3] is interconnected to GPIO1 [3] signal

1: Port1 [3] is interconnected to PWM [3] signal

Bit 4:

Sel_P14 Port1 [4] I/O multiplexing scheme:

0: Port1 [4] is interconnected to GPIO1 [4] signal

1: Port1 [4] is interconnected to PWM [4] signal

Bit 5:

Sel_P15 Port1 [5] I/O multiplexing scheme:

0: Port1 [5] is interconnected to GPIO1 [5] signal

1: Port1 [5] is interconnected to PWM [5] signal

Bit 7 - 6:

RFU reserved; in order to guarantee future compatibility, the bits are kept or set to 0 during register write operations.

MSC_IOMXP2 (Port P2 I/O MUX control register)

Table 11. MSC_IOMXP2 (Port P2 I/O MUX control register)

Offset: 0x13 (indirect area)							
Default value: 0xFF							
7	6	5	4	3	2	1	0
Sel_SWIM	RFU	Sel_P25	Sel_P24	Sel_P23	RFU	Sel_P21	RFU
r/w	r	r/w	r/w	r/w	r	r/w	r

The Port1 I/O multifunction signal configurations register (for functionality description refer to *Section 7.4 on page 39*).

Check device feature availability.

Bit 0:

RFU reserved; must be kept 0 during register writing for future compatibility

Bit 1:

Sel_P21 Port2 [1] I/O multiplexing scheme:

0: Port2 [1] is interconnected to GPIO1 [6].

1: Port2 [1] is interconnected to DIGIN [1] signals.

Bit 2:

RFU reserved; must be kept 0 during register writing for future compatibility

Bit 3:

Sel_P23 Port2 [3] I/O multiplexing scheme:

0: Port2 [3] is interconnected to GPIO0 [7].

1: Port2 [3] is interconnected to DIGIN [3] signals.

Bit 5-4:

00: Port2 [5:4] are interconnected to GPIO1 [7:6] signals.

01: Selects the following signal assignment:

- Port2 [5] is interconnected to the GPIO1 [7] signal.
- Port2 [4] is interconnected to the DIGIN [4] signal.

10: Port2 [5:4] are interconnected to I2C_Scl and I2C_Sda signals.

11: Port2 [5:4] are interconnected to DIGIN [5:4] signals.

Note: The AFR_IOMXP2 [4] register field is capable only to configure the coding value 00 and 01:

00: Port2 [5:4] are interconnected to GPIO1 [7:6] signals.

01: Following signal assignment selection:

- *Port2 [5] is interconnected to the GPIO1 [7] signal.*
- *Port2 [4] is interconnected to the DIGIN [4] signal*.

Bit 6:

RFU reserved; in order to guarantee future compatibility, the bits are kept or set to 0 during register write operations.

Bit 7:

Sel_SWIM SWIM alternate function signal enable; this feature is active when the SWD field of the register CFG_GCR is set.

0: SWIM pin is configured with the GPIO0 [6] signal.

1: SWIM functionality is preserved.

MSC_INPP2AUX1 (INPP aux register)

Table 12. MSC_INPP2AUX1 (INPP aux register)

Offset: 0x08 (indirect area)							
Default value: 0x00							
7	6	5	4	3	2	1	0
ADCTRG_EN	RFU	INPP2_PULCTR [5:0]					
r/w	r	r/w					

Check device feature availability.

Bit 5 - 0:

INPP2_PULCTR [5:0].This register configures respectively the INPP2 [5:0] pull-up functionality as follows:

0: enable pad pull-up features (enabled by default)

1: disable pad pull-up

Bit 6:

RFU reserved; in order to guarantee future compatibility, the bits are kept or set to 0 during register write operations.

Bit 7:

ADCTRG_EN controls the ADC HW triggered conversion request:

0: disable the ADC HW triggered conversion request (disabled by default)

1: enable the ADC HW triggered conversion request. Set/cleared by SW. Cleared by HW when SW/HW conversion starts or when the stop command is issued

Note: Due to DIGINs interconnections, the pull-up functionality must be configured in the same way if the two pins are connected together:

- *DIGIN10 is controlled by the register field INPP2_PULCTR [1:0]*
- *DIGIN32 is controlled by the register field INPP2_PULCTR [3:2]*
- *DIGIN54 is controlled by the register field INPP2_PULCTR [5:4].*

When the DIGIN1 signal is selected on the SWIM pin the pull-up is always enabled.

8 Memory and register map

8.1 Memory map overview

This section describes the register map implemented in STNRG devices. *Table 13* shows the main memory map organization. All registers and memory spaces are configured within the first 64 Kbytes of memory, the remaining address spaces are kept reserved for the future use.

Table 13. Internal memory map

Address	Description
00.0000h 00.17FFh	6 kB RAM [data and stack area(1)]
00.1800h 00.3FFFh	Reserved
00.4000h 00.43FFh	1 kB data E^2PROM
00.4400h 00.47FFh	Reserved
00.4800h 00.487Fh	128 option bytes
00.4880h 00.4FFFh	Reserved
00.5000h 00.57FFh	Peripheral register region
00.5800h 00.5FFFh	Reserved
00.6000h 00.67FFh	2 kB boot ROM
00.6800h 00.7EFFh	Reserved
00.7F00h 00.7FFFh	Core register region
00.8000h	32 interrupt vectors
00.8080h 00.FFFFh	32 kB program Flash
01.0000h FF.FFFFh	Reserved

1. By default, the stack address is initialized at 0x07FF and rolls over when it reaches the address value of 0x0400. The stack address value may be modified by the user at runtime.

8.2 Register map

Section 8.2.1 shows the STNRG memory map.

8.2.1 General purpose I/O GPIO0 register map

Table 14. General purpose I/O GPIO0 register map

Address	Block	Register name	Register description
0x00.5000	GPIO0	P0_ODR	Output data
0x00.5001		P0_IDR	Input data
0x00.5002		P0_DDR	Data direction
0x00.5003		P0_CR1	Control register 1
0x00.5004		P0_CR2	Control register 2

8.2.2 General purpose I/O GPIO1 register map

Table 15. General purpose I/O GPIO0 register map

Address	Block	Register name	Register description
0x00.5005	GPIO1	P1_ODR	Output data
0x00.5006		P1_IDR	Input data
0x00.5007		P1_DDR	Data direction
0x00.5008		P1_CR1	Control register 1
0x00.5009		P1_CR2	Control register 2

8.2.3 Miscellaneous registers

Direct register address mode

Table 16. Miscellaneous direct register address mode

Address	Block	Register name	Register description
0x00.5010	MSC	MSC_CFGP00	P00 input line control
0x00.5011		MSC_CFGP01	P01 input line control
0x00.5012		MSC_CFGP02	P02 input line control
0x00.5013		MSC_CFGP03	P03 input line control
0x00.5014		MSC_CFGP04	P04 input line control
0x00.5015		MSC_CFGP05	P05 input line control
0x00.5016		MSC_CFGP20	P20 input line control
0x00.5017		MSC_CFGP21	P21 input line control
0x00.5018		MSC_CFGP22	P22 input line control
0x00.5019		MSC_CFGP23	P23 input line control
0x00.501A		MSC_CFGP24	P24 input line control
0x00.501B		MSC_CFGP25	P25 input line control
0x00.501C		MSC_STSP0	Port0 status
0x00.501D		MSC_STSP2	Port2 status
0x00.501E		MSC_INPP2	Port2 read
0x00.501F		RFU	Reserved for future use
0x00.5020		MSC_DACCTR	Comparator and DAC configuration(1)
0x00.5021		MSC_DACIN0	DAC0 input data
0x00.5022		MSC_DACIN1	DAC1 input data
0x00.5023		MSC_DACIN2	DAC2 input data
0x00.5024		MSC_DACIN3	DAC3 input data
0x00.5025		MSC_SMDCFG01	SMED 0 - 1 behavior
0x00.5026		MSC_SMDCFG23	SMED 2 - 3 behavior
0x00.5027		MSC_SMDCFG45	SMED 4 - 5 behavior
0x00.5028		MSC_SMSWEV	SMED software events
0x00.5029		MSC_SMUNLOCK	SMED unlock
0x00.502A		MSC_CBOXS0	Connection matrix selection for SMED 0
0x00.502B		MSC_CBOXS1	Connection matrix selection for SMED 1
0x00.502C		MSC_CBOXS2	Connection matrix selection for SMED 2
0x00.502D		MSC_CBOXS3	Connection matrix selection for SMED 3
0x00.502E		MSC_CBOXS4	Connection matrix selection for SMED 4
0x00.502F		MSC_CBOXS5	Connection matrix selection for SMED 5

Table 16. Miscellaneous direct register address mode (continued)

Address	Block	Register name	Register description
0x00.5030	MSC	MSC_IOMXSMD	SMED Trace multiplexing on port 0
0x00.5031		MSC_CFGP10	P10 input line control
0x00.5032		MSC_CFGP11	P11 input line control
0x00.5033		MSC_CFGP12	P12 input line control
0x00.5034		MSC_CFGP13	P13 input line control
0x00.5035		MSC_CFGP14	P14 input line control
0x00.5036		MSC_CFGP15	P15 input line control
0x00.5037		MSC_STSP1	Port 1 status
0x00.5038		RFU	Reserved for future use
0x00.5039		MSC_INPP3	Port 3 (COMP) read
0x00.503A		MSC_IOMXP0	Port 0 alternate function MUX
0x00.503B		MSC_IOMXP1	Port 1 alternate function MUX
0x00.503C		MSC_IDXADD	MSC indirect register
0x00.503D		MSC_IDXDAT	MSC indirect data

1. The register bitmask definition depends on product.

Indirect register address mode

Table 17. Miscellaneous indirect register address mode

Address (IDX)	Block	Register name	Register description
0x00	MSC (indirect)	MSC_FTM0CKSEL	Basic timer source clock selection
0x01		MSC_FTM0CKDIV	Basic Timer0 clock prescaler
0x02		MSC_FTM0CONF	Basic Timer0 counter value
0x03		MSC_FTM1CKDIV	Basic Timer1 clock prescaler
0x04		MSC_FTM1CONF	Basic Timer1 counter value
0x05		MSC_DALICKSEL	DALI clock selection
0x06		MSC_DALICKDIV	DALI filter clock division factor
0x07		MSC_DALICONF	DALI filter mode configuration
0x08		MSC_INPP2AUX1	INPP2 auxiliary configuration register 1
0x09		MSC_INPP2AUX2	INPP2 auxiliary configuration register 2
0x0A		MSC_DAC0HYS	DAC0 hysteresis controls
0x0B		MSC_DAC1HYS	DAC1 hysteresis controls
0x0C		MSC_DAC2HYS	DAC2 hysteresis controls
0x0D		MSC_DAC3HYS	DAC3 hysteresis controls
0x0E		MSC_CFGP30	P30 input line control
0x0F		MSC_CFGP31	P31 input line control
0x10		MSC_CFGP32	P32 input line control
0x11		MSC_CFGP33	P33 input line control
0x12		MSC_STSP3	Port 3 status
0x13		MSC_IOMXP2	Port2 alternate function MUX register

8.2.4 Flash and E^{2}PROM non-volatile memories

Table 18. Non-volatile memory register map

Address	Block	Register name	Register description
0x00.505A	MIF	FLASH_CR1	Control register 1
0x00.505B		FLASH_CR2	Control register 2
0x00.505C		FLASH_nCR2	Control register 2 (protection)
0x00.505D		FLASH_FPR	Memory protection
0x00.505E		FLASH_nFPR	Memory protection (complemented register)
0x00.505F		FLASH_IAPSR	Flash status
0x00.5062		FLASH_PUKR	Write memory protection removal key register
0x00.5063		RFU	Reserved for future use
0x00.5064		FLASH_DUKR	Write memory protection removal data
0x00.5071		FLASH_WAIT	Time access wait-state reg.

8.2.5 Reset register

Table 19. RST_SR register map

Address	Block	Register name	Register description
0x00.50B3	RSTC	RST_SR	Reset control status

8.2.6 Clock controller register

Table 20. Clock controller register map

Address	Block	Register name	Register description
0x00.50B4	CKC	CLK_SMD0	SMED 0 clock configuration
0x00.50B5		CLK_SMD1	SMED 1 clock configuration
0x00.50B6		CLK_SMD2	SMED 2 clock configuration
0x00.50B7		CLK_SMD3	SMED 3 clock configuration
0x00.50B8		CLK_SMD4	SMED 4 clock configuration
0x00.50B9		CLK_SMD5	SMED 5 clock configuration
0x00.50BA		RFU	Reserved for future use
0x00.50BB		RFU	Reserved for future use
0x00.50BC		RFU	Reserved for future use
0x00.50BD		RFU	Reserved for future use
0x00.50BE		CLK_PLLDIV	PLL clock divisor
0x00.50BF		CLK_AWUDIV	AWU clock divisor
0x00.50C0		CLK_ICKR	Internal clock control
0x00.50C1		CLK_ECKR	External clock control
0x00.50C2		CLK_PLLR	PLL control
0x00.50C3		CLK_CMSR	Clock master
0x00.50C4		CLK_SWR	Clock switch
0x00.50C5		CLK_SWCR	Switch control
0x00.50C6		CLK_CKDIVR	Clock dividers
0x00.50C7		CLK_PCKENR1	Peripherals clock enable
0x00.50C8		CLK_CSSR	Clock security system
0x00.50C9		CLK_CCOR	Configurable clock output
0x00.50CA		CLK_PCKENR2	Peripherals clock enable
0x00.50CB		RFU	Reserved for future use
0x00.50CC		CLK_HSITRIMR	HSI calibration trimmer
0x00.50CD		CLK_SWIMCCR	SWIM clock division
0x00.50CE		CLK_CCODIVR	CCO divider
0x00.50CF		CLK_ADCR	ADC clock configuration

8.2.7 WWDG timers

Table 21. WWDG timer register map

Address	Block	Register name	Register description
0x00.50D1	WWDG	WWDG_CR	Watchdog control
0x00.50D2		WWDG_WR	Watchdog window

8.2.8 IWDG timers

Table 22. IWDG timer register map

Address	Block	Register name	Register description
0x00.50E0	IWDG	IWDG_KR	Watchdog key
0x00.50E1		IWDG_PR	Watchdog time base
0x00.50E2		IWDG_RLR	Watchdog counter value after reload

8.2.9 AWU timers

Table 23. AWU timer register map

Address	Block	Register name	Register description
0x00.50F0	AWU	AWU_CSR	AWU control status
0x00.50F1		AWU_APR	AWU asynchronous prescaler buffer
0x00.50F2		AWU_TBR	AWU time base selection

8.2.10 Inter-integrated circuit interface (I^2C)

Table 24. I^2C register map

Address	Block	Register name	Register description
0x00.5210	I^2C	I^2C_CR1	I^2C control register 1
0x00.5211		I^2C_CR2	I^2C control register 2
0x00.5212		I^2C_FREQR	I^2C frequency register
0x00.5213		I^2C_OARL	I^2C own add-low register
0x00.5214		I^2C_OARH	I^2C own add-high register
0x00.5215		RFU	Reserved for future use
0x00.5216		I^2C_DR	I^2C data register
0x00.5217		I^2C_SR1	I^2C status register 1
0x00.5218		I^2C_SR2	I^2C status register 2
0x00.5219		I^2C_SR3	I^2C status register 3
0x00.521A		I^2C_ITR	I^2C interrupt
0x00.521B		I^2C_CCRL	I^2C clock control
0x00.521C		I^2C_CCRH	I^2C clock control
0x00.521D		I^2C_TRISER	I^2C rising edge

8.2.11 Universal asynchronous receiver/transmitter (UART)

Table 25. UART register map

Address	Block	Register name	Register description
0x00.5230	UART	UART_SR	UART status
0x00.5231		UART_DR	UART data
0x00.5232		UART_BRR1	UART baud rate div mantissa [7:0]
0x00.5233		UART_BRR2	UART baud rate div mantissa [11:8] SCIDIV FRACT [3:0]
0x00.5234		UART_CR1	UART control register 1
0x00.5235		UART_CR2	UART control register 2
0x00.5236		UART_CR3	UART control register 3
0x00.5237		UART_CR4	UART control register 4

8.2.12 System timer registers

Table 26. System timer register map

Address	Block	Register name	Register description
0x00.5340	STMR	STMR_CR1	Control register 1
0x00.5341		STMR_IER	Interrupt enable
0x00.5342		STMR_SR1	Status register 1
0x00.5343		STMR_EGR	Event generation
0x00.5344		STMR_CNTH	Counter high
0x00.5345		STMR_CNTL	Counter low
0x00.5346		STMR_PSCL	Prescaler low
0x00.5347		STMR_ARRH	Autoreload high
0x00.5348		STMR_ARRL	Autoreload low

8.2.13 Auxiliary timer registers

Table 27. Auxiliary timer register map

Address	Block	Register name	Register description
0x00.5009	GPIO1	P1CR2	Control register 2
0x00.5036	MSC	MSC_CFGP15	P15 input line control
0x00.5037		MSC_STSP1	Port 1 status
0x00.50C6	CKC	CLK_CCODIVR	CCO clock dividers
0x00.50C9		CLK_CCOR	Configurable clock output

8.2.14 Basic timer0 registers

Table 28. Basic timer0 register map

Address	Offset	Block	Register name	Register description
0x00.5031	N.A.	MSC	MSC_CFGP10	P10 input line control
0x00.5037	N.A.		MSC_STSP1	Port 1 status
0x00.503C	0x00	MSC (indirect)	MSC_FTM0CKSEL	Basic timer source clock selection
0x00.503C	0x01		MSC_FTM0CKDIV	Basic Timer0 clock prescaler
0x00.503C	0x02		MSC_FTM0CONF	Basic Timer0 counter value

8.2.15 Basic timer1 registers

Table 29. Basic timer1 register map

Address	Offset	Block	Register name	Register description
0x00.5032	N.A.	MSC	MSC_CFGP11	P11 input line control
0x00.5037	N.A.		MSC_STSP1	Port 1 status
0x00.503C	0x00	MSC (indirect)	MSC_FTM0CKSEL	Basic timer source clock selection
0x00.503C	0x03		MSC_FTM1CKDIV	Basic Timer1 clock prescaler
0x00.503C	0x04		MSC_FTM1CONF	Basic Timer1 counter value

8.2.16 Digital addressable lighting interface (DALI)

Table 30. DALI register map

Address	Block	Register name	Register description
0x00.53C0	DALI	DALI_CLK_L	Data rate control
0x00.53C1		DALI_CLK_H	Data rate control
0x00.53C2		DALI_FB0	Forward message
0x00.53C3		DALI_FB1	Forward message
0x00.53C4		DALI_FB2	Forward message
0x00.53C5		DALI_BD	Backward message
0x00.53C6		DALI_CR	Control
0x00.53C7		DALI_CSR	Control and status register
0x00.53C8		DALI_CSR1	Control and status register 1
0x00.53C9		DALI_REVLN	Control reverse signal line

8.2.17 DALI noise rejection filter registers

Table 31. DALI filter register map

Address	Offset	Block	Register name	Register description
0x00.503C	0x05	MSC (indirect)	MCS_DALICKSEL	DALI clock selection
0x00.503C	0x06		MSC_DALICKDIV	DALI filter clock division factor
0x00.503C	0x07		MSC_DALICONF	DALI filter mode configuration

8.2.18 Analog-to-digital converter (ADC)

Table 32. ADC register map and reset value

Address	Block	Register name	Register description
0x00.5400	ADC	ADC_CFG	Configuration
0x00.5401		ADC_SOC	Start of conversion
0x00.5402		ADC_IER	Interrupt enable
0x00.5403		ADC_SEQ	Sequencer
0x00.5404		ADC_DATL_0	Low part data 0 converted
0x00.5405		ADC_DATH_0	High part data 0 converted
0x00.5406		ADC_DATL_1	Low part data 1 converted
0x00.5407		ADC_DATH_1	High part data 1 converted
0x00.5408		ADC_DATL_2	Low part data 2 converted
0x00.5409		ADC_DATH_2	High part data 2 converted
0x00.540A		ADC_DATL_3	Low part data 3 converted
0x00.540B		ADC_DATH_3	High part data 3 converted
0x00.540C		ADC_DATL_4	Low part data 4 converted
0x00.540D		ADC_DATH_4	High part data 4 converted
0x00.540E		ADC_DATL_5	Low part data 5 converted
0x00.540F		ADC_DATH_5	High part data 5 converted
0x00.5410		ADC_DATL_6	Low part data 6 converted
0x00.5411		ADC_DATH_6	High part data 6 converted
0x00.5412		ADC_DATL_7	Low part data 7 converted
0x00.5413		ADC_DATH_7	High part data 7 converted
0x00.5414		ADC_SR	Status
0x00.5415		ADC_DLYCNT	SOC delay counter

8.2.19 State machine event driven (SMEDs)

The SMED<n> address register is:

ADD_REG = (5500h + (40h) * n) + offset

where <n> is the SMED instance number 0 - 5.

Table 33. SMED register map

Address (offset)	Block	Register name	Register description
0x00	SMED<n>	SMD<n>_CTR	Control
0x01		SMD<n>_CTR_TMR	Control time
0x02		SMD<n>_CTR_INP	Control input
0x03		SMD<n>_CTR_DTR	Dithering
0x04		SMD<n>_TMR_T0L	Time T0 LSB
0x05		SMD<n>_TMR_T0H	Time T0 MSB
0x06		SMD<n>_TMR_T1L	Time T1 LSB
0x07		SMD<n>_TMR_T1H	Time T1 MSB
0x08		SMD<n>_TMR_T2L	Time T2 LSB
0x09		SMD<n>_TMR_T2H	Time T2 MSB
0x0A		SMD<n>_TMR_T3L	Time T3 LSB
0x0B		SMD<n>_TMR_T3H	Time T3 MSB
0x0C		SMD<n>_PRM_ID0	IDLE state parameter0
0x0D		SMD<n>_PRM_ID1	IDLE state parameter1
0x0E		SMD<n>_PRM_ID2	IDLE state parameter2
0x0F		SMD<n>_PRM_S00	S0 state parameter0
0x10		SMD<n>_PRM_S01	S0 state parameter1
0x11		SMD<n>_PRM_S02	S0 state parameter2
0x12		SMD<n>_PRM_S10	S1 state parameter0
0x13		SMD<n>_PRM_S11	S1 state parameter1
0x14		SMD<n>_PRM_S12	S1 state parameter2
0x15		SMD<n>_PRM_S20	S2 state parameter0
0x16		SMD<n>_PRM_S21	S2 state parameter1
0x17		SMD<n>_PRM_S22	S2 state parameter2
0x18		SMD<n>_PRM_S30	S3 state parameter0
0x19		SMD<n>_PRM_S31	S3 state parameter1
0x1A		SMD<n>_PRM_S32	S3 state parameter2

Table 33. SMED register map (continued)

Address (offset)	Block	Register name	Register description
0x1B	SMED<n>	SMD<n>_CFG	Timer configuration register
0x1C		SMD<n>_DMP_L	Counter dump LSB
0x1D		SMD<n>_DMP_H	Counter dump MSB
0x1E		SMD<n>_GSTS	General status
0x1F		SMD<n>_IRQ	Interrupt request register
0x20		SMD<n>_IER	Interrupt enable register
0x21		SMD<n>_ISEL	External events control
0x22		SMD<n>_DMP	Dump enable
0x23		SMD<n>_FSM_STS	FSM core status

8.2.20 CPU register

Table 34. CPU register map

Address	Block	Register name	Register description
0x00.7F00	CPU	A	Accumulator
0x00.7F01		PCE	Program counter extended
0x00.7F02		PCH	Program counter high
0x00.7F03		PCL	Program counter low
0x00.7F04		XH	X - index high
0x00.7F05		XL	X - index low
0x00.7F06		YH	Y - index high
0x00.7F07		YL	Y - index low
0x00.7F08		SPH	Stack pointer high
0x00.7F09		SPL	Stack pointer low
0x00.7F0A		CC	Code condition

Note: Register space accessible in debug mode only.

8.2.21 Global configuration register

Table 35. CFG_GCR register map

Address	Block	Register name	Register description
0x00.7F60	GCR	CFG_GCR	Global configuration

8.2.22 Interrupt controller

Table 36. Interrupt software priority register map

Address	Block	Register name	Register description
0x00.7F70	ITC	ITC_SPR0	Interrupt SW priority register 0
0x00.7F71		ITC_SPR1	Interrupt SW priority register 1
0x00.7F72		ITC_SPR2	Interrupt SW priority register 2
0x00.7F73		ITC_SPR3	Interrupt SW priority register 3
0x00.7F74		ITC_SPR4	Interrupt SW priority register 4
0x00.7F75		ITC_SPR5	Interrupt SW priority register 5
0x00.7F76		ITC_SPR6	Interrupt SW priority register 6
0x00.7F77		ITC_SPR7	Interrupt SW priority register 7

8.2.23 SWIM control register

Table 37. SWIM register map

Address	Block	Register name	Register description
0x00.7F80	SWIM	SWIM_CSR	SWIM control status
0x00.7F90	DM	DM_BK1E	DM internal registers
….		…	
0x00.7F9B		DM_VER	

9 Interrupt table

Table 38 shows the STNRG internal controller's interrupt.

Table 38. Interrupt vector exception

Priority	Source block	Description	Wakeup from Halt	Wakeup from active- halt	Interrupt vector address
	RESET	Reset	Yes	Yes	8000h
	TRAP	Software interrupt			8004h
0	NMI	NMI (not maskable interrupt)	Yes(1)	Yes(1)	8008h
1	AWU	Auto-wakeup from Halt		Yes	800Ch
2	CKC	Clock controller			8010h
3	PO	GPIO0 [5:0] external interrupts	Yes(1), (2)	Yes(1), (2)	8014h
4	P1	GPIO1 [5:0], Aux/Basic timers interrupts	Yes(1), (2)	Yes(1), (2)	8018h
5	P2	DIGIN[5:0] external interrupts	Yes(1), (2)	Yes(1), (2)	801Ch
6	SMED0	SMED-0 interrupt			8020h
7	SMED1	SMED-1 interrupt			8024h
8	P3	Comparator [3:0] interrupts	Yes(1), (2)	Yes(1), (2)	8028h
9	RFU(3)	Reserved for future use			802Ch
10	RFU(3)	Reserved for future use			8030h
11	RFU(3)	Reserved for future use			8034h
12	RFU(3)	Reserved for future use			8038h
13	RFU(3)	Reserved for future use			803Ch
14	RFU(3)	Reserved for future use			8040h
15	SMED2	SMED-2 interrupt			8044h
16	SMED3	SMED-3 interrupt			8048h
17	UART	Tx complete			804Ch
18	UART	Receive register DATA FULL	Indirect(4)	Indirect(4)	8050h
19	I^2C	I^2C interrupt	Indirect(4)	Yes	8054h
20	RFU(3)	Reserved for future use			8058h
21	RFU(3)	Reserved for future use			805Ch
22	ADC	End of conversion			8060h
23	SYS-TMR	Update/overflow			8064h
24	FLASH	EOP/WR_PG_DIS			8068h
25	DALI	DALI interrupt line	Indirect(4)	Indirect(4)	806Ch
26	SMED4	SMED-4 interrupt			8070h
27	SMED5	SMED-5 interrupt			8074h

Table 38. Interrupt vector exception (continued)

Priority	Source block	Description	Wakeup from Halt	Wakeup from active- halt	Interrupt vector address
28	RFU(3)	Reserved future use			8078h
29	RFU(3)	Reserved future use			807Ch

1. The P [2, 0] [x] may be configured to generate a NMI requests.
2. The P [3, 0] [x] may be configured to generate an IRQ requests.
3. All RFU and unused interrupts should be initialized with 'IRET' for robust programming.
4. The P0 [x] may be configured to generate an IRQ and NMI request.

10 Option bytes

The user option byte is a memory E²PROM area allowing users to customize the IC device major functionalities:

- ROP: read-out protection control field
- UBC: user boot code protection
- PWM: configurable reset output value
- WDG: internal watchdog HW configuration
- AFR: alternate multifunction signals configuration
- CKC: clock controller functionalities (PLL, HSE enable, AWU clock selection, etc.)
- HSE: clock stabilization counter
- WAIT: Flash and E²PROM wait state access time has to be configured with value 0x00
- BOOT: configurable internal boot sources
- BL: bootloader control sequences

Except the ROP byte all the other option bytes are stored twice in a regular (OPT) and complemented format (NOPT) for redundancy. The option byte can be programmed in ICP mode through the SWIM interface or in IAP mode by the application with the exception of the ROP byte that can be only configured via the SWIM interface.

For further information about Flash programming refer to the programming manual “How to program STM8S and STM8A Flash program memory and data EEPROM” (PM0051).

For information on SWIM programming procedures refer to the “STM8 SWIM communication protocol and debug module” user manual (UM0470).

10.1 Option byte register overview

Table 39. Option byte register overview - STNRG388A

Address	Option name	Option bits								Default settings
		7	6	5	4	3	2	1	0	
4800h	ROP	ROP [7:0]								00h
4801h	UCB	UBC [7:0]								00h
4802h	nUCB	nUBC [7:0]								FFh
4803h	GENCFG	Rst_PWM5	Rst_PWM4	Rst_PWM3	Rst_PWM2	Rst_PWM1	Rst_PWM0	-	EN_COLD_CFG	00h
4804h	nGENCFG	nRst_PWM5	nRst_PWM4	nRst_PWM3	nRst_PWM2	nRst_PWM1	nRst_PWM0	-	nEN_COLD_CFG	FFh
4805h	MISCUOPT	-	-	1	-	LSI_EN	IWdg_HW	WWdg_HW	WWDG_HALT	28h
4806h	nMISCUOPT	-	-	0	-	nLSI_EN	nIWdg_HW	nWWdg_HW	nWWDG_HALT	D7h
4807h	CLKCTL	PWM_OD	-	SMD_HWtrg	CKAWUSEL1	EXTCLK	CKAWUSEL0	PRSC [1:0]		89h
4808h	nCLKCTL	nPWM_OD	-	nSMD_HWtrg	nCKAWUSEL1	nEXTCLK	nCKAWUSEL0	nPRSC [1:0]		76h
4809h	HSESTAB	HSECNT [7:0]								00h
480Ah	nHSESTAB	nHSECNT [7:0]								FFh
480Bh	ENHFEAT	-	BscTim1	ADC_MFlush	BscTim0	-	-	-	-	00h
480Ch	nENHFEAT	-	nBscTim1	nADC_MFlush	nBscTim0	-	-	-	-	FFh
480Dh	WAITSTATE	-	ADC_NAbt	-	ADC_AFlush	-	ADC_ARlod	WaitStat [1:0]		00h
480Eh	nWAITSTATE	-	nADC_NAbt	-	nADC_AFlush	-	nADC_ARlod	nWaitStat [1:0]		FFh
480Fh	AFR_IOMXP0	-	-	Sel_P054 [1:0]		Sel_P032 [1:0]		Sel_P010 [1:0] (2)		00h
4810h	nAFR_IOMXP0	-	-	nSel_P054 [1:0]		nSel_P032 [1:0]		nSel_P010 [1:0] (2)		FFh
4811h	AFR_IOMXP1	AUXTMR	-	Sel_P15	Sel_P14	Sel_P13	Sel_P12	Sel_P11	Sel_P10	3Fh
4812h	nAFR_IOMXP1	nAUXTMR	-	nSel_P15	nSel_P14	nSel_P13	nSel_P12	nSel_P11	nSel_P10	C0h
4813h	AFR_IOMXP2	Sel_SWIM	ADC_HWtrg	1	Sel_P24	Sel_P23	-	Sel_P21	-	7Ah
4814h	nAFR_IOMXP2	nSel_SWIM	nADC_HWtrg	0	nSel_P24	nSel_P23	-	nSel_P21	-	85h

Table 39. Option byte register overview - STNRG388A (continued)

Address	Option name	Option bits								Default settings
		7	6	5	4	3	2	1	0	
4815h	MSC_OPT0	-	-	UARTLine [1:0]		-	-	BootSel [1:0]		01h
4816h	nMSC_OPT0	-	-	nUARTLine [1:0]		-	-	nBootSel [1:0]		FEh
4817h 487Dh	RESERVED	-	-	-	-	-	-	-	-	00h
487Eh	OPTBL	BL [7:0]								00h
487Fh	nOPTBL	nBL [7:0]								FFh

Note: The default setting values refer to the factory configuration. The factory configuration can be overwritten by the user in accordance with the target application requirements.
The factory configuration values are loosed after user programming fields or in case of the ROP unprotecting attempt causing a “Global Flash Erase”.
The predefined initialized bit-values (1 or 0) must be preserved during memory writing.
An undefined option bit must be keep 0 and the complement value at 1 during the memory writing sequence.

10.2 Option byte register description

The option byte registers are mapped inside the E²PROM data region.

10.2.1 ROP (memory read-out protection register)

Table 40. ROP (memory read-out protection register)

Offset: 0x004800							
Default value: 0x00							
7	6	5	4	3	2	1	0
ROP [7:0]							
r/w							

Bit 7 - 0:

ROP [7:0] memory read-out protection:

0xAA: enable read-out protection. When read-out protection is enabled, reading or modifying the Flash program memory and DATA area in ICP mode (using the SWIM interface) is forbidden, whatever the write protection settings are.

10.2.2 UBC (UBC user boot code register)

Table 41. UBC (UBC user boot code register)

Offset: 0x004801							
Default value: 0x00							
7	6	5	4	3	2	1	0
UBC [7:0]							
r/w							

Bit 7 - 0:

UBC [7:0] user boot code write protection memory size: 0x00: no UBC, no Flash memory write-protection

0x01: pages 0 to 1 defined as UBC; 1 Kbyte memory write-protected (0x00.8000-0x00.83FF)

0x02: pages 0 to 3 defined as UBC; 2 Kbyte memory write-protected (0x00.8000-0x00.87FF)

0x03: pages 0 to 4 defined as UBC; 2.5 Kbyte memory write-protected (0x00.8000-0x00.89FF)

... (512 byte every page)

0x3E: pages 0 to 63 defined as UBC; 32 Kbyte memory write-protected (0x00.8000-0x00.FFFF)

Other values: reserved.

10.2.3 nUBC (UBC user boot code register protection)

Table 42. nUBC (UBC user boot code register protection)

Offset: 0x004802							
Default value: 0xFF							
7	6	5	4	3	2	1	0
nUBC [7:0]							
r/w							

nUBC: not (UBC) EMC byte protection.

10.2.4 GENCFG (general configuration register)

Table 43. GENCFG (general configuration register)

Offset: 0x004803							
Default value: 0x00							
7	6	5	4	3	2	1	0
Rst_PWM [5:0]						RFU	EN_COLD_CFG
r/w						r	r/w

Bit 0:

The EN_COLD_CFG enables IC cold configuration through the option byte register AFR_IOMXP0, P1 and P2:

0: default case, the IC multifunction signal configuration is performed by the miscellaneous registers MSC_IOMXP0, MSC_IOMXP1 and MSC_IOMXP2 (warm configuration).

1: enables the multifunction signal configuration through the option byte registers AFR_IOMXP0, AFR_IOMXP1 and AFR_IOMXP2 (cold configuration).

Bit 1:

RFU reserved; must be kept 0 during register writing for future compatibility

Bit 7:2:

Rst_PWM [5:0] configures the PWM [n] reset value after the NRST signal

0: PWM [n] output low level (native default value)

1: PWM [n] output high level.

Note: The PWM signal programmed reset value is configured during the option byte loader phase, then before the NRST is released it assumes its proper initial values.

10.2.5 nGENCFG (general configuration register protection)

Table 44. nGENCFG (general configuration register protection)

Offset: 0x004804							
Default value: 0xFF							
7	6	5	4	3	2	1	0
nRst_PWM [5:0]						nRFU	nEN_COLD_CFG
r/w						r	r/w

nGENCFG: not (GENCFG) EMC byte protection

10.2.6 MISCUOPT (miscellaneous configuration register)

Table 45. MISCUOPT (miscellaneous configuration register)

Offset: 0x004805							
Default value: 0x28 (factory configuration)							
7	6	5	4	3	2	1	0
RFU		RFU	RFU	LSI_EN	IWdg_hw	WWdg_hw	WWdg_HALT
r		r	r	r/w	r/w	r/w	r/w

Bit 0:

WWdg_HALT window watchdog reset on Halt:

0: no reset generated on Halt if WWDG is active

1: reset generated on Halt if WWDG is active.

Bit 1:

WWdg_hw window watchdog hardware enable:

0: window watchdog activation by SW

1: window watchdog activation by HW.

Bit 2:

IWdg_hw independent watchdog hardware enable:

0: independent watchdog activation by SW

1: independent watchdog activation by HW.

Bit 3:

LSI_EN low speed internal RCOSC clock enable:

0: LSI clock is not available to CPU

1: LSI cock is enabled for CPU.

Bit 4:

RFU reserved; must be kept 0 during register writing for future compatibility.

Bit 5:

RFU reserved; must be kept 1 during register writing for future compatibility.

Bit 7 - 6:

RFU reserved; must be kept 0 during register writing for future compatibility.

10.2.7 nMISCUOPT (miscellaneous configuration register protection)

Table 46. nMISCUOPT (miscellaneous configuration register protection)

Offset: 0x004806							
Default value: 0xD7 (factory configuration)							
7	6	5	4	3	2	1	0
nRFU		nRFU	nRFU	nLSI_EN	nIWdg_hw	nWWdg_hw	nWWdg_HALT
r		r	r	r/w	r/w	r/w	r/w

nMISCUOPT: not (MISCUOPT) EMC byte protection

10.2.8 CLKCTL (CKC configuration register)

Table 47. CLKCTL (CKC configuration register)

Offset: 0x004807							
Default value: 0x89 (factory configuration)							
7	6	5	4	3	2	1	0
PWM_OD	RFU	SMD_HWtrg	CKAWUSEL1	EXTCLK	CKAWUSEL0	PRSC [1:0]	
r/w	r	r/w	r/w	r/w	r/w	r/w	

Bit 1 - 0:

PRSC [1:0] prescaler value for HSE to provide AWU unit with the low speed clock:

00: 24 MHz to 128 kHz prescaler

01: 16 MHz to 128 kHz prescaler

10: 8 MHz to 128 kHz prescaler

11: 4 MHz to 128 kHz prescaler.

Bit 3:

EXTCLK external clock selection:

0: external crystal oscillator clock connected to HseOscin and HseOscout signals

1: external direct drive clock connected to HseOscin.

Bit 4, 2:

CKAWUSEL [1:0] AWU clock selection:

00: low speed internal clock used for AWU module

01: HSE high speed external clock with prescaler used for AWU module

10: reserved encoding value

11: reserved encoding value.

Bit 5:

SMD_HWtrg enable SMED ADC HW trigger functionality:

0: disable SMED ADC HW trigger request

1: enable SMED ADC HW trigger request; this functionality requires that all SMEDs must be configured with $f_{SMED} \geq f_{MASTER}$ and the ADC_HWtrg option bit of the AFR_IOMXP2 register programmed at '0'.

Bit 6:

RFU reserved; must be kept 0 during register writing for future compatibility.

Bit 7:

PWM_OD PWM output pseudo- open drain features:

0: enable PWM output signal open drain. This functionality is configurable by GPIO1 internal registers.

1: disable PWM output signal open drain functionality.

10.2.9 nCLKCTL (CKC configuration register protection)

Table 48. nCLKCTL (CKC configuration register protection)

Offset: 0x004808							
Default value: 0x76 (factory configuration)							
7	6	5	4	3	2	1	0
nPWM_OD	nRFU	nSMD_HWtrg	nCKAWUSEL1	nEXTCLK	nCKAWUSEL0	nPRSC [1:0]	
r/w	r	r/w	r/w	r/w	r/w	r/w	

nCLKCTL: not (CLKCTL) EMC byte protection.

10.2.10 HSESTAB (HSE clock stabilization register)

Table 49. HSESTAB (HSE clock stabilization register)

Offset: 0x004809							
Default value: 0x00							
7	6	5	4	3	2	1	0
HSECNT [7:0]							
r/w							

Bit 7 - 0:

HSECNT [7:0] HSE crystal oscillator stabilization cycles:

0x00: 2048 clock cycles

0xB4: 128 clock cycles

0xD2: 8 clock cycles

0xE1: 0.5 clock cycles.

10.2.11 nHSESTAB (HSE clock stabilization register protection)

Table 50. nHSESTAB (HSE clock stabilization register protection)

Offset: 0x00480A							
Default value: 0xFF							
7	6	5	4	3	2	1	0
nHSECNT [7:0]							
r/w							

nHSESTAB: not (HSESTAB) EMC byte protection.

10.2.12 ENHFEAT (EXP features configuration register)

Table 51. ENHFEAT (EXP features configuration register)

Offset: 0x00480B							
Default value: 0x00							
7	6	5	4	3	2	1	0
RFU	BscTim1	ADC_MFlush	BscTim0	RFU			
r	r/w	r/w	r/w	r			

Bit 0 - 3:

RFU reserved; must be kept 0 during register writing for future compatibility.

Bit 4:

BscTim0 enable basic Timer0:

0: enable basic Timer0

1: disable basic Timer0.

Bit 5:

ADC_MFlush enable ADC mode flush:

0: enable ADC mode flush

1: disable ADC mode flush.

Bit 6:

BscTim1 enable basic Timer1:

0:enable basic Timer0

1: disable basic Timer0.

Bit 7:

RFU reserved; must be kept 0 during register writing for future compatibility.

10.2.13 nENHFEAT (EXP features configuration register)

Table 52. nENHFEAT (EXP features configuration protection)

Offset: 0x00480C							
Default value: 0xFF							
7	6	5	4	3	2	1	0
nRFU	nBscTim1	nADC_MFlush	nBscTim0	nRFU			
r	r/w	r/w	r/w	r			

nENHFEAT: not (ENHFEAT) EMC byte protection.

10.2.14 WAITSTATE (Flash wait state register)

Table 53. WAITSTATE (Flash wait state register)

Offset: 0x00480D							
Default value: 0x00							
7	6	5	4	3	2	1	0
RFU	ADC_NAbt	RFU	ADC_AFlush	RFU	ADC_ARlod	WaitStat[1:0]	
r	r/w	r	r/w	r	r/w	r/w	

Bit 1 - 0:

WaitStat [1:0] configures the E²PROM and Flash programmable delay read access time:

00: 0 no delay cycle (default case f_{MASTER} at 16 MHz)

01: 1 delay cycles

10: 2 delay cycles

11: 3 delay cycles.

Bit 2:

ADC_ARlodenable ADC auto-reload conversion command:

0: enable ADC auto-reload conversion command

1: disable ADC auto-reload conversion command

Bit 3:

RFU reserved; must be kept 0 during register writing for future compatibility.

Bit 4:

ADC_AFlush enable ADC auto-flush:

0: enable ADC auto-flush command

1: disable ADC auto-flush command

Bit 5:

RFU reserved; must be kept 0 during register writing for future compatibility.

Bit 6:

ADC_NAbt enable ADC new abort mode:

0: enable ADC new abort/flush mode

1: disable ADC new abort/flush mode (ADC abort/flush sequence compliant with the STLUXxxxA family).

Bit 7:

RFU reserved; must be kept 0 during register writing for future compatibility.

10.2.15 nWAITSTATE (Flash wait state register protection)

Table 54. nWAITSTATE (Flash wait state protection)

Offset: 0x00480E							
Default value: 0xFF							
7	6	5	4	3	2	1	0
nRFU	nADC_NAbt	nRFU	nADC_AFlush	nRFU	nADC_ARlod	nWaitStat [1:0]	
r	r/w	r	r/w	r	r/w	r/w	

nWAITSTATE: not (WAITSTATE) EMC byte protection.

10.2.16 AFR_IOMXP0 (alternative Port0 configuration register)

Table 55. AFR_IOMXP0 (alternative Port0 configuration register)

Offset: 0x00480F							
Default value: 0x00							
7	6	5	4	3	2	1	0
RFU		Sel_P054 [1:0]		Sel_P032 [1:0]		Sel_P010 [1:0] (1)	
r		r/w		r/w		r/w	

1. Available only on the STNRG388A, otherwise keep 0.

Bit 5 - 0:

Refer to MSC_IOMXP0 miscellaneous register field description in *Section 7.6 on page 42*.

Bit 7 - 6:

RFU reserved; must be kept 0 during register writing for future compatibility.

10.2.17 nAFR_IOMXP0 (alternative Port0 configuration register protection)

Table 56. nAFR_IOMXP0 (alternative Port0 configuration register protection)

Offset: 0x004810							
Default value: 0xFF							
7	6	5	4	3	2	1	0
nRFU		nSel_P054 [1:0]		nSel_P032 [1:0]		nSel_P010 [1:0]	
r		r/w		r/w		r/w	

nAFR_IOMXP0: not (AFR_IOMXP0) EMC byte protection.

10.2.18 AFR_IOMXP1 (alternative Port1 configuration register)

Table 57. AFR_IOMXP1 (alternative Port1 configuration register)

Offset: 0x004811							
Default value: 0x3F, 0x1F or 0F depends of devices							
7	6	5	4	3	2	1	0
AUXTIM	RFU	Sel_p15	Sel_p14	Sel_p13	Sel_p12	Sel_p11	Sel_p10
r/w	r	r/w	r/w	r/w	r/w	r/w	r/w

Bit 5 - 0:

Refer to MSC_IOMXP1 miscellaneous register field description in *Section 7.6 on page 42*.

Bit 6:

RFU reserved; must be kept 0 during register writing for future product compatibility.

Bit 7:

AUXTIM CCO aux timer compatibility features

0: CCOaux timer enabled

1: CCOaux timer disabled.

10.2.19 nAFR_IOMXP1 (alternative Port1 configuration register protection)

Table 58. nAFR_IOMXP1 (alternative Port1 configuration register protection)

Offset: 0x004812							
Default value: 0xC0, 0xE0 or 0xF0 depends on devices							
7	6	5	4	3	2	1	0
nAUXTIM	nRFU	nSel_p15	nSel_p14	nSel_p13	nSel_p12	nSel_p11	nSel_p10
r/w	r	r/w	r/w	r/w	r/w	r/w	r/w

nAFR_IOMXP1: not (AFR_IOMXP1) EMC byte protection.

10.2.20 AFR_IOMXP2 (alternative Port2 configuration register)

Table 59. AFR_IOMXP2 (alternative Port2 configuration register)

Offset: 0x004813							
Default value: 0x7A or 50, depends on devices							
7	6	5	4	3	2	1	0
SEL_SWIM	ADC_HWtrg	RFU	Sel_P24	Sel_P23	RFU	Sel_P21	RFU
r/w	r/w	r	r/w	r/w	r	r/w	r

Bit 0:

RFU reserved; must be kept 0 during register writing for future product compatibility.

Bit 1:

Sel_P21; refer to MSC_IOMXP2 miscellaneous register field description in *Section 7.6 on page 42*.

Bit 2:

RFU reserved; must be kept 0 during register writing for future product compatibility.

Bit 3:

Sel_P23; refer to MSC_IOMXP2 miscellaneous register field description in *Section 7.6*.

Bit 4:

Sel_P24; refer to MSC_IOMXP2 miscellaneous register field description in *Section 7.6*.

Bit 5:

RFU1 reserved; must be kept 1 during register writing for future products compatibility.

Bit 6:

ADC_HWtrg: enable ADC HW trigger functionality.

0: enable ADC HW trigger.

1: disable ADC HW trigger.

Bit 7:

Sel_SWIM; refer to MSC_IOMXP2 miscellaneous register field description in *Section 7.4 on page 39*.

10.2.21 nAFR_IOMXP2 (alternative Port2 configuration register protection)

Table 60. nAFR_IOMXP2 (alternative Port2 configuration register protection)

Offset: 0x004814							
Default value: 0x85 or AF, depends on devices							
7	6	5	4	3	2	1	0
nSEL_SWIM	nADC_HWtrg	nRFU	nSel_P24	nSel_P23	nRFU	nSel_P21	nRFU
r/w	r/w	r	r/w	r/w	r	r/w	r

nAFR_IOMXP2: not (AFR_IOMXP2) EMC byte protection.

10.2.22 MSC_OPT0 (miscellaneous configuration reg0)

Table 61. MSC_OPT0 (miscellaneous configuration reg0)

Offset: 0x004815							
Default value: 0x01							
7	6	5	4	3	2	1	0
RFU		UARTline [1:0]		RFU		BootSel [1:0]	
r		r/w		r		r/w	

Bit 1 - 0:

BootSel [1:0] boot-ROM peripheral enables:

00: automatic scan boot sources; this selection enables the automatic scan configuration sequence of all possible initializing peripheral devices: Periph0 (UART), Periph1 (RFU).

01: enable boot source: Periph0

10: enable boot source: Periph1

11: enable boot sources: Periph1, Periph0

Bit 2 - 3:

RFU reserved; must be kept 0 during register writing for future compatibility.

Bit 5 - 4:

UARTline [1:0] selects the UART port configuration pins involved during the bootload sequence in warm configuration mode; in case of cold configuration, this field is ignored since the UART port is selected by the register AFR_IOXP0.

00: boot sequence with UART i/f configured in all possible UART multiplexed signal schemes. This sequence is used when the UART i/f position is not specified.

01: boot sequence with UART i/f configured on P0 (1, 0) available only on the STNRG388A.

10: boot sequence with UART i/f configured on P0 (3, 2)

11: boot sequence with UART i/f configured on P0 (5, 4).

Bit 7 - 6:

RFU reserved; must be kept 0 during register writing for future compatibility.

10.2.23 nMSC_OPT0 (miscellaneous configuration reg0 protection)

Table 62. nMSC_OPT0 (miscellaneous configuration reg0 protection)

Offset: 0x004816							
Default value: 0xFE							
7	6	5	4	3	2	1	0
nRFU		nUARTline [1:0]		nRFU		nBootSel [1:0]	
r		r/w		r		r/w	

nMSC_OPT0: not (MSC_OPT0) EMC byte protection.

10.2.24 OPTBL (option byte bootloader)

Table 63. OPTBL (option byte bootloader)

Offset: 0x00487E							
Default value: 0x00							
7	6	5	4	3	2	1	0
BL [7:0]							
r/w							

Bit 7 - 0:

BL [7:0] bootloader field checked by the internal BootROM code during the STNRG initialization phase. The content of register locations 0x00487E, 0x00487F and 0x008000 determine the bootloader SW flow execution sequence.

10.2.25 nOPTBL (option byte boot loader protection)

Table 64. nOPTBL (option byte boot loader protection)

Offset: 0x00487F							
Default value: 0x00							
7	6	5	4	3	2	1	0
nBL [7:0]							
r/w							

nOPTBL: not (OPTBL) EMC byte protection.

11 Device identification

11.1 Unique ID

The STNRG family provides a 56-bit unique identifier code usable as a device identification number which can be used to increase the device security. The unique ID code is a frozen signature not alterable by the user.

The unique device identifier is ideally used by the application software and is suited for:

- Serial code
- Security keys in conjunction with cryptographic software to increase the embedded Flash code security
- Activating the secure boot sequence.

Table 65. Unique ID register overview

Address	Option name	Unique ID bits							
		7	6	5	4	3	2	1	0
48E0h	UID0	LotNum [7:0]							
48E1h	UID1	LotNum [15:8]							
48E2h	UID2	LotNum [23:16]							
48E3h	UID3	WaferNum [4:0]					Xcoord [7:5]		
48E4h	UID4	Xcoord [4:0]					Ycoord [7:5]		
48E5h	UID5	Ycoord [4:0]					LotNum [42:40]		
48E6h	UID6	LotNum [31:24]							
48E7h	UID7	LotNum [39:32]							

11.2 Device ID

The STNRG device identification model is coded in the following register area and it cannot be altered by the user.

Table 66. Dev ID register overview

Address	Option name	Dev ID bits								Default settings
		7	6	5	4	3	2	1	0	
4896h	DVD0	DEV_ID[7:0]								(1)
4897h	nDVD0	nDEV_ID[7:0]								(2)
4898h	DVD1	RFU			Rev_ID [4:0]					(1)
4899h	nDVD1	nRFU			nRev_ID [4:0]					(2)

1. Refer to *Table 67*.
2. The values are the complement of the first of the twice register.

The RFU and nRFU values are reserved and the value may be changed within devices.

Table 67. Device revision model overview

STNRG device revision model		
DEV_ID[7:0]	**Rev_ID[4:0]**	**Device name**
0x04	0b00001	STNRG388A

Note: Mask the DVD1 and nDVD1 register with 0x1F when read the Rev_ID [4:0] field.

12 Electrical characteristics

12.1 Parameter conditions

Unless otherwise specified, all voltages are referred to VSS. VDDA and VDD must be connected to the same voltage value. VSS and VSSA must be connected together with the shortest wire loop.

12.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = T_A max. (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated according to each table specific notes and are not tested in production.

12.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} and V_{DDA} = 3.3 V. They are given only as design guidelines and are not tested. Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range.

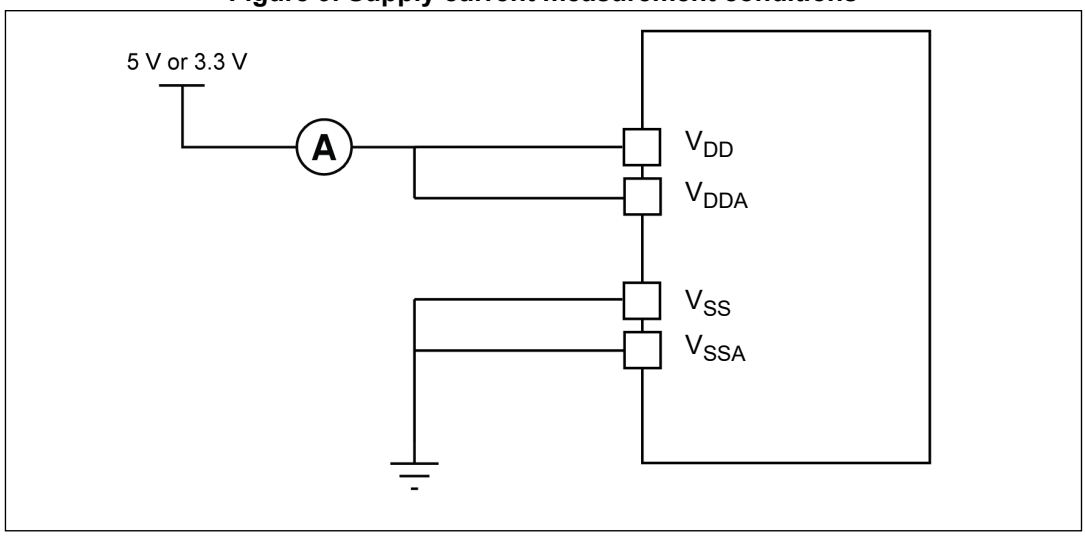
12.1.3 Typical curves

Unless otherwise specified, all typical curves are given as design guidelines only and are not tested.

12.1.4 Typical current consumption

For typical current consumption measurements, V_{DD} and V_{DDA} are connected together as shown in *Figure 9*.

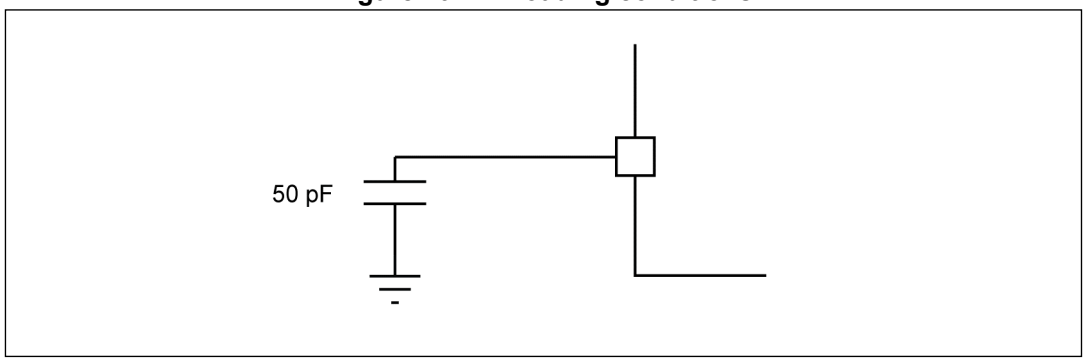
Figure 9. Supply current measurement conditions



12.1.5 Loading capacitors

The loading conditions used for pin parameter measurement are shown in *Figure 10*:

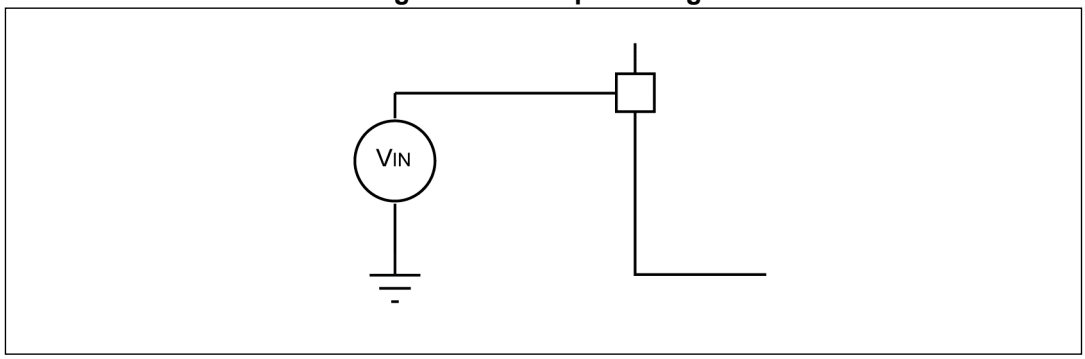
Figure 10. Pin loading conditions



12.1.6 Pin output voltage

The input voltage measurement on a pin is described in *Figure 11*.

Figure 11. Pin input voltage



12.2 Absolute maximum ratings

Stresses above those listed as 'absolute maximum ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect the device reliability.

Table 68. Voltage characteristics

Symbol	Ratings	Min.	Max.	Unit
V_{DDX} - V_{SSX}	Supply voltage(1)	-0.3	6.5	V
V_{IN}	Input voltage on any other pin(2)	V_{SS} - 0.3	V_{DD} + 0.3	
V_{DD} - V_{DDA}	Variation between different power pins		50	mV
V_{SS} - V_{SSA}	Variation between all the different ground pins(3)		50	
V_{ESD}	Electrostatic discharge voltage	Refer to absolute maximum ratings (electrical sensitivity) in *Section 12.4.1 on page 116*		

1. All power V_{DDX} (V_{DD}, V_{DDA}) and ground V_{SSX} (V_{SS}, V_{SSA}) pins must always be connected to the external power supply.
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$.
3. V_{SS} and V_{SSA} signals must be interconnected together with a short wire loop.

Table 69. Current characteristics

Symbol	Ratings	Max.(1)	Unit
I_{VDDX}	Total current into VDDX power lines(2)	100	mA
I_{VSSX}	Total current out of VSSX power lines(2)	100	
I_{IO}	Output current sunk by any I/Os and control pin	Ref. to *Table 84 on page 100*	
	Output current source by any I/Os and control pin		
$I_{INJ(PIN)}$ (3), (4)	Injected current on any pin	±4	
$I_{INJ(TOT)}$ (3), (4), (5)	Sum of injected currents	±20	

1. Data based on characterization results, not tested in production.
2. All power V_{DDX} (V_{DD}, V_{DDA}) and ground V_{SSX} (V_{SS}, V_{SSA}) pins must always be connected to the external power supply.
3. IINJ(PIN) must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$.
4. Negative injection disturbs the analog performance of the device.
5. When several inputs are submitted to a current injection, the maximum $I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with $I_{INJ(PIN)}$ maximum current injection on four I/O port pins of the device.

Table 70. Thermal characteristics

Symbol	Ratings	Max.	Unit
T_{STG}	Storage temperature range	-65 to 150	°C
T_J	Maximum junction temperature	150	

12.3 Operating conditions

The device must be used in operating conditions that respect the parameters listed in *Table 71*. In addition, a full account must be taken for all physical capacitor characteristics and tolerances.

Table 71. General operating conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{CPU}	Internal CPU clock frequency	$-40 \le T_A \le 105$ °C	0		16	MHz
V_{DD1}, V_{DDA1}	Operating voltages		3(1)		5.5(1)	V
V_{DD}, V_{DDA}	Nominal operating voltages		3.3(1)		5(1)	
V_{OUT}	Core digital power supply			1.8(2)		
	CVOUT: capacitance of external capacitor(3)	at 1 MHz	470		3300	nF
	ESR of external capacitor(2)		0.05		0.2	Ω
	ESL of external capacitor(2)				15	nH
Θ_{JA}(4)	FR4 multilayer PCB	TSSOP38		80		°C/W
TA	Ambient temperature	Pd = 100 mW	-40		105	°C

1. The external power supply can be within range from 3 V up to 5.5 V although IC performances are optimized for a power supply equal to 3.3 V.
2. Internal core power supply voltage.
3. Care should be taken when the capacitor is selected due to its tolerance, its dependency on temperature, DC bias and frequency.
4. To calculate P_{Dmax} (T_A), use the formula $P_{Dmax} = (T_{Jmax} - T_A)/\Theta_{JA}$.

Table 72. Operating conditions at power-up/power-down

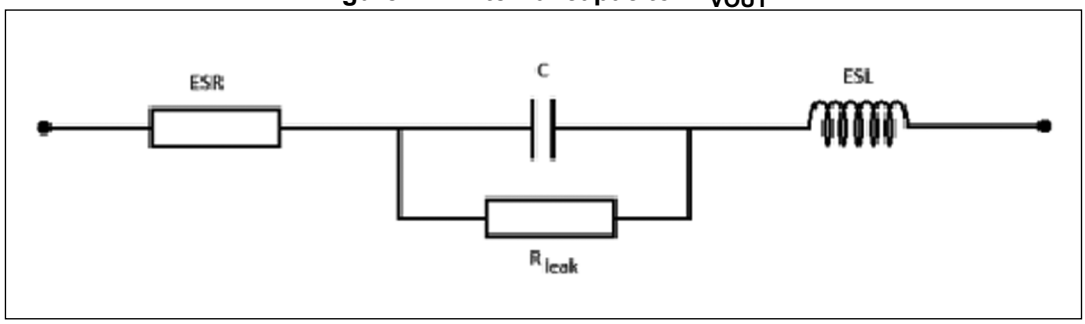
Symbol	Parameter	Conditions	Min.(1)	Typ.	Max.(1)	Unit
t_{VDD}	VDD rise time rate		2 µs/V		1 sec./V(2)	
	VDD fall time rate		2 µs/V		1 sec./V(2)	
t_{TEMP}	Reset release delay	V_{DD} rising		3		ms
V_{IT}+	Power-on reset threshold		2.65	2.8	2.98	V
V_{IT}-	Brownout reset threshold		2.58	2.73	2.88	
$V_{HYS(BOR)}$	Brownout reset hysteresis			70		mV

1. Guaranteed by design, not tested in production.
2. Power supply ramp must be monotone.

12.3.1 VOUT external capacitor

The stabilization of the main regulator is achieved by connecting an external capacitor C_{VOUT}[(c)] to the VOUT pin. The C_{VOUT} is specified in *Section 12.3: Operating conditions* Care should be taken to limit the series inductance to less than 15 nH.

Figure 12. External capacitor C_{VOUT}



12.3.2 Supply current characteristics

The STNRG supply current is calculated by summing the supply base current in the desired operating mode as per *Table 73*, with the peripheral supply current value reported in*Table 65 on page 79* and *Table 66 on page 80*.

For example, considering an application where:

- $f_{MASTER} = f_{CPU}$ = 16 MHz provided by HSI internal RC oscillator
- CPU code execution in Flash
- All base peripheral actives: I^2C, UART, DALI, ITC, GPIO0, SysTmr, WWDG and IWDG
- ADC conversion frequency f_{ADC} = 5.3 MHz
- ACU (comparator and DAC units) active
- 6 PWM toggling at f_{PWM} = 0.5 MHz provided by 6 SMEDs running at f_{SMED} = 12 MHz (N_{PWM} = 6).

c. ESR is the equivalent series resistance and ESL is the equivalent inductance.

The total current consumption is given by *Equation 1*:

Equation 1

$$I_{DD} = I_{DD(Run2)} + I_{DD(ADC2)} + I_{DD(ACU)} + I_{DD(PLL)} + I_{DD(PWM)}$$

where $I_{DD(PWM)} = I_{DD(PWM1)} \times N_{PWM}$

More generally, the PWM current consumption is given for each fSMED clock grouping, by *Equation 2*:

Equation 2

$$I_{DD(PWM)} = \Sigma_{i=1}^{Nf_{SMED}} \{I_{DD[PWM(i1)]} \bullet N_i\}$$

where $i = f_{SMED}$ clock group index; N_i = PWM number of the i_th clock group;

$N_{fSMED} = f_{SMED}$ clock group number.

IC supply base current consumption

Table 73 summarizes the current consumption measured on V_{DD}/V_{DDA} supply pins in relevant operative conditions.

Table 73. Supply base current consumption at V_{DD}/V_{DDA} = 3.3/5 V

Symbol	Code	Clock			Peripheral	Consumption(1)		Note
Op. mode	Code area	f_{MASTER}		f_{CPU}	Periph(2), (3)	Typ.(4)	Max.(4)	Description
		Clock	MHz	MHz	Enb/Dis	mA	mA	
$I_{DD(Run1)}$	Flash	HSI	2	2	All	2.3	2.77	Reset exit condition
$I_{DD(Run2)}$	Flash	HSI	16	16	All	9.4	11.3	
$I_{DD(Run3)}$	RAM	HSI	16	16	All	4.2	5.1	
$I_{DD(Run4)}$	Flash	HSE(5)	16	16	All	10.0	12.1	V_{DD}/V_{DDA} = 3.3 V
						10.6	12.74	V_{DD}/V_{DDA} = 5 V
$I_{DD(Run5)}$	RAM	HSE(5)16	16	16	All	4.6	5.53	V_{DD}/V_{DDA}= 3.3 V
					All	5.2	6.63	V_{DD}/V_{DDA} = 5 V
$I_{DD(SLOW1)}$	Flash	HSI	16	2	All	3.6	4.33	
$I_{DD(SLOW2)}$	RAM	HSI	16	2	All	2.9	3.5	
$I_{DD(SLOW3)}$	Flash	HSE(5)	16	2	All	3.9	4.7	V_{DD}/V_{DDA} = 3.3 V
					All	4.5	5.5	V_{DD}/V_{DDA} = 5 V
$I_{DD(SLOW4)}$	Flash	HSI	16	0.125	All	2.7	3.3	
$I_{DD(SLOW5)}$	Flash	HSE(5)	16	0.125	All	3.0	3.7	V_{DD}/V_{DD} = 3.3 V
					All	3.6	4.4	V_{DD}/V_{DDA} = 5 V
$I_{DD(SLOW6)}$	Flash	LSI	0.153	0.153	All	1.5	1.9	
$I_{DD(WFI1)}$	Flash	HSI	16	16	All	2.6	3.2	
$I_{DD(WFI2)}$	Flash	HSE(5)	16	16	All	3.1	3.8	V_{DD}/V_{DDA} =3.3 V
					All	3.8	5.6	V_{DD}/V_{DDA} =5 V

1. Data based on characterization results not tested in production.
2. “All” means: I^2C, UART, DALI, ITC, GPIO0, SysTmr, WWDG and IWDG peripherals active.
3. The peripheral current consumption is supplied by the VCORE voltage (1.8 V).
4. Temperature operating: T_A = 25 °C.
5. HSE frequency provided by external quartz.

IC low power current consumption

Table 74 summarizes the current consumption measured on V_{DD}/V_{DDA} supply pins in power saving conditions.

Table 74. Supply low power consumption at V_{DD}/V_{DDA} = 3.3/5 V

Symbol	Code	Clock		Peripheral		Consumption(1)		Note
Op. mode (2), (3)	Code area	f_{MASTER}		E^2PROM(4)	MVReg.(5)	Typ.(6), (7)	Max.(7), (8)	Description
		Source	MHz	Enable	Enable	mA	mA	
$I_{DD(AHLT1)}$	Flash	HSI	16	Enable	Enable	0.23	0.32	AWU clocked by LSI
$I_{DD(AHLT2)}$	Flash	HSI	16	Enable	Disable	0.085	0.12	AWU clocked by LSI
$I_{DD(AHLT3)}$	Flash	HSE(9), (10)	16	Enable	Enable	0.73	0.90	V_{DD}/V_{DDA} =3.3 V
						1.4	1.7	V_{DD}/V_{DDA} = 5 V
$I_{DD(AHLT4)}$	Flash	HSE(9), (10)	16	Enable	Disable	0.65	0.95	V_{DD}/V_{DDA} =3.3 V
						1.2	1.45	V_{DD}/V_{DDA} = 5 V
$I_{DD(HLT1)}$	Flash	HSI	16	Enable	Disable	0.087	0.13	
$I_{DD(HLT2)}$	Flash	HSE(9), (10)	16	Enable	Disable	0.075	0.11	V_{DD}/V_{DDA} =3.3 V
						0.090	0.15	V_{DD}/V_{DDA}= 5 V

1. Data based on characterization results not tested in production.
2. Active-halt op. mode: all peripherals except AWU and IWDG are disabled (clock gated).
3. HALT op. mode: all peripherals are disabled (clock gated).
4. E^2PROM is considered always enabled.
5. V_{CORE} main DC voltage regulator.
6. Temperature operating: T_A= 25 °C.
7. All the analog input signals are connected to GND; the signals of the port P0, P1 and P2 are configured as input with pull-up enabled.
8. Temperature operating: T_A= 105 °C.
9. HSE frequency provided by external quartz.
10. AWU clocked by HSE source clock.

IC peripheral current consumption (3.3 V)

Table 75 summarizes the peripheral current consumption measured on V_{DD}/V_{DDA} supply pins.

Table 75. Peripheral supply current consumption at V_{DD}/V_{DDA} = 3.3 V

Symbol	Clock				Peripherals			Consumption(1)	
Op. mode	PLL	f_{SMED}(2)	f_{PWM}(3)	f_{ADC}(4)	ADC(5)	PWM(6),(7)	ACU(8)	Typ.(9)	Max(9)
	Enb/dis	MHz	MHz	MHz	Enb/dis	Num	Enb/dis	mA	mA
$I_{DD(PLL)}$	Enab	0	0	0	Disab	0	Disab	2.3	2.7
$I_{DD(ACU)}$	Disab	0	0	0	Disab	0	Enab	1.9	2.3
$I_{DD(PWM1PLL96)}$	Enab	96	0.5	0	Disab	1	Disab	1.8	2.1
$I_{DD(PWM4PLL96)}$						4		6.69	8.32
$I_{DD(PWM5PLL96)}$						5		8.55	10.4
$I_{DD(PWM6PLL96)}$						6		10.12	12.2
$I_{DD(PWM1PLL48)}$	Enab	48	0.5	0	Disab	1	Disab	1.12	1.4
$I_{DD(PWM4PLL48)}$						4		4.31	5.31
$I_{DD(PWM5PLL48)}$						5		5.6	6.8
$I_{DD(PWM6PLL48)}$						6		6.54	7.85
$I_{DD(PWM1PLL24)}$	Enab	24	0.5	0	Disab	1	Disab	0.71	0.9
$I_{DD(PWM4PLL24)}$						4		2.89	3.54
$I_{DD(PWM5PLL24)}$						5		3.9	4.7
$I_{DD(PWM6PLL24)}$						6		4.39	5.27
$I_{DD(PWM1PLL12)}$	Enab	12	0.5	0	Disab	1	Disab	0.6	0.7
$I_{DD(PWM4PLL12)}$						4		2.2	2.69
$I_{DD(PWM5PLL12)}$						5		2.95	3.6
$I_{DD(PWM6PLL12)}$						6		3.33	4
$I_{DD(PWM1PLL6)}$	Enab	6	0.5	0	Disab	1	Disab	0.5	0.6
$I_{DD(PWM4PLL6)}$						4		1.85	2.26
$I_{DD(PWM5PLL6)}$						5		2.6	3.2
$I_{DD(PWM6PLL6)}$						6		2.81	3.4
$I_{DD(PWM1HSI16)}$	Enab	16	0.5	0	Disab	1	Disab	0.5	0.6
$I_{DD(PWM4HSI16)}$						4		1.79	2.19
$I_{DD(PWM5HSI16)}$						5		2.3	3
$I_{DD(PWM6HSI16)}$						6		2.63	3.3

Table 75. Peripheral supply current consumption at V_{DD}/V_{DDA} = 3.3 V (continued)

Symbol	Clock				Peripherals			Consumption[1]	
Op. mode	PLL	f_{SMED}[2]	f_{PWM}[3]	f_{ADC}[4]	ADC[5]	PWM[6],[7]	ACU[8]	Typ.[9]	Max.[9]
	Enb/dis	MHz	MHz	MHz	Enb/dis	Num.	Enb/dis	mA	mA
$I_{DD(PWM1HSI8)}$	Enab	8	0.5	0	Disab	1	Disab	0.4	0.5
$I_{DD(PWM4HSI8)}$						4		1.39	1.7
$I_{DD(PWM5HSI8)}$						5		1.95	2.4
$I_{DD(PWM6HSI8)}$						6		2.12	2.55
$I_{DD(PWM1HSI4)}$	Enab	4	0.5	0	Disab	1	Disab	0.3	0.4
$I_{DD(PWM4HSI4)}$						4		1.21	1.48
$I_{DD(PWM5HSI4)}$						5		1.7	2.2
$I_{DD(PWM6HSI4)}$						6		1.78	2.2
$I_{DD(PWM1HSI2)}$	Enab	2	0.5	0	Disab	1	Disab	0.25	0.3
$I_{DD(PWM4HSI2)}$						4		1.07	1.31
$I_{DD(PWM5HSI2)}$						5		1.52	1.9
$I_{DD(PWM6HSI2)}$						6		1.60	1.93
$I_{DD(ADC1)}$	Disab	0	0	1	Enab	0	Disab	1.55	1.87
$I_{DD(ADC2)}$	Disab	0	0	5.3	Enab	0	Disab	1.6	1.95
$I_{DD(ADC3)}$	Enab	0	0	6	Enab	0	Disab	1.56	1.88

1. Data based on characterization results not tested in production.
2. SMED frequency:
   - 96 MHz and 6 MHz frequencies require the PLL enabled.
   - Current table shows only a subset value of possible SMED frequencies.
3. PWM frequency:
   - PWM toggle frequency is considered fixed to 500 kHz, close to the maximum applicative value.
4. ADC frequency:
   - 6 MHz frequency requires the PLL enabled.
   - Current table shows only a subset value of possible ADC frequencies
5. ADC configured in circular mode.
6. Number of active PWMs.
7. PWM pins are loaded with a CL (load capacitance) of 50 pF.
8. If enabled all DACs and comparator units are active.
9. Temperature operating: T_A = 25 °C

IC peripheral current consumption (5 V)

Table 76 summarizes the peripheral current consumption measured on V_{DD}/V_{DDA} supply pins.

Table 76. Peripheral supply current consumption at V_{DD}/V_{DDA} = 5 V

Symbol	Clock				Peripherals			Consumption(1)	
Op. mode	PLL	f_{SMED}(2)	f_{PWM}(3)	f_{ADC}(4)	ADC(5)	PWM(6), (7)	ACU(8)	Typ.(9)	Max.(9)
	Enb/dis	MHz	MHz	MHz	Enb/dis	Num.	Enb/dis	mA	mA
$I_{DD(PLL)}$	Enab	0	0	0	Disab	0	Disab	2.32	2.78
$I_{DD(ACU)}$	Disab	0	0	0	Disab	0	Enab	2.22	2.66
$I_{DD(PWM1PLL96)}$	Enab	96	0.5	0	Disab	1	Disab	1.81	2.17
$I_{DD(PWM4PLL96)}$						4		6.98	8.69
$I_{DD(PWM5PLL96)}$						5		9.0	10.8
$I_{DD(PWM6PLL96)}$						6		10.49	12.52
$I_{DD(PWM1PLL48)}$	Enab	48	0.5	0	Disab	1	Disab	1.18	1.42
$I_{DD(PWM4PLL48)}$						4		4.58	5.65
$I_{DD(PWM5PLL48)}$						5		5.9	7.5
$I_{DD(PWM6PLL48)}$						6		6.88	8.26
$I_{DD(PWM1PLL24)}$	Enab	24	0.5	0	Disab	1	Disab	0.8	0.95
$I_{DD(PWM4PLL24)}$						4		3.16	3.88
$I_{DD(PWM5PLL24)}$						5		4.2	5.2
$I_{DD(PWM6PLL24)}$						6		4.73	5.68
$I_{DD(PWM1PLL12)}$	Enab	12	0.5	0	Disab	1	Disab	0.6	0.7
$I_{DD(PWM4PLL12)}$						4		2.46	3.01
$I_{DD(PWM5PLL12)}$						5		3.3	4.2
$I_{DD(PWM6PLL12)}$						6		3.66	4.4
$I_{DD(PWM1PLL6)}$	Enab	6	0.5	0	Disab	1	Disab	0.5	0.6
$I_{DD(PWM4PLL6)}$						4		2.11	2.58
$I_{DD(PWM5PLL6)}$						5		2.9	3.6
$I_{DD(PWM6PLL6)}$						6		3.11	3.75
$I_{DD(PWM1HSI16)}$	Enab	16	0.5	0	Disab	1	Disab	0.6	0.7
$I_{DD(PWM4HSI16)}$						4		2.04	2.49
$I_{DD(PWM5HSI16)}$						5		2.8	3.4
$I_{DD(PWM6HSI16)}$						6		3.13	3.78

Table 76. Peripheral supply current consumption at V_{DD}/V_{DDA} = 5 V (continued)

Symbol	Clock				Peripherals			Consumption(1)	
Op. mode	PLL	f_{SMED}(2)	f_{PWM}(3)	f_{ADC}(4)	ADC(5)	PWM(6), (7)	ACU(8)	Typ.(9)	Max.(9)
	Enb/dis	MHz	MHz	MHz	Enb/dis	Num.	Enb/dis	mA	mA
$I_{DD(PWM1HSI8)}$	Enab	8	0.5	0	Disab	1	Disab	0.5	0.6
$I_{DD(PWM4HSI8)}$						4		1.64	2
$I_{DD(PWM5HSI8)}$						5		2.3	2.9
$I_{DD(PWM6HSI8)}$						6		2.56	3.1
$I_{DD(PWM1HSI4)}$	Enab	4	0.5	0	Disab	1	Disab	0.47	0.55
$I_{DD(PWM4HSI4)}$						4		1.48	1.81
$I_{DD(PWM5HSI4)}$						5		2.2	2.7
$I_{DD(PWM6HSI4)}$						6		2.33	2.78
$I_{DD(PWM1HSI2)}$	Enab	2	0.5	0	Disab	1	Disab	0.4	0.54
$I_{DD(PWM4HSI2)}$						4		1.31	1.6
$I_{DD(PWM5HSI2)}$						5		1.9	2.3
$I_{DD(PWM6HSI2)}$						6		2.1	2.49
$I_{DD(ADC1)}$	Disab	0	0	1	Enab	0	Disab	2.11	2.54
$I_{DD(ADC2)}$	Disab	0	0	5.3	Enab	0	Disab	2.16	2.6
$I_{DD(ADC3)}$	Enab	0	0	6	Enab	0	Disab	2.17	2.61

1. Data based on characterization results not tested in production.|
2. SMED frequency:
   - 96 MHz and 6 MHz frequencies require the PLL enabled.
   - Current table shows only a subset value of possible SMED frequencies.
3. PWM frequency:
   - PWM toggle frequency is considered fixed to 500 kHz, close to the maximum applicative value.
4. ADC frequency:
   - 6 MHz frequency requires the PLL enabled.
   - Current table shows only a subset value of possible ADC frequencies.
5. ADC configured in circular mode.
6. Number of active PWMs.
7. PWM pins are loaded with a CL (load capacitance) of 50 pF.
8. If enabled all DACs and comparator units are active.
9. Temperature operating: T_A = 25 °C.

PWM current consumption overview

From *Figure 13* to *Figure 16* provide an outline view of PWM current consumption results.The consumptions are evaluated considering the maximum current at T_A = 25 °C with different SMED operating frequencies. The charts summarize the measurements carried out from *Table 75* and *Table 76* allowing users to derive the PWM current consumption values.

Figure 13. PWM current consumption with f_{SMED} = PLL f_{PWM} = 0.5 MHz at V_{DD}/V_{DDA} = 3.3 V

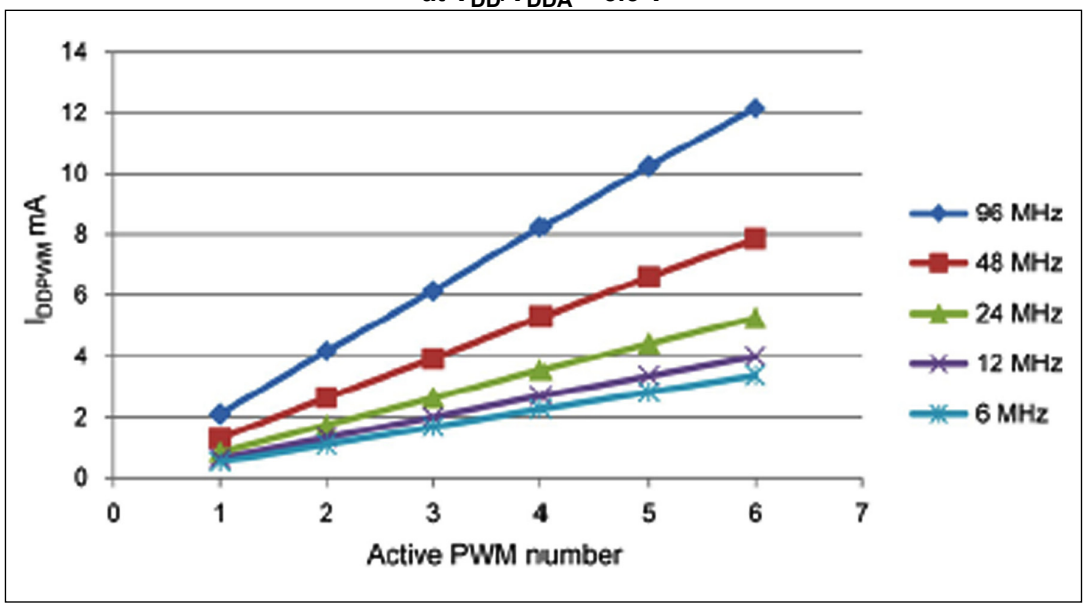


Figure 14. PWM current consumption with f_{SMED} = PLL f_{PWM} = 0.5 MHz at V_{DD}/V_{DDA} = 5 V

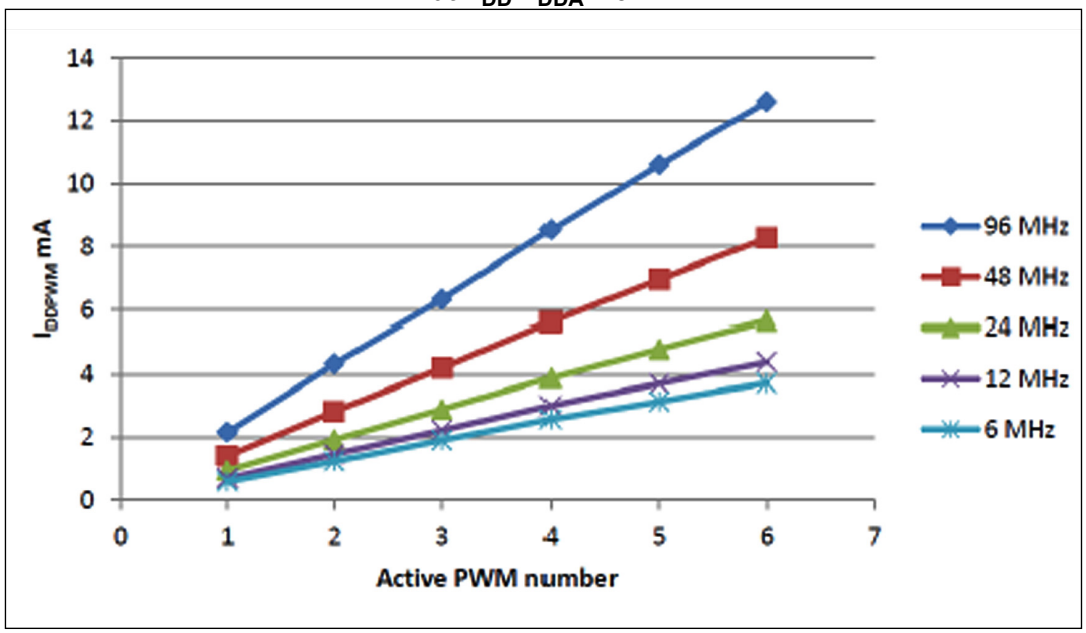


Figure 15. PWM current consumption with f_{SMED} = HSI f_{PWM} = 0.5 MHz at V_{DD}/V_{DDA} = 3.3 V

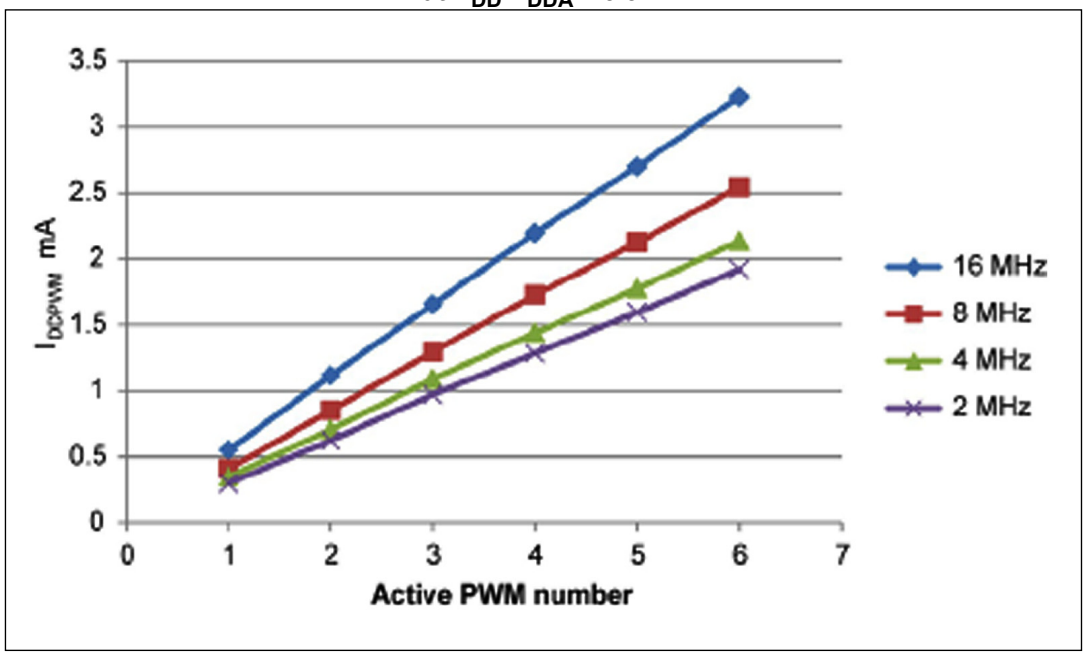
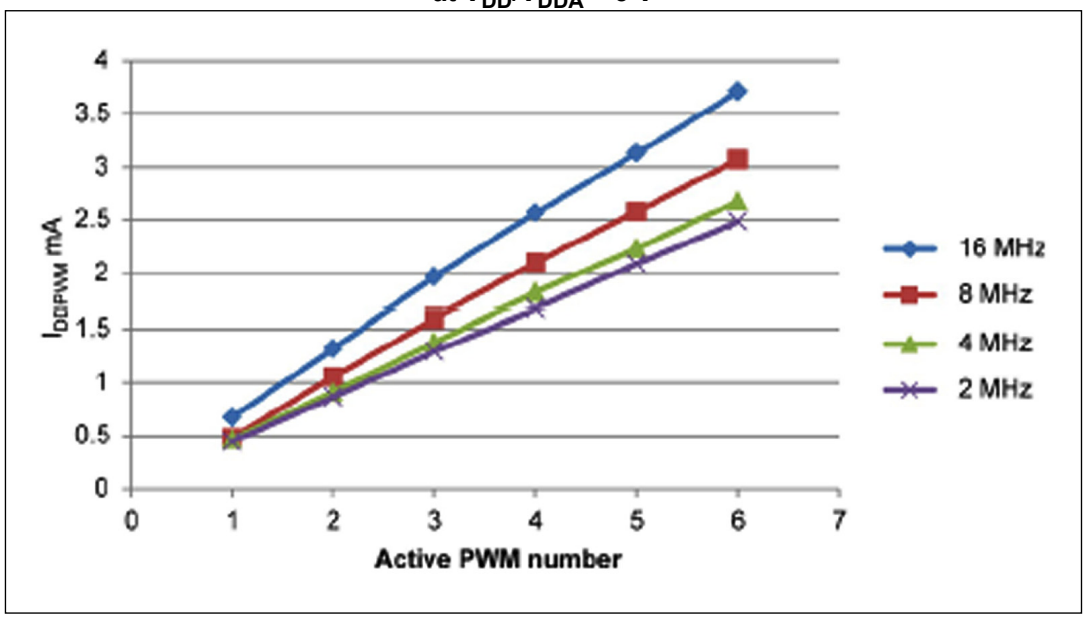


Figure 16. PWM current consumption with f_{SMED} = HSI f_{PWM} = 0.5 MHz at V_{DD}/V_{DDA} = 5 V



12.3.3 Low power mode wake-up time

Table 77 shows the wakeup time to resume the normal operating mode from different low power state.

Table 77. Wake-up times

Symbol	Parameter	Conditions			Typ.(1)	Max.(1)	Unit
$t_{WU(WFI)}$	Wake-up time from wait mode to run mode(2)	$f_{CPU} \neq f_{MASTER}$ = 0 to 16 MHz				Ref.(3)	µs
		$f_{CPU} = f_{MASTER}$ = 16 MHz			0.56		
$t_{WU(AH)}$	Wake-up time active halt mode to run mode(2)	MVR voltage regulator on(4)	Flash in operating mode(5)	HSI (after wake-up)	4(6)		
			Flash in power- down mode(5)		6(6)		
		MVR voltage regulator off(4)	Flash in operating mode(5)		47(6)		
			Flash in power- down mode(5)		49(6)		
$t_{WU(H)}$	Wake-up time from halt mode to run mode(2)	Flash in operating mode(5)			51		
		Flash in power-down mode(5)			53		

1. Data based on characterization results, not tested in production.
2. Measured from the interrupt event to the interrupt vector fetch.
3. $t_{WU(WFI)} = 2 \times 1/f_{MASTER} + 7 \times 1/f_{CPU}$.
4. Configured by the REGAH bit in the CLK_ICKR register.
5. Configured by the AHALT bit in the FLASH_CR1 register.
6. Plus 1 LSI clock depending on synchronization (f_{LSI} = 153.6 kHz).

12.3.4 External clock sources and timing characteristics

HSE user external clock

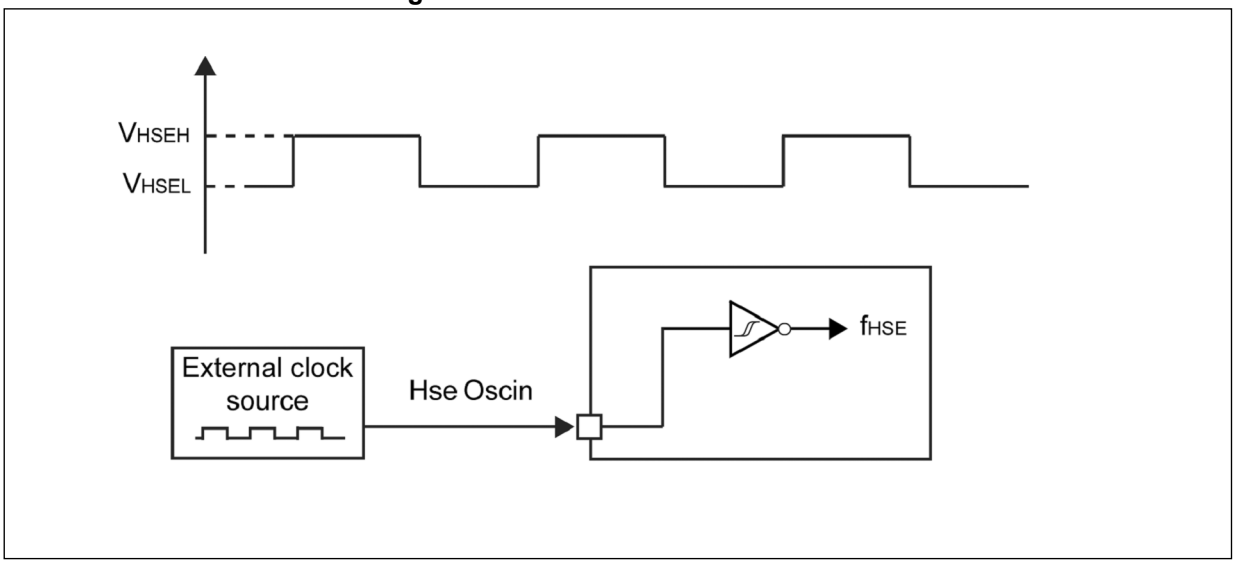
Subject to general operating conditions for V_{DD} and T_A.

Table 78. HSE user external clock characteristics

Symbol	Parameter	Conditions	Min.	Max.	Unit
f_{HSE_ext}	User external clock source frequency	-40 °C ≤ T_A ≤ 105 °C	0	16(1)	MHz
V_{HSEH}(2)	HSEOSCIN input pin high level voltage		0.7 x V_{DD}	V_{DD}	V
V_{HSEL}(2)	HSEOSCIN input pin low level voltage		V_{SS}	0.3 x V_{DD}	
$I_{LEAKHSE}$(2)	HSEOSCIN input pin leakage	$V_{SS} \leq V_{IN} \leq V_{DD}$	-1	+1	µA

1. In case fHSE is configured as a direct clock for the SMED logics the maximum frequency can be 24 MHz.
2. Data based on characterization results, not tested in production.

Figure 17. HSE external clock source



HSE crystal/ceramic resonator oscillator

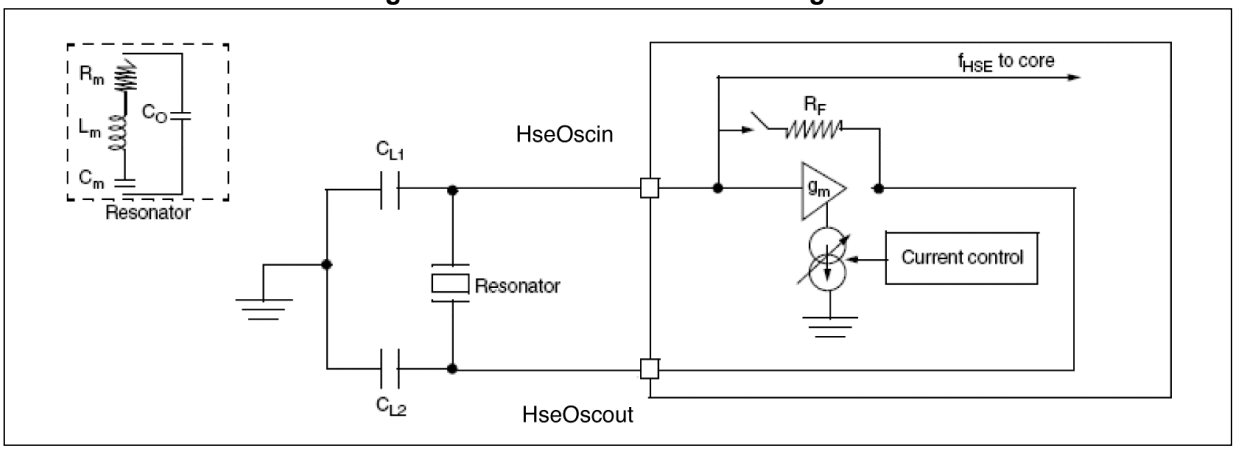
The HSE clock can be supplied with a 1 to 24 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph is based on characterization results with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and start-up stabilization time. Refer to the crystal resonator manufacturer for more details (frequency, package, accuracy, etc.).

Table 79. HSE crystal/ceramic resonator oscillator

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{HSE}	External high speed oscillator frequency		1		16(1)	MHz
R_F	Feedback resistor			220		kΩ
C_{L1}, C_{L2}(2)	Recommended load capacitance(3)				20	pF
$I_{DD(HSE)}$	HSE oscillator power consumption				6 (startup) 2 (stabilized)	mA
g_m	Oscillator transconductance		5			mA/V
$t_{SU(HSE)}$(4)	Startup time	V_{DD} is stabilized		2.8		ms

1. In case fHSE is configured as a direct clock for the SMED logic the maximum frequency can be 24 MHz.
2. The oscillator needs two load capacitors, CL1 and CL2, to act as load for the crystal. The total load capacitance (Cload) is (CL1 x CL2) / (CL1 + CL2). If CL1 = CL2, Cload = CL1 / 2. Some oscillators have built-in load capacitors, CL1 and CL2.
3. The oscillator selection can be optimized in terms of supply current using a high quality resonator with small Rm value.
4. $t_{SU(HSE)}$ is the start-up time measured from the moment it is enabled (by software) to a stabilized 16 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Figure 18. HSE oscillator circuit diagram



The crystal characteristics have to be checked by *Equation 3*.

Equation 3

$$gm \gg g_{mCritic}$$

where $g_{mCritic}$ is calculated with the crystal parameters as follows:

Equation 4

$$g_{mCritic} = (2 \times \pi \times f_{HSE})^2 \times R_m (2C_O + C)^2$$

and where:

- *Rm*: motional resistance[d]
- *Lm*: motional inductance[d]
- *Cm*: motional capacitance[d]
- *CO:* shunt capacitance[d]
- *CL1* = *CL2* = *C*: grounded external capacitance

d. Refer to the application crystal specification.

12.3.5 Internal clock sources and timing characteristics

HSI RC oscillator

Subject to general operating conditions for V_{DD} and T_A.

Table 80. HSI RC oscillator

Symbol	Parameter	Conditions	Min.(1)	Typ.	Max.(1)	Unit
f_{HSI}	Frequency			16		MHz
ACC_{HSI}	Accuracy of HSI oscillator (factory calibrated)(1), (2)	V_{DD} = 3.3 V T_A= 25 °C	-1%		+1%	%
		V_{DD} = 3.3 V -40 °C ≤ T_A ≤ 105 °C	-4%		+4%	
		V_{DD} = 5 V -40 °C ≤ T_A ≤ 105 °C	-4%		+4%	
$t_{SU(HSI)}$	HSI oscillator wakeup time including calibration			1		µs

1. Data based on characterization results, not tested in production.
2. Variation referred to f_{HSI} nominal value.

LSI RC oscillator

Subject to general operating conditions for V_{DD} and T_A.

Table 81. LSI RC oscillator

Symbol	Parameter	Conditions	Min.(1)	Typ.	Max.(1)	Unit
f_{LSI}	Frequency			153.6		kHz
ACC_{LSI}	Accuracy of LSI oscillator	3.3 V ≤ V_{DD} ≤ 5 V -40 °C ≤ T_A ≤ 105 °C	-10%		10%	%
$t_{SU(LSI)}$	LSI oscillator wake-up time			7		µs

1. Guaranteed by design, not tested in production.

PLL internal source clock

Table 82. PLL internal source clock

Symbol	Parameter	Conditions	Min.	Typ.	Max.(1)	Unit
f_{IN}	Input frequency(2)	3.3 V ≤ V_{DD} ≤ 5 V -40 °C ≤ T_A ≤ 105 °C		16		MHz
f_{OUT}	Output frequency			96		
t_{lock}	PLL lock time				200	µs

1. Data based on characterization results, not tested in production.
2. PLL maximum input frequency 16 MHz.

12.3.6 Memory characteristics

Flash program and memory/data E^2PROM memory

General conditions: T_A = -40 °C to 105 °C.

Table 83. Flash program memory/data E^2PROM memory

Symbol	Parameter	Conditions	Min.(1)	Typ.(1)	Max.(1)	Unit
t_{PROG}	Standard programming time (including erase) for byte/word/block (1 byte/4 bytes/128 bytes)			6	6.6	ms
	Fast programming time for 1 block (128 bytes)			3	3.3	
t_{ERASE}	Erase time for 1 block (128 bytes)			3	3.3	
N_{WE}	Erase/write cycles(2)(program memory)	T_A = 25 °C	10 K			Cycles
	Erase/write cycles(2) (data memory)	T_A = 85 °C	100 K			
		T_A = 105 °C	35 K			
t_{RET}	Data retention (program memory) after 10 K erase/write cycles at T_A= 25 °C	T_{RET} = 85 °C	15			Years
	Data retention (program memory) after 10 K erase/write cycles at T_A= 25 °C	T_{RET} = 105 °C	11			
	Data retention (data memory) after 100 K erase/write cycles at T_A= 85 °C	T_{RET} = 85 °C	15			
	Data retention (data memory) after 35 K erase/write cycles at T_A= 105 °C	T_{RET} = 105 °C	6			
I_{DDPRG}	Supply current during program and erase cycles	-40 ºC ≤ T_A ≤ 105 ºC		2		mA

1. Data based on characterization results, not tested in production.
2. The physical granularity of the memory is 4 bytes, so cycling is performed on 4 bytes even when a write/erase operation addresses a single byte.

12.3.7 I/O port pin characteristics

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified. Unused input pins should not be left floating.

Table 84. Voltage DC characteristics

Symbol	Description	Min.(1)	Typ.	Max.(1)	Unit
V_{IL}	Input low voltage	-0.3		0.3 x V_{DD}	V
V_{IH}	Input high voltage(2)	0.7 x V_{DD}		V_{DD}	
V_{OL1}	Output low voltage at 3.3 V(3), (4)			0.4	
V_{OL2}	Output low voltage at 5 V(3), (4)			0.5	
V_{OL3}	Output low voltage high sink at 3.3 V / 5 V(2),(5), (6)			0.6	
V_{OH1}	Output high voltage at 3.3 V(3), (4)	V_{DD} - 0.4			
V_{OH2}	Output high voltage at 5 V(3), (4)	V_{DD} - 0.5			
V_{OH3}	Output high voltage high sink at 3.3 V / 5 V(2), (5), (6)	V_{DD} - 0.6			
H_{VS}	Hysteresis input voltage(7)	0.1 x V_{DD}			
R_{PU}	Pull-up resistor	30	45	60	kΩ

1. Data based on characterization result, not tested in production.
2. All signals are not 5 V tolerant (input signals can't be exceeded V_{DDX} (V_{DDX} = V_{DD}, V_{DDA}).
3. The parameter applicable to signalsGPIO0 [5:0] (product depending) (high sink selectable by high speed config.).
4. The parameter applicable to signals: GPIO1 [5:0]/PWM [5:0] (product depending).
5. The parameter applicable to the signal: SWIM.
6. The parameter applicable to the signal: DIGIN [0]/CCO_clk.
7. Applicable to any digital inputs.

Table 85. Current DC characteristics

Symbol	Description	Min.	Typ.	Max.(1)	Unit
I_{OL1}	Standard output low level current at 3.3 V and VOL1(2), (3)			1.5	mA
I_{OL2}	Standard output low level current at 5 V and VOL2(2), (3)			3	
I_{OLhs1}	High sink output low level current at 3.3 V and VOL3(2), (4), (5)			5	
I_{OLhs2}	High sink output low level current at 5 V and VOL3(2),(4), (5)			7.75	
I_{OH1}	Standard output high level current at 3.3 V and VOH1(2), (3)			1.5	
I_{OH2}	Standard output high level current at 5 V and VOLH2(2), (3)			3	
I_{OHhs1}	High sink output high level current at 3.3 V and VOH3(2), (4), (5)			5	
I_{OHhs2}	High sink output high level current at 5 V and VOH3(2), (4), (5)			7.75	
I_{LKg}	Input leakage current digital - analog $V_{SS} \le V_{IN} \le V_{DD}$(6)			± 1	µA
$I_{\_Inj}$	Injection current(7), (8)			± 4	mA
$\Sigma I_{\_Inj}$	Total injection current (sum of all I/O and control pins)(7)			± 20	

1. Data based on characterization result, not tested in production.
2. A high sink selectable by high speed configuration; the parameter applicable to signals: GPIO0 [5:0] (product depending).
3. The parameter applicable to signals: GPIO1 [5:0]/PWM [5:0] (product depending).
4. The parameter applicable to the signal: SWIM.
5. The parameter applicable to the signal: DIGIN [0]/CCO_clk.
6. Applicable to any digital inputs.
7. Maximum value must never be exceeded.
8. Negative injection current on the ADCIN [7:0] signals (product depending) have to avoid since impact the ADC conversion accuracy.

Table 86. Operating frequency characteristics

Symbol	Description	Min.	Typ.	Max.(1)	Unit
f_{IL1}	Digital input signal operating frequency(2), (3), (4)			12	MHz
f_{IH1}	Analog input signal operating frequency(5), (6)			24	
f_{IH2}	High speed input signal operating frequency(7), (8)			128	
f_{OL1}	Standard output signal operating frequency with 50 pF max. load(2)			2	
f_{OL2}	High sink output signal operating frequency with 50 pF max. load(2), (3)			10	
f_{OH1}	High speed output signal operating frequency with 50 pF max. load(7)			12	
f_{OH2}	High speed output signal operating frequency with 50 pF max. load(8)			32	

1. Data based on characterization result, not tested in production
2. A high sink selectable by high speed configuration; parameter applicable to signals: GPIO0 [5:0] (product depending).
3. The parameter applicable to the signal: SWIM.
4. The parameter applicable to signals: DIGIN [5:1] (product depending).
5. The parameter applicable to signals: GPIO0 [3:2] when configured as HSE_Oscin/Oscout.
6. The parameter applicable to any analog signals: ADCIN [7:0], CPP [3:0] and CPM3 (product depending).
7. The parameter applicable to signals: GPIO1 [5:0]/PWM [5:0] (product depending).
8. The parameter applicable to the signal: DIGIN [0]/CCO_clk.

12.3.8 Typical output level curves

This section shows the typical output voltage level curves measured on a single output pin for the three pad family present in the STNRG device.

Standard pad

This pad is associated to the following signals: DIGIN [5:1], SWIM and GPIO0 [5:0] when available.

Figure 19. V_{OH} standard pad at 3.3 V

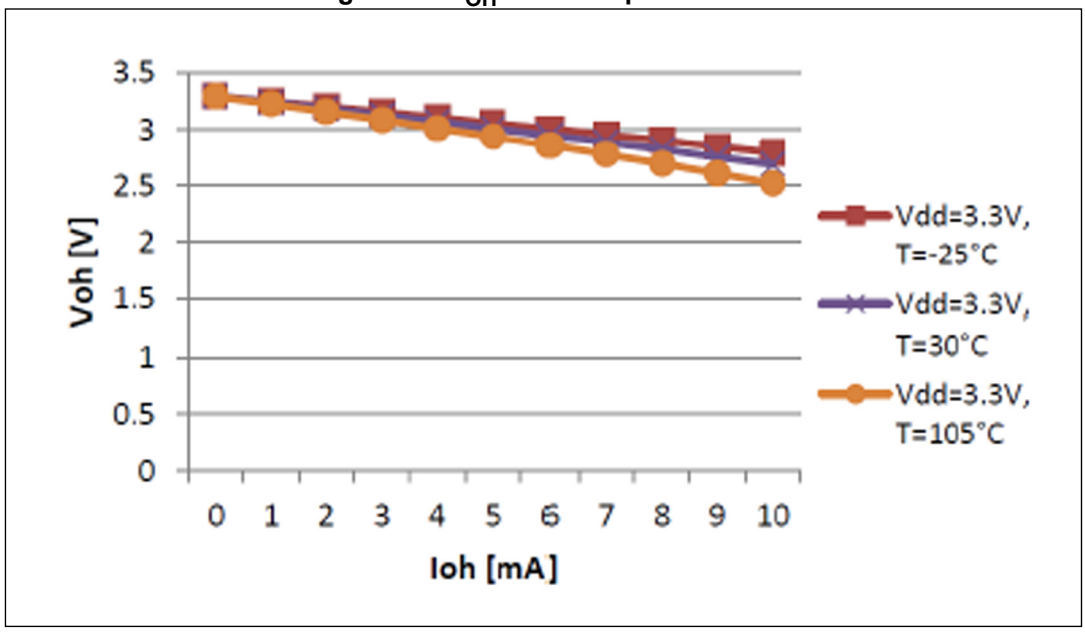


Figure 20. V_{OL} standard pad at 3.3 V

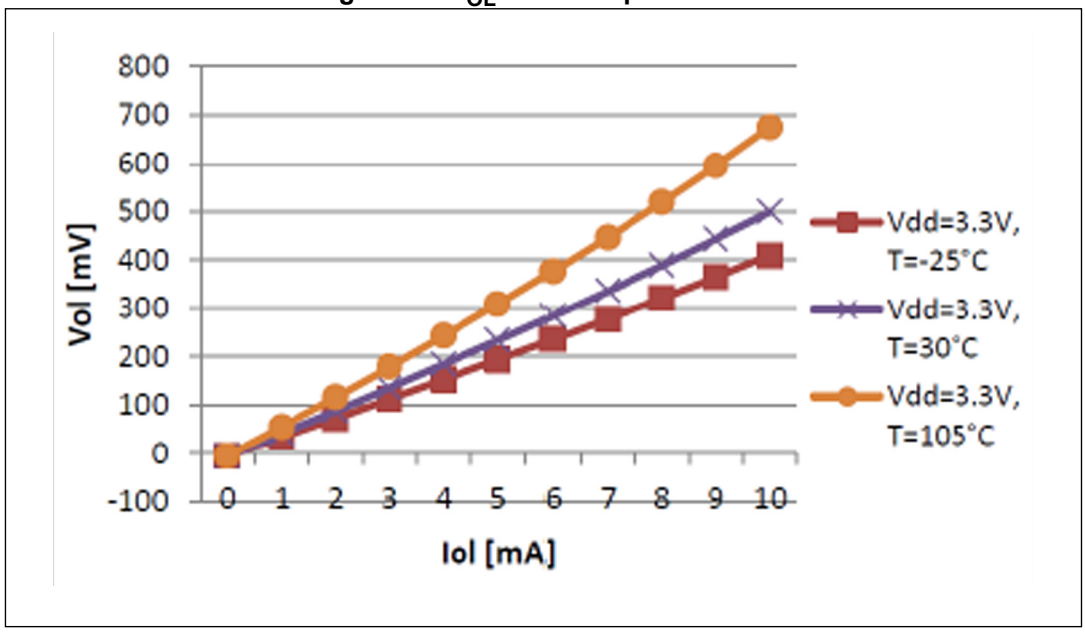


Figure 21. V_{OH} standard pad at 5 V

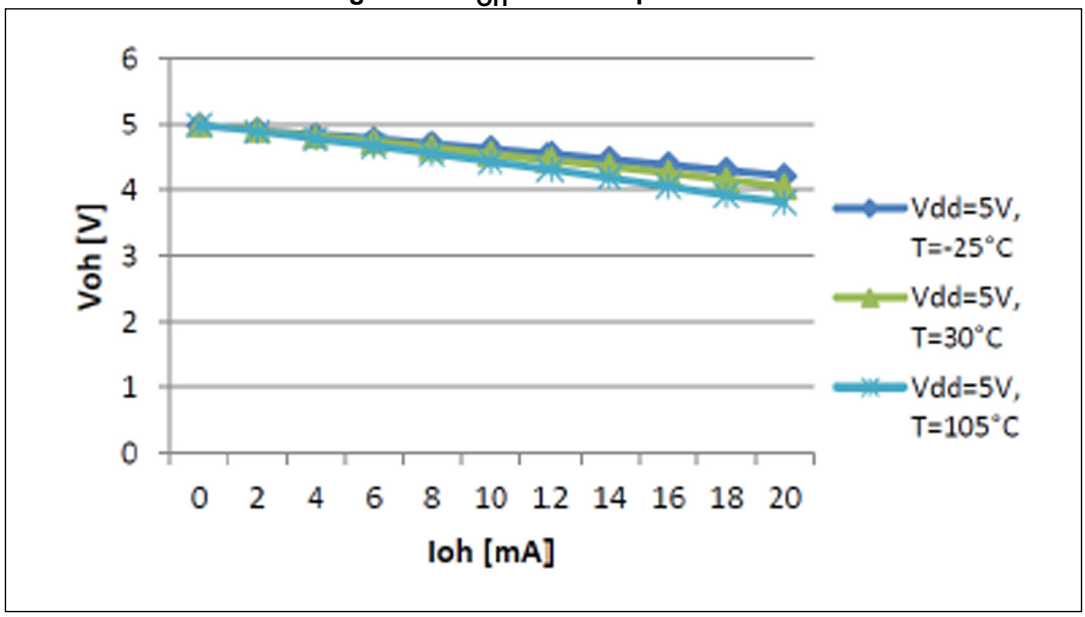
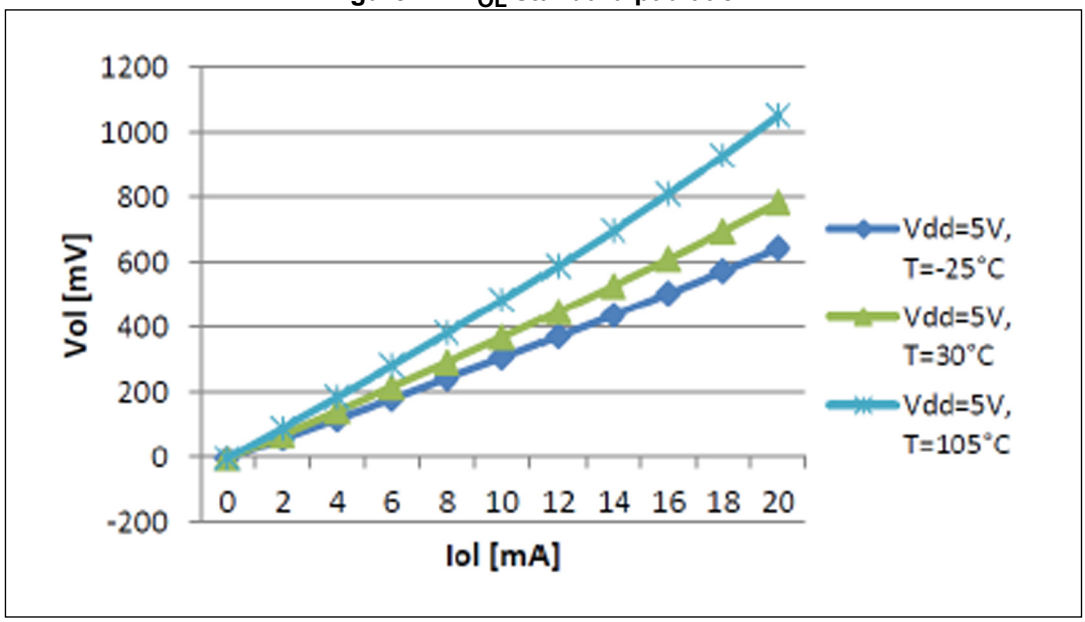


Figure 22. V_{OL} standard pad at 5 V



Fast pad

This pad is associated to the PWM [5:0] signals if the external pin is available.

Figure 23. V_{OH} fast pad at 3.3 V

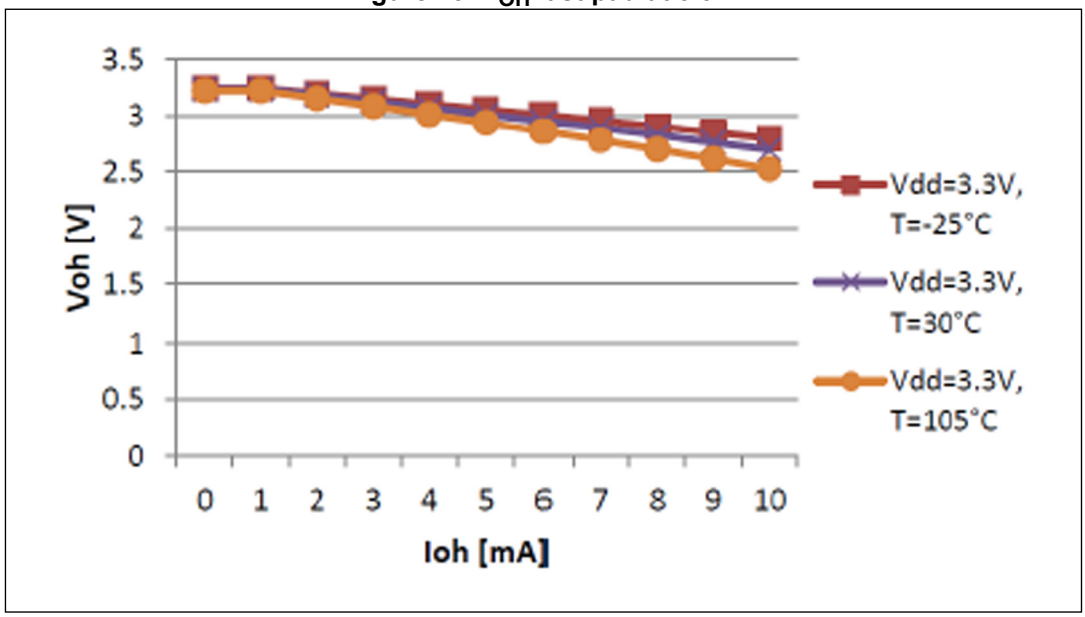


Figure 24. V_{OL} fast pad at 3.3 V

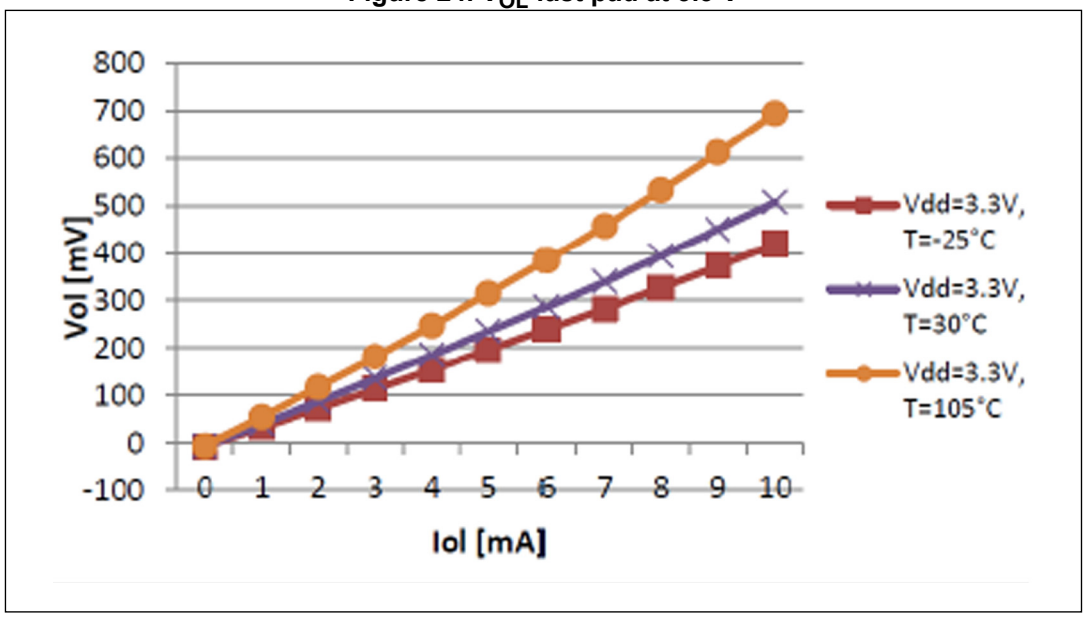


Figure 25. V_{OH} fast pad at 5 V

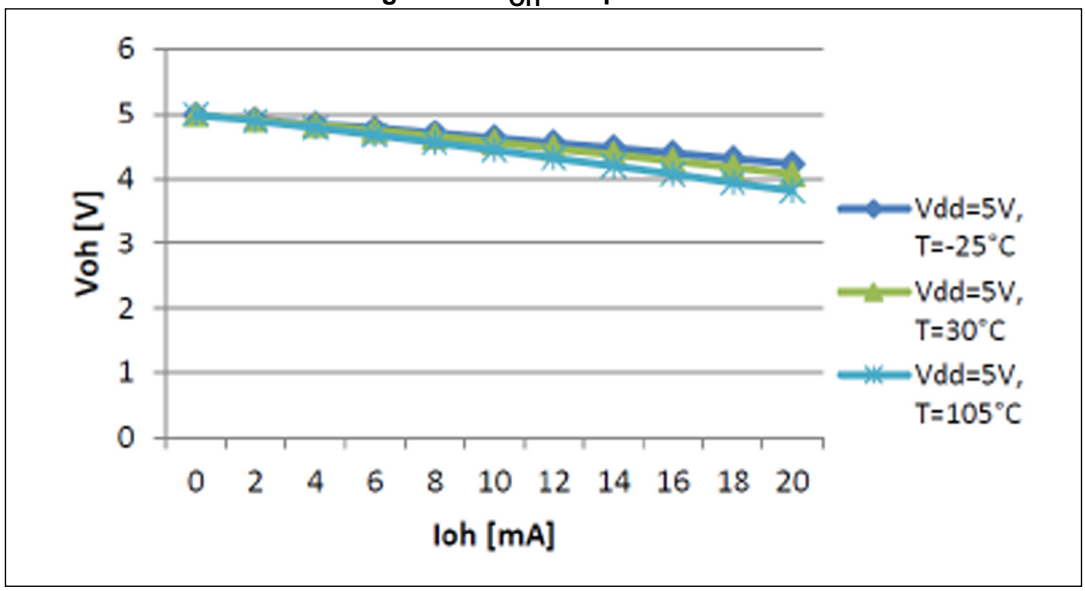
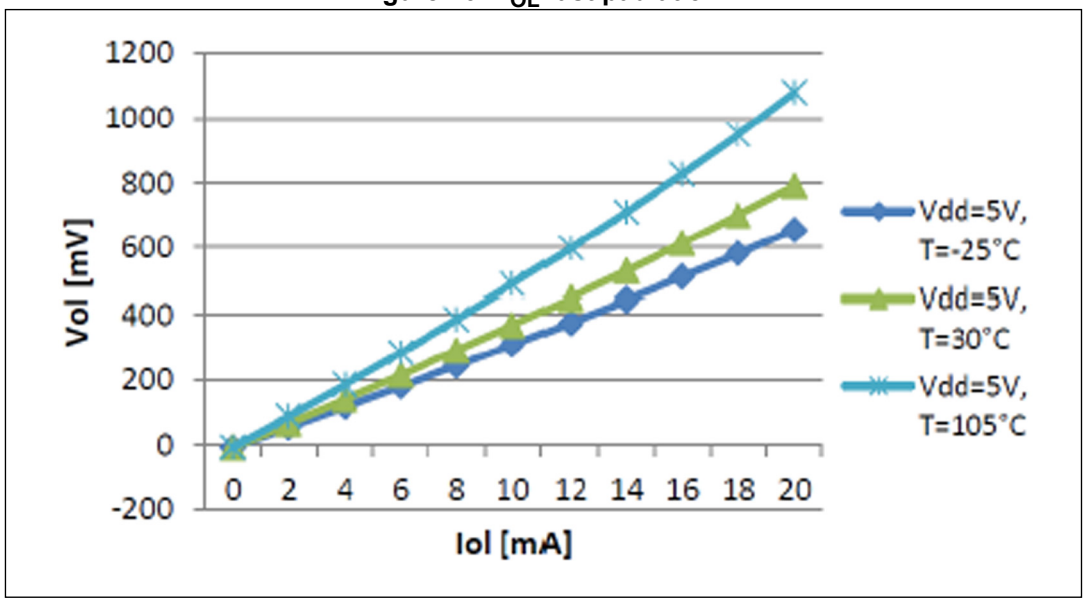


Figure 26. V_{OL} fast pad at 5 V



High speed pad

This pad is associated to the DIGIN [0] signals.

Figure 27. V_{OH} high speed pad at 3.3 V

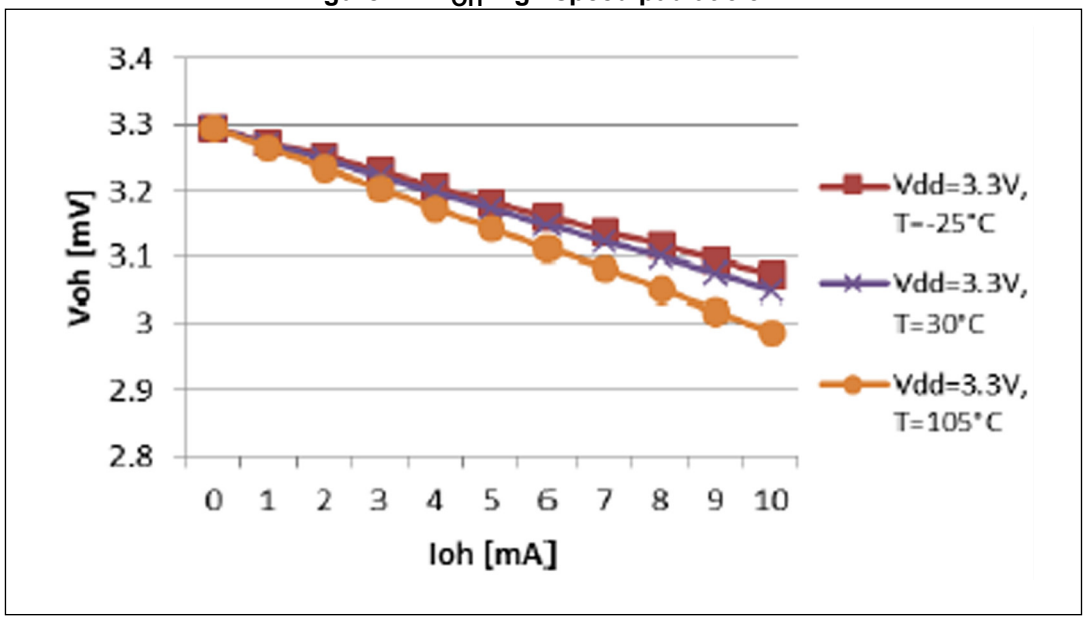


Figure 28. V_{OL} high speed pad at 3.3 V

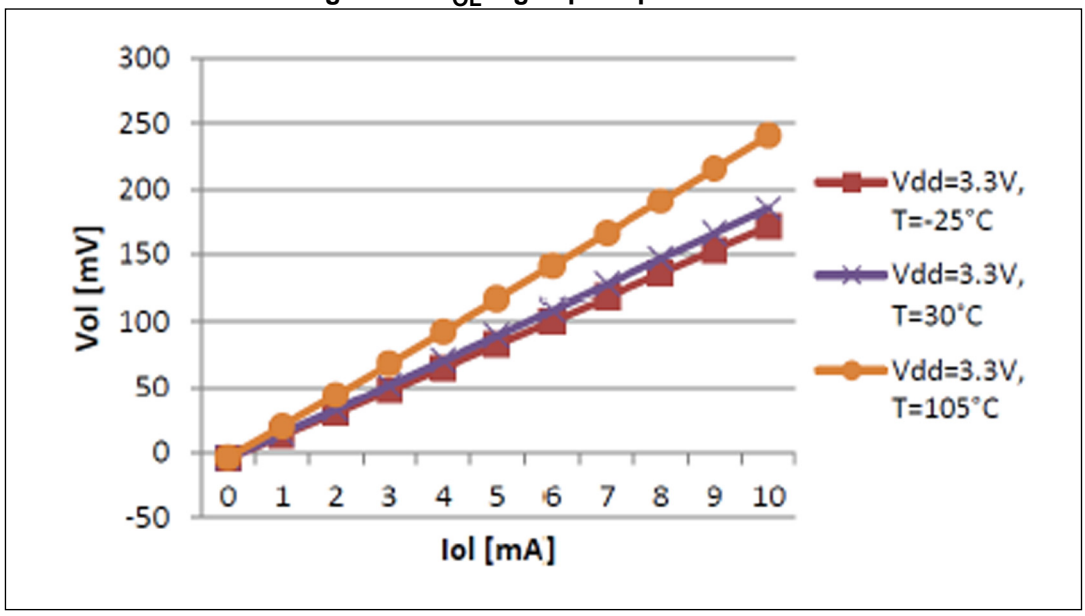


Figure 29. V_{OH} high speed pad at 5 V

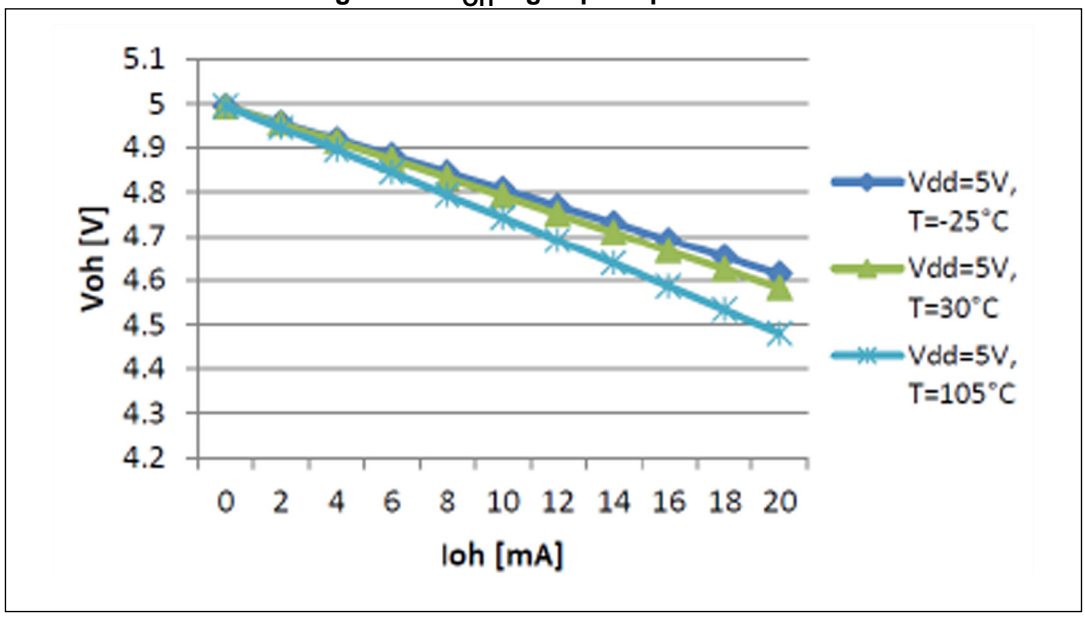
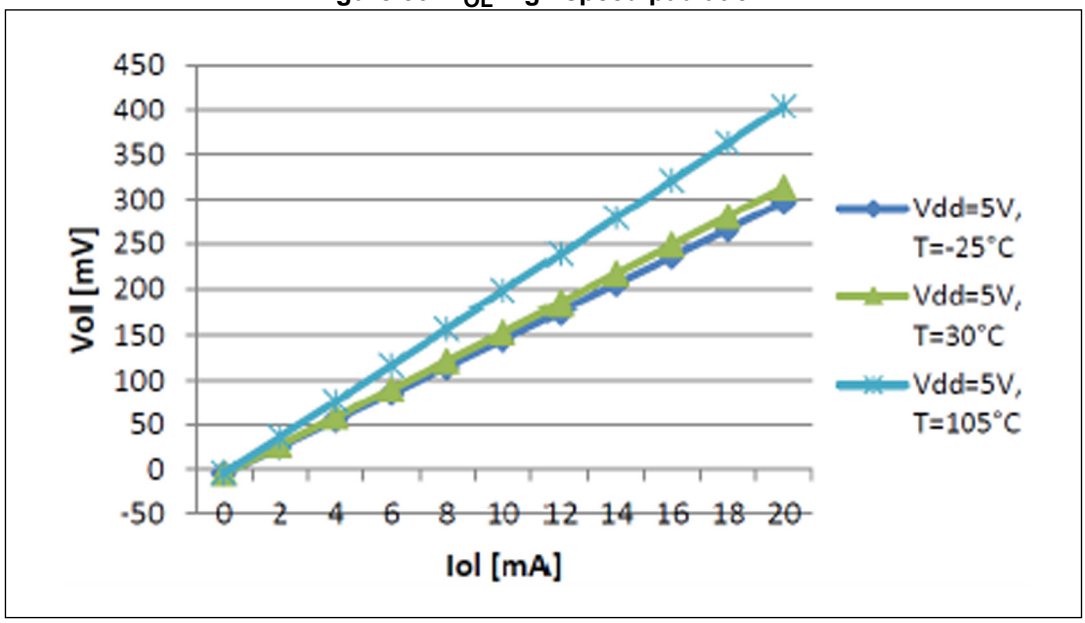


Figure 30. V_{OL} high speed pad at 5 V



12.3.9 Reset pin characteristics

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 87. NRST pin characteristics

Symbol	Parameter	Conditions	Min.(1)	Typ.	Max.(1)	Unit
$V_{IL(NRST)}$	NRST input low level voltage(1)		-0.3		0.3 x V_{DD}	V
$V_{IH(NRST)}$	NRST input high level voltage(1)		0.7 x V_{DD}		V_{DD} + 0.3	
$V_{OL(NRST)}$	NRST output low level voltage(1)	I_{OL}= 2 mA			0.5	
$R_{PU(NRST)}$	NRST pull-up resistor(2)		30	40	60	kΩ
$t_{IFP(NRST)}$	NRST input filtered pulse(3)				75	ns
$t_{INFP(NRST)}$	NRST not input filtered pulse(3)		500			
$t_{OP(NRST)}$	NRST output filtered pulse(3)		15			µs

1. Data based on characterization results, not tested in production.
2. The RPU pull-up equivalent resistor is based on a resistive transistor.
3. Data guaranteed by design, not tested in production.

12.3.10 I^2C interface characteristics

Table 88. I^2C interface characteristics

Symbol	Parameter	Standard mode		Fast mode(1)		Unit
		Min.(2)	Max.(2)	Min.(2)	Max.(2)	
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0(3)		0(3)	900(3)	
$t_{r(SDA)}$, $t_{r(SCL)}$	SDA and SCL rise time (V_{DD} = 3.3 to 5 V)(4)		1000		300	
$t_{f(SDA)}$, $t_{f(SCL)}$	SDA and SCL fall time (V_{DD} = 3.3 to 5 V)(4)		300		300	
$t_{h(STA)}$	START condition hold time	4.0		0.6		µs
$t_{su(STA)}$	Repeated START condition setup time	4.7		0.6		
$t_{su(STO)}$	STOP condition setup time	4.0		0.6		
$t_{w(STO:STA)}$	STOP to START condition time (bus free)	4.7		1.3		
C_b	Capacitive load for each bus line(5)		50		50	pF

1. f_{MASTER}, must be at least 8 MHz to achieve maximum fast I^2C speed (400 kHz).
2. Data based on standard I^2C protocol requirement, not tested in production.
3. The maximum hold time of the start condition has only to be met if the interface does not stretch the low time.
4. I^2C multifunction signals require the high sink pad configuration and the interconnection of 1 KΩ pull-up resistances.
5. 50 pF is the maximum load capacitance value to meet the I^2C STD timing specifications.

12.3.11 10-bit SAR ADC characteristics

Subject to general operating conditions for V_{DDA}, f_{MASTER}, and T_A unless otherwise specified.

Table 89. ADC characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
N	Resolution			10		bit
R_{ADCIN}	ADC input impedance		1			MΩ
f_{ADC}	ADC Clock frequency		1		6(1)	MHz
V_{IN1}	Conversion voltage range for gain x1		0		1.25(2), (3)	V
V_{IN2}	Conversion voltage range for gain x4(4)		0		0.3125(2), (3)	
V_{ref}	ADC main reference voltage(5)			1.250		
t_S	Sampling time	f_{ADC} = 6 MHz		0.50		µs
t_{STAB}	Wakeup time from ADC standby			30		
t_{CONV1}	Single conversion time including sampling time	f_{ADC} = 6 MHz		2.42		
t_{CONV2}	Continuous conversion time including sampling time	f_{ADC} = 6 MHz		3		

1. Frequency generated selecting the PLL source clock.
2. Maximum input analog voltage cannot exceed V_{DDA}.
3. Exceeding the maximum voltage on the ADCIN [7:0] signals (product depending) for the related conversion scale must be avoided since the ADC conversion accuracy can be impacted.
4. Product depending
5. ADC reference voltage at T_A = 25 °C.

ADC accuracy characteristics at V_{DD}/V_{DDA} 3.3 V

Table 90. ADC accuracy characteristics at V_{DD}/V_{DDA} 3.3 V

Symbol	Parameter	Conditions[1]	Typ.[2]	Min.[3]	Max.[3]	Unit
$\|E_T\|$	Total unadjusted error[4], [5], [6]	f_{ADC} = 6 MHz gain 1	2.8			LSB
$\|E_O\|$	Offset error[4], [5], [6]		0.3			
$\|E_G\|$	Gain error[4], [5], [6], [7]		0.4			
E_{O+G}	Offset + gain error[7], [8]			-8.5	9.3	
E_{O+G}	Offset + gain error[7], [9]			-11	11	
E_{O+G}	Offset + gain error[7], [10]			-14.3	11.3	
$\|E_D\|$	Differential linearity error[2], [3],[4]		0.5			
$\|E_L\|$	Integral linearity error[4], [5], [6]		1.4			
$\|E_T\|$	Total unadjusted error[4], [5], [6]	f_{ADC} = 6 MHz gain 4[11]	2.8			
$\|E_O\|$	Offset error[4], [5], [6]		0.3			
$\|E_G\|$	Gain error[4], [5], [6], [7]		0.4			
E_{O+G}	Offset + gain error[7], [8]			-12.7	15.5	
E_{O+G}	Offset + gain error[5], [9]			-16.7	18.8	
E_{O+G}	Offset + gain error[7], [10]			-19.2	18.8	
$\|E_D\|$	Differential linearity error[4], [5], [6]		0.5			
$\|E_L\|$	Integral linearity error[4], [5], [6]		1.4			

1. Measured with RAIN < 10 kΩ (RAIN external series resistance interconnected between the AC signal generator and the ADC input pin).
2. Temperature operating: T_A = 25 °C.
3. Data based on characterization results, not tested in production.
4. ADC accuracy vs. negative injection current. Injecting negative current on any of the analog input pins should be avoided as this reduces the accuracy of the conversion being performed on another analog input. It is recommended a Schottky diode (pin to ground) to be added to standard analog pins which may potentially inject the negative current. Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in the I/O port pin characteristic section does not affect the ADC accuracy. The ADC accuracy parameters may be also impacted exceeding the ADC maximum input voltage V_{IN1} or V_{IN2}.
5. Results in manufacturing test mode.
6. Data aligned with trimming voltage parameters.
7. Gain error evaluation with the two point method.
8. Temperature operating range: 0 ºC ≤ T_A ≤ 85 ºC.
9. Temperature operating range: -25 ºC ≤ T_A ≤ 105 ºC.
10. Temperature operating range: -40 ºC ≤ T_A ≤ 105 ºC.
11. Product depending.

ADC accuracy characteristics at V_{DD}/V_{DDA} 5 V

Table 91. ADC accuracy characteristics at V_{DD}/V_{DDA} 5 V

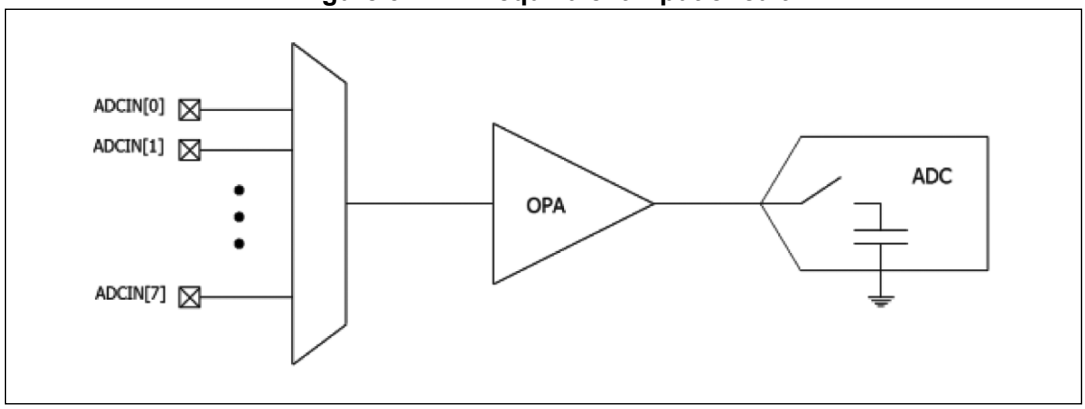
Symbol	Parameter	Conditions[1]	Typ.[2]	Min.[3]	Max.[3]	Unit
$\|E_T\|$	Total unadjusted error[4], [5], [6]	f_{ADC} = 6 MHz gain 1	TBD			LSB
$\|E_O\|$	Offset error[4], [5], [6]		0.5			
$\|E_G\|$	Gain error[4], [5], [6], [7]		0.4			
E_{O+G}	Offset + gain error[7], [8]			-8.3	8.9	
E_{O+G}	Offset + gain error[7], [9]			-10.9	10.9	
E_{O+G}	Offset + gain error[7], [10]			-13.8	10.9	
$\|E_D\|$	Differential linearity error[2], [3], [4]		0.8			
$\|E_L\|$	Integral linearity error[4], [5], [6]		2.0			
$\|E_T\|$	Total unadjusted error[4], [5], [6]	f_{ADC} = 6 MHz gain 4[11]	TBD			
$\|E_O\|$	Offset error[4], [5], [6]		1.2			
$\|E_G\|$	Gain error[4], [5], [6], [7]		0.2			
E_{O+G}	Offset + gain error[7], [8]			-12.2	15.3	
E_{O+G}	Offset + gain error[5], [9]			-16.4	18.5	
E_{O+G}	Offset + gain error[7], [10]			-18.8	18.5	
$\|E_D\|$	Differential linearity error[4], [5], [6]		0.8			
$\|E_L\|$	Integral linearity error[4], [5], [6]		2.0			

1. Measured with RAIN <10 kΩ (RAIN external series resistance interconnected between the AC signal generator and the ADC input pin).
2. Temperature operating: T_A = 25 °C.
3. Data based on characterization results, not tested in production.
4. ADC accuracy vs. negative injection current. Injecting negative current on any of the analog input pins should be avoided as this reduces the accuracy of the conversion being performed on another analog input. It is recommended a Schottky diode (pin to ground) to be added to standard analog pins which may potentially inject negative current. Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in the I/O port pin characteristic section does not affect the ADC accuracy. The ADC accuracy parameters may be also impacted exceeding the ADC maximum input voltage V_{IN1} or V_{IN2}.
5. Results in manufacturing test mode.
6. Data aligned with trimming voltage parameters.
7. Gain error evaluation with the two point method.
8. Temperature operating range: 0 ºC ≤ T_A ≤ 85 ºC.
9. Temperature operating range: -25 ºC ≤ T_A ≤ 105 ºC.
10. Temperature operating range: -40 ºC ≤ T_A ≤ 105 ºC.
11. Product depending.

ADC equivalent input circuit

Figure 31 shows the ADC equivalent input circuit.

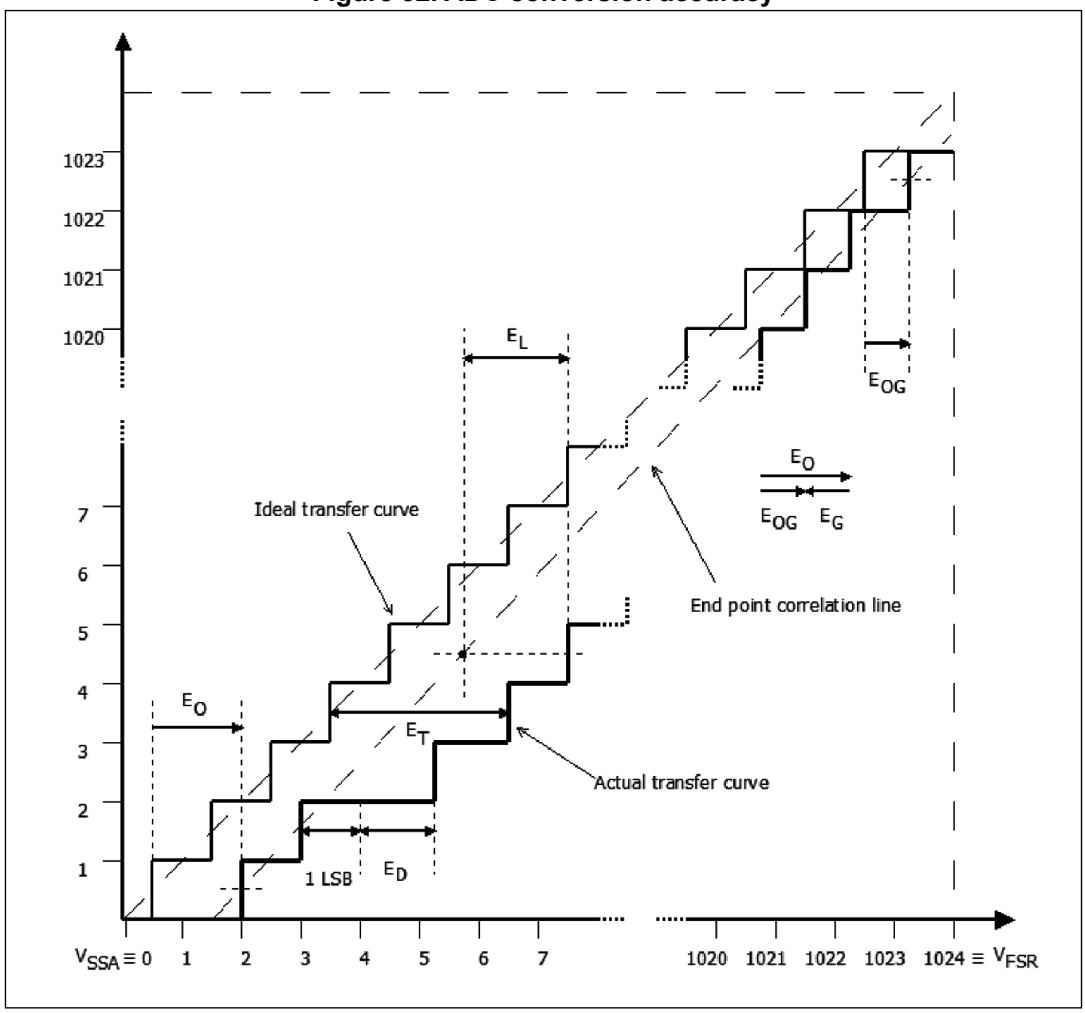
Figure 31. ADC equivalent input circuit



Note: The gain x1 ADC input analog voltage range is from 0 up to 1.25 V.
The gain x4 ADC input analog voltage range is from 0 up to 312.5 mV (check availability on device).
Maximum input analog voltage cannot exceed V_{DDA}.
ADC input impedance > 1 MΩ.
The ADCIN [7:0] input pins are provided by the ESD protection diodes.

ADC conversion accuracy

Figure 32. ADC conversion accuracy



ADC accuracy parameter definitions:

- E_T = total unadjusted error: maximum deviation between the actual and the ideal transfer curves.
- E_O = offset error: deviation between the first actual transition and the first ideal one.
- E_{OG} = offset + gain error (1-point gain): deviation between the last ideal transition and the last actual one.
- E_G = gain error (2-point gain): defined so that $E_{OG} = E_O + E_G$ (parameter correlated to the deviation of the characteristic slope).
- E_D = differential linearity error: maximum deviation between actual steps and the ideal one.
- E_L = integral linearity error: maximum deviation between any actual transition and the end-point correlation line.

12.3.12 Analog comparator characteristics

Table 92. Analog comparator characteristics

Symbol	Parameter	Conditions	Min.(1)	Typ.	Max.(1)	Unit
V_{CPP}	Comparator positive input voltage range	-40 ºC ≤ T_A ≤ 105 ºC	0		1.23(2)	V
V_{CPM}	Comparator negative external input voltage range		0		1.23(2), (3)	V
C_{IN}	Input capacitance			3		pF
V_{offset}	Comparator offset error				15	mV
t_{COMP}	Comparison delay time				50(4), (5)	ns

1. Data based on characterization results, not tested in production.
2. Maximum analog input voltage cannot exceed V_{DDA}.
3. The comparator 3 can be configured with the external reference voltage signal CPM3.
4. The overdrive voltage is ± 50 mV.
5. This parameter doesn't consider the delay time of comparator signal synchronization stages and SMED logic.

Table 93. Analog comparator hysteresis at V_{DD}/V_{DDA} 3.3 V

Symbol	Parameter	Conditions	Hysteresis positive(1)		Hysteresis negative(1)		Unit
			Min.	Max.	Max.	Max.	
V_{HYST0}	Hysteresis voltage code 0	-40 ºC ≤ T_A ≤ 105 ºC	No hysteresis				mV
V_{HYST1}, V_{HYST2}	Hysteresis voltage code1, 2		N. A.				
V_{HYST3}	Hysteresis voltage code 3		4	52	0	-60	
V_{HYST4}	Hysteresis voltage code 4		13	78	-13	-80	
V_{HYST5}	Hysteresis voltage code 5		41	148	-45	-150	
V_{HYST6}	Hysteresis voltage code 6		56	203	-58	-205	
V_{HYST7}	Hysteresis voltage code 7		123	406	-125	-403	

1. Data based on characterization results, not tested in production.

Table 94. Analog comparator hysteresis at V_{DD}/V_{DDA} 5 V

Symbol	Parameter	Conditions	Hysteresis positive(1)		Hysteresis negative(1)		Unit
			Min.	Max.	Max.	Max.	
V_{HYST0}	Hysteresis voltage code 0	-40 °C ≤ T_A ≤ 105 °C	No hysteresis				mV
V_{HYST1}, V_{HYST2}	Hysteresis voltage code1, 2		N. A.				
V_{HYST3}	Hysteresis voltage code 3		N. A.		-1	-56	
V_{HYST4}	Hysteresis voltage code 4		2	82	-13	-81	
V_{HYST5}	Hysteresis voltage code 5		17	154	-42	-148	
V_{HYST6}	Hysteresis voltage code 6		37	202	-57	-203	
V_{HYST7}	Hysteresis voltage code 7		119	398	-124	-400	

1. Data based on characterization results, not tested in production.

12.3.13 DAC characteristics

Table 95. DAC characteristics

Symbol	Parameter	Conditions	Min.(1)	Typ.	Max.(1)	Unit
N	Resolution	-40 °C ≤ T_A ≤ 105 °C		4		bit
$V_{full\ scale}$	DAC full scale		1.2		1.26	V
V_{offset}	DAC offset				4	mV
V_{dac}	DAC out voltage		V_{offset}		$V_{full\ scale}$	mV
LSB				82		mV
INL	Integral non linearity				0.12	LSB

1. Data based on characterization results, not tested in production.

Equation 5

$$n[0, 15] : V_{dac(n)} = \frac{(V_{fullscale} - V_{offset})}{15} \bullet (n) + V_{offset}$$

Equation 6

$$n[1, 14] : V_{dac(n)} = \frac{(V_{fullscale} - V_{offset})}{15} \bullet (n + INL) + V_{offset}$$

where:

- $V_{fullscale}$ = $V_{fullscale}$(sample, T)
- V_{offset} = V_{offset} (sample, T)
- *INL* = INL (sample, n)

12.4 EMC characteristics

12.4.1 Electrostatic discharge (ESD)

Electrostatic discharges (3 positive then 3 negative pulses separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts * (n + 1) supply pin).

Table 96. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Maximum value	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = 25 °C, conforming to JEDEC/JESD22-A114E	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = 25 °C, conforming to ANSI/ESD STM 5.3.1 ESDA	500	
$V_{ESD(MM)}$	Electrostatic discharge voltage (machine model)	T_A = 25 °C, conforming to JEDEC/JESD-A115-A	200	

Data based on characterization results, not tested in production.

12.4.2 Static latch-up

Two complementary static tests are required on 10 parts to assess the latch-up performance.

A supply overvoltage (applied to each power supply pin) and a current injection (applied to each input, output and configurable I/O pin) are performed on each sample. This test conforms to the EIA/JESD 78 IC latch-up standard.

Table 97. Electrical sensitivity

Symbol	Parameter	Conditions	Level
LU	Static latch-up class	T_A = 105 °C	A

13 Thermal characteristics

The STNRG functionality cannot be guaranteed when the device operating exceeds the maximum chip junction temperature (T_{Jmax}).

T_{Jmax}, in °C, may be calculated using *Equation 7*:

Equation 7

$$T_{Jmax} = T_{Amax} + (PD_{max} \times \Theta J_A)$$

where:

T_{Amax} is the maximum ambient temperature in °C

ΘJ_A is the package junction to ambient thermal resistance in °C/W

P_{Dmax} is the sum of P_{INTmax} and $P_{I/Omax}$ ($P_{Dmax} = P_{INTmax} + P_{I/Omax}$)

P_{INTmax} is the product of I_{DD} and V_{DD}, expressed in watts. This is the maximum chip internal power.

$P_{I/Omax}$ represents the maximum power dissipation on output pins where:

$P_{I/Omax} = (V_{OL} \times I_{OL}) + \Sigma[(V_{DD} - V_{OH}) \times I_{OH}]$,

taking into account the actual V_{OL}/I_{OL} and V_{OH}/I_{OH} of the I/Os at low and high level.

Table 98. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	TSSOP38 - thermal resistance junction to ambient(1)	80	°C/W

1. Thermal resistance is based on the JEDEC JESD51-2 with the 4-layer PCB in a natural convection environment.

14 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

14.1 TSSOP38 package information

Figure 33. TSSOP38 package outline

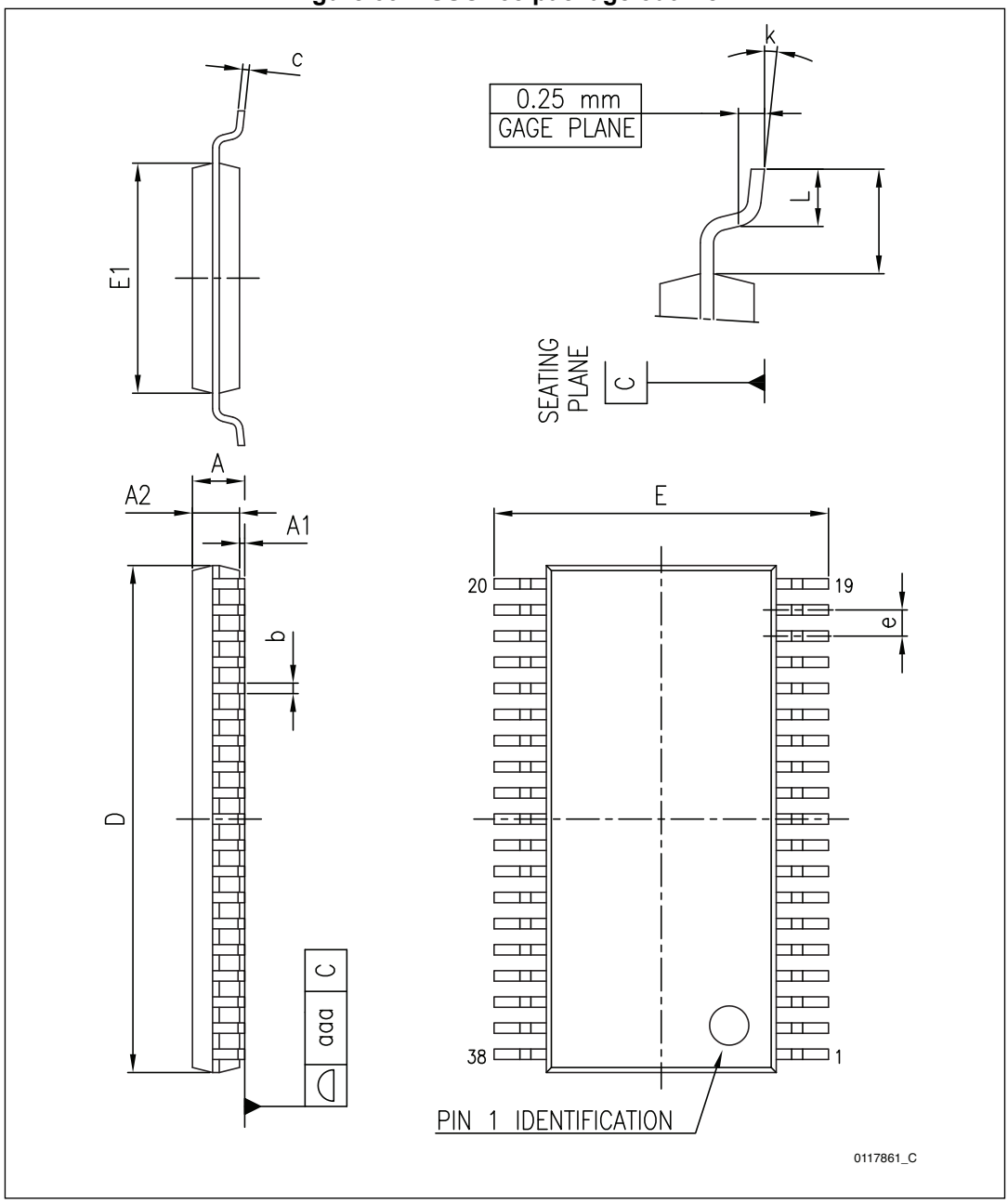


Table 99. TSSOP38 package mechanical data(1)

Symbol	Dimensions (mm)		
	Min.	Typ.	Max.
A			1.20
A1	0.05		0.15
A2	0.80	1.00	1.05
b	0.17		0.27
c	0.09		0.20
D(2)	9.60	9.70	9.80
E	6.20	6.40	6.60
E1(2)	4.30	4.40	4.50
e		0.50	
L	0.45	0.60	0.75
L1		1.00	
k	0		8
aaa			0.10

1. “TSSOP stands for “Thin Shrink Small Outline Package”.
2. “Dimensions “D” and “E1”do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.

15 STNRG development tools

The development tools for the STNRG microcontroller are provided by:

- Raisonance with the C compiler and the integrated development environment (Ride7), which provides start-to-finish control of application development including the code editing, compilation, optimization and debugging.
  The Ride7 supports the RLink in-circuit debugger/programmer using the SWIM interface (USB/SWIM).
- IAR Embedded Workbench® for STM8. The IAR Embedded Workbench IAR-EWSTM8 is a software development tool with the highly optimizing C and C++ compiler for the STM8 CPU device.
  The workbench supports the ST-LINK and STice debug probes using the SWIM interface (USB/SWIM).

16 Order codes

Table 100. Ordering information

Order code	Package	Packaging
STNRG388A	TSSOP38	Tube
STNRG388ATR		Tape and reel

17 Revision history

Table 101. Document revision history

Date	Revision	Changes
28-Apr-2015	1	Initial release.
18-Oct-2016	2	Updated *Table 2 on page 12* (added DALI peripheral to “Communication”). Updated *Figure 1 on page 14* (replaced by new figure). Updated *Section 4 on page 14* and *Figure 2 on page 15* (added DALI). Added *Section 5.5.3 on page 28*. Updated *Table 38 on page 62* (replaced “control logic” by “interrupt” in SMED-x descriptions, updated cross-references to notes in “Priority” 28 and 29). Updated *Table 45 on page 68* (several modifications). Updated cross-references in *Section 10.2.16 on page 73*, *Section 10.2.18 on page 74*, and *Section 10.2.20 on page 75*. Updated *Table 66 on page 80* (added note *2.*, updated cross-references). Minor modifications throughout document.
13-Dec-2021	3	Removed all examples of STNRG228A and STNRG328A. Removed all examples of VFQFPN32 and TSSOP28 package. Updated cover image on Page 1