ecoSwitch™ Advanced Load Management

Controlled Load Switch with Low R_{ON}

NCP45732

The NCP45732 load management devices provide a component and area−reducing solution for efficient power domain switching with inrush current limit via soft start. These devices are designed to integrate control and driver functionality with a high performance low on−resistance power MOSFET in a single package offering safeguards and monitoring via fault protection and power−good signaling. This cost effective solution is ideal for power management and disconnect functions in USB Type−C ports and power management applications requiring low power consumption in a small footprint.

Features

- Advanced Controller with Charge Pump
- Integrated N−Channel MOSFET with Low R_{ON}
- Soft−Start via Controlled Slew Rate
- Fault Detection with Power Good Output
- Thermal Shutdown and Under Voltage Lockout
- Short−Circuit and Adjustable Over−Current Protections
- Input Voltage Range 3 V to 24 V
- Extremely Low Standby Current
- This is a Pb−free, RoHS/REACH Compliant Device

Typical Applications

- USB Type C Power Delivery
- Servers, Set−Top Boxes and Gateways
- Notebook and Tablet Computers
- Telecom, Networking, Medical and Industrial Equipment
- Hot−Swap Devices and Peripheral Ports

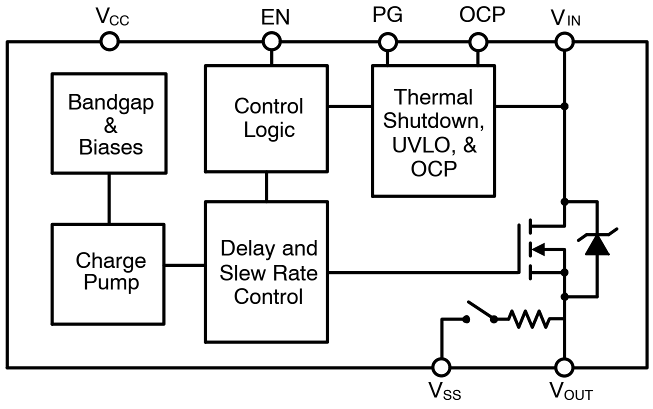
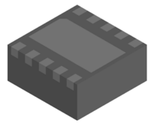


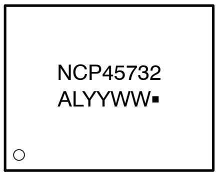
Figure 1. Block Diagram

R_{ON} TYP	V_{CC}	V_{IN}	I_{MAX}
11.7 mΩ	4.5 V	3.0 V	8 A
11.7 mΩ	3.3 V	4.5 V	
11.7 mΩ	3.3 V	15 V	
11.7 mΩ	3.3 V	24 V	



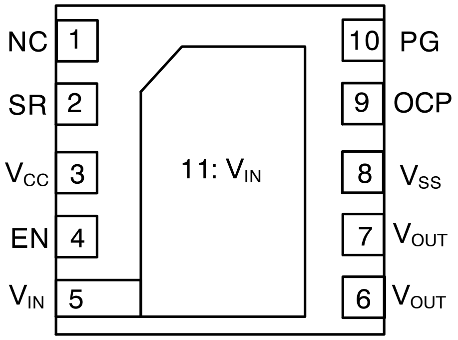
DFN10 2x2, 0.4P
CASE 506FB

MARKING DIAGRAM



A = Assembly Location
L = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

PIN CONFIGURATION



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCP45732IMN24TWG	DFN10 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Table 1. PIN DESCRIPTION

Pin	Name	Function
2	SR	Slew rate adjustment made with an external capacitor to V_{SS}; float if not used.
3	V_{CC}	Driver supply voltage (3.0 V − 5.5 V)
4	EN	Active−high digital input used to turn on the MOSFET driver, pin has an internal pull down resistor to V_{SS}
5,11	V_{IN}	Input voltage (3 V − 24 V) − **Pin 11 should be used for high current (>0.5A)**
6,7	V_{OUT}	Source of MOSFET connected to load. Includes an internal bleed resistor to V_{SS}. − **All pins must be connected to provide correct R_{ON}, OCP, and current capability.**
8	V_{SS}	Driver ground
9	OCP	Over−current protection trip point adjustment made with an external resistor, pin has an internal pull up resistor to EN; Connect to ground if over−current protection is not needed.
10	PG	Active−high, open−drain output that indicates when the gate of the MOSFET is fully charged, external pull up resistor ≥ 100 kΩ to an external voltage source required; tie to V_{SS} if not used.

Table 2. ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage Range	V_{CC}	−0.3 to 6	V
Input Voltage Range	V_{IN}	−0.3 to 30	V
Output Voltage Range	V_{OUT}	−0.3 to 30	V
EN Input Voltage Range	V_{EN}	GND−0.3 to (V_{CC} + 0.3)	V
PG Output Voltage Range (Note 1)	V_{PG}	−0.3 to 6	V
OCP Input Voltage Range	V_{OCP}	−0.3 to 6	V
Thermal Resistance, Junction−to−Ambient, Steady State (Note 2)	$R_{\theta JA}$	200.57	°C/W
Thermal Resistance, Junction−to−Case (V_{IN} Paddle)	$R_{\theta JC}$	8.46	°C/W
Continuous MOSFET Current @ T_A = 25°C (Note 2)	I_{MAX}	20	A
Total Power Dissipation @ T_A = 25°C (Note 2) Derate above T_A = 25°C	P_D	3.49 34.9	W mW/°C
Storage Temperature Range	T_{STG}	−55 to 150	°C
Lead Temperature, Soldering (10 sec.)	T_{SLD}	260	°C
ESD Capability, Human Body Model (Notes 3 and 4)	ESD_{HBM}	2	kV
ESD Capability, Charged Device Model (Notes 3 and 4)	ESD_{CDM}	1	kV
Latch−up Current Immunity (Note 3)	LU	100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. PG is an open−drain output that requires an external pull−up resistor > 100 kΩ to an external voltage source.
2. Simulated as surface−mounted on 12 mm x 12 mm FR4 board, 2 oz Cu. See the Layout Guidelines section in Applications Information.
3. Tested by the following methods @ T_A = 25°C:
   ESD Human Body Model tested per JESD22−A114
   ESD Charged Device Model per ESD STM5.3.1
   Latch−up Current tested per JESD78
4. Rating is for all pins except for V_{IN} and V_{OUT} which are tied to the internal MOSFET's Drain and Source. Typical MOSFET ESD performance for V_{IN} and V_{OUT} should be expected and these devices should be treated as ESD sensitive.

Table 3. OPERATING RANGES

Rating	Symbol	Min	Max	Unit
V_{CC} – (V_{IN} > 4.5 V)	V_{CC}	3	5.5	V
V_{CC} – (V_{IN} < 4.5 V)	V_{CC}	4.5	5.5	V
V_{IN} – (V_{CC} > 4.5 V)	V_{IN}	3	24	V
V_{IN} – (V_{CC} < 4.5 V)	V_{IN}	4.5	24	V
OCP External Resistor to V_{SS}	R_{OCP}	short	open	kΩ
OFF to ON Energy Dissipation Limit (See application section.)	E_{TRANS}		50	mJ
V_{SS}	V_{SS}		0	V
Ambient Temperature	T_A	−40	85	°C
Junction Temperature	T_J	−40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 4. ELECTRICAL CHARACTERISTICS (T_J = 25°C, V_{CC} = 3 V – 5.5 V, unless otherwise specified)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
On−Resistance	V_{CC} = 4.5 V; V_{IN} = 3 V	R_{ON}		11.7	13.5	mΩ
	V_{CC} = 3.3 V; V_{IN} = 4.5 V			11.7	13.5	
	V_{CC} = 3.3 V; V_{IN} = 15 V			11.7	13.5	
	V_{CC} = 3.3 V; V_{IN} = 24 V			11.7	13.5	
Leakage Current – V_{IN} to V_{OUT} (Note 5)	V_{EN} = 0 V; V_{IN} = 24 V	I_{LEAK}	−100	−15	100	nA
V_{IN} Control Current – V_{IN} to V_{SS}	V_{EN} = 0 V; V_{IN} = 24 V (for typical)	I_{INCTL}	−1.5	0.8	1.5	µA
V_{IN} Control Current – V_{IN} to V_{SS}	V_{EN} = V_{CC}; V_{IN} = 24 V (for typical)	I_{INCTL_EN}	−300	145	300	µA
Supply Standby Current (Note 6)	V_{EN} = 0 V; V_{IN} = 24 V (for typical)	I_{STBY}		1	5	µA
Supply Dynamic Current (Note 7)	V_{EN} = V_{CC}; V_{IN} = 24 V (for typical)	I_{DYN}		350	500	µA
Bleed Resistance		R_{BLEED}	75	100	200	kΩ
EN Input High Voltage		V_{IH}	2			V
EN Input Low Voltage		V_{IL}			0.8	V
EN Input Leakage Current	V_{EN} = 0 V	I_{IL}	−1.0	0	1	µA
EN Pull Down Resistance		R_{PD}	76	100	124	kΩ
PG Output Low Voltage	I_{SINK} = 5 mA	V_{OL}			0.1	V
PG Output Leakage Current	V_{TERM} = 3.3 V	I_{OH}		5	100	nA
Slew Rate Control Constant (Note 8)		K_{SR}	70	103	130	µA

FAULT PROTECTIONS

Thermal Shutdown Threshold (Note 9)		T_{SDT}		145		°C
Thermal Shutdown Hysteresis (Note 9)		T_{HYS}		20		°C
V_{IN} Under Voltage Lockout Threshold	V_{IN} rising	V_{UVLO}	1.8	2	2.3	V
V_{IN} Under Voltage Lockout Hysteresis		V_{HYS}	150	200	300	mV

Table 4. ELECTRICAL CHARACTERISTICS (T_J = 25°C, V_{CC} = 3 V − 5.5 V, unless otherwise specified)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
FAULT PROTECTIONS						
Over−Current Protection Trip	R_{OCP} = open	I_{TRIP}	0.6	1	1.3	A
	R_{OCP} = 100 kΩ			4		
	R_{OCP} = 22 kΩ			7		
	R_{OCP} = 1 kΩ			8		
	R_{OCP} = short to GND			8		
Over−Current Protection Blanking Time		t_{OCP}		2.25		ms
Short−Circuit Protection Trip Current		I_{SC}		8.0		A

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Average current from V_{IN} to V_{OUT} with MOSFET turned off.
6. Average current from V_{CC} to GND with MOSFET turned off.
7. Average current from V_{CC} to GND after charge up time of MOSFET.
8. See Applications Information section for details on how to adjust the gate slew rate.
9. Operation above T_J = 125°C is not guaranteed.

Table 5. SWITCHING CHARACTERISTICS (T_J = 25°C unless otherwise specified) (Notes 10 and 11)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Output Slew Rate − Default	V_{CC} = 4.5 V; V_{IN} = 3 V	SR	15	21	29	V/ms
	V_{CC} = 5.0 V; V_{IN} = 3 V		15	21	29	
	V_{CC} = 3.3 V; V_{IN} = 24 V		15	24	29	
	V_{CC} = 5.0 V; V_{IN} = 24 V		15	24	29	
Output Turn−on Delay	V_{CC} = 4.5 V; V_{IN} = 3 V	T_{ON}	100	148	600	μs
	V_{CC} = 5.0 V; V_{IN} = 3 V		100	149	600	
	V_{CC} = 3.3 V; V_{IN} = 24 V		100	264	600	
	V_{CC} = 5.0 V; V_{IN} = 24 V		100	267	600	
Output Turn−off Delay	V_{CC} = 4.5 V; V_{IN} = 3 V	T_{OFF}		25		μs
	V_{CC} = 5.0 V; V_{IN} = 3 V			20		
	V_{CC} = 3.3 V; V_{IN} = 24 V			15		
	V_{CC} = 5.0 V; V_{IN} = 24 V			10		
Power Good Turn−on Time	V_{CC} = 4.5 V; V_{IN} = 3 V	$T_{PG,ON}$	0.25	0.4	2.0	ms
	V_{CC} = 5.0 V; V_{IN} = 3 V		0.25	0.4	2.0	
	V_{CC} = 3.3 V; V_{IN} = 24 V		0.25	1.4	2.0	
	V_{CC} = 5.0 V; V_{IN} = 24 V		0.25	1.4	2.0	
Power Good Turn−off Time	V_{CC} = 4.5 V; V_{IN} = 3 V	$T_{PG,OFF}$		15		ns
	V_{CC} = 5.0 V; V_{IN} = 3 V			15		
	V_{CC} = 3.3 V; V_{IN} = 24 V			15		
	V_{CC} = 5.0 V; V_{IN} = 24 V			15		

10. See below figure for Test Circuit and Timing Diagram.
11. Tested with the following conditions: V_{TERM} = V_{CC}; R_{PG} = 100 kΩ; R_L = 10 Ω; C_L = 0.1 μF.

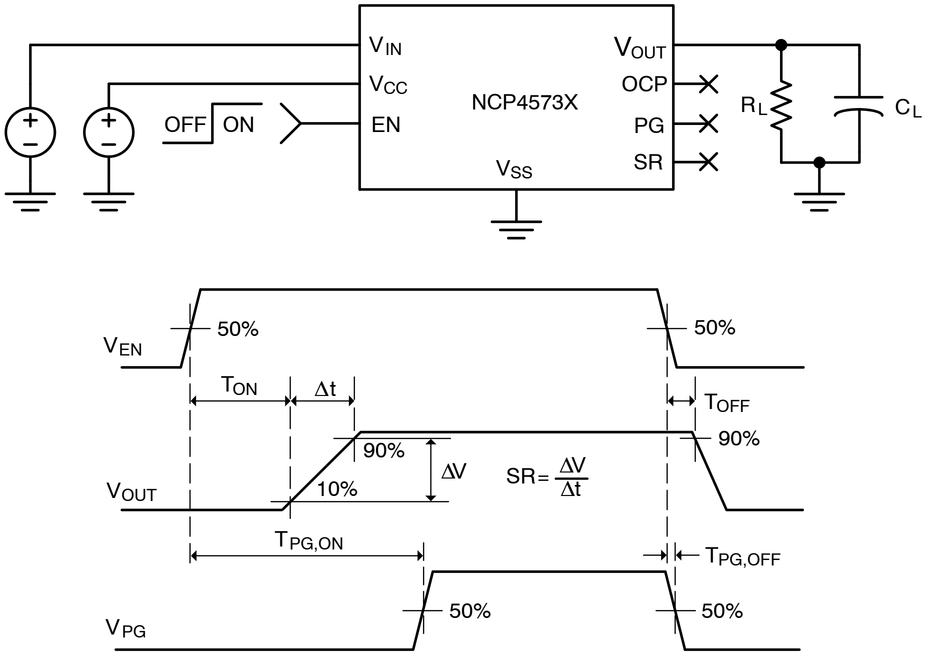


Figure 2. Switching Characteristics Test Circuit and Timing Diagrams

TYPICAL CHARACTERISTICS

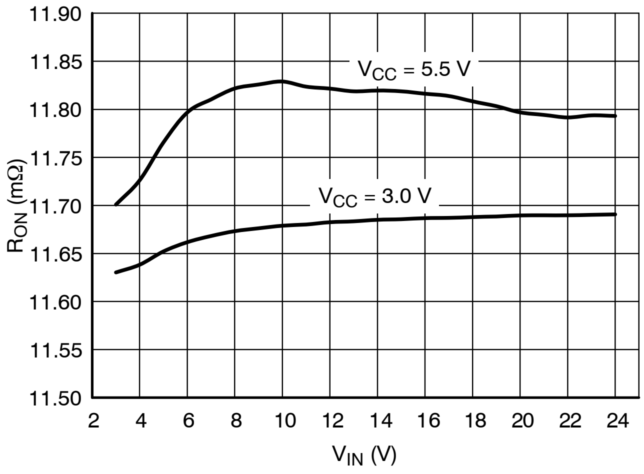


Figure 3. On−Resistance vs. Input Voltage

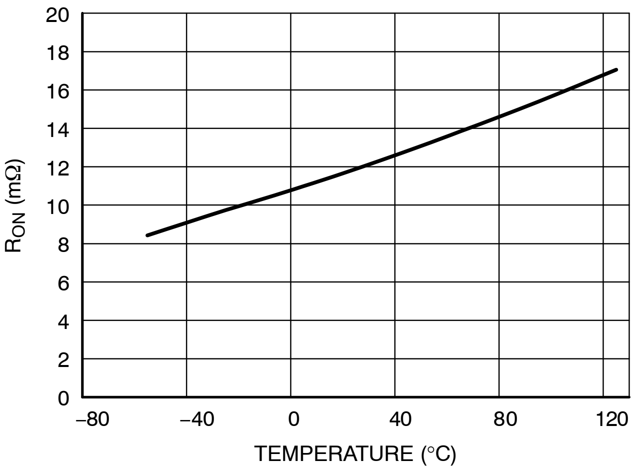


Figure 4. On−Resistance vs. Temperature

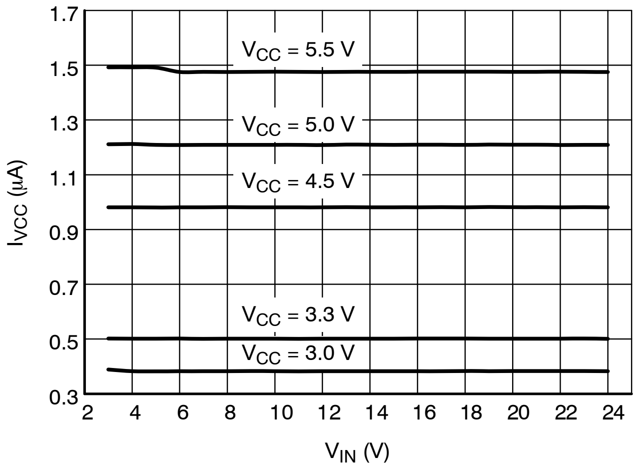


Figure 5. Supply Standby Current vs. Input Voltage

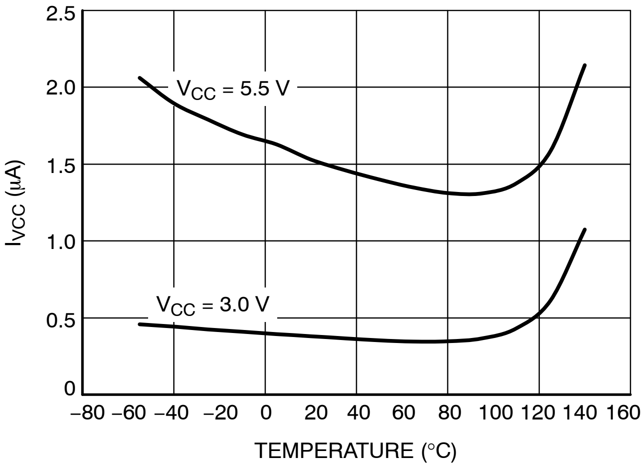


Figure 6. Supply Standby Current vs. Temperature

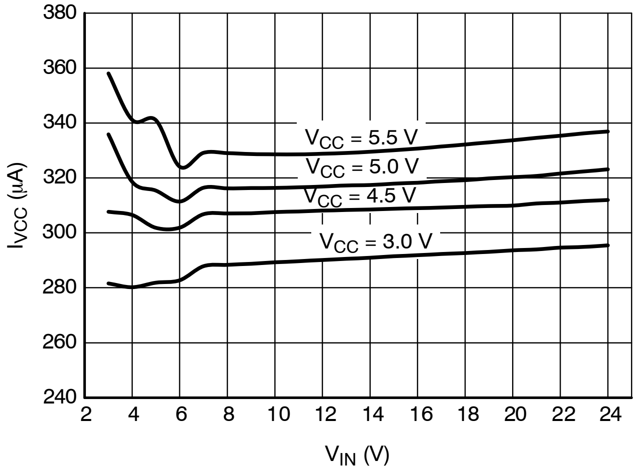


Figure 7. Supply Dynamic Current vs. Input Voltage

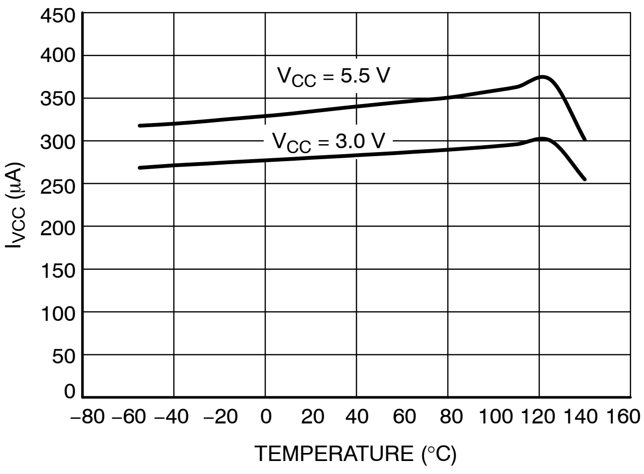


Figure 8. Supply Dynamic Current vs. Temperature

TYPICAL CHARACTERISTICS

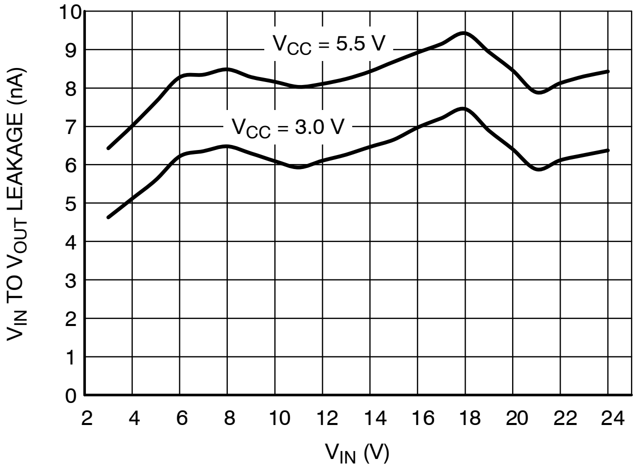


Figure 9. Input to Output Leakage vs. Input Voltage (EN = 0)

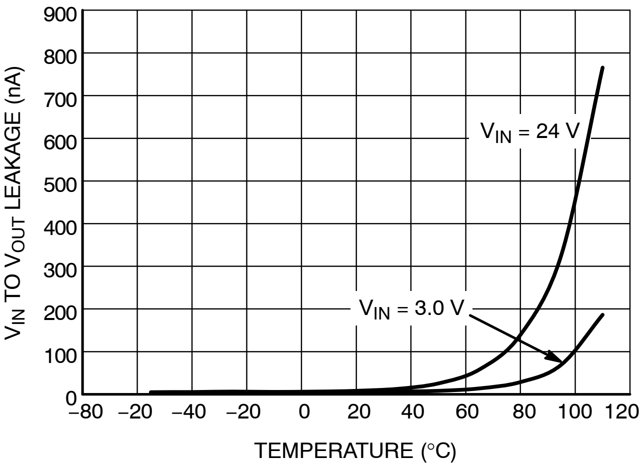


Figure 10. Input to Output Leakage vs. Temperature

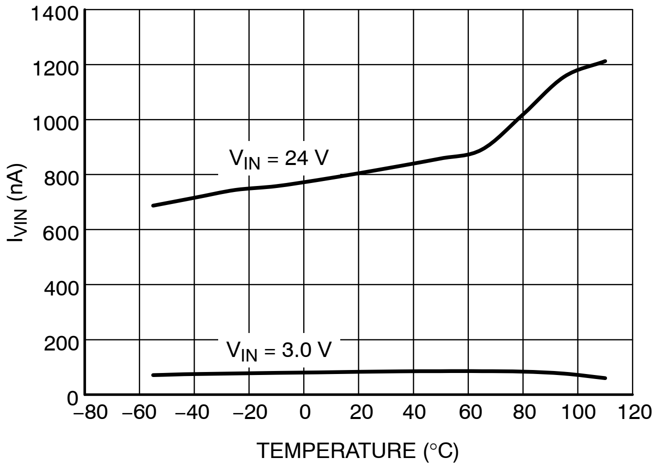


Figure 11. V_{IN} Controller Current vs. Temperature (EN = 0)

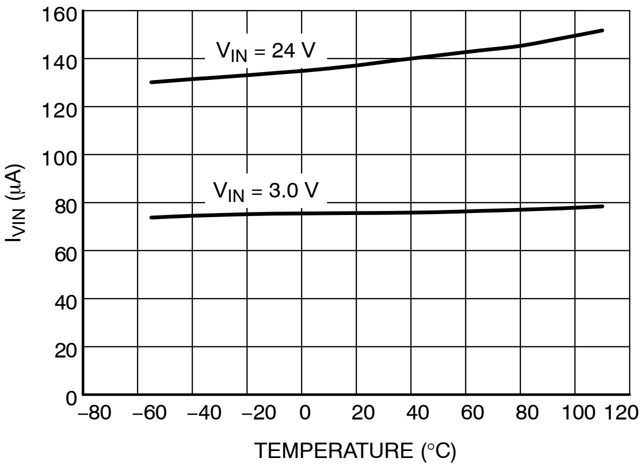


Figure 12. V_{IN} Controller Current vs. Temperature (EN = V_{CC})

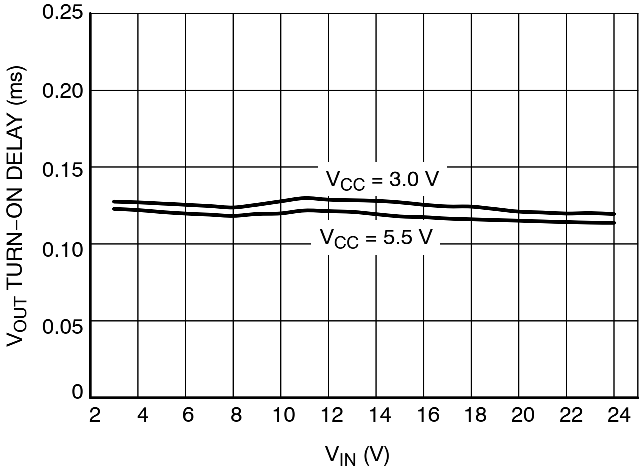


Figure 13. Output Turn−On Delay vs. Input Voltage

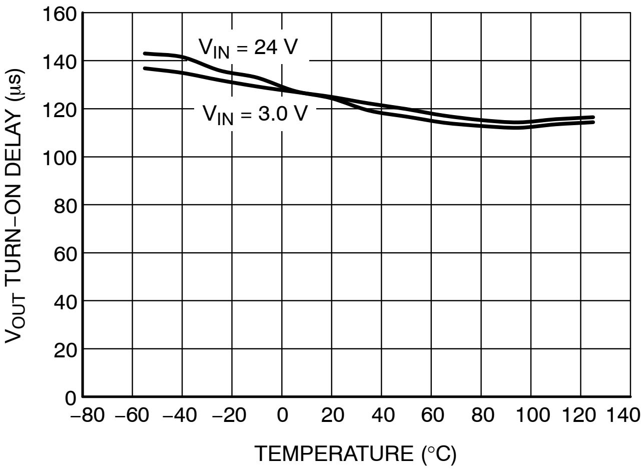


Figure 14. Output Turn−On Delay vs. Temperature

TYPICAL CHARACTERISTICS

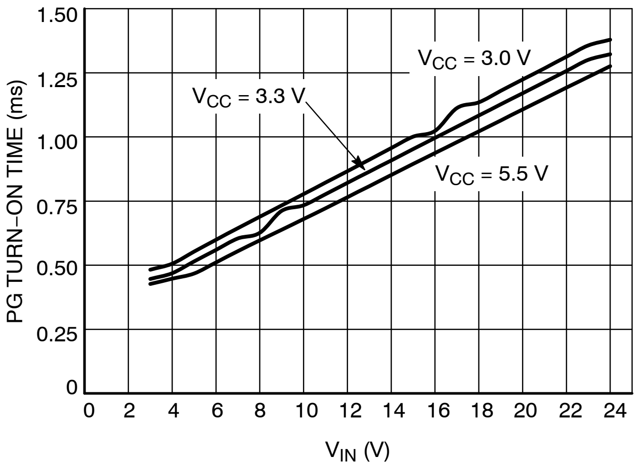


Figure 15. Power Good Turn−On Time vs. Input Voltage

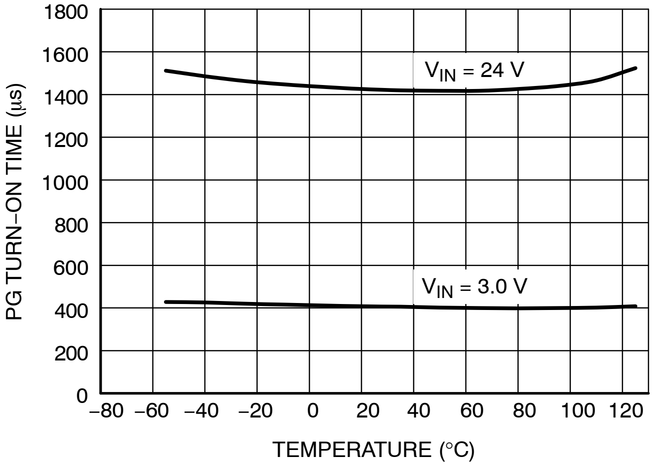


Figure 16. Power Good Turn−On Delay vs. Temperature

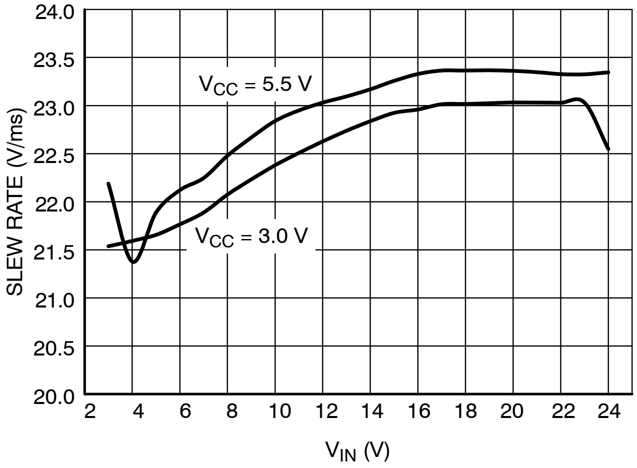


Figure 17. Default Slew Rate vs. Input Voltage (SR = float)

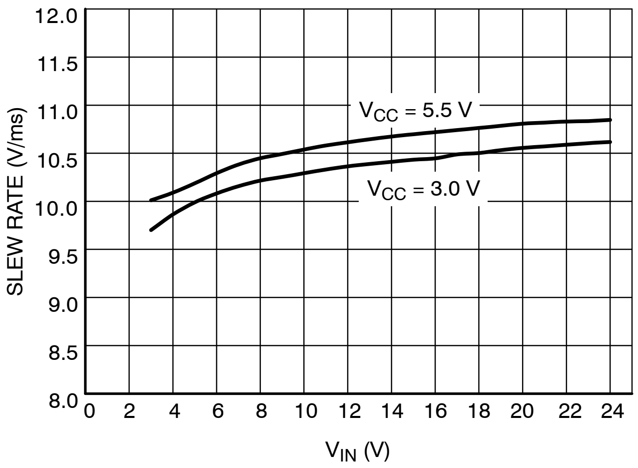


Figure 18. Slew Rate vs. Input Voltage (SR = 10 nF to GND)

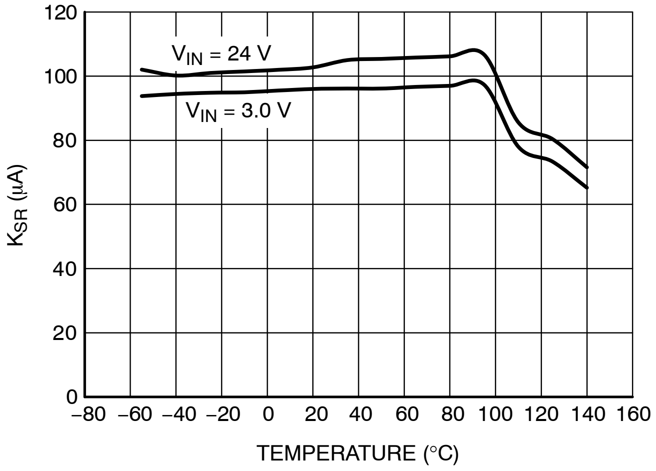


Figure 19. K_{SR} vs. Temperature

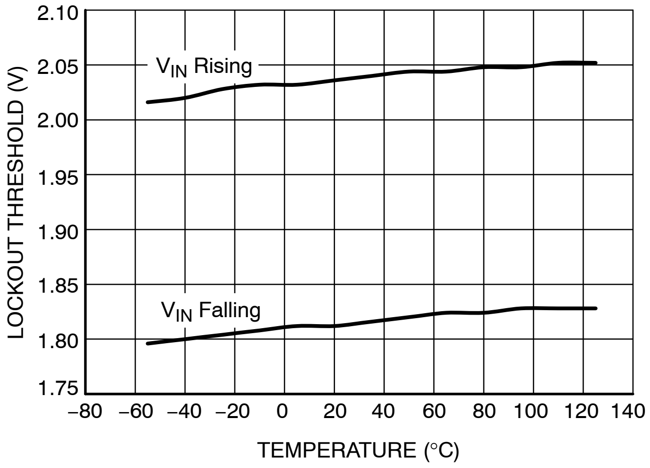


Figure 20. UVLO Trip Voltage vs. Temperature

TYPICAL CHARACTERISTICS

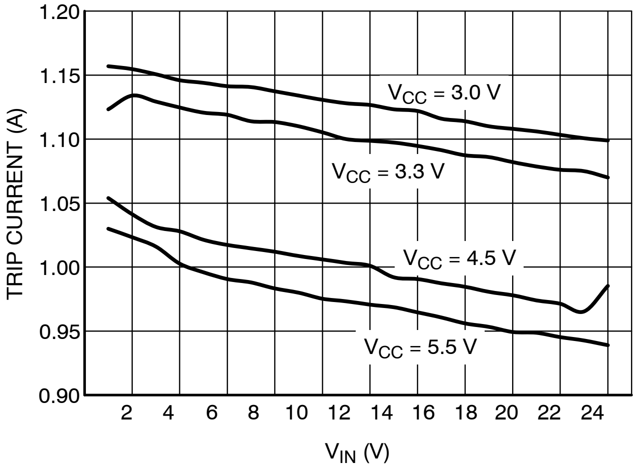


Figure 21. OCP Trip Current vs. Input Voltage (OCP = Open)

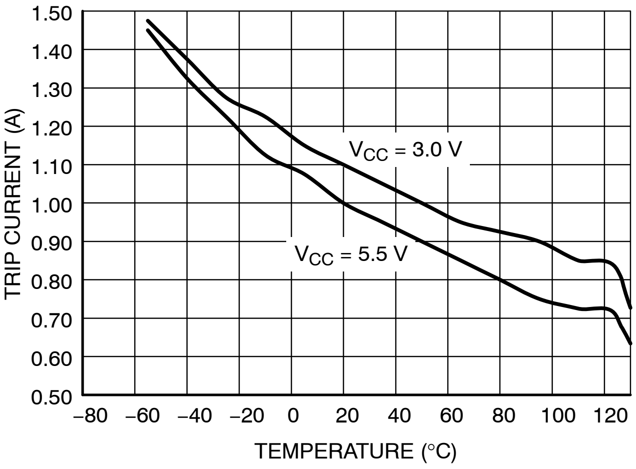


Figure 22. OCP Trip Current vs. Temperature (OCP = Open)

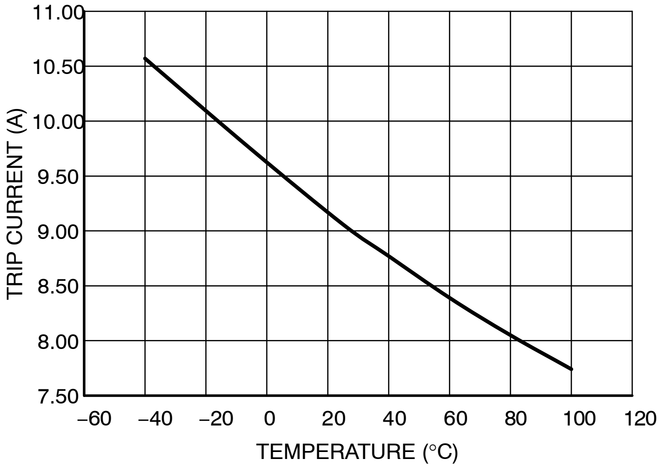


Figure 23. SCP Trip Current vs. Temperature

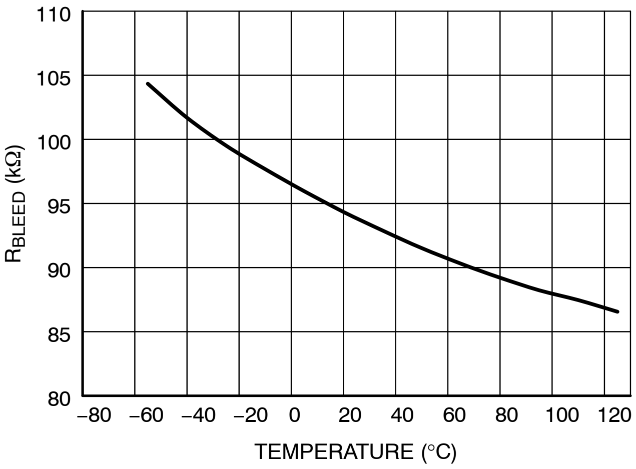


Figure 24. R_{BLEED} vs. Temperature

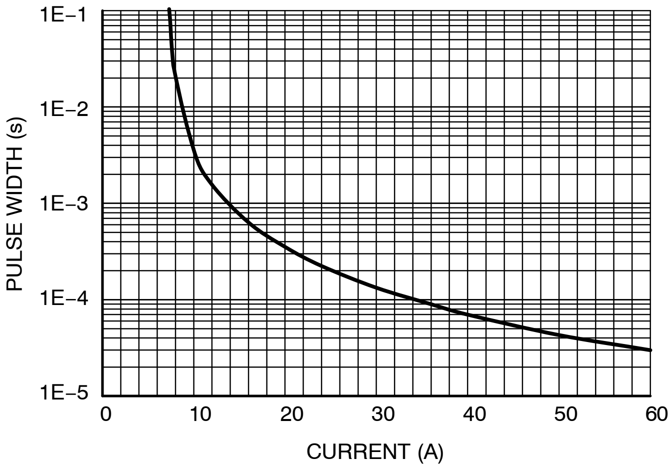


Figure 25. Safe Operating Area Transient Current

APPLICATIONS INFORMATION

Enable Control

The NCP45732 part enables the MOSFET in an active−high configuration. When the EN pin is at a logic high level and the V_{CC} supply pin has an adequate voltage applied, the MOSFET will be enabled. When the EN pin is at a logic low level, the MOSFET will be disabled. An internal pull down resistor to ground on the EN pin ensures that the MOSFET will be disabled when not driven.

Short−Circuit Protection (Hard Short)

The NCP45732 device is equipped with a short−circuit protection that helps protect the part and the system from a sudden high−current event, such as the output, V_{OUT}, being hard−shorted to ground.

Once active, the circuitry monitors the voltage difference between the V_{IN} pin and the V_{OUT} pin. When the difference is equal to the short−circuit protection threshold voltage, the MOSFET is turned off and the load bleed is activated. The part remains off and is latched in the Fault state until EN is toggled or V_{CC} supply voltage is cycled, at which point the MOSFET will be turned on in a controlled fashion with the normal output turn−on delay and slew rate.

Over−Current Protection (Soft Short)

The NCP45732 device is equipped with an over−current protection (OCP) that helps protect the part and the system from a high current event which exceeds the expected operational current (e.g., a soft short).

In the event that the current from the V_{IN} pin to the V_{OUT} pin exceeds the OCP threshold for longer than the blanking time, the MOSFET will shut down and the PG pin is driven low. Like the short−circuit protection, the part remains latched in the Fault state until EN is toggled or V_{CC} supply voltage is cycled, at which point the MOSFET will be turned on in a controlled fashion with the normal output turn−on delay and slew rate.

The over−current trip point is determined by the resistance between the OCP pin and ground. If no over−current protection is needed, then the OCP pin should be tied to ground; if the OCP protection is disabled in this way, the short−circuit protection will still remain active.

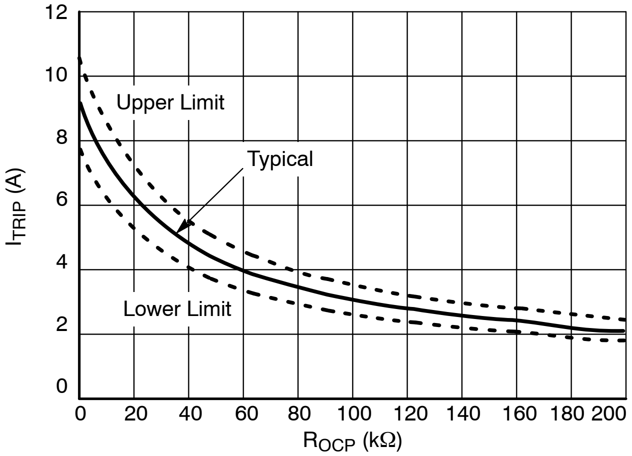


Figure 26. OCP Trip Current vs. R_{OCP} Resistance

Thermal Shutdown

The thermal shutdown of the NCP45732 device protects the part from internally or externally generated excessive temperatures. This circuitry is disabled when EN is not active to reduce standby current. When an over−temperature condition is detected, the MOSFET is turned off and the load bleed is activated.

The part comes out of thermal shutdown when the junction temperature decreases to a safe operating temperature as dictated by the thermal hysteresis. Upon exiting a thermal shutdown state, and if EN remains active, the MOSFET will be turned on in a controlled fashion with the normal output turn−on delay and slew rate.

Under Voltage Lockout

The under voltage lockout of the NCP45732 device turns the MOSFET off and activates the load bleed when the input voltage, V_{IN}, drops below the under voltage lockout threshold. This circuitry is disabled when EN is not active to reduce standby current.

If the V_{IN} voltage rises above the under voltage lockout threshold, and EN remains active, the MOSFET will be turned on in a controlled fashion with the normal output turn−on delay and slew rate.

Power Good

The NCP45732 device has a power good output (PG) that can be used to indicate when the gate of the MOSFET is fully charged. The PG pin is an active−high, open−drain output that requires an external pull up resistor, R_{PG}, greater than or equal to 100 kΩ to an external voltage source, V_{TERM}, that is compatible with input levels of all devices connected to this pin, as shown in Figure 27.

The power good output can be used as the enable signal for other active−high devices in the system, as shown in Figure 27. This allows for guaranteed by design power sequencing and reduces the number of enable signals needed from the system controller. If the power good feature is not used in the application, the PG pin should be tied to GND.

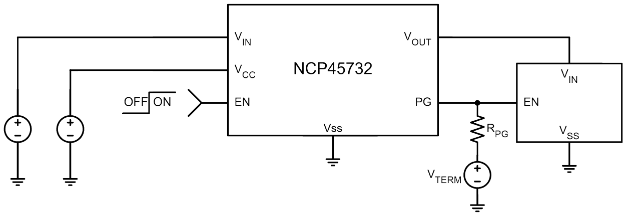


Figure 27. Guaranteed−by−Design Power Sequencing Example

Slew Rate Control

The NCP45732 device is equipped with controlled output slew rate which provides soft start functionality. This limits the inrush current caused by capacitor charging and enables these devices to be used in hot swapping applications.

The slew rate can be decreased with an external capacitor added between the SR pin and ground. With an external capacitor present, the slew rate can be determined by the following equation:

$$\text{Slew Rate} = \frac{K_{SR}}{C_{SR}} \ [\text{V/s}] \qquad \text{(eq. 1)}$$

where K_{SR} is the specified slew rate control constant, found in Table 4, and C_{SR} is the capacitor added between the SR pin and ground. Note that the slew rate of the device will always be the lower of the default slew rate and the adjusted slew rate. Therefore, if the C_{SR} is not large enough to decrease the slew rate more than the specified default value, the slew rate of the device will be the default value.

Capacitive Load

The peak in−rush current associated with the initial charging of the application load capacitance needs to stay below the specified I_{max}. C_L (capacitive load) should be less then C_{max} as defined by the following equation:

$$C_{max} = \frac{I_{max}}{SR_{typ}} \qquad \text{(eq. 2)}$$

where I_{max} is the maximum load current, and SR_{typ} is the typical default slew rate when no external load capacitor is added to the SR pin.

OFF TO ON TRANSITION ENERGY DISSIPATION

The energy dissipation due to load current traveling from V_{IN} to V_{OUT} is very low during steady state operation due to the low R_{ON}. When the EN signal is asserted high, the load switch transitions from an OFF state to an ON state. During this time, the resistance from V_{IN} to V_{OUT} transitions from high impedance to R_{ON}, and additional energy is dissipated in the device for a short period of time. The worst case energy dissipated during the OFF to ON transition can be approximated by the following equation:

$$E = 0.5 \cdot V_{IN}(I_{INRUSH} + 0.8 \cdot I_{LOAD}) \cdot dt \qquad \text{(eq. 3)}$$

where V_{IN} is the voltage on the V_{IN} pin, I_{INRUSH} is the inrush current caused by capacitive loading on V_{OUT}, and dt is the time it takes V_{OUT} to rise from 0 V to V_{IN}. I_{INRUSH} can be calculated using the following equation:

$$I_{INRUSH} = \frac{dv}{dt} \cdot C_L \qquad \text{(eq. 4)}$$

where dv/dt is the programmed slew rate, and C_L is the capacitive loading on V_{OUT}. To prevent thermal lockout or damage to the device, the energy dissipated during the OFF to ON transition should be limited to E_{TRANS} listed in the operating ranges table.

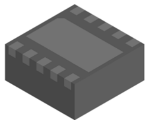
ecoSwitch LAYOUT GUIDELINES

Electrical Layout Considerations

Correct physical PCB layout is important for proper low noise accurate operation of all ecoSwitch products.

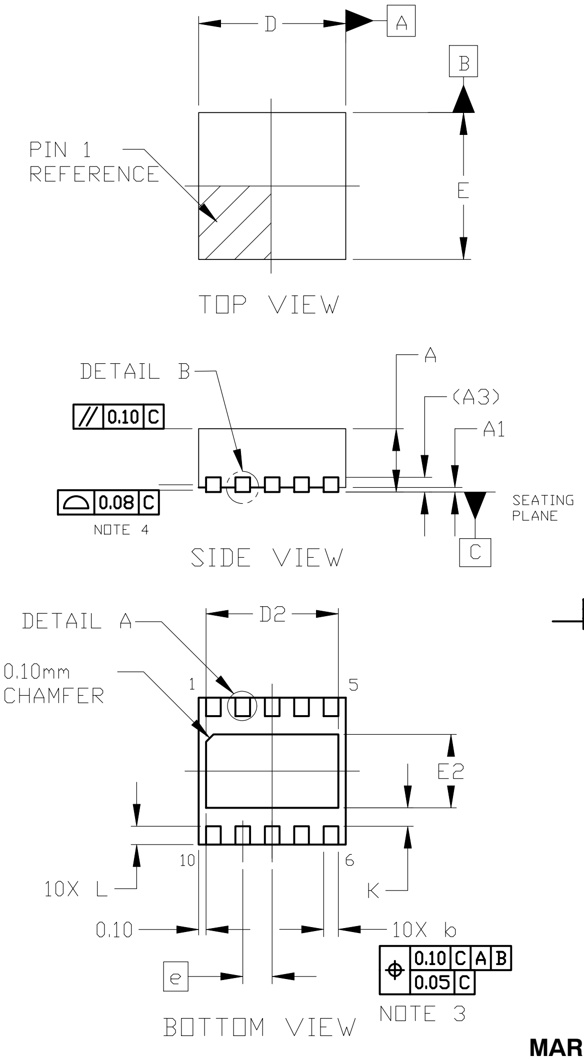
Power Planes: The ecoSwitch is optimized for extremely low R_{ON} resistance, however, improper PCB layout can substantially increase source to load series resistance by adding PCB board parasitic resistance. Solid connections to the V_{IN} and V_{OUT} pins of the ecoSwitch to copper planes should be used to achieve low series resistance and good thermal dissipation. The ecoSwitch requires ample heat dissipation for correct thermal lockout operation. The internal FET dissipates load condition dependent amounts of power in the milliseconds following the rising edge of enable, and providing good thermal conduction from the packaging to the board is critical. The amount of heat spreading available to the part affects the maximum OCP threshold. Higher self−heating will cause the OCP trip point to decrease. Direct coupling of V_{IN} to V_{OUT} should be avoided, as this will adversely affect slew rates. The number and location of pins for specific ecoSwitch products may vary.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

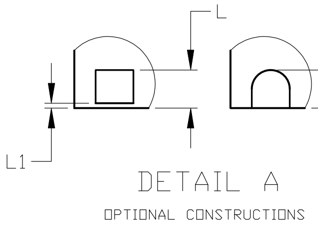


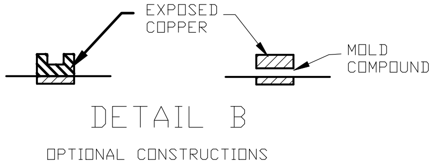
DFN10 2x2, 0.4P
CASE 506FB
ISSUE O

DATE 18 MAR 2021

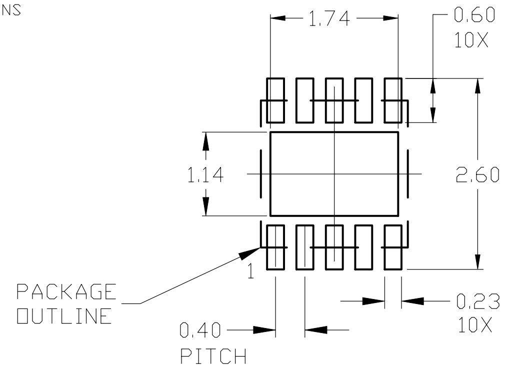


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.





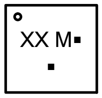
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	—	0.05
A3	0.20 REF		
b	0.15	0.20	0.25
D	1.90	2.00	2.10
D2	1.60	1.70	1.80
E	1.90	2.00	2.10
E2	0.90	1.00	1.10
e	0.40 BSC		
K	0.25 REF		
L	0.20	0.25	0.30
L1	—	—	0.15



RECOMMENDED MOUNTING FOOTPRINT

For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XX	= Specific Device Code
M	= Month Code
▪	= Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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