

Gate Drive Optocoupler, High Noise Immunity, 1.0 A Output Current

FOD3150

Description

The FOD3150 is a 1.0 A Output Current Gate Drive Optocoupler, capable of driving most 800 V / 20 A IGBT / MOSFET. It is ideally suited for fast switching driving of power IGBT and MOSFETs used in motor control inverter applications, and high performance power system.

It utilizes ON Semiconductor patented coplanar packaging technology, Optoplanar[®], and optimized IC design to achieve high noise immunity, characterized by high common mode rejection.

It consists of a gallium aluminum arsenide (AlGaAs) light emitting diode optically coupled to an integrated circuit with a high-speed driver for push-pull MOSFET output stage.

Features

- High Noise Immunity characterized by 20 kV/μs minimum Common Mode Rejection
- Use of P-channel MOSFETs at Output Stage Enables Output Voltage Swing close to the Supply Rail
- Wide Supply Voltage Range from 15 V to 30 V
- Fast Switching Speed
 - ◆ 500 ns maximum Propagation Delay
 - ◆ 300 ns maximum Pulse Width Distortion
- Under Voltage LockOut (UVLO) with Hysteresis
- Extended Industrial Temperature Range, -40°C to 100°C Temperature Range
- Safety and Regulatory Approvals
 - ◆ UL1577, 5000 V_{RMS} for 1 minute
 - ◆ DIN EN/IEC60747-5-5
- >8.0 mm Clearance and Creepage Distance (Option 'T')
- This is a Pb-Free Device

Applications

- Industrial Inverter
- Uninterruptible Power Supply
- Induction Heating
- Isolated IGBT/Power MOSFET Gate Drive

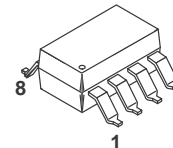
Related Resources

- FOD3120, 2.5 A Output Current, Gate Drive Optocoupler Datasheet
- www.onsemi.com/products/opto/

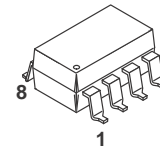


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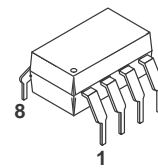
www.onsemi.com



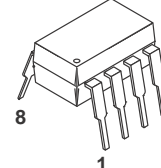
PDIP8 GW
CASE 709AD



PDIP8 GW
CASE 709AC

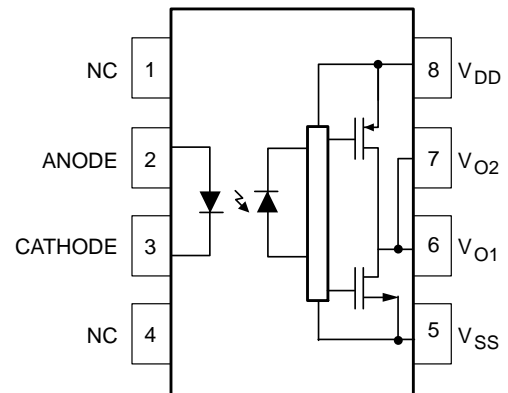


PDIP8 6.6x3.81, 2.54P
CASE 646BW



PDIP8 9.655x6.6, 2.54P
CASE 646CQ

FUNCTIONAL BLOCK DIAGRAM



Note: A 0.1 μF bypass capacitor must be connected between pins 5 and 8.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 12 of this data sheet.

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Table 1. TRUTH TABLE

LED	$V_{DD} - V_{SS}$ "Positive Going" (Turn-on)	$V_{DD} - V_{SS}$ "Negative Going" (Turn-off)	V_O
Off	0 V to 30 V	0 V to 30 V	Low
On	0 V to 11 V	0 V to 9.7 V	Low
On	11 V to 14 V	9.7 V to 12.7 V	Transition
On	14 V to 30 V	12.7 V to 30 V	High

Table 2. PIN DEFINITIONS

Pin #	Name	Description
1	NC	Not Connected
2	Anode	LED Anode
3	Cathode	LED Cathode
4	NC	Not Connected
5	V_{SS}	Negative Supply Voltage
6	V_{O2}	Output Voltage 2 (internally connected to V_{O1})
7	V_{O1}	Output Voltage 1
8	V_{DD}	Positive Supply Voltage

Table 3. SAFETY AND INSULATION RATINGS

As per IEC 60747-5-2. This optocoupler is suitable for "safe electrical insulation" only within the safety limit data. Compliance with the safety ratings shall be ensured by means of protective circuits.

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Installation Classifications per DIN VDE 0110/1.89 Table 1				
	For Rated Main Voltage < 150 Vrms		I-IV		
	For Rated Main Voltage < 300 Vrms		I-IV		
	For Rated Main Voltage < 450 Vrms		I-III		
	For Rated Main Voltage < 600 Vrms		I-III		
	Climatic Classification		55/100/21		
	Pollution Degree (DIN VDE 0110/1.89)		2		
CTI	Comparative Tracking Index	175			
V_{PR}	Input to Output Test Voltage, Method b, $V_{IORM} \times 1.875 = V_{PR}$, 100% Production Test with $t_m = 1$ s, Partial Discharge < 5 pC	1669			
	Input to Output Test Voltage, Method a, $V_{IORM} \times 1.5 = V_{PR}$, Type and Sample Test with $t_m = 60$ s, Partial Discharge < 5 pC	1335			
V_{IORM}	Max Working Insulation Voltage	890			V_{peak}
V_{IOTM}	Highest Allowable Over Voltage	6000			V_{peak}
	External Creepage	8			mm
	External Clearance	7.4			mm
	External Clearance (for Option T-0.4" Lead Spacing)	10.16			mm
	Insulation Thickness	0.5			mm
T_{Case}	Safety Limit Values – Maximum Values Allowed in the Event of a Failure Case Temperature	150			°C
$I_{S,INPUT}$	Input Current	25			mA
$P_{S,OUTPUT}$	Output Power (Duty Factor $\leq 2.7\%$)	250			mW
R_{IO}	Insulation Resistance at T_S , $V_{IO} = 500$ V	10^9			Ω

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Table 4. ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise specified.)

Symbol	Parameter	Value	Units
T_{STG}	Storage Temperature	-55 to +125	$^\circ\text{C}$
T_{OPR}	Operating Temperature	-40 to +100	$^\circ\text{C}$
T_J	Junction Temperature	-40 to +125	$^\circ\text{C}$
T_{SOL}	Lead Wave Solder Temperature (refer to page 12 for reflow solder profile)	260 for 10 sec	$^\circ\text{C}$
$I_{F(AVG)}$	Average Input Current	25	mA
V_R	Reverse Input Voltage	5	V
$I_{O(PEAK)}$	Peak Output Current ⁽¹⁾	1.5	A
$V_{DD} - V_{SS}$	Supply Voltage	0 to 35	V
$V_{O(PEAK)}$	Peak Output Voltage	0 to V_{DD}	V
$t_{R(IN)}, t_{F(IN)}$	Input Signal Rise and Fall Time	500	ns
PD_I	Input Power Dissipation ^{(2) (4)}	45	mW
PD_O	Output Power Dissipation ^{(3) (4)}	250	mW

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Maximum pulse width = 10 μs , maximum duty cycle = 0.2 %.
2. Derate linearly above 87 $^\circ\text{C}$, free air temperature at a rate of 0.77 mW/ $^\circ\text{C}$.
3. No derating required across temperature range.
4. Functional operation under these conditions is not implied. Permanent damage may occur if the device is subjected to conditions outside these ratings.

Table 5. RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Units
T_A	Ambient Operating Temperature	-40 to +100	$^\circ\text{C}$
$V_{DD} - V_{SS}$	Power Supply	15 to 30	V
$I_{F(ON)}$	Input Current (ON)	7 to 16	mA
$V_{F(OFF)}$	Input Voltage (OFF)	0 to 0.8	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 6. ISOLATION CHARACTERISTICS

Apply over all recommended conditions, typical value is measured at $T_A = 25^\circ\text{C}$

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{ISO}	Input-Output Isolation Voltage	$T_A = 25^\circ\text{C}$, R.H. < 50 %, $t = 1.0$ minute, $I_{I-O} \leq 10 \mu\text{A}$, 50 Hz ^{(5) (6)}	5000			V_{RMS}
R_{ISO}	Isolation Resistance	$V_{I-O} = 500 \text{ V}$ ⁽⁵⁾		10^{11}		Ω
C_{ISO}	Isolation Capacitance	$V_{I-O} = 0 \text{ V}$, Frequency = 1.0 MHz ⁽⁵⁾		1		pF

5. Device is considered a two terminal device: pins 2 and 3 are shorted together and pins 5, 6, 7 and 8 are shorted together.
6. 5,000 V_{RMS} for 1 minute duration is equivalent to 6,000 V_{ACRMS} for 1 second duration.

Table 7. ELECTRICAL CHARACTERISTICS

Apply over all recommended conditions, typical value is measured at $V_{DD} = 30 \text{ V}$, $V_{SS} = \text{Ground}$, $T_A = 25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_F	Input Forward Voltage	$I_F = 10 \text{ mA}$	1.2	1.5	1.8	V
$\Delta(V_F / T_A)$	Temperature Coefficient of Forward Voltage			-1.8		mV/ $^\circ\text{C}$
BV_R	Input Reverse Breakdown Voltage	$I_R = 10 \mu\text{A}$	5			V

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Table 7. ELECTRICAL CHARACTERISTICS (continued)

Apply over all recommended conditions, typical value is measured at $V_{DD} = 30\text{ V}$, $V_{SS} = \text{Ground}$, $T_A = 25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
C_{IN}	Input Capacitance	$f = 1\text{ MHz}$, $V_F = 0\text{ V}$		60		pF
I_{OH}	High Level Output Current ⁽⁷⁾	$V_O = V_{DD} - 0.75\text{ V}$	0.2			A
		$V_O = V_{DD} - 4\text{ V}$	1.0			
I_{OL}	Low Level Output Current ⁽⁷⁾	$V_O = V_{DD} + 0.75\text{ V}$	0.2			A
		$V_O = V_{DD} + 4\text{ V}$	1.0			
V_{OH}	High Level Output Voltage	$I_F = 10\text{ mA}$, $I_O = -1\text{ A}$	$V_{DD} - 6\text{ V}$	$V_{DD} - 4\text{ V}$		V
		$I_F = 10\text{ mA}$, $I_O = -100\text{ mA}$	$V_{DD} - 0.5\text{ V}$	$V_{DD} - 0.1\text{ V}$		
V_{OL}	Low Level Output Voltage	$I_F = 0\text{ mA}$, $I_O = 1\text{ A}$		$V_{SS} + 4\text{ V}$	$V_{SS} + 6\text{ V}$	V
		$I_F = 0\text{ mA}$, $I_O = 100\text{ mA}$		$V_{SS} + 0.1\text{ V}$	$V_{SS} + 0.5\text{ V}$	
I_{DDH}	High Level Supply Current	$V_O = \text{Open}$, $I_F = 7\text{ to }16\text{ mA}$		2.8	5	mA
I_{DDL}	Low Level Supply Current	$V_O = \text{Open}$, $V_F = 0\text{ to }0.8\text{ V}$		2.8	5	mA
I_{FLH}	Threshold Input Current Low to High	$I_O = 0\text{ mA}$, $V_O > 5\text{ V}$		2.3	5.0	mA
V_{FHL}	Threshold Input Voltage High to Low	$I_O = 0\text{ mA}$, $V_O < 5\text{ V}$	0.8			V
V_{UVLO+}	Under Voltage Lockout Threshold	$I_F = 1\text{ mA}$, $V_O > 5\text{ V}$	11	12.7	14	V
V_{UVLO-}		$I_F = 10\text{ mA}$, $V_O < 5\text{ V}$	9.7	11.2	12.7	V
$UVLO_{HYS}$	Under Voltage Lockout Threshold Hysteresis			1.5		V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Maximum pulse width = 10 μs , maximum duty cycle = 0.2 %.

Table 8. SWITCHING CHARACTERISTICS

Apply over all recommended conditions, typical value is measured at $V_{DD} = 30\text{ V}$, $V_{SS} = \text{Ground}$, $T_A = 25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
t_{PHL}	Propagation Delay Time to Logic Low Output	$I_F = 7\text{ mA to }16\text{ mA}$, $R_g = 20\ \Omega$, $C_g = 10\text{ nF}$, $f = 10\text{ kHz}$, Duty Cycle = 50 %	100	275	500	ns
t_{PLH}	Propagation Delay Time to Logic High Output		100	255	500	ns
PWD	Pulse Width Distortion, $ t_{PHL} - t_{PLH} $			20	300	ns
PDD (Skew)	Propagation Delay Difference Between Any Two Parts or Channels, $(t_{PHL} - t_{PLH})$ ⁽⁸⁾			-350	350	ns
t_r	Output Rise Time (10% – 90%)				60	ns
t_f	Output Fall Time (90% – 10%)				60	ns
$t_{UVLO\ ON}$	UVLO Turn On Delay		$I_F = 10\text{ mA}$, $V_O > 5\text{ V}$		1.6	
$t_{UVLO\ OFF}$	UVLO Turn Off Delay	$I_F = 10\text{ mA}$, $V_O < 5\text{ V}$		0.4		μs
$ CM_H $	Common Mode Transient Immunity at Output High	$T_A = 25^\circ\text{C}$, $V_{DD} = 30\text{ V}$, $I_F = 7\text{ to }16\text{ mA}$, $V_{CM} = 2000\text{ V}$ ⁽⁹⁾	20	50		kV/ μs
$ CM_L $	Common Mode Transient Immunity at Output Low	$T_A = 25^\circ\text{C}$, $V_{DD} = 30\text{ V}$, $V_F = 0\text{ V}$, $V_{CM} = 2000\text{ V}$ ⁽¹⁰⁾	20	50		kV/ μs

8. The difference between t_{PHL} and t_{PLH} between any two FOD3150 parts under same test conditions.

9. Common mode transient immunity at output high is the maximum tolerable negative dV_{cm}/dt on the trailing edge of the common mode impulse signal, V_{cm} , to assure that the output will remain high (i.e., $V_O > 15.0\text{ V}$).

10. Common mode transient immunity at output low is the maximum tolerable positive dV_{cm}/dt on the leading edge of the common pulse signal, V_{cm} , to assure that the output will remain low (i.e., $V_O < 1.0\text{ V}$).

TYPICAL PERFORMANCE CURVES

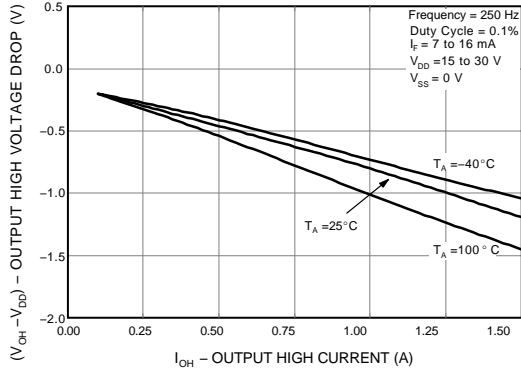


Figure 1. Output High Voltage Drop vs. Output High Current

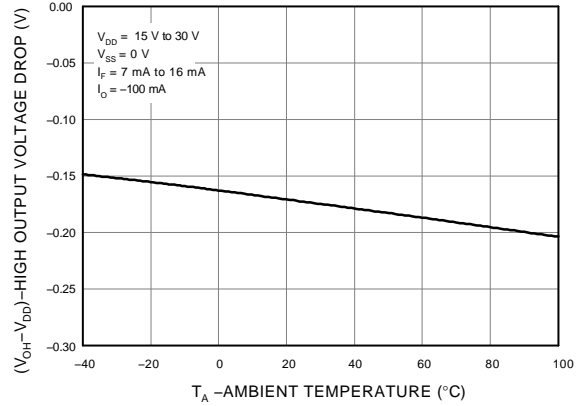


Figure 2. Output High Voltage Drop vs. Ambient Temperature

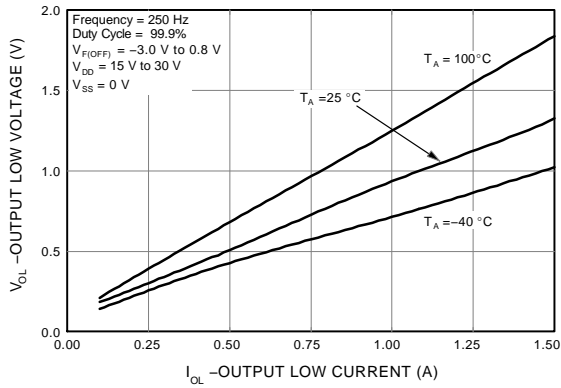


Figure 3. Output Low Voltage vs. Output Low Current

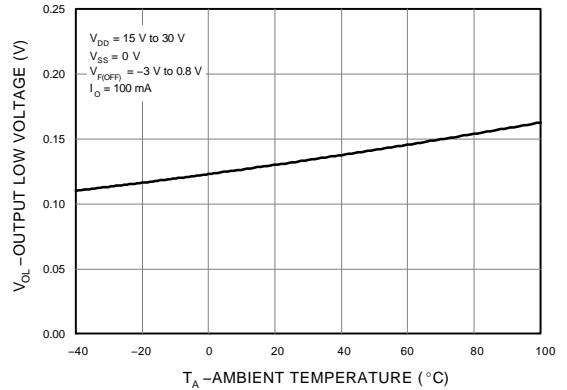


Figure 4. Output Low Voltage vs. Ambient Temperature

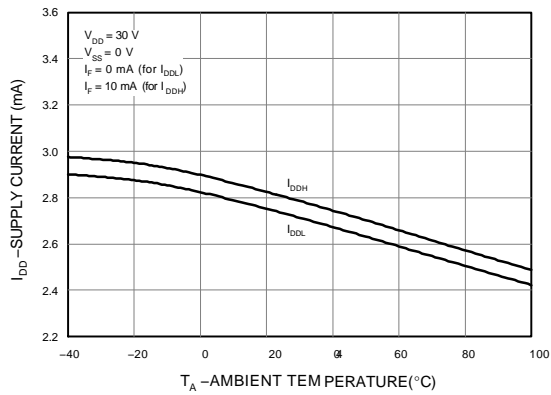


Figure 5. Supply Current vs. Ambient Temperature

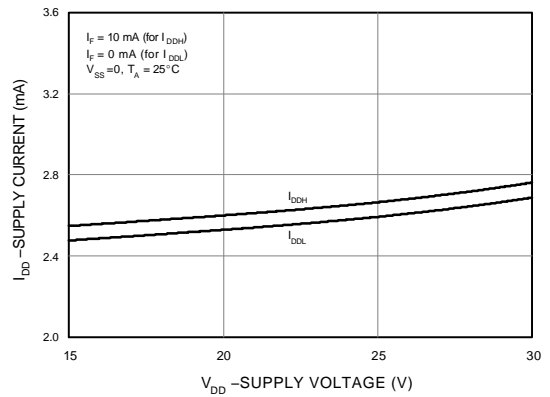


Figure 6. Supply Current vs. Supply Voltage

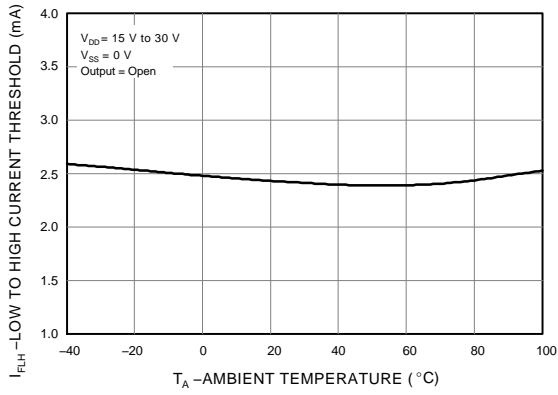


Figure 7. Low to High Input Current Threshold vs. Ambient Temperature

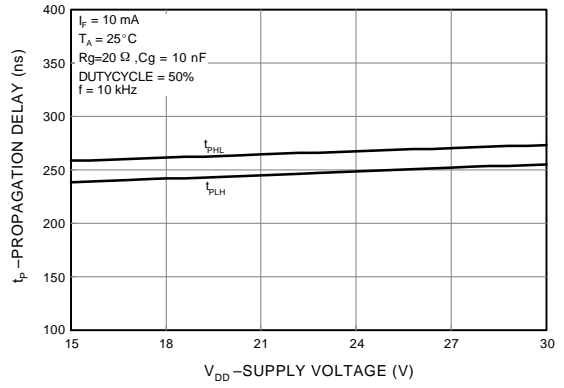


Figure 8. Propagation Delay vs. Supply Voltage

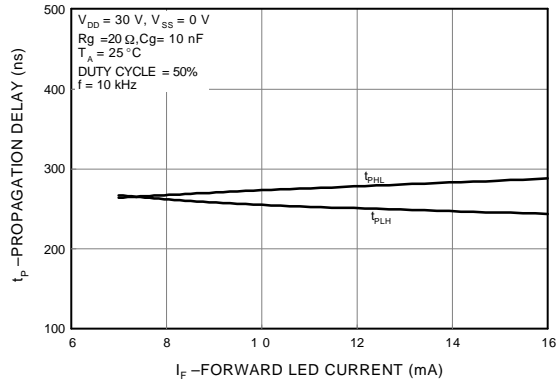


Figure 9. Propagation Delay vs. LED Forward Current

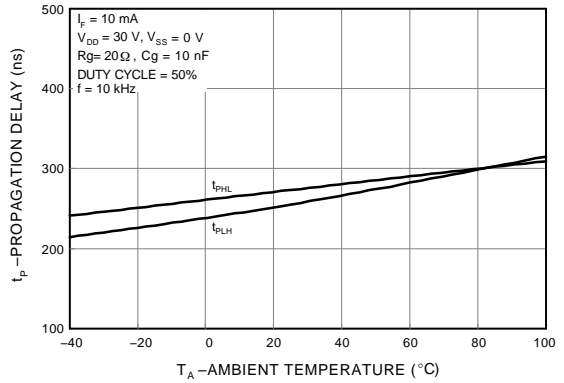


Figure 10. Propagation Delay vs. Ambient Temperature

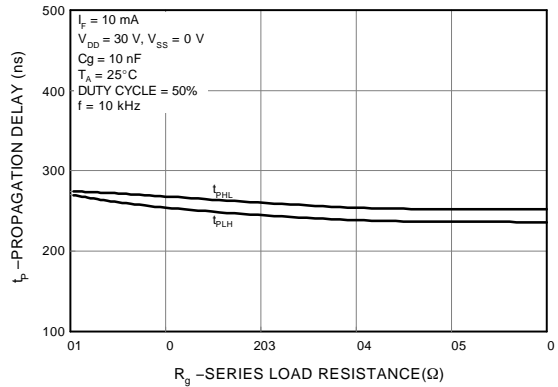


Figure 11. Propagation Delay vs. Series Load Resistance

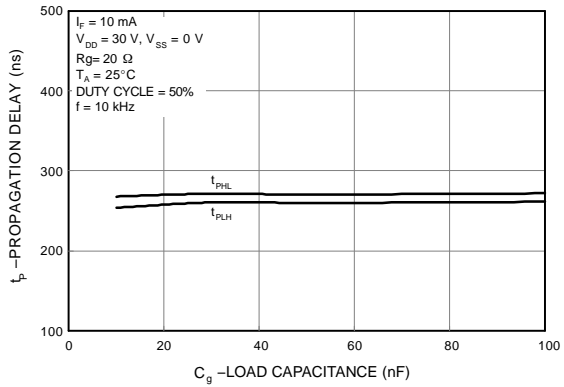


Figure 12. Propagation Delay vs. Load Capacitance

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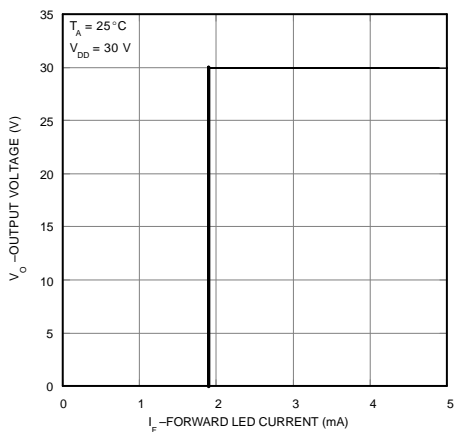


Figure 13. Transfer Characteristics

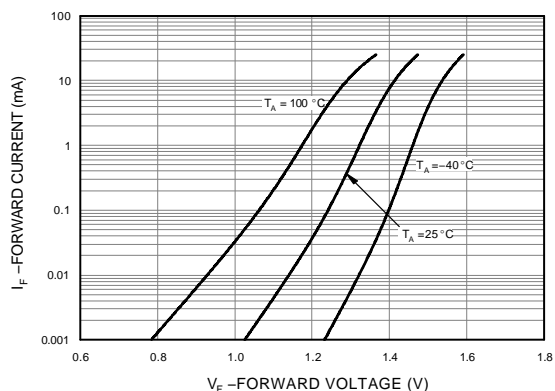


Figure 14. Input Forward Current vs. Forward Voltage

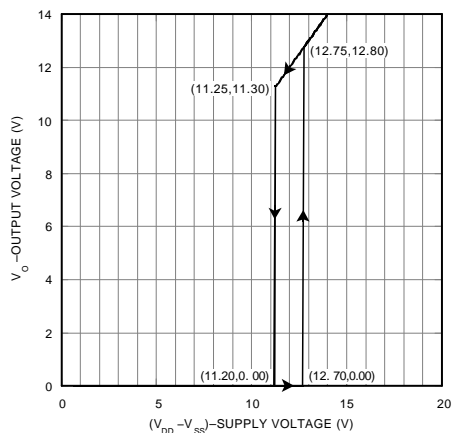


Figure 15. Under Voltage Lockout

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TEST CIRCUIT

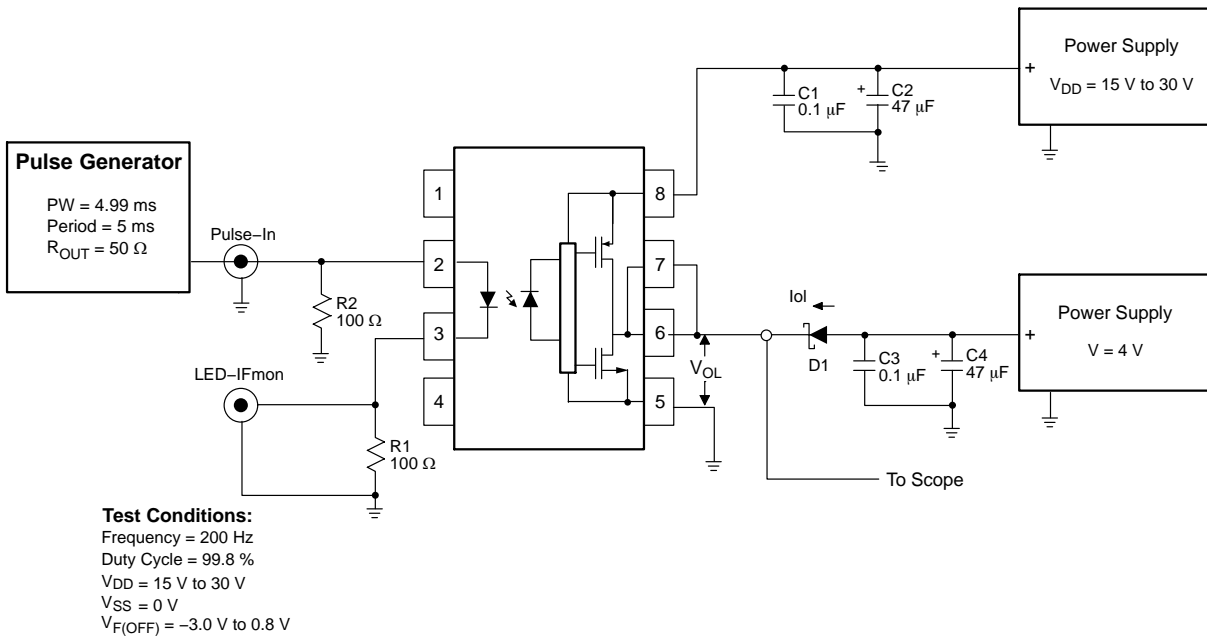


Figure 16. I_{OL} Test Circuit

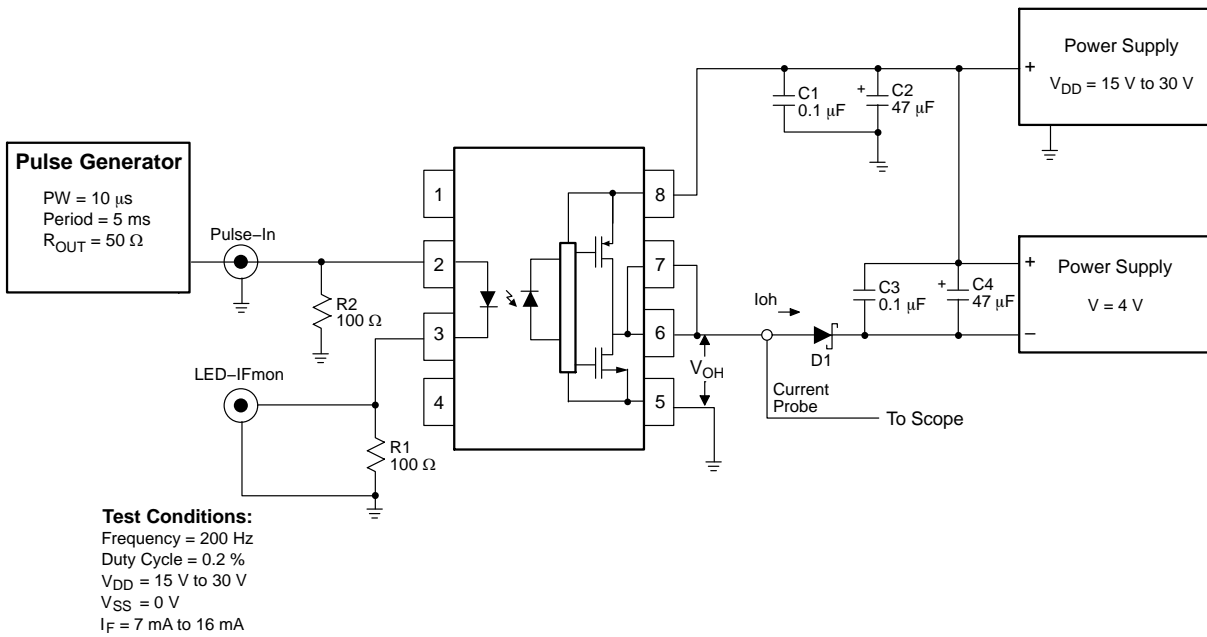


Figure 17. I_{OH} Test Circuit

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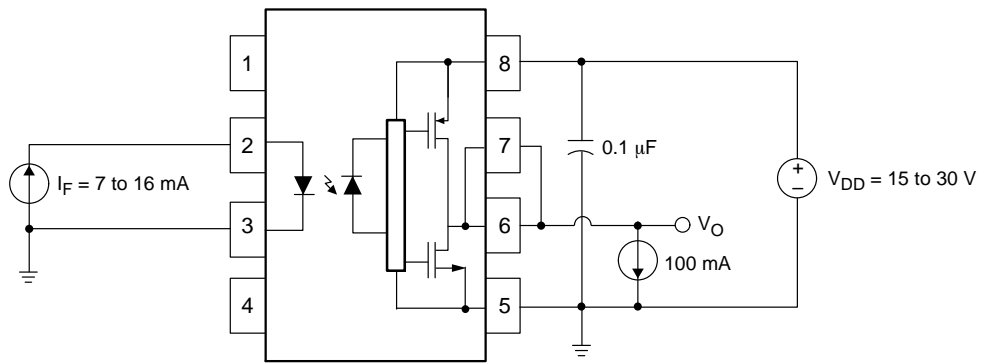


Figure 18. V_{OH} Test Circuit

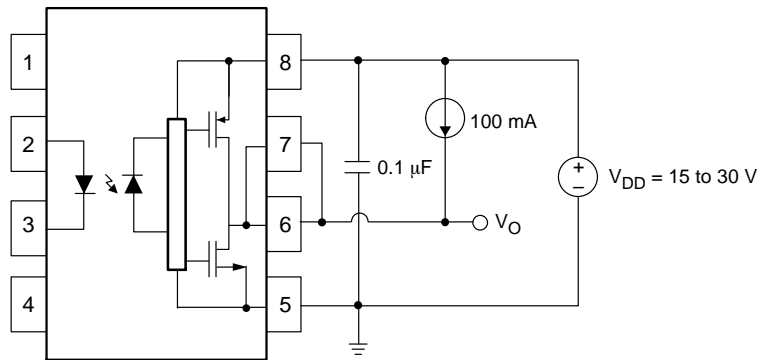


Figure 19. V_{OL} Test Circuit

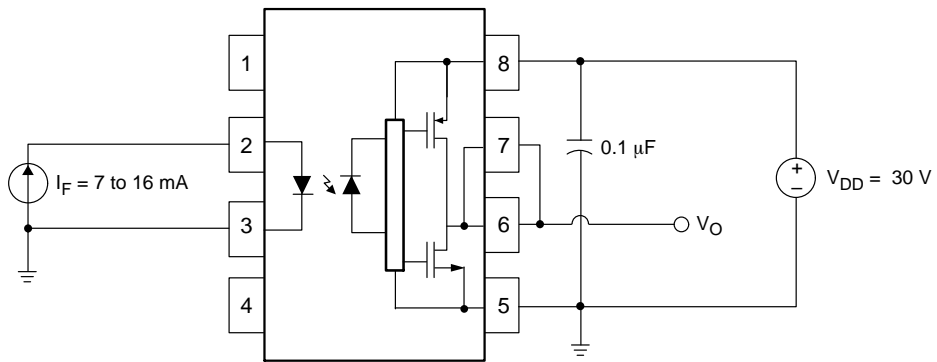


Figure 20. I_{DDH} Test Circuit

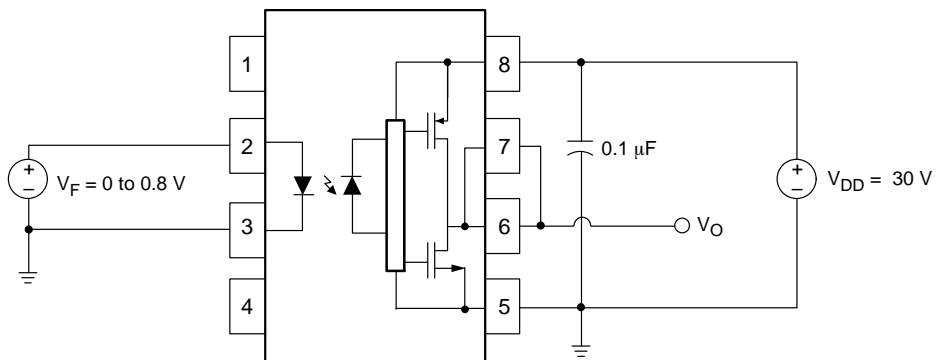


Figure 21. I_{DDL} Test Circuit

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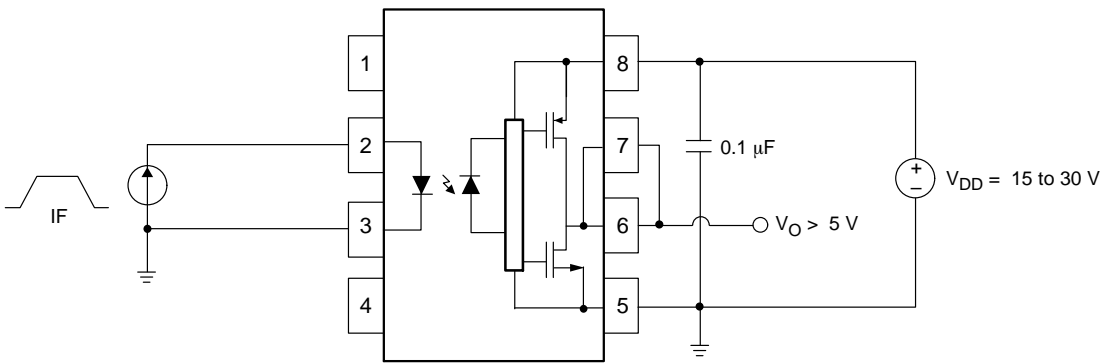


Figure 22. I_{FLH} Test Circuit

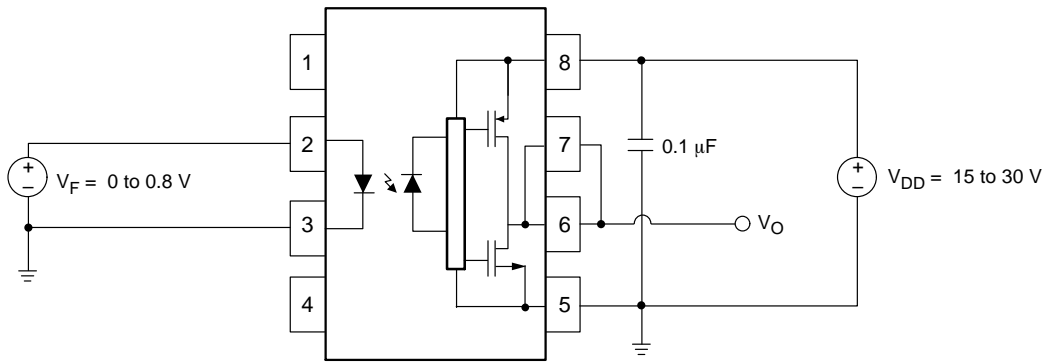


Figure 23. V_{FHL} Test Circuit

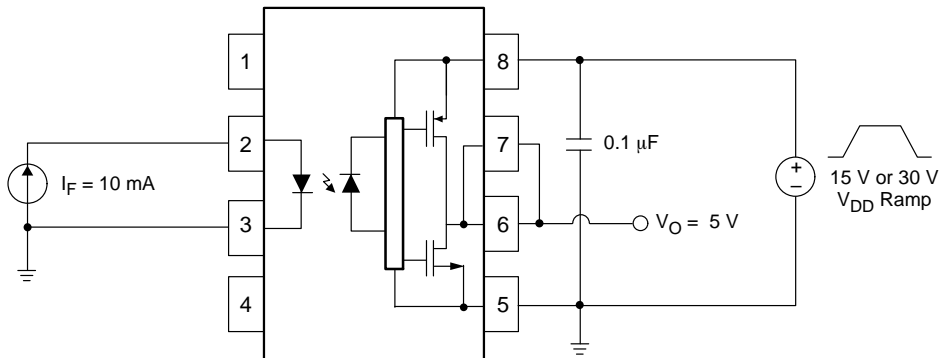


Figure 24. UVLO Test Circuit

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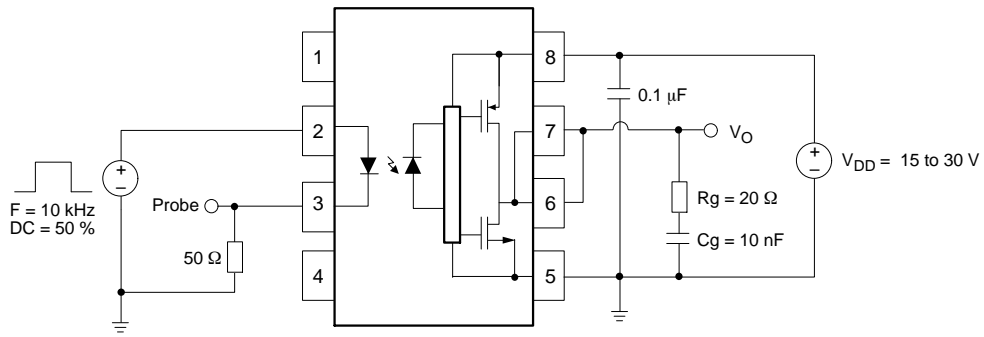


Figure 25. t_{PHL} , t_{PLH} , t_R and t_F Test Circuit and Waveforms

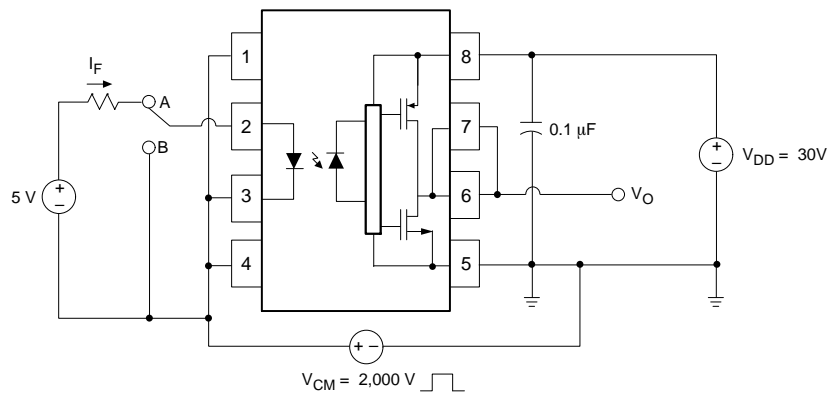
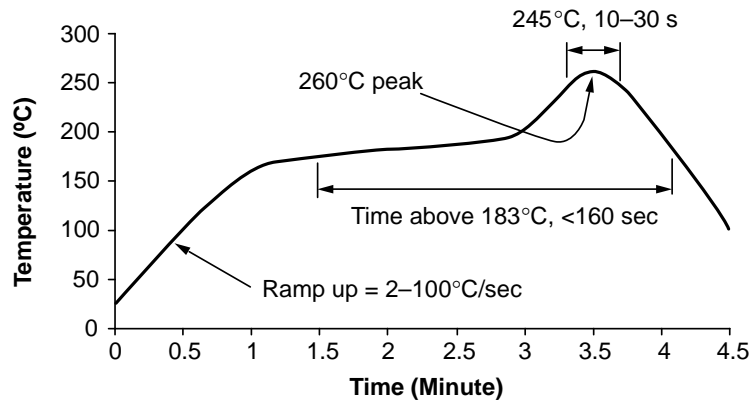


Figure 26. CMR Test Circuit and Waveforms

FOD3150

REFLOW PROFILE



Notes:

- Peak reflow temperature: 260°C (package surface temperature)
- Time of temperature higher than 183°C for 160 seconds or less
- One time soldering reflow is recommended

Figure 27. Reflow Profile

ORDERING INFORMATION

Part Number	Package	Shipping†
FOD3150	DIP 8-Pin	50 / Tube
FOD3150S	SMT 8-Pin (Lead Bend)	50 / Tube
FOD3150SD	SMT 8-Pin (Lead Bend)	1,000 / Tape & Reel
FOD3150V	DIP 8-Pin, IEC60747-5-5 option	50 / Tube
FOD3150SV	SMT 8-Pin (Lead Bend), IEC60747-5-5 option	50 / Tube
FOD3150SDV	SMT 8-Pin (Lead Bend), IEC60747-5-5 option	1,000 / Tape & Reel
FOD3150TV	DIP 8-Pin, 0.4" Lead Spacing, IEC60747-5-5 option	50 / Tube
FOD3150TSV	SMT 8-Pin, 0.4" Lead Spacing, IEC60747-5-5 option	50 / Tube
FOD3150TSR2V	SMT 8-Pin, 0.4" Lead Spacing, IEC60747-5-5 option	700 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D

MARKING INFORMATION

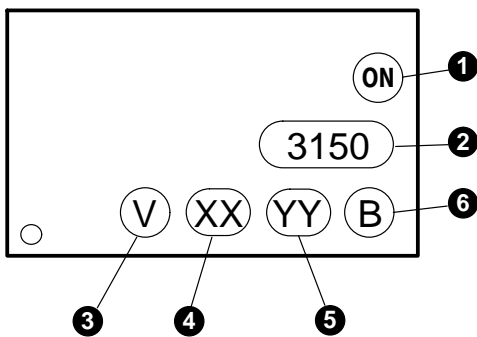


Figure 28. Device Marking

Definitions	
1	ON Semiconductor logo
2	Device number
3	IEC60747-5-5 Option (only appears on component ordered with this option)
4	Two digit year code, e.g., '18'
5	Two digit work week ranging from '01' to '53'
6	Assembly package code

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CARRIER TAPE SPECIFICATIONS

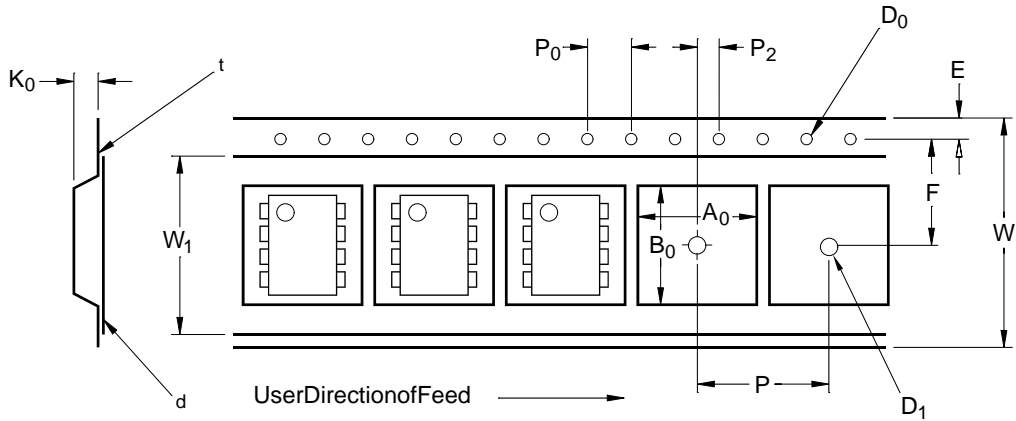


Figure 29. Carrier Tape Specifications

Symbol	Description	Dimension in mm
W	Tape Width	16.0 ± 0.3
t	Tape Thickness	0.30 ± 0.05
P ₀	Sprocket Hole Pitch	4.0 ± 0.1
D ₀	Sprocket Hole Diameter	1.55 ± 0.05
E	Sprocket Hole Location	1.75 ± 0.10
F	Pocket Location	7.5 ± 0.1
P ₂		2.0 ± 0.1
P	Pocket Pitch	12.0 ± 0.1
A ₀	Pocket Dimensions	10.30 ± 0.20
B ₀		10.30 ± 0.20
K ₀		4.90 ± 0.20
W ₁	Cover Tape Width	13.2 ± 0.2
d	Cover Tape Thickness	0.1 max
	Max. Component Rotation or Tilt	10°
R	Min. Bending Radius	30

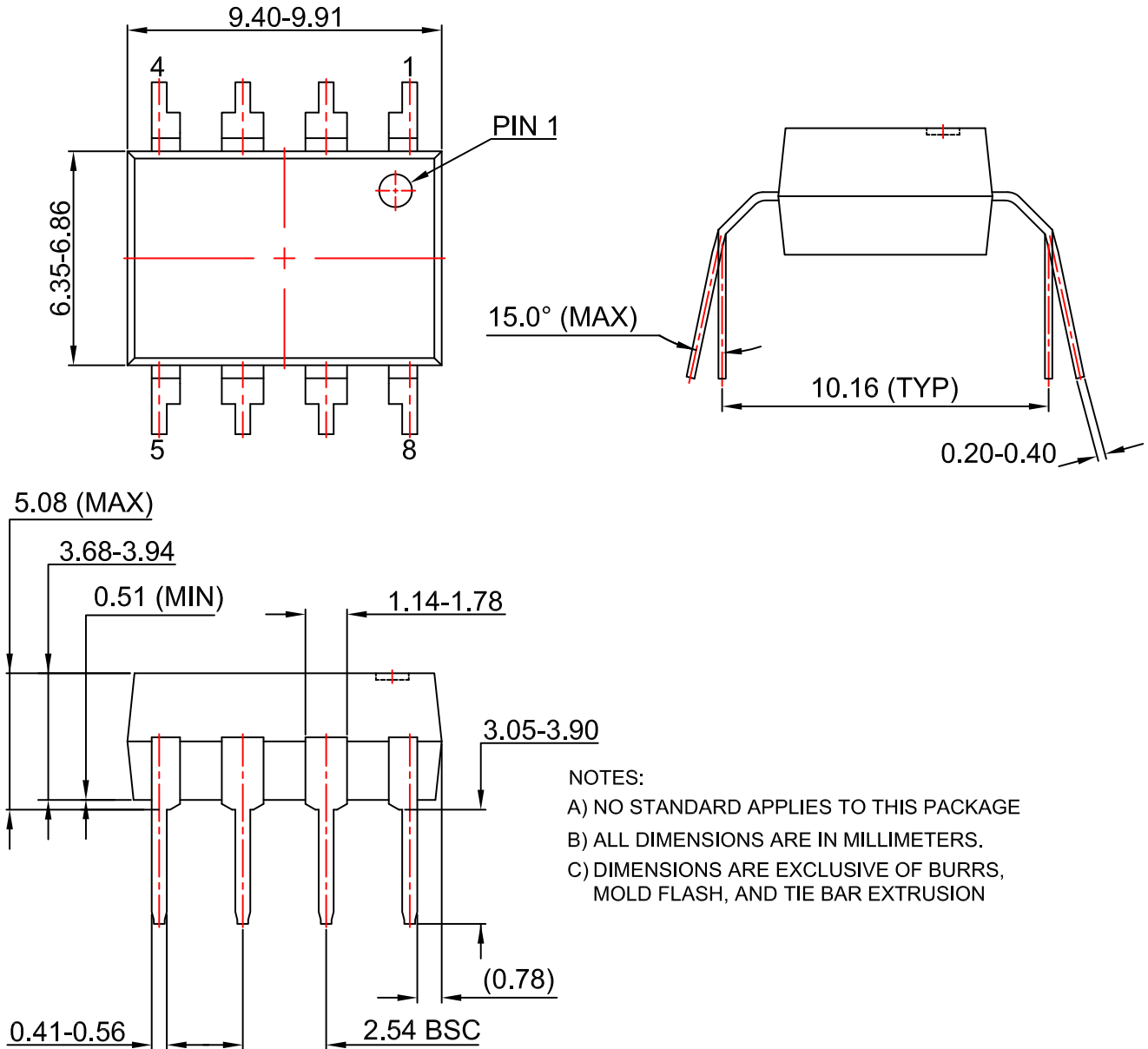
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®



PDIP8 6.6x3.81, 2.54P
CASE 646BW
ISSUE O

DATE 31 JUL 2016



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MECHANICAL CASE OUTLINE

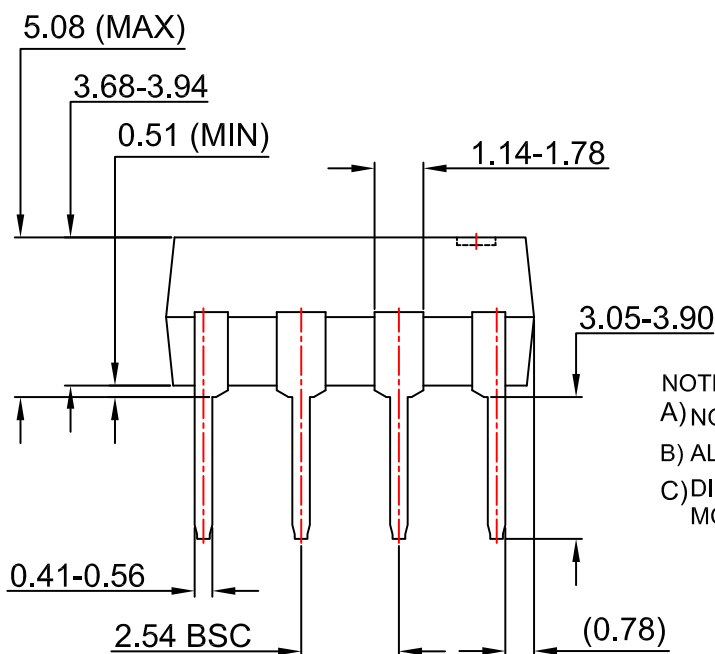
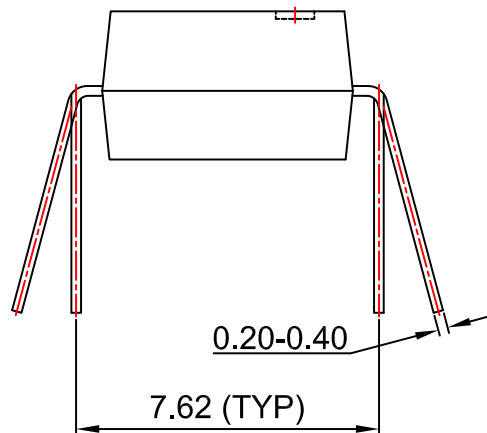
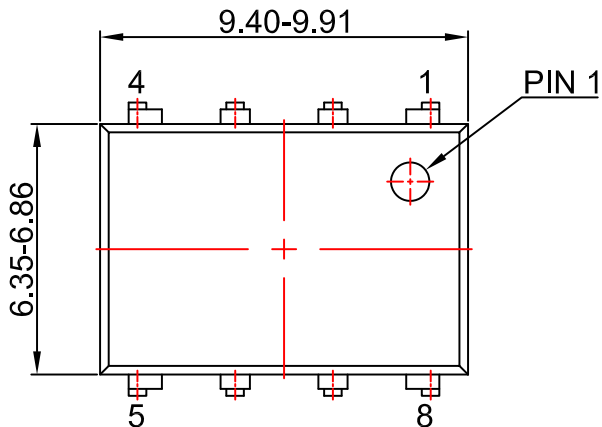
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PDIP8 9.655x6.6, 2.54P
CASE 646CQ
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MECHANICAL CASE OUTLINE

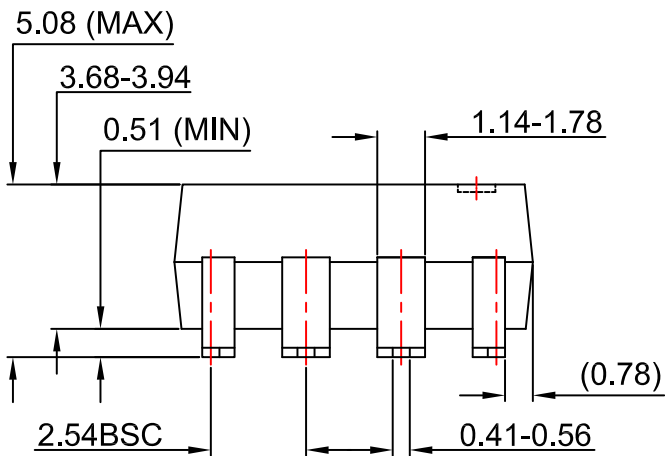
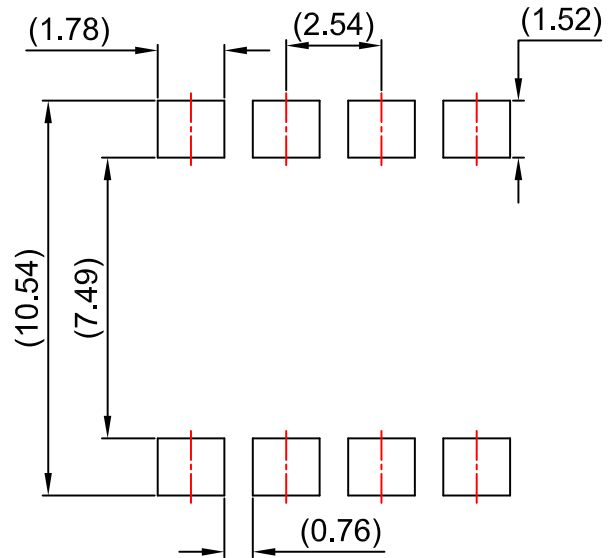
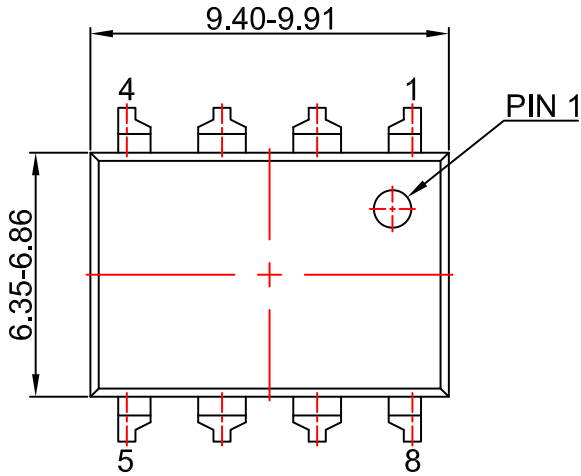
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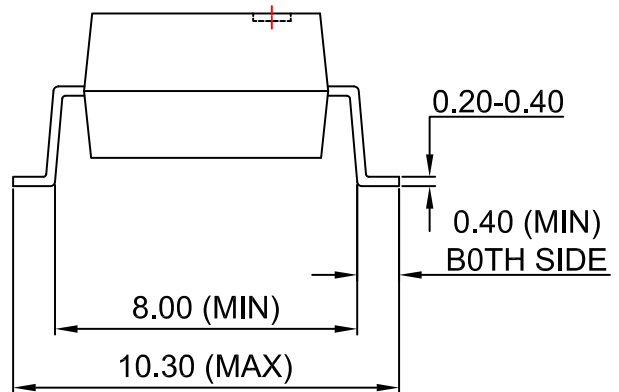


PDIP8 GW
CASE 709AC
ISSUE O

DATE 31 JUL 2016



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MECHANICAL CASE OUTLINE

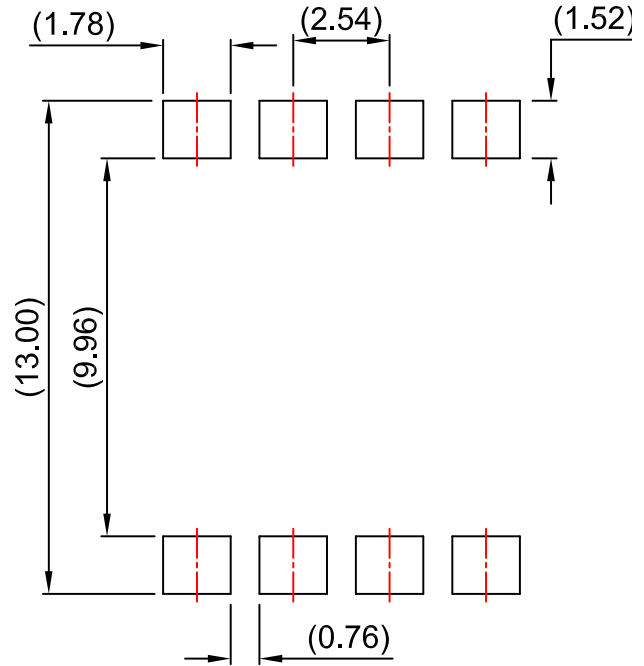
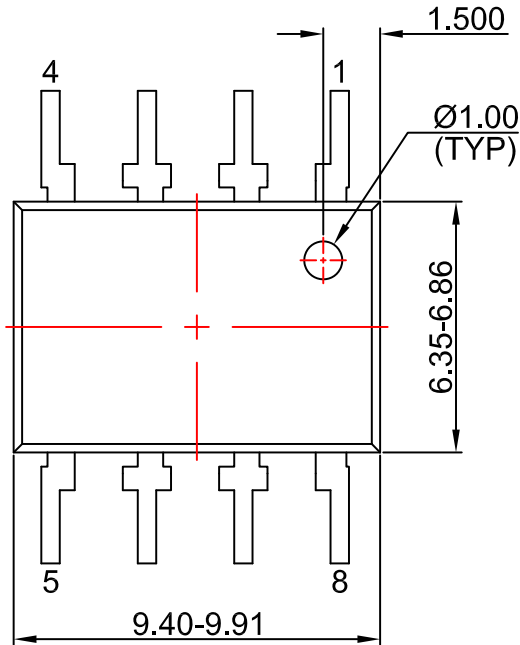
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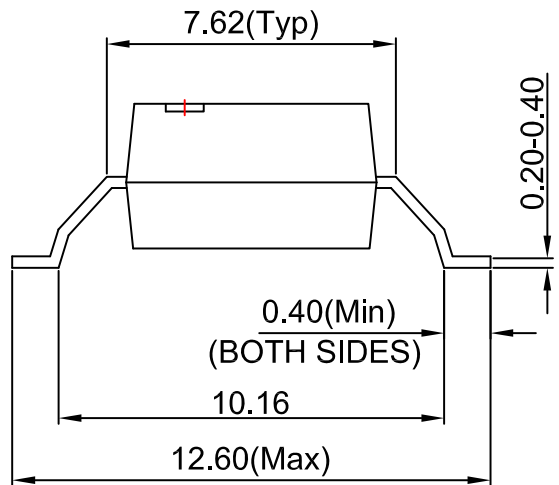
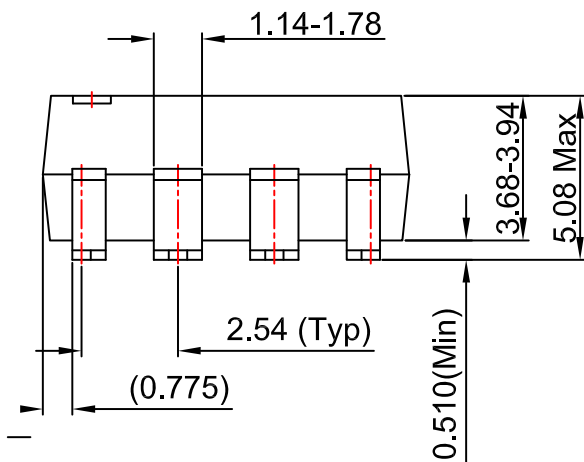


PDIP8 GW
CASE 709AD
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