

3A Ultra-Small Low Ron and Controlled Load Switch with Auto-Discharge Path

NCP451

The NCP451 is a very low Ron MOSFET controlled by external logic pin, allowing optimization of battery life, and portable device autonomy.

Indeed, due to a current consumption optimization with NMOS structure, leakage currents are eliminated by isolating connected IC on the battery when not used.

Output discharge path is also embedded to eliminate residual voltages on the output rail.

Proposed in a wide input voltage range from 0.75 V to 5.5 V, in a small 0.9 x 1.4 mm WLCSP6, pitch 0.5 mm.

Features

- 0.75 V – 5.5 V Operating Range
- 12 mΩ N MOSFET from 3.6 V to 5.5 V
- 13 mΩ N MOSFET from 1 V to 3.3 V
- DC Current Up to 3 A
- Output Auto-Discharge
- Active High EN Pin
- WLCSP6 0.9 x 1.4 mm
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Mobile Phones
- Tablets
- Digital Cameras
- GPS
- Portable Devices

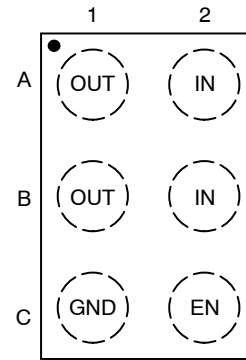


MARKING DIAGRAM



XXXX = Specific Device Code
 A = Assembly Location
 Y = Year
 W = Work Week
 ▪ = Pb-Free Package

PINOUT DIAGRAM



(Top View)

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 10 of this data sheet.

NCP451

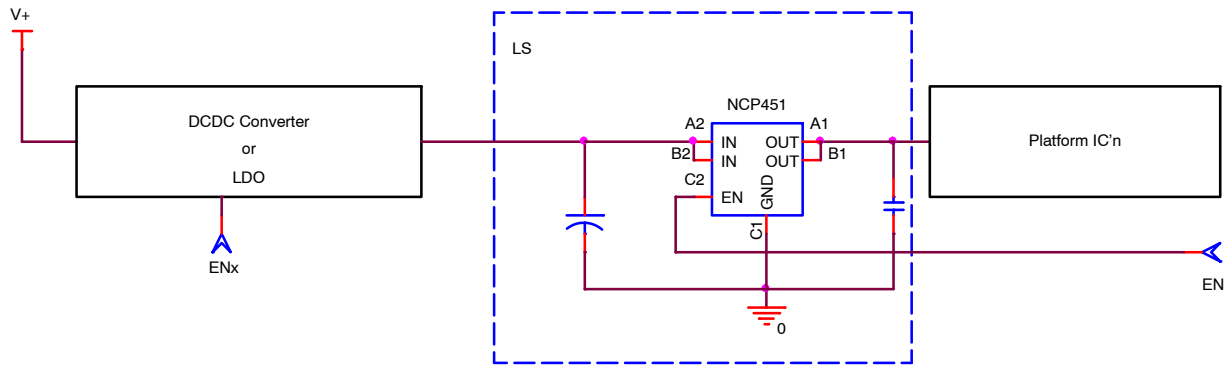


Figure 1. Typical Application Circuit

PIN FUNCTION DESCRIPTION

| Pin Name | Pin Number | Type | Description |
|----------|------------|--------|--|
| IN | A2, B2 | POWER | Load-switch input voltage; connect a 1 μ F or greater ceramic capacitor from IN to GND as close as possible to the IC. |
| GND | C1 | POWER | Ground connection. |
| EN | C2 | INPUT | Enable input, logic high turns on power switch. |
| OUT | A1, B1 | OUTPUT | Load-switch output; connect a 1 μ F ceramic capacitor from OUT to GND as close as possible to the IC is recommended. |

BLOCK DIAGRAM

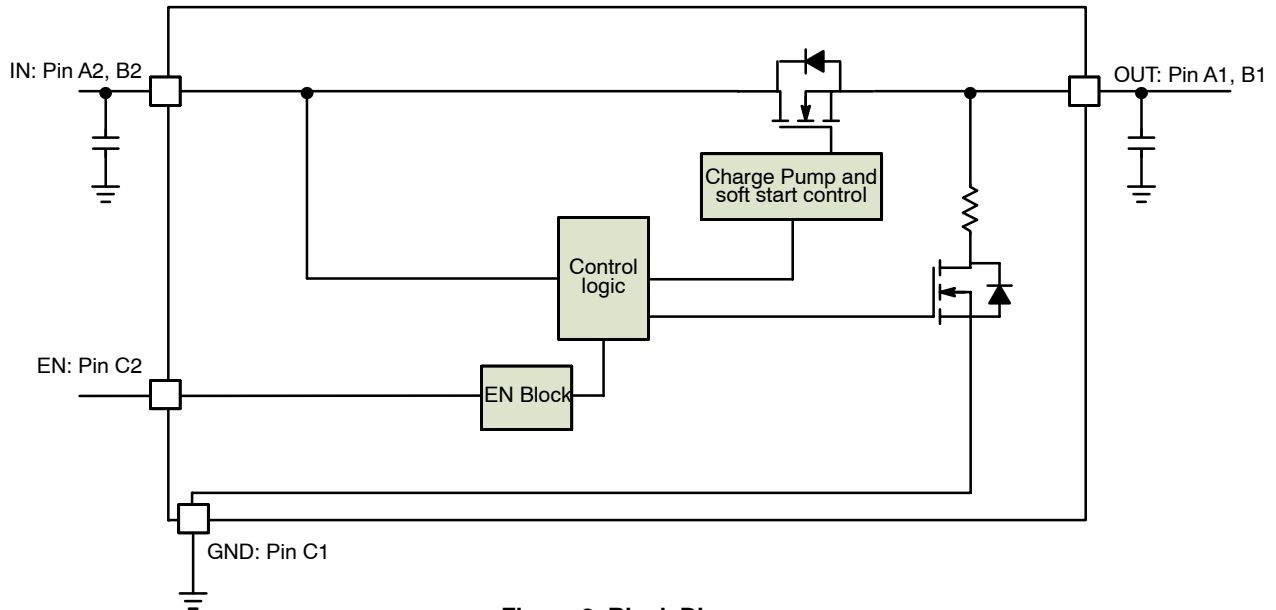


Figure 2. Block Diagram

NCP451

MAXIMUM RATINGS

| Symbol | Rating | Value | Unit |
|--|---------------------------|---------------|------|
| IN, OUT, EN, Pins: (Note 1) | V_{EN}, V_{IN}, V_{OUT} | -0.3 to + 7.0 | V |
| From IN to OUT Pins: Input/Output (Note 1) | V_{IN}, V_{OUT} | 0 to + 7.0 | V |
| Human Body Model (HBM) ESD Rating are (Notes 1 and 2) | ESD HBM | 1.5 | kV |
| Machine Model (MM) ESD Rating are (Notes 1 and 2) | ESD MM | 250 | V |
| Charge Device Model (CDM) ESD Rating are (Notes 1 and 2) | ESD CDM | 2000 | V |
| Latch-up protection (Note 3) -Pins IN, OUT, EN | LU | 100 | mA |
| Maximum Junction Temperature | T_J | -40 to + 125 | °C |
| Storage Temperature Range | T_{STG} | -40 to + 150 | °C |
| Moisture Sensitivity (Note 4) | MSL | Level 1 | |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. According to JEDEC standard JESD22-A108.
2. This device series contains ESD protection and passes the following tests:
Human Body Model (HBM) ± 1.5 kV per JEDEC standard: JESD22-A114 for all pins.
Machine Model (MM) ± 250 V per JEDEC standard: JESD22-A115 for all pins.
Charge Device Model (CDM) ± 2.0 kV per JEDEC standard: JESD22-C101 for all pins.
3. Latchup Current Maximum Rating: ± 100 mA per JEDEC standard: JESD78 class II.
4. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J-STD-020.

OPERATING CONDITIONS

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------|------------------------------------|------------------|------|-------|------|---------|
| V_{IN} | Operational Power Supply | | 0.75 | | 5.5 | V |
| V_{EN} | Enable Voltage | | 0 | | 5.5 | V |
| T_A | Ambient Temperature Range | | -40 | 25 | +85 | °C |
| T_J | Junction Temperature Range | | -40 | 25 | +125 | °C |
| C_{IN} | Decoupling input capacitor | | 1 | | | μF |
| C_{OUT} | Decoupling output capacitor | | 0.1 | | | μF |
| $R_{\theta JA}$ | Thermal Resistance Junction to Air | (Note 5) | | 100 | | °C/W |
| I_{OUT} | Maximum DC current | | | | 3 | A |
| P_D | Power Dissipation Rating (Note 6) | Over temperature | | 0.315 | | W |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

5. The $R_{\theta JA}$ is dependent of the PCB heat dissipation and thermal via.
6. The maximum power dissipation (P_D) is given by the following formula:

$$P_D = \frac{T_{JMAX} - T_A}{R_{\theta JA}}$$

NCP451

ELECTRICAL CHARACTERISTICS Min & Max Limits apply for T_A between -40°C to $+85^{\circ}\text{C}$ for V_{IN} between 0.75 V to 5.0 V (Unless otherwise noted). Typical values are referenced to $T_A = +25^{\circ}\text{C}$ and $V_{IN} = 3.6\text{ V}$ (Unless otherwise noted).

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit | |
|---------------------|---|--------------------------|---|-----|-----|---------------|------------|
| POWER SWITCH | | | | | | | |
| $R_{DS(on)}$ | Static drain-source on-state resistance | $V_{IN} = 5\text{ V}$ | $I_{OUT} = 200\text{ mA}, T_A = 25^{\circ}\text{C}$ | | 12 | 20 | m Ω |
| | | | $T_J = 125^{\circ}\text{C}$ | | | 25 | |
| | | $V_{IN} = 3.6\text{ V}$ | $I_{OUT} = 200\text{ mA}, T_A = 25^{\circ}\text{C}$ | | 12 | 20 | |
| | | | $T_J = 125^{\circ}\text{C}$ | | | 25 | |
| | | $V_{IN} = 3.3\text{ V}$ | $I_{OUT} = 200\text{ mA}, T_A = 25^{\circ}\text{C}$ | | 13 | 24 | |
| | | | $T_J = 125^{\circ}\text{C}$ | | | 28 | |
| | | $V_{IN} = 2.5\text{ V}$ | $I_{OUT} = 200\text{ mA}, T_A = 25^{\circ}\text{C}$ | | 13 | 24 | |
| | | | $T_J = 125^{\circ}\text{C}$ | | | 28 | |
| | | $V_{IN} = 1.8\text{ V}$ | $I_{OUT} = 200\text{ mA}, T_A = 25^{\circ}\text{C}$ | | 13 | 24 | |
| | | | $T_J = 125^{\circ}\text{C}$ | | | 28 | |
| | | $V_{IN} = 1.0\text{ V}$ | $I_{OUT} = 200\text{ mA}, T_A = 25^{\circ}\text{C}$ | | 13 | 24 | |
| | | | $T_J = 125^{\circ}\text{C}$ | | | 28 | |
| | | $V_{IN} = 0.75\text{ V}$ | $I_{OUT} = 200\text{ mA}, T_A = 25^{\circ}\text{C}$ | | 15 | 28 | |
| | | | $T_J = 125^{\circ}\text{C}$ | | | 35 | |
| R_{dis} | Output discharge path | EN = low | NCP451 | | 1.2 | 1.7 | M Ω |
| | | | NCP451A | | 1.0 | 1.7 | k Ω |
| V_{IH} | High-level input voltage | | 0.8 | | | V | |
| V_{IL} | Low-level input voltage | | | | 0.4 | | |
| I_{EN} | EN pin leakage current | $V_{IN} = 3.6\text{ V}$ | | | 0.1 | μA | |

QUIESCENT CURRENT

| | | | | | | | |
|-----------|-------------------|---|-----------------------------|--|-----|----|---------------|
| I_{std} | Standby current | $V_{IN} = 4.2\text{ V}$ | EN = low, No load | | 0.9 | 2 | μA |
| I_q | Quiescent current | $V_{IN} = 3.6\text{ V}$ $V_{IN} = 2.5\text{ V}$ $V_{IN} = 1.8\text{ V}$ $V_{IN} = 1.2\text{ V}$ $V_{IN} = 1.0\text{ V}$ $V_{IN} = 0.75\text{ V}$ | EN = high, No load (Note 7) | | 8 | 15 | μA |

TIMINGS

| | | | | | | | |
|----------|----------------------------|-------------------------------------|--|--|------|--|---------------|
| T_{EN} | Enable time | $V_{IN} = 3.6\text{ V}$ (Note 8) | $R_L = 25\ \Omega, C_{OUT} = 1\ \mu\text{F}$ | | 600 | | μs |
| T_R | Output rise time | | $R_L = 25\ \Omega, C_{OUT} = 1\ \mu\text{F}$ | | 800 | | |
| T_{ON} | ON time ($T_{EN} + T_R$) | | $R_L = 25\ \Omega, C_{OUT} = 1\ \mu\text{F}$ | | 1400 | | |
| T_F | Output fall time | | $R_L = 25\ \Omega, C_{OUT} = 1\ \mu\text{F}$ | | 55 | | |

TIMINGS

| | | | | | | | |
|----------|----------------------------|-------------------------------------|--|--|------|--|---------------|
| T_{EN} | Enable time | $V_{IN} = 3.6\text{ V}$ (Note 8) | $R_L = 10\ \Omega, C_{OUT} = 0.1\ \mu\text{F}$ | | 540 | | μs |
| T_R | Output rise time | | $R_L = 10\ \Omega, C_{OUT} = 0.1\ \mu\text{F}$ | | 670 | | |
| T_{ON} | ON time ($T_{EN} + T_R$) | | $R_L = 10\ \Omega, C_{OUT} = 0.1\ \mu\text{F}$ | | 1210 | | |
| T_F | Output fall time | | $R_L = 10\ \Omega, C_{OUT} = 0.1\ \mu\text{F}$ | | 2.5 | | |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Production tested at $V_{IN} = 3.6\text{ V}$.

8. Parameters are guaranteed for C_{LOAD} and R_{LOAD} connected to the OUT pin with respect to the ground

NCP451

TIMINGS

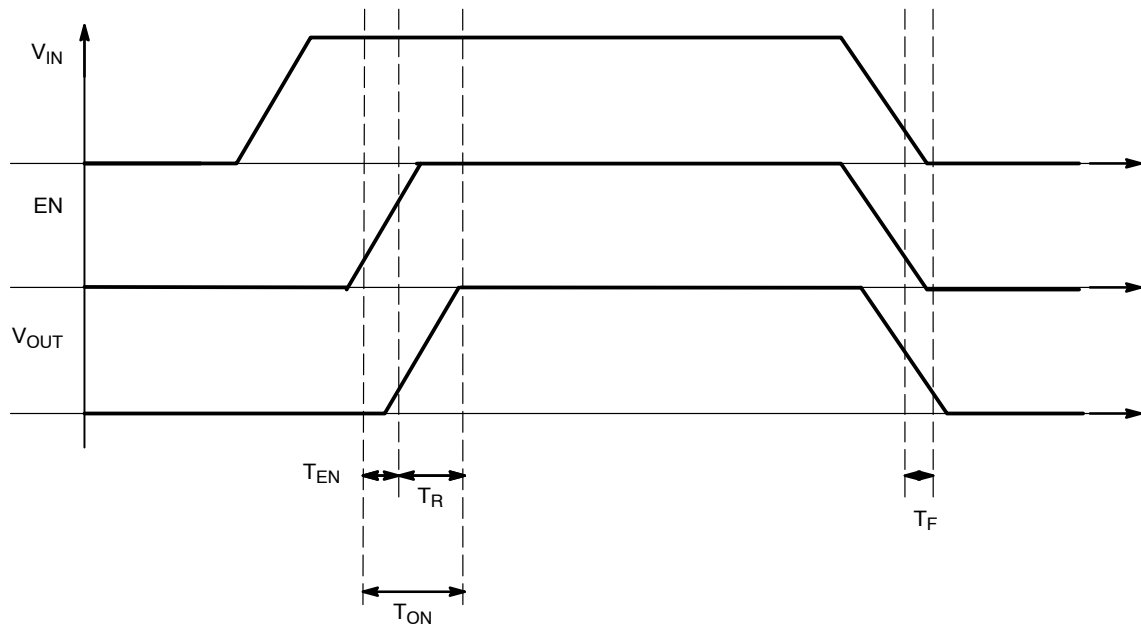


Figure 3. Enable, Rise and Fall Time

NCP451

ELECTRICAL CURVES

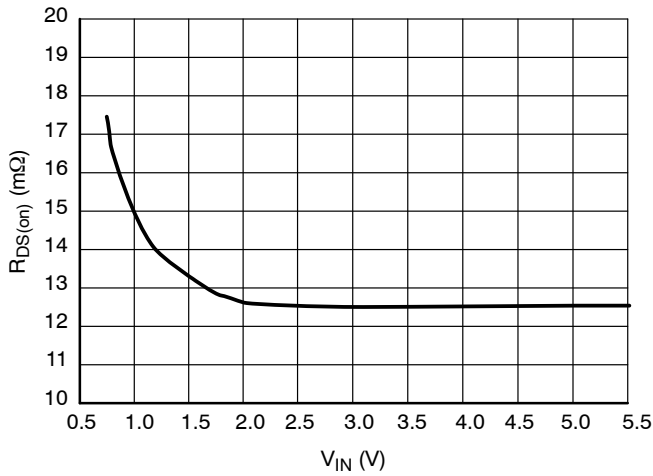


Figure 4. $R_{DS(on)}$ vs. V_{IN} , Low Load

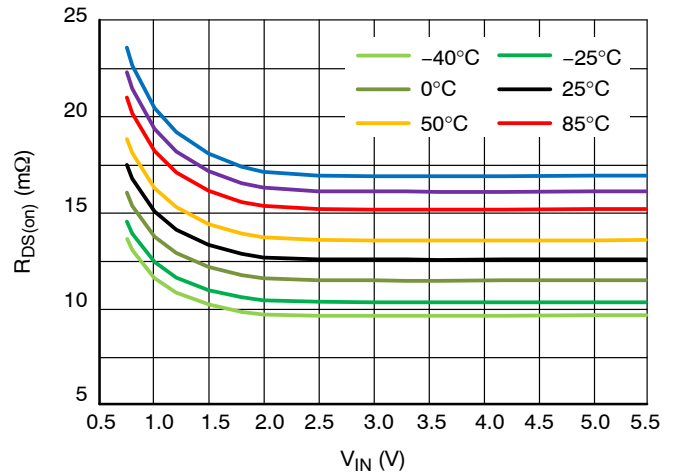


Figure 5. $R_{DS(on)}$ vs. V_{IN} , Low Load, Multi Temperature

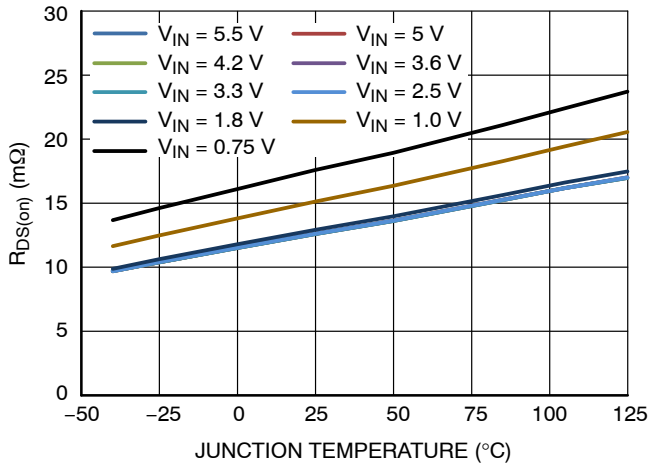


Figure 6. $R_{DS(on)}$ vs. Temperature, Multi V_{IN} Voltage

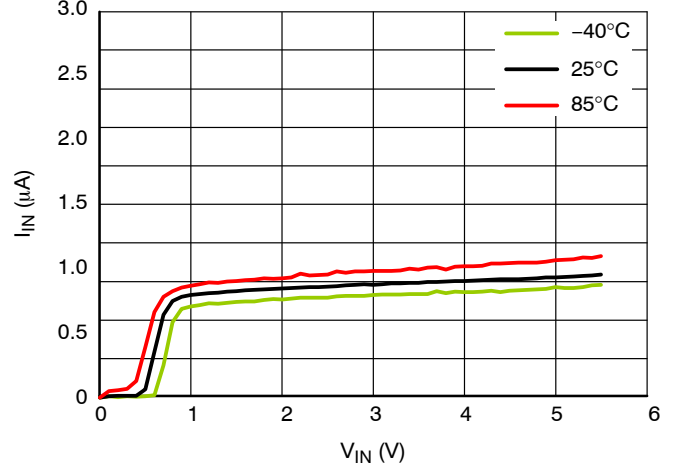


Figure 7. Standby Current (μA) vs. Temperature

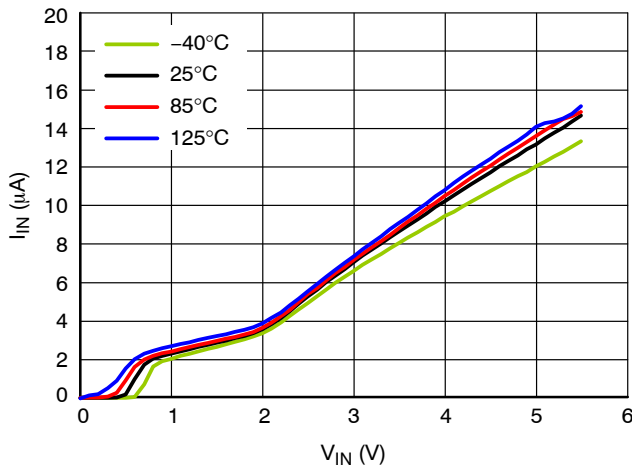


Figure 8. Quiescent Current (μA) vs. Temperature

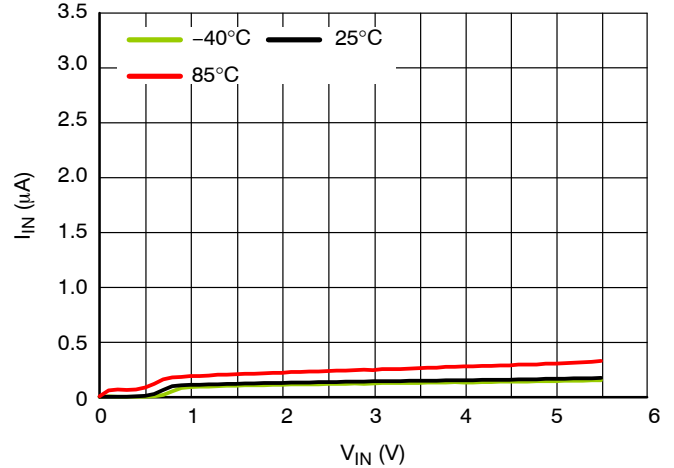


Figure 9. MOSFET Leakage Current (μA) vs. Temperature

NCP451

ELECTRICAL CURVES

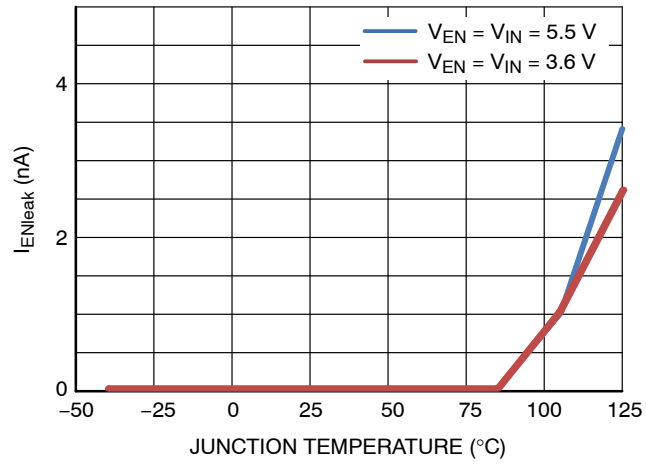


Figure 10. EN Pin Leakage vs. Temperature

NCP451

FUNCTIONAL DESCRIPTION

Overview

The NCP451 is a high side N channel MOSFET power distribution switch designed to isolate ICs connected on the battery in order to save energy. The part can be turned on, with a wide range of battery from 0.75 V to 5.5 V.

Enable Input

Enable pin is an active high. The path is opened when EN pin is tied low (disable), forcing N–MOSFET switch off.

The IN/OUT path is activated with a minimum of V_{in} of 0.75 V and EN forced to high level.

Auto Discharge

N–MOSFET is placed between the output pin and GND, in order to discharge the application capacitor connected on OUT pin.

The auto–discharge is activated when EN pin is set to low level (disable state).

The discharge path (Pull down NMOS) stays activated as long as EN pin is set at low level and $V_{IN} > 0.75$ V.

In order to limit the current across the internal discharge N–MOSFET, the typical value is set at R_{DIS} .

C_{IN} and C_{OUT} Capacitors

IN and OUT, 1 μ F, at least, capacitors must be placed as close as possible the part to for stability improvement.

APPLICATION INFORMATION

Power Dissipation

Main contributor in term of junction temperature is the power dissipation of the power MOSFET. Assuming this, the power dissipation and the junction temperature in normal mode can be calculated with the following equations:

$$P_D = R_{DS(on)} \times (I_{OUT})^2$$

- P_D = Power dissipation (W)
- $R_{DS(on)}$ = Power MOSFET on resistance (Ω)
- I_{OUT} = Output current (A)
- $T_J = P_D \times R_{\theta JA} + T_A$
- T_J = Junction temperature ($^{\circ}C$)
- $R_{\theta JA}$ = Package thermal resistance ($^{\circ}C/W$)
- T_A = Ambient temperature ($^{\circ}C$)

PCB Recommendations

The NCP451 integrates an up to 3 A rated NMOS FET, and the PCB design rules must be respected to properly evacuate the heat out of the silicon. By increasing PCB area, especially around IN and OUT pins, the $R_{\theta JA}$ of the package can be decreased, allowing higher power dissipation.

Routing example: 2 oz, 4 layers with vias across 2 internal inners.

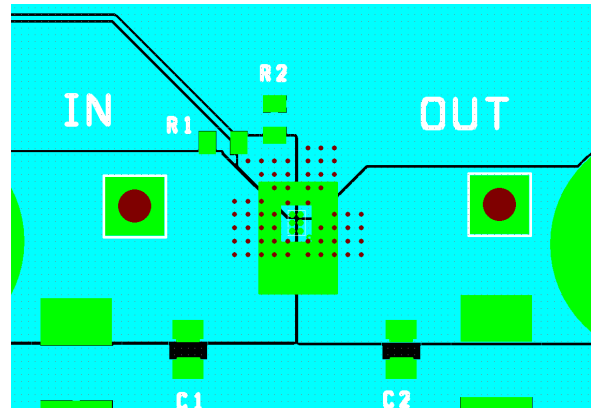


Figure 11.

Example of application definition.

$$T_J - T_A = R_{\theta JA} \times R_{DS(on)} \times I^2$$

T_J : junction temperature.

T_A : ambient temperature.

$R_{\theta JA}$: Thermal resistance between IC and air, through PCB.

$R_{DS(on)}$: intrinsic resistance of the IC MOSFET.

I : load DC current.

NCP451

Taking into account of Rtheta obtain with:

1 oz, 2 layers: 100°C/W.

At 3 A, 25°C ambient temperature, $R_{DS(on)}$ 20 mΩ @ V_{IN} 5 V, the junction temperature will be:

$$T_J - T_A = R_{\theta} \times P_D = 25 + (0.02 \times 3^2) \times 100 = 43^\circ C$$

Taking into account of Rtheta obtain with:

2 oz, 4 layers: 60°C/W.

At 3 A, 65°C ambient temperature, $R_{DS(on)}$ 24 mΩ @ V_{IN} 5 V, the junction temperature will be:

$$T_J = T_A + R_{\theta} \times P_D = 65 + (0.024 \times 3^2) \times 60 = 78^\circ C$$

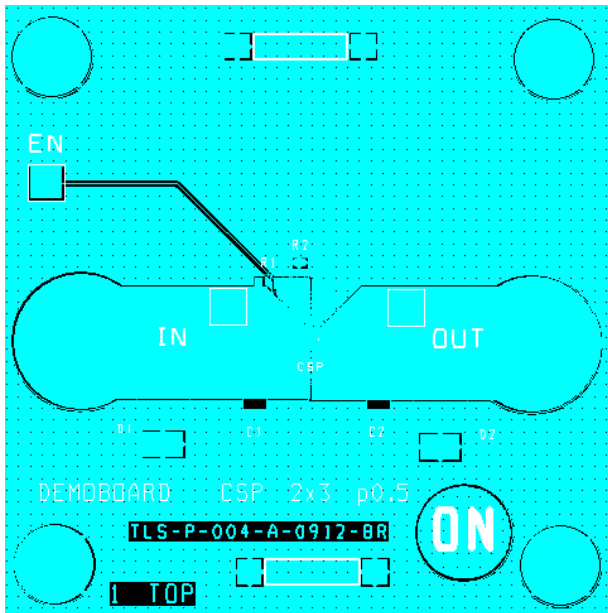


Figure 12. Demoboard PCB Top View

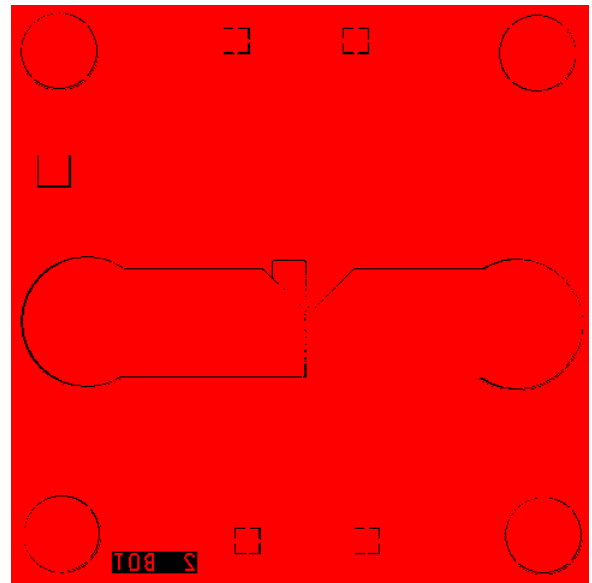


Figure 13. Demoboard PCB Top View

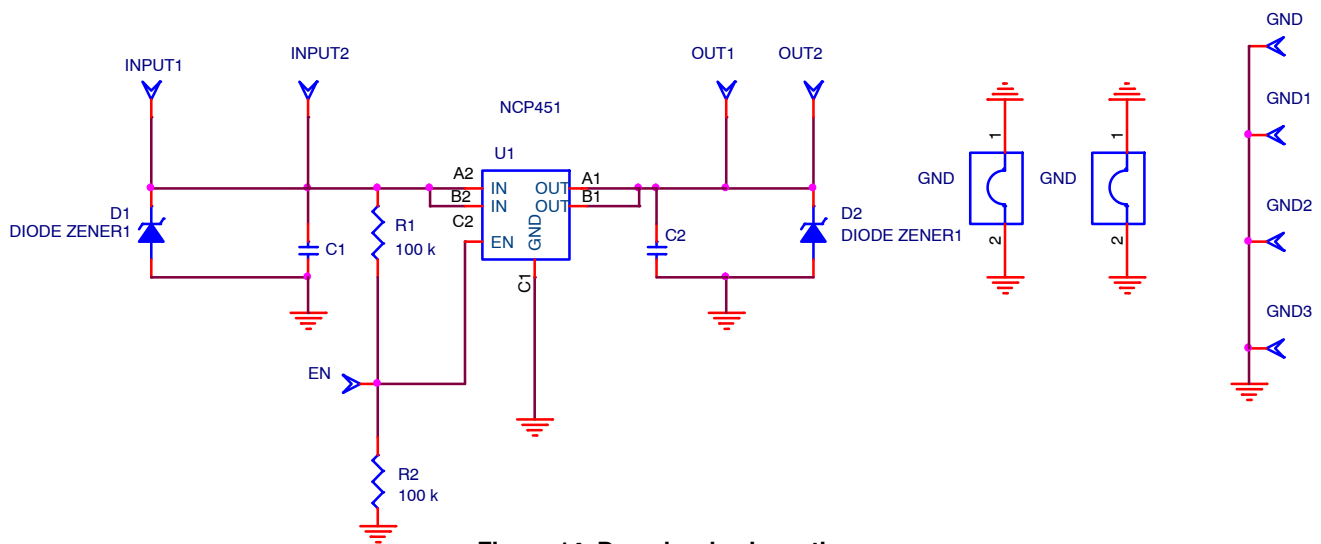


Figure 14. Demobard schematic

NCP451

BILL OF MATERIAL

| Quantity | Reference Scheme | Part Description | Part Number | Manufacturer |
|----------|-------------------|-------------------------|-------------------------|--------------|
| 2 | IN, OUT | Socket, 4mm, metal, PK5 | B010 | HIRSCHMANN |
| 3 | IN_2, OUT_2, , EN | HEADER200 | 2.54 mm, 77313-101-06LF | FC |
| 3 | C1, C2 | 1uF | GRM155R70J105KA12# | Murata |
| 1 | D1, D2 | TVS (not mounted) | ESD9x | onsemi |
| 2 | GND2,GND | GND JUMPER | D3082F05 | Harvin |
| 2 | R2, R3 | Resistor 100k 0603 | MC 0.063 0603 1% 100K | MULTICOMP |
| 1 | U1 | Load switch | NCP451 | onsemi |

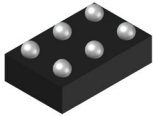
ORDERING INFORMATION

| Device | Marking | Option | Package* | Shipping† |
|---------------|---------|--------------------------|--------------------------|--------------------|
| NCP451FCT2G | 451 | Auto Discharge 1.2 MΩ | Case 499BR (Pb-Free) | 3000 / Tape & Reel |
| NCP451AFCT2G | 51A | Auto Discharge 1.0 kΩ | Case 567KB* (Pb-Free) | 3000 / Tape & Reel |
| NCP451AFCT2GA | 51A | Auto Discharge 1.0 kΩ | Case 567KB* (Pb-Free) | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

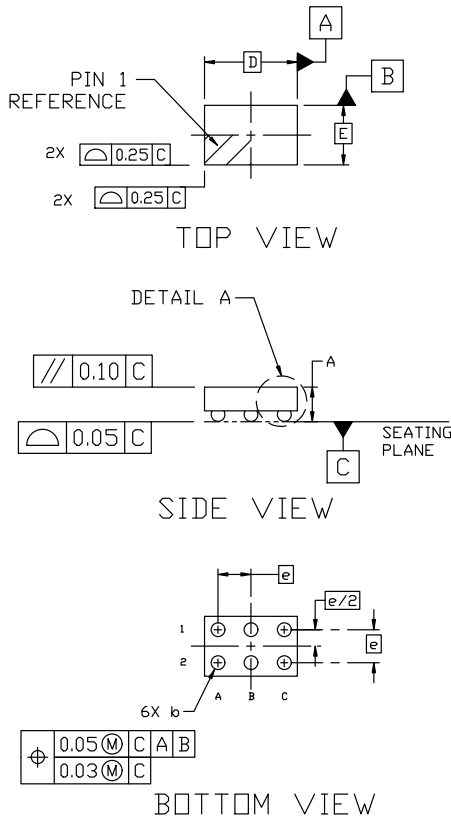
*UBM = 190 μm

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



WLCSP6, 1.40x0.90x0.521
CASE 499BR
ISSUE B

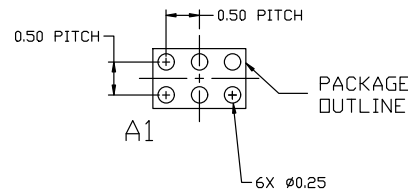
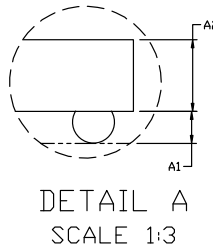
DATE 07 JUN 2022



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION *b* IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO DATUM C.
4. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. DATUM C, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

| DIM | MILLIMETERS | | |
|----------|-------------|-------|-------|
| | MIN. | NOM. | MAX. |
| A | 0.476 | 0.521 | 0.566 |
| A1 | 0.141 | 0.161 | 0.181 |
| A2 | 0.335 | 0.360 | 0.385 |
| <i>b</i> | 0.191 | 0.211 | 0.231 |
| D | 1.40 BSC | | |
| E | 0.90 BSC | | |
| <i>e</i> | 0.50 BSC | | |



**RECOMMENDED
MOUNTING FOOTPRINT***

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

**GENERIC
MARKING DIAGRAM***



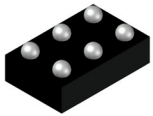
XXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

| | | |
|-------------------------|--------------------------------|--|
| DOCUMENT NUMBER: | 98AON84803E | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION: | WLCSP6, 1.40X0.90x0.521 | PAGE 1 OF 1 |

onsemi and ONSEMI are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

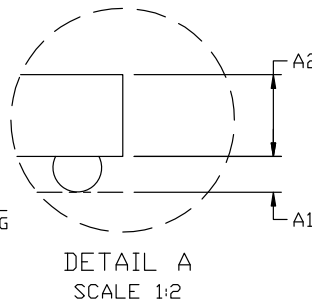
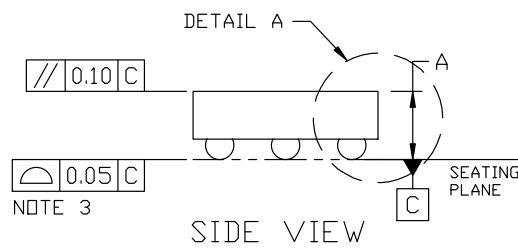
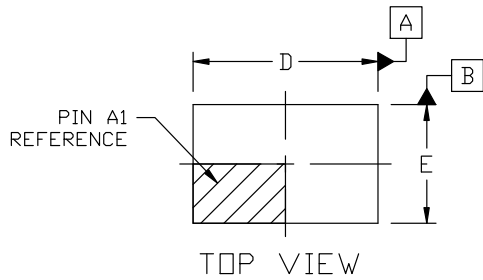


WLCSP6 1.40x0.90x0.516
CASE 567KB
ISSUE C

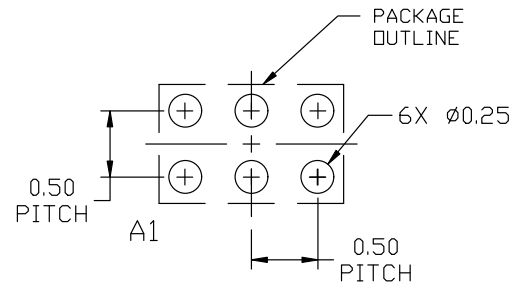
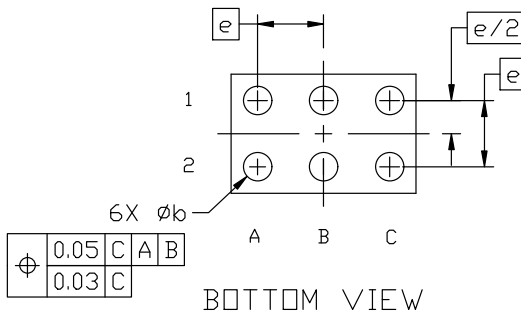
DATE 21 JUN 2022

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.



| DIM | MILLIMETERS | | |
|-----|-------------|-------|-------|
| | MIN. | NOM. | MAX. |
| A | 0.478 | 0.516 | 0.554 |
| A1 | 0.136 | 0.156 | 0.176 |
| A2 | 0.342 | 0.360 | 0.378 |
| b | 0.194 | 0.214 | 0.234 |
| D | 1.360 | 1.400 | 1.440 |
| E | 0.860 | 0.900 | 0.940 |
| e | 0.50 BSC | | |



RECOMMENDED
MOUNTING FOOTPRINT*

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

| | | |
|-------------------------|-------------------------------|--|
| DOCUMENT NUMBER: | 98AON85977F | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| DESCRIPTION: | WLCSP6 1.40x0.90x0.516 | PAGE 1 OF 1 |

onsemi and ONSEMI are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales