

## High-accuracy 6-axis inertial measurement unit (IMU) with extended temperature range for ASIL B automotive applications



LGA-14L  
Typ: 2.5 x 3.0 x 0.83 mm<sup>3</sup>

### Product status link

[ASM330LHBG1](#)

### Product summary

Order code	ASM330LHBG1TR
Temp. range [°C]	-40 to +125
Package	LGA-14L (2.5 x 3.0 x 0.83 mm <sup>3</sup> )
Packing	Tape and reel


### Product resources

[AN5691](#) (ASIL B library safety manual)  
[UM3134](#) (using the ASIL B library in Unico)  
[TN0018](#) (design and soldering)

### Product labels



## Features

- AEC-Q100 qualified 
- ASIL B compliant if used in conjunction with a certified software library (ISO 26262:2018)
- Android Auto™ compliant and CarPlay® compliant
- Extended temperature range from -40 to +125°C
- Embedded compensation for high stability over temperature
- Accelerometer user-selectable full scale up to ±16 g
- Extended gyroscope range from ±125 to ±4000 dps
- Dual operating modes: high-performance and low-power mode
- I<sup>2</sup>C, MIPI I3C<sup>SM</sup>, and SPI serial interfaces
- Six-channel synchronized output to enhance accuracy of dead-reckoning algorithms
- Programmable finite state machine
- Machine learning core
- Smart programmable interrupts
- Embedded 3 KB FIFO available to underload host processor
- **ECOPACK** and RoHS compliant

## Applications

- Satellite precise positioning
- Vehicle-to-everything (V2X)
- ADAS systems
- Active suspension
- Radar, lidar, and camera digital stabilization
- Door/trunk modules
- Motion-activated functions

## Description

The **ASM330LHBG1** is a 6-axis IMU that offers ASIL B compliance if used in conjunction with a certified software library and features a 3-axis digital accelerometer and a 3-axis digital gyroscope with an extended temperature range up to +125°C.

A safety manual and a software library, certified according to ISO 26262:2018, are provided to support the development of applications using the ASM330LHBG1 and targeting ASIL B requirements.

ST's family of MEMS sensor modules leverages the robust and mature manufacturing processes already used for the production of micromachined accelerometers and gyroscopes to serve both the automotive and consumer market. The ASM330LHBG1 is AEC-Q100 compliant and industrialized through a dedicated MEMS production flow to meet automotive reliability standards. All the parts are fully tested with respect to temperature to ensure the highest quality level.

The sensing elements are manufactured using ST's proprietary micromachining processes, while the IC interfaces are developed using CMOS technology that allows the design of a dedicated circuit, which is trimmed to better match the characteristics of the sensing element.

The ASM330LHBG1 has a full-scale acceleration range of  $\pm 2/\pm 4/\pm 8/\pm 16$  g and a wide angular rate range of  $\pm 125/\pm 250/\pm 500/\pm 1000/\pm 2000/\pm 4000$  dps that enables its usage in a broad range of automotive applications.

The device supports dual operating modes: high-performance mode and low-power mode.

All the design aspects of the ASM330LHBG1 have been optimized to reach superior output stability, extremely low noise, and full data synchronization to the benefit of sensor-assisted applications like dead reckoning and sensor fusion.

The ASM330LHBG1 is available in a 14-lead plastic, land grid array (LGA) package.

## 1 Overview

The ASM330LHBG1 is a system-in-package featuring a high-performance 3-axis digital accelerometer and 3-axis digital gyroscope.

This device is suitable for telematics and dead-reckoning applications as well as vehicle-to-vehicle (V2X) and impact detection as a result of its high stability over temperature and time, combined with superior sensing precision.

Supporting dual operating modes, the device has enhanced flexibility versus application requirements, leveraging on multiple voltage and multiple ODR selections. The device also includes digital features like a finite state machine and an ST proprietary machine learning core, allowing defined motion pattern detection or some complex algorithms run in the application processor to be moved to the MEMS sensor with the advantage of consistent reduction in power consumption.

The event-detection interrupts enable efficient and reliable motion-activated functions, implementing hardware recognition of free-fall events, 6D orientation, activity or inactivity, and wake-up events.

Like the entire portfolio of MEMS sensor modules, the ASM330LHBG1 leverages the robust and mature in-house manufacturing processes already used for the production of micromachined accelerometers and gyroscopes. The various sensing elements are manufactured using specialized micromachining processes, while the IC interfaces are developed using CMOS technology that allows the design of a dedicated circuit, which is trimmed to better match the characteristics of the sensing element.

The ASM330LHBG1 is available in a small plastic, land grid array (LGA) package of 2.5 x 3.0 x 0.83 mm to address ultracompact solutions.

This device, used in redundancy (as two modules) and in combination with a dedicated software library, has been evaluated as compatible to be adopted in ASIL B automotive applications. This solution is described in detail in application note AN5691.

## 2 Embedded low-power features

The ASM330LHBG1 has been designed to feature the following on-chip functions:

- 3 KB data buffering
  - 100% efficiency with flexible configurations and partitioning
  - Possibility to store timestamp
- Event-detection interrupts (fully configurable)
  - Free-fall
  - Wake-up
  - 6D orientation
  - Activity/inactivity recognition
  - Stationary/motion detection
- Specific IP blocks with negligible power consumption and high performance
  - Finite state machine (FSM) for the accelerometer and gyroscope
  - Machine learning core (MLC) for the accelerometer and gyroscope

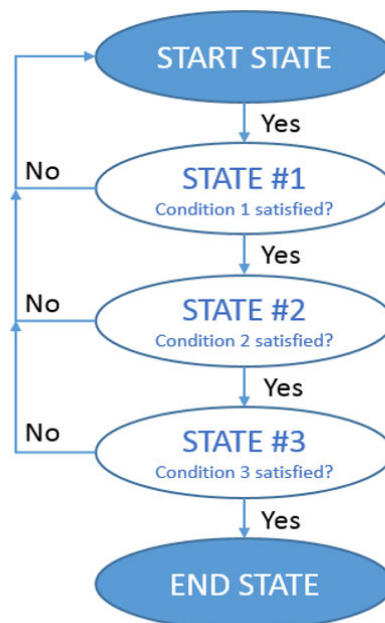
### 2.1 Finite state machine

The ASM330LHBG1 can be configured to generate interrupt signals activated by user-defined motion patterns. To do this, up to 16 embedded finite state machines can be programmed independently for motion detection such as vehicle status (stationary or moving), antitheft alarm and shock detection.

#### Definition of finite state machine

A state machine is a mathematical abstraction used to design logic connections. It is a behavioral model composed of a finite number of states and transitions between states, similar to a flow chart in which one can inspect the way logic runs when certain conditions are met. The state machine begins with a start state, goes to different states through transitions dependent on the inputs, and can finally end in a specific state (called stop state). The current state is determined by the past states of the system. The figure below shows a generic state machine.

Figure 1. Generic state machine



**Finite state machine in the ASM330LHBG1**

The ASM330LHBG1 works as a combo accelerometer-gyroscope sensor, generating acceleration and angular rate output data. These data can be used as the input in up to 16 programs in the embedded finite state machine (Figure 2. State machine in the ASM330LHBG1).

All 16 finite state machines are independent: each one has its dedicated memory area and it is independently executed. An interrupt is generated when the end state is reached or when some specific command is performed.

**Figure 2. State machine in the ASM330LHBG1**



## 2.2 Machine learning core

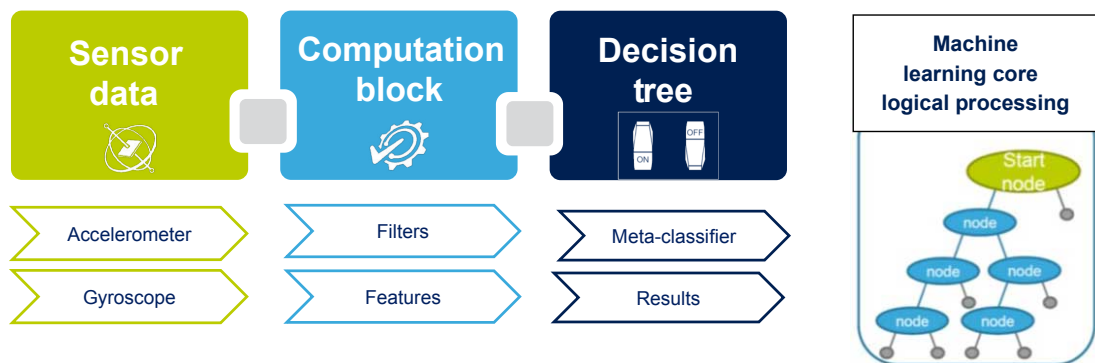
The ASM330LHBG1 embeds a dedicated core for machine learning processing that provides system flexibility, allowing some algorithms run in the application processor to be moved to the MEMS sensor with the advantage of consistent reduction in power consumption.

Machine learning core logic allows identifying if a data pattern (for example motion, pressure, temperature, magnetic data, and so forth) matches a user-defined set of classes. Typical examples of applications could be activity detection like running, walking, driving, and so forth.

The ASM330LHBG1 machine learning core works on data patterns coming from the accelerometer and gyro sensors. The input data can be filtered using a dedicated configurable computation block containing filters and features computed in a fixed time window defined by the user.

Machine learning processing is based on logical processing composed of a series of configurable nodes characterized by "if-then-else" conditions where the "feature" values are evaluated against defined thresholds.

Figure 3. Machine learning core in the ASM330LHBG1



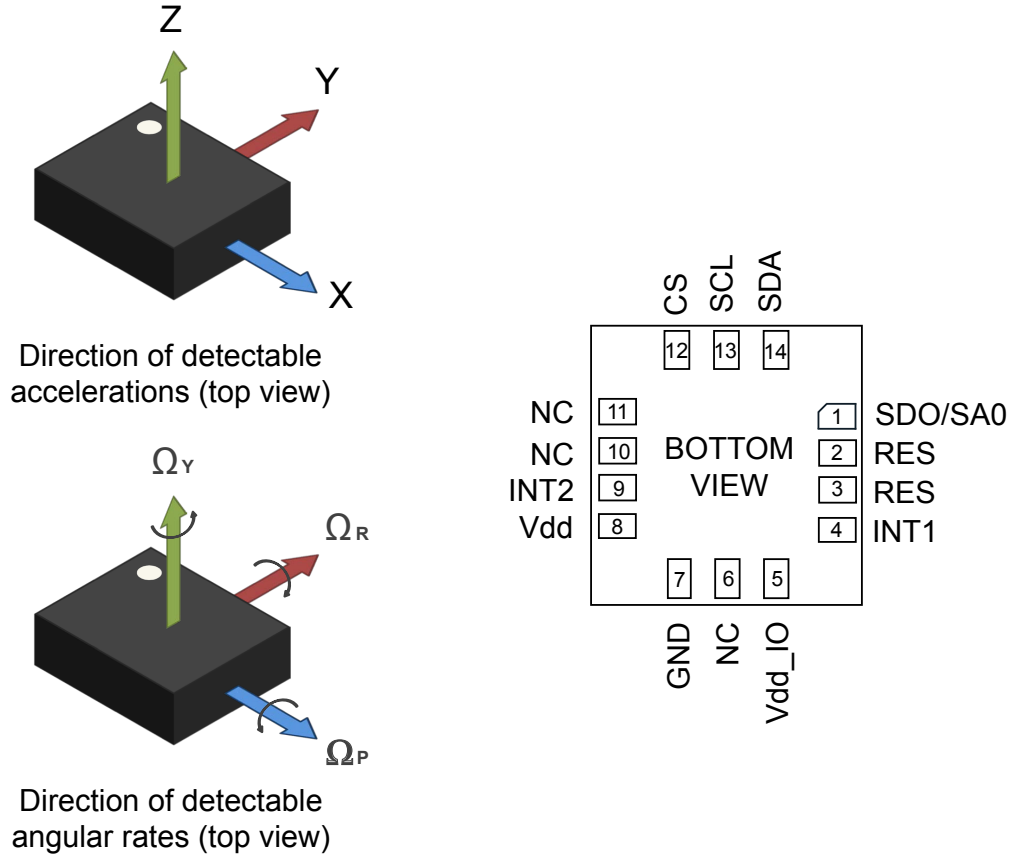
The ASM330LHBG1 can be configured to run up to 8 flows simultaneously and independently and every flow can generate up to 256 results. The total number of nodes can be up to 512.

The results of the machine learning processing are available in dedicated output registers readable from the application processor at any time.

The ASM330LHBG1 machine learning core can be configured to generate an interrupt when a change in the result occurs.

### 3 Pin description

Figure 4. Pin connections



**Table 1. Pin description**

Pin#	Name	Function
1	SDO/SA0	SPI 4-wire interface serial data output (SDO) I <sup>2</sup> C least significant bit of the device address (SA0) MIPI I3C <sup>SM</sup> least significant bit of the static address (SA0)
2	RES	Connect to Vdd_IO or GND
3	RES	Connect to Vdd_IO or GND
4	INT1	Programmable interrupt in I <sup>2</sup> C and SPI
5	Vdd_IO <sup>(1)</sup>	Power supply for I/O pins
6	NC	Connect to Vdd_IO or GND or leave unconnected
7	GND	0 V supply
8	Vdd <sup>(1)</sup>	Power supply
9	INT2	Programmable interrupt 2 (INT2) / data enabled (DEN)
10	NC	Leave unconnected <sup>(2)</sup>
11	NC	Leave unconnected <sup>(2)</sup>
12	CS	I <sup>2</sup> C/MIPI I3C <sup>SM</sup> /SPI mode selection (1: SPI idle mode / I <sup>2</sup> C/MIPI I3C <sup>SM</sup> communication enabled; 0: SPI communication mode / I <sup>2</sup> C/MIPI I3C <sup>SM</sup> disabled)
13	SCL	I <sup>2</sup> C/MIPI I3C <sup>SM</sup> serial clock (SCL) SPI serial port clock (SPC)
14	SDA	I <sup>2</sup> C/MIPI I3C <sup>SM</sup> serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)

1. Vdd\_IO: Recommended 100 nF filter capacitor. Vdd: Recommended 100 nF plus 10 µF capacitors.

2. Leave pin electrically unconnected and soldered to PCB.



## 4 Module specifications

### 4.1 Mechanical characteristics

@Vdd = 3.0 V, T = -40°C to +125°C, up to gyroscope FS = ±2000 dps unless otherwise noted.

The product is factory calibrated at 3.0 V. The operational power supply range is from 1.71 V to 3.6 V.

**Table 2. Mechanical characteristics**

Symbol	Parameter	Test conditions	Min.	Typ. <sup>(1)</sup>	Max.	Unit
LA_FS	Linear acceleration measurement range			±2		g
				±4		
				±8		
				±16		
G_FS	Angular rate measurement range			±125		dps
				±250		
				±500		
				±1000		
				±2000		
LA_So	Linear acceleration sensitivity	@LA_FS = ±2 g		0.061		mg/LSB
		@LA_FS = ±4 g		0.122		
		@LA_FS = ±8 g		0.244		
		@LA_FS = ±16 g		0.488		
G_So	Angular rate sensitivity	@G_FS = ±125 dps		4.37		mdps/LSB
		@G_FS = ±250 dps		8.75		
		@G_FS = ±500 dps		17.5		
		@G_FS = ±1000 dps		35.0		
		@G_FS = ±2000 dps		70.0		
		@G_FS = ±4000 dps		140.0		
LA_TySo%	Linear acceleration sensitivity tolerance <sup>(2)</sup>	@25°C		±2		%
G_TySo%	Angular rate sensitivity tolerance <sup>(2)</sup>	@25°C		±2		%
LA_So%	Linear acceleration sensitivity tolerance - long term <sup>(3)</sup>	from -40 to +125°C	-6		+6	%
G_So%	Angular rate sensitivity tolerance - long term <sup>(3)</sup>	from -40 to +125°C	-10		+10	%
LA_SoDr	Linear acceleration sensitivity change vs. temperature			±100		ppm/°C
G_SoDr	Angular rate sensitivity change vs. temperature			±70		ppm/°C
LA_TyOff	Linear acceleration zero-g level offset accuracy <sup>(2)</sup>	@25°C		±20		mg
LA_Off	Linear acceleration offset accuracy - long term <sup>(3)</sup>	from -40 to +125°C	-200		+200	mg
G_TyOff	Angular rate zero-rate level accuracy <sup>(2)</sup>	@25°C		±2		dps
G_Off	Angular rate offset accuracy - long term <sup>(3)</sup>	from -40 to +125°C	-10		+10	dps
LA_TCOff	Linear acceleration zero-g level change vs. temperature			±0.10		mg/°C
G_TCOff	Angular rate typical zero-rate level change vs. temperature			±0.005		dps/°C
LA_Cx	Linear acceleration cross-axis sensitivity	@25°C		±1		%

Symbol	Parameter	Test conditions	Min.	Typ. <sup>(1)</sup>	Max.	Unit
G_Cx	Angular rate cross-axis sensitivity	@25°C		±1		%
An	Acceleration noise density <sup>(4)(6)</sup>	@LA_FS = ±2 g @25°C		60	200	µg/√Hz
AnRMS	Acceleration RMS noise in low-power mode <sup>(5)</sup>			1.8		mg(RMS)
Rn	Rate noise density <sup>(4)(6)</sup>	@25°C		5	12	mdps/√Hz
RnRMS	Gyroscope RMS noise in low-power mode <sup>(5)</sup>			90		mdps(RMS)
XL_NL	Accelerometer nonlinearity <sup>(7)</sup>	Best-fit straight line		0.5		%FS
G_NL	Gyroscope nonlinearity <sup>(7)</sup>	Best-fit straight line		0.01		% FS
VRW	Velocity random walk <sup>(7)</sup>	@25°C		0.03		m/sec/√h
XL_BI	Accelerometer bias instability <sup>(7)</sup>	@25°C		40		µg
ARW	Angular random walk <sup>(7)</sup>	@25°C		0.21		°/√h
G_BI	Gyroscope bias instability <sup>(7)</sup>	@25°C		3		°/h
LA_ODR	Linear acceleration output data rate			1.6 <sup>(8)</sup> 12.5 26 52 104 208 416 833 1667		Hz
G_ODR	Angular rate output data rate			12.5 26 52 104 208 416 833 1667		Hz
Vst	Linear acceleration self-test output change <sup>(9)(10)(11)</sup>	from -40 to +125°C	40		1700	mg
	Angular rate self-test output change <sup>(12)(13)</sup>	FS = ±250 dps from -40 to +125°C	20		80	dps
		FS = ±2000 dps from -40 to +125°C	150		700	dps
Top	Operating temperature range		-40		+125	°C

1. Typical specifications are not guaranteed.
2. Values after factory calibration test and trimming at T = 25°C.
3. Long term includes the following conditions: post solder, drift in temperature in the range [-40°C to +125°C] and over life.
4. Max. values from design and characterization at ambient temperature (T = 25°C).
5. RMS noise is the same for all ODRs.
6. Noise density is the same for all ODRs.
7. Based on characterization data on a limited number of samples. Not measured during final test for production.
8. This ODR is available when the accelerometer is in low-power mode.
9. Accelerometer self-test limits are full-scale independent.
10. The sign of the linear acceleration self-test output change is defined by the STx\_XL bits in a dedicated register for all axes.

11. The linear acceleration self-test output change is defined with the device in stationary condition as the absolute value of:  $OUTPUT[LSb]$  (self-test enabled) -  $OUTPUT[LSb]$  (self-test disabled). 1LSb = 0.061 mg at  $\pm 2$  g full scale.
12. The angular rate self-test output change is defined with the device in stationary condition as the absolute value of:  $OUTPUT[LSb]$  (self-test enabled) -  $OUTPUT[LSb]$  (self-test disabled). 1LSb = 70 mdps at  $\pm 2000$  dps full scale.
13. The sign of the angular rate self-test output change is defined by the  $STx\_G$  bits in a dedicated register for all axes.

## 4.2 Electrical characteristics

@Vdd = 3.0 V, T = -40°C to +125°C, up to gyroscope FS = ±2000 dps unless otherwise noted.

**Table 3. Electrical characteristics**

Symbol	Parameter	Test conditions	Min.	Typ. <sup>(1)</sup>	Max.	Unit
Vdd	Supply voltage		1.71		3.6	V
Vdd_IO	Power supply for I/O		1.62		3.6	V
GA_Idd	Gyroscope and accelerometer current consumption	Vdd = 3.0 V, ODR = 1.6 kHz -40 to +125°C		1.3	1.7	mA
LA_IddHP	Accelerometer current consumption in high-performance mode	Vdd = 3.0 V, ODR = 1.6 kHz -40 to +125°C		360	750	µA
LA_IddLM	Accelerometer current consumption in low-power mode	Vdd = 3.0 V, ODR = 52 Hz @25°C		50	500	µA
		Vdd = 3.0 V, ODR = 12.5 Hz @25°C <sup>(3)</sup>		14		µA
		Vdd = 3.0 V, ODR = 1.6 Hz @25°C <sup>(3)</sup>		7		µA
		Vdd = 1.71 V, ODR = 52 Hz @25°C		40	500	µA
		Vdd = 1.71 V, ODR = 12.5 Hz @25°C <sup>(3)</sup>		11		µA
		Vdd = 1.71 V, ODR = 1.6 Hz @25°C <sup>(3)</sup>		5.5		µA
LC_IddLM	Current consumption in low-power mode, combo	Vdd = 3.0 V, ODR = 52 Hz -40 to +125°C		530	1000	µA
		Vdd = 3.0 V, ODR = 12.5 Hz @25°C <sup>(3)</sup>		475		µA
		Vdd = 1.71 V, ODR = 52 Hz -40 to +125°C		520	1000	µA
		Vdd = 1.71 V, ODR = 12.5 Hz @25°C <sup>(3)</sup>		470		µA
IddPD	Gyroscope and accelerometer current consumption during power-down	Vdd = 3.0 V, @25°C		5	13	µA
Ton	Turn-on time <sup>(2)</sup>			35		ms
V <sub>IH</sub> <sup>(3)</sup>	Digital high-level input voltage		0.7 * Vdd_IO			V
V <sub>IL</sub> <sup>(3)</sup>	Digital low-level input voltage				0.3 * Vdd_IO	V
V <sub>OH</sub> <sup>(3)</sup>	High-level output voltage	I <sub>OH</sub> = 4 mA <sup>(4)</sup>	Vdd_IO - 0.2			V
V <sub>OL</sub> <sup>(3)</sup>	Low-level output voltage	I <sub>OL</sub> = 4 mA <sup>(4)</sup>			0.2	V
Top	Operating temperature range		-40		+125	°C

1. Typical specifications are not guaranteed.
2. Time to obtain stable sensitivity (within ±5% of final value) switching from power-down to normal operation
3. Evaluated by characterization - not tested in production
4. 4 mA is the minimum driving capability, that is, the minimum DC current that can be sourced/sunk by the digital pad in order to guarantee the correct digital output voltage levels V<sub>OH</sub> and V<sub>OL</sub>.

### 4.3 Temperature sensor characteristics

@Vdd = 3.0 V, T = 25 °C unless otherwise noted. The product is factory calibrated at 3.0 V.

**Table 4. Temperature sensor characteristics**

Symbol	Parameter	Test condition	Min.	Typ. <sup>(1)</sup>	Max.	Unit
TODR <sup>(2)</sup>	Temperature refresh rate			52		Hz
Toff	Temperature offset <sup>(3)</sup>		-15		+15	°C
TSen	Temperature sensitivity			256		LSB/°C
TST	Temperature stabilization time <sup>(4)</sup>				500	µs
T_ADC_res	Temperature ADC resolution			16		bit
Top	Operating temperature range		-40		+125	°C

1. Typical specifications are not guaranteed.
2. When the accelerometer is in low-power mode and the gyroscope part is turned off, the TODR value is equal to the accelerometer ODR.
3. The output of the temperature sensor is 0 LSB (typ.) at 25 °C.
4. Time from power ON to valid output data. Based on characterization.

## 4.4 Communication interface characteristics

### 4.4.1 SPI - serial peripheral interface

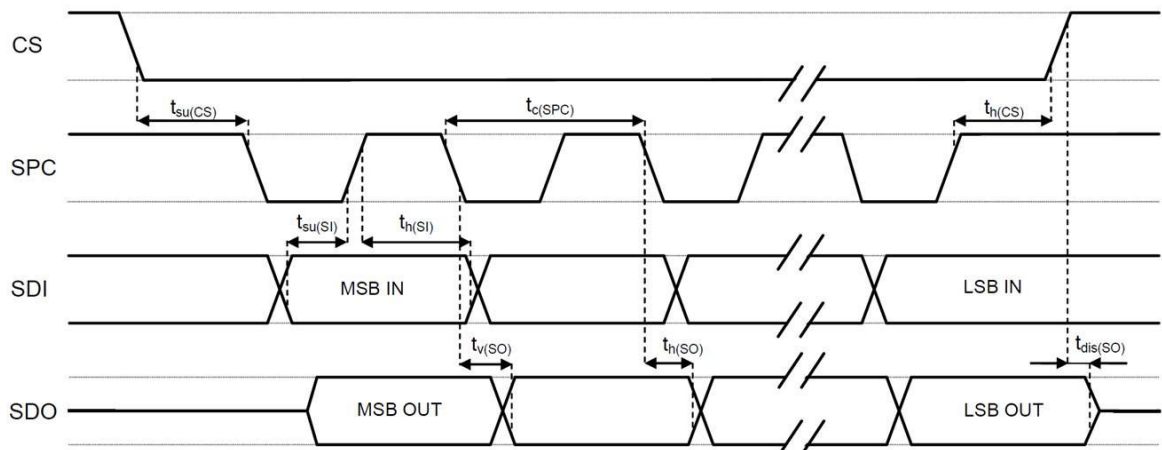
Subject to general operating conditions for Vdd and Top.

**Table 5. SPI slave timing values (in mode 3)**

Symbol	Parameter	Value <sup>(1)</sup>		Unit
		Min	Max	
$t_{c(SPC)}$	SPI clock cycle	100		ns
$f_{c(SPC)}$	SPI clock frequency		10	MHz
$t_{su(CS)}$	CS setup time	5		ns
$t_{h(CS)}$	CS hold time	20		
$t_{su(SI)}$	SDI input setup time	5		
$t_{h(SI)}$	SDI input hold time	15		
$t_{v(SO)}$	SDO valid output time		50	
$t_{h(SO)}$	SDO output hold time	5		
$t_{dis(SO)}$	SDO output disable time		50	

1. Values are evaluated at 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results, not tested in production

**Figure 5. SPI slave timing diagram (in mode 3)**



Note: Measurement points are done at  $0.3 \cdot V_{dd\_IO}$  and  $0.7 \cdot V_{dd\_IO}$  for both input and output ports.

#### 4.4.2 I<sup>2</sup>C - inter-IC control interface

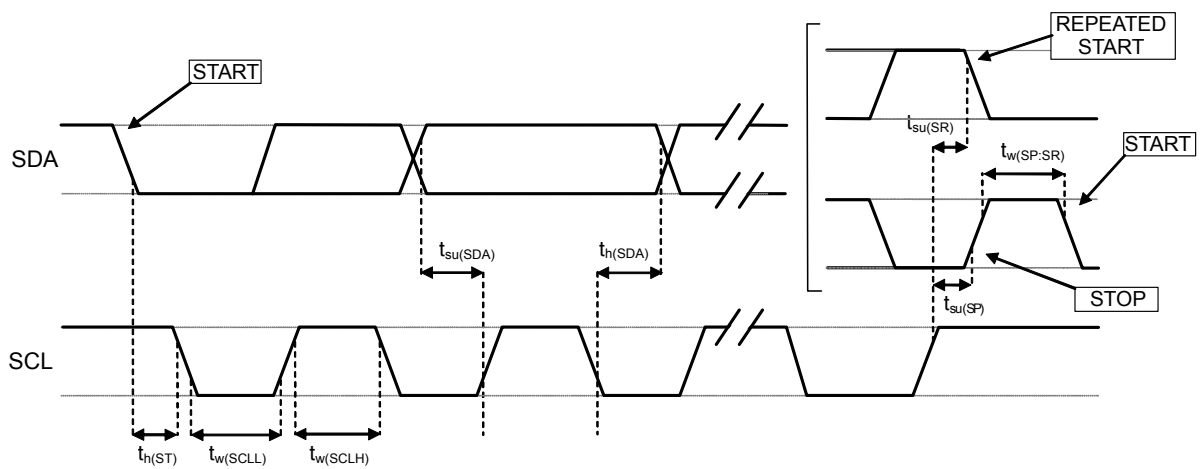
Subject to general operating conditions for V<sub>dd</sub> and Top.

**Table 6. I<sup>2</sup>C slave timing values**

Symbol	Parameter	I <sup>2</sup> C standard mode <sup>(1)</sup>		I <sup>2</sup> C fast mode <sup>(1)</sup>		Unit
		Min	Max	Min	Max	
f <sub>(SCL)</sub>	SCL clock frequency	0	100	0	400	kHz
t <sub>w(SCLL)</sub>	SCL clock low time	4.7		1.3		μs
t <sub>w(SCLH)</sub>	SCL clock high time	4.0		0.6		
t <sub>su(SDA)</sub>	SDA setup time	250		100		ns
t <sub>h(SDA)</sub>	SDA data hold time	0	3.45	0	0.9	μs
t <sub>h(ST)</sub>	START condition hold time	4		0.6		
t <sub>su(SR)</sub>	Repeated START condition setup time	4.7		0.6		
t <sub>su(SP)</sub>	STOP condition setup time	4		0.6		
t <sub>w(SP:SR)</sub>	Bus free time between STOP and START condition	4.7		1.3		

1. Data based on standard I<sup>2</sup>C protocol requirement, not tested in production.

**Figure 6. I<sup>2</sup>C slave timing diagram**



Note: Measurement points are done at 0.3·V<sub>dd\_IO</sub> and 0.7·V<sub>dd\_IO</sub> for both ports.

**Table 7. I<sup>2</sup>C high-speed mode specifications at 1 MHz**

	Symbol	Parameter	Min.	Max.	Unit
Fast mode plus <sup>(1)</sup>	f <sub>SCL</sub>	SCL clock frequency	0	1	MHz
	t <sub>HD;STA</sub>	Hold time (repeated) START condition	260	-	ns
	t <sub>LOW</sub>	Low period of the SCL clock	500	-	
	t <sub>HIGH</sub>	High period of the SCL clock	260	-	
	t <sub>SU;STA</sub>	Setup time for a repeated START condition	260	-	
	t <sub>HD;DAT</sub>	Data hold time	0	-	
	t <sub>SU;DAT</sub>	Data setup time	50	-	
	t <sub>rDA</sub>	Rise time of SDA signal	-	120	
	t <sub>fDA</sub>	Fall time of SDA signal	-	120	
	t <sub>rCL</sub>	Rise time of SCL signal	20*Vdd/5.5	120	
	t <sub>fCL</sub>	Fall time of SCL signal	20*Vdd/5.5	120	
	t <sub>SU;STO</sub>	Setup time for STOP condition	260	-	
	C <sub>b</sub>	Capacitive load for each bus line	-	550	pF
	t <sub>VD;DAT</sub>	Data valid time	-	450	ns
	t <sub>VD;ACK</sub>	Data valid acknowledge time	-	450	
	V <sub>nL</sub>	Noise margin at low level	0.1Vdd	-	V
V <sub>nH</sub>	Noise margin at high level	0.2Vdd	-		
t <sub>SP</sub>	Pulse width of spikes that must be suppressed by the input filter	0	50	ns	

1. Data based on characterization, not tested in production



## 4.5 Absolute maximum ratings

Stresses above those listed as “Absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Table 8. Absolute maximum ratings**

Symbol	Ratings	Maximum value	Unit
Vdd	Supply voltage	-0.3 to 4.8	V
T <sub>STG</sub>	Storage temperature range	-40 to +125	°C
Sg	Acceleration <i>g</i> for 0.5 ms	3000	<i>g</i>
ESD	Electrostatic discharge protection (HBM)	2	kV
V <sub>in</sub>	Input voltage on any control pin (including CS, SCL/SPC, SDA/SDI/SDO, SDO/SA0)	-0.3 to Vdd_IO +0.3	V

*Note: Supply voltage on any pin should never exceed 4.8 V.*



This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.



This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part.

## 4.6 Terminology

### 4.6.1 Sensitivity

Linear acceleration sensitivity can be determined, for example, by applying 1 g acceleration to the device. Because the sensor can measure DC accelerations, this can be done easily by pointing the selected axis towards the ground, noting the output value, rotating the sensor 180 degrees (pointing towards the sky) and noting the output value again. By doing so,  $\pm 1$  g acceleration is applied to the sensor. Subtracting the larger output value from the smaller one, and dividing the result by 2, leads to the actual sensitivity of the sensor. This value changes very little over temperature and over time. The sensitivity tolerance describes the range of sensitivities of a large number of sensors (see [Table 2](#)).

An angular rate gyroscope is a device that produces a positive-going digital output for counterclockwise rotation around the axis considered. Sensitivity describes the gain of the sensor and can be determined by applying a defined angular velocity to it. This value changes very little over temperature and time (see [Table 2](#)).

### 4.6.2 Zero-g and zero-rate level

Linear acceleration zero-g level offset (TyOff) describes the deviation of an actual output signal from the ideal output signal if no acceleration is present. A sensor in a steady state on a horizontal surface measures 0g on both the X-axis and Y-axis, whereas the Z-axis measures 1 g. Ideally, the output is in the middle of the dynamic range of the sensor (content of OUT registers 00h, data expressed as two's complement number). A deviation from the ideal value in this case is called zero-g offset.

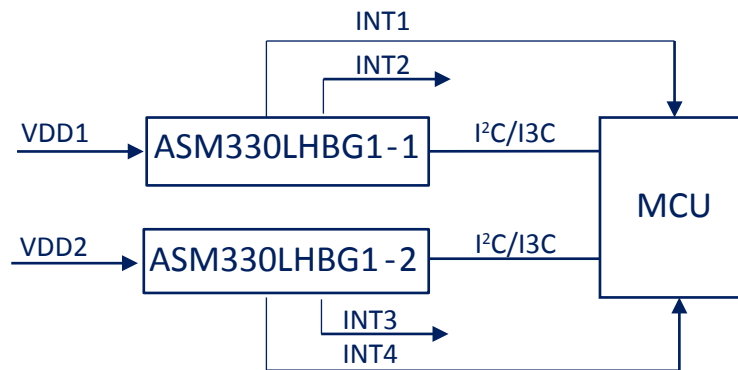
Offset is to some extent a result of stress to the MEMS sensor and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress. Offset changes little over temperature, see "Linear acceleration zero-g level change vs. temperature" in [Table 2](#). The zero-g level tolerance (TyOff) describes the standard deviation of the range of zero-g levels of a group of sensors.

Zero-rate level describes the actual output signal if there is no angular rate present. The zero-rate level of precise MEMS sensors is, to some extent, a result of stress to the sensor and therefore the zero-rate level can slightly change after mounting the sensor onto a printed circuit board or after exposing it to extensive mechanical stress. This value changes very little over temperature and time (see [Table 2](#)).

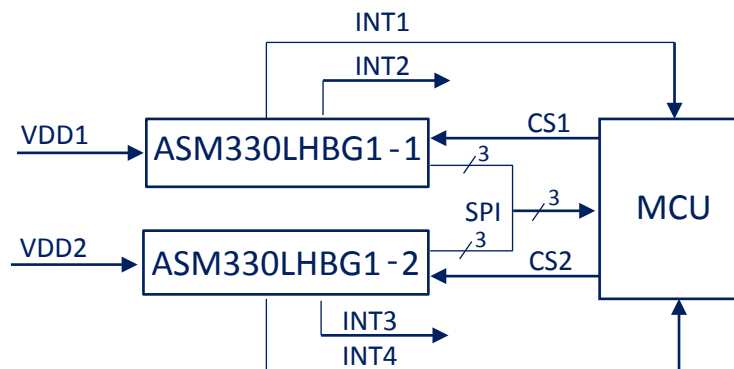
## 5 Digital interfaces

The ASM330LHBG1 offers two communication protocols I<sup>2</sup>C / MIPI I3C<sup>SM</sup> slave interface or SPI (3- and 4-wire) serial interface.

**Figure 7. Reference design - block diagram, I<sup>2</sup>C communication protocol**



**Figure 8. Reference design - block diagram, SPI4 communication protocol**



## 5.1 I<sup>2</sup>C/SPI interface

The registers embedded inside the ASM330LHBG1 may be accessed through both the I<sup>2</sup>C and SPI serial interfaces. The latter may be SW configured to operate either in 3-wire or 4-wire interface mode. The device is compatible with SPI modes 0 and 3.

The serial interfaces are mapped onto the same pins. To select/exploit the I<sup>2</sup>C interface, the CS line must be tied high (that is, connected to Vdd\_IO).

**Table 9. Serial interface pin description**

Pin name	Pin description
CS	Enable SPI I <sup>2</sup> C/SPI mode selection (1: SPI idle mode / I <sup>2</sup> C communication enabled; 0: SPI communication mode / I <sup>2</sup> C disabled)
SCL/SPC	I <sup>2</sup> C serial clock (SCL) SPI serial port clock (SPC)
SDA/SDI/SDO	I <sup>2</sup> C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
SDO/SA0	SPI serial data output (SDO) I <sup>2</sup> C less significant bit of the device address

### 5.1.1 I<sup>2</sup>C serial interface

The ASM330LHBG1 I<sup>2</sup>C is a bus slave. The I<sup>2</sup>C is employed to write the data to the registers, whose content can also be read back.

The relevant I<sup>2</sup>C terminology is provided in the table below.

**Table 10. I<sup>2</sup>C terminology**

Term	Description
Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by the master

There are two signals associated with the I<sup>2</sup>C bus: the serial clock line (SCL) and the serial data line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. Both the lines must be connected to Vdd\_IO through external pull-up resistors. When the bus is free, both the lines are high.

The I<sup>2</sup>C interface is implemented with fast mode (400 kHz) I<sup>2</sup>C standards as well as with the standard mode.

In order to disable the I<sup>2</sup>C block, (I2C\_disable) = 1 must be written in CTRL4\_C (13h).

**5.1.1.1 I<sup>2</sup>C operation**

The transaction on the bus is started through a start (ST) signal. A start condition is defined as a high to low transition on the data line while the SCL line is held high. After this has been transmitted by the master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the master.

The slave address (SAD) associated to the ASM330LHBG1 is 110101xb. The SDO/SA0 pin can be used to modify the less significant bit of the device address. If the SDO/SA0 pin is connected to the supply voltage, LSb is 1 (address 1101011b); else if the SDO/SA0 pin is connected to ground, the LSb value is 0 (address 1101010b). This solution permits to connect and address two different inertial modules to the same I<sup>2</sup>C bus.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line low so that it remains stable low during the high period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The I<sup>2</sup>C embedded inside the ASM330LHBG1 behaves like a slave device and the following protocol must be adhered to. After the start condition (ST) a slave address is sent, once a slave acknowledge (SAK) has been returned, an 8-bit subaddress (SUB) is transmitted. The increment of the address is configured by CTRL3\_C (12h) (IF\_INC).

The slave address is completed with a read/write bit. If the bit is 1 (read), a repeated start (SR) condition must be issued after the two subaddress bytes; if the bit is 0 (write) the master transmits to the slave with direction unchanged. Table 11 explains how the SAD+read/write bit pattern is composed, listing all the possible configurations.

**Table 11. SAD+read/write patterns**

Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	110101	0	1	11010101 (D5h)
Write	110101	0	0	11010100 (D4h)
Read	110101	1	1	11010111 (D7h)
Write	110101	1	0	11010110 (D6h)

**Table 12. Transfer when master is writing one byte to slave**

Master	ST	SAD + W		SUB		DATA		SP
Slave			SAK		SAK		SAK	

**Table 13. Transfer when master is writing multiple bytes to slave**

Master	ST	SAD + W		SUB		DATA		DATA		SP
Slave			SAK		SAK		SAK		SAK	

**Table 14. Transfer when master is receiving (reading) one byte of data from slave**

Master	ST	SAD + W		SUB		SR	SAD + R			NMAK	SP
Slave			SAK		SAK			SAK	DATA		

**Table 15. Transfer when master is receiving (reading) multiple bytes of data from slave**

Master	ST	SAD+W		SUB		SR	SAD+R			MAK		MAK		NMAK	SP
Slave			SAK		SAK			SAK	DATA		DATA		DATA		

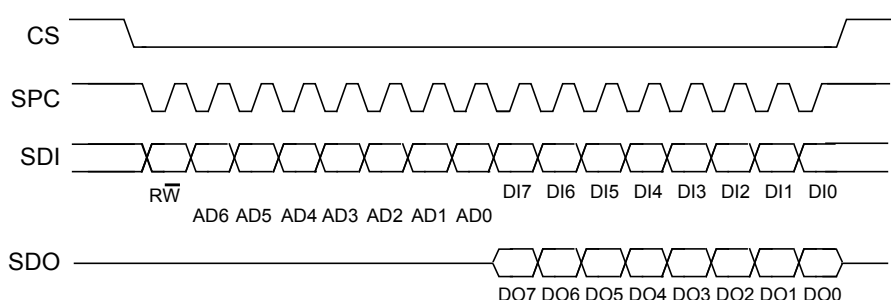
Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the most significant bit (MSb) first. If a slave receiver doesn't acknowledge the slave address (that is, it is not able to receive because it is performing some real-time function) the data line must be left high by the slave. The master can then abort the transfer. A low to high transition on the SDA line while the SCL line is high is defined as a stop condition. Each data transfer must be terminated by the generation of a stop (SP) condition.

In the presented communication format MAK is master acknowledge and NMAK is no master acknowledge.

### 5.1.2 SPI bus interface

The ASM330LHBG1 SPI is a bus slave. The SPI allows writing to and reading from the registers of the device. The serial interface communicates to the application using 4 wires: **CS**, **SPC**, **SDI** and **SDO**.

**Figure 9. Read and write protocol (in mode 3)**



**CS** enables the serial port and it is controlled by the SPI master. It goes low at the start of the transmission and goes back high at the end. **SPC** is the serial port clock and it is controlled by the SPI master. It is stopped high when **CS** is high (no transmission). **SDI** and **SDO** are, respectively, the serial port data input and output. Those lines are driven at the falling edge of **SPC** and should be captured at the rising edge of **SPC**.

Both the read register and write register commands are completed in 16 clock pulses or in multiples of 8 in case of multiple read/write bytes. Bit duration is the time between two falling edges of **SPC**. The first bit (bit 0) starts at the first falling edge of **SPC** after the falling edge of **CS** while the last bit (bit 15, bit 23, ...) starts at the last falling edge of **SPC** just before the rising edge of **CS**.

**bit 0**: RW bit. When 0, the data DI(7:0) is written into the device. When 1, the data DO(7:0) from the device is read. In the latter case, the chip drives **SDO** at the start of bit 8.

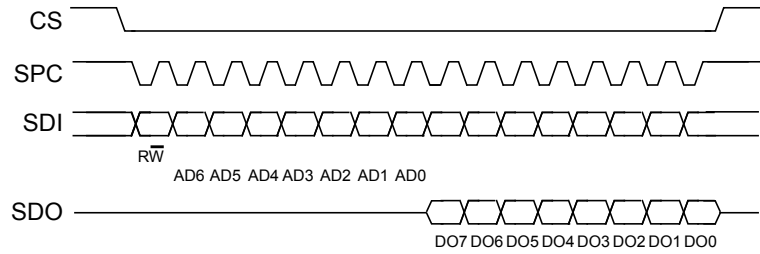
**bit 1-7**: address AD(6:0). This is the address field of the indexed register.

**bit 8-15**: data DI(7:0) (write mode). This is the data that is written into the device (MSb first).

**bit 8-15**: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

In multiple read/write commands further blocks of 8 clock periods are added. When the CTRL3\_C (12h) (IF\_INC) bit is 0, the address used to read/write data remains the same for every block. When the CTRL3\_C (12h) (IF\_INC) bit is 1, the address used to read/write data is increased at every block.

The function and the behavior of **SDI** and **SDO** remain unchanged.

**5.1.2.1 SPI read**
**Figure 10. SPI read protocol (in mode 3)**


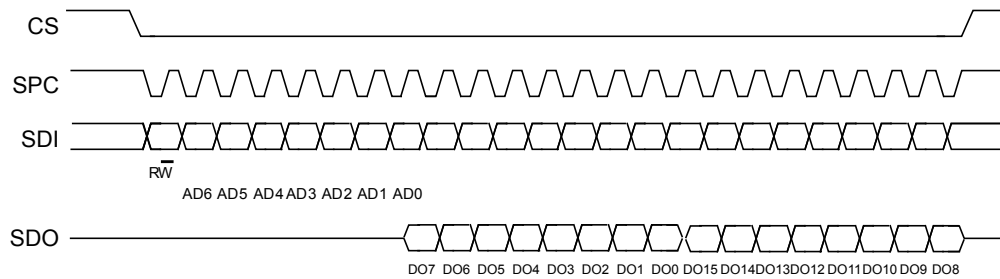
The SPI read command is performed with 16 clock pulses. A multiple byte read command is performed by adding blocks of 8 clock pulses to the previous one.

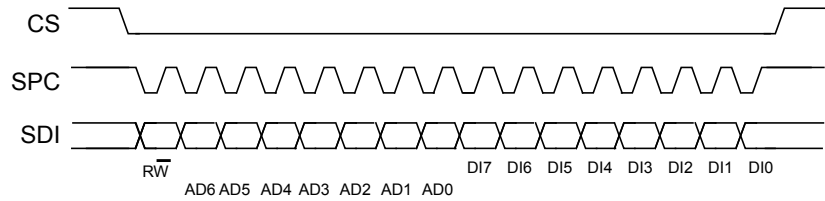
**bit 0:** READ bit. The value is 1.

**bit 1-7:** address AD(6:0). This is the address field of the indexed register.

**bit 8-15:** data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

**bit 16-...:** data DO(...-8). Further data in multiple byte reads.

**Figure 11. Multiple byte SPI read protocol (2-byte example) (in mode 3)**


**5.1.2.2 SPI write**
**Figure 12. SPI write protocol (in mode 3)**


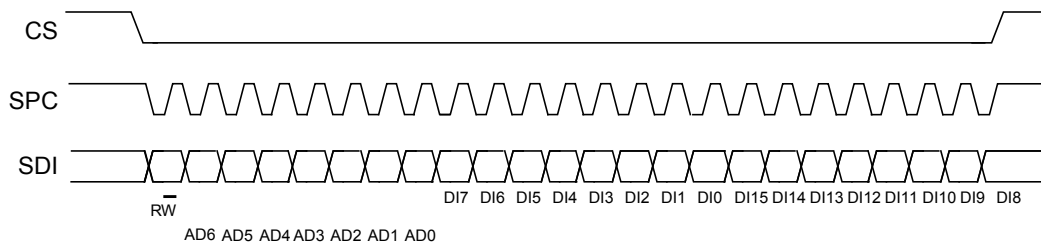
The SPI write command is performed with 16 clock pulses. A multiple byte write command is performed by adding blocks of 8 clock pulses to the previous one.

**bit 0:** WRITE bit. The value is 0.

**bit 1-7:** address AD(6:0). This is the address field of the indexed register.

**bit 8-15:** data DI(7:0) (write mode). This is the data that is written inside the device (MSb first).

**bit 16-...** : data DI(...-8). Further data in multiple byte writes.

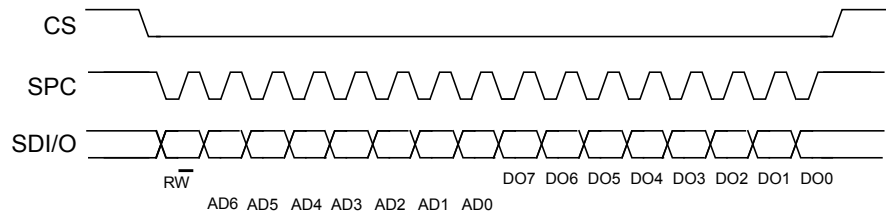
**Figure 13. Multiple byte SPI write protocol (2-byte example) (in mode 3)**




**5.1.2.3 SPI read in 3-wire mode**

A 3-wire mode is entered by setting the CTRL3\_C (12h) (SIM) bit equal to 1 (SPI serial interface mode selection).

**Figure 14. SPI read protocol in 3-wire mode (in mode 3)**



The SPI read command is performed with 16 clock pulses:

**bit 0:** READ bit. The value is 1.

**bit 1-7:** address AD(6:0). This is the address field of the indexed register.

**bit 8-15:** data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

A multiple read command is also available in 3-wire mode.

## 5.2 MIPI I3C<sup>SM</sup> interface

### 5.2.1 MIPI I3C<sup>SM</sup> slave interface

The ASM330LHBG1 interface includes a MIPI I3C<sup>SM</sup> SDR only slave interface with MIPI I3C<sup>SM</sup> SDR embedded features:

- CCC command
- Direct CCC communication (SET and GET)
- Broadcast CCC communication
- Private communications
- Private read and write for single byte
- Multiple read and write
- Error detection and recovery methods

Refer to [Section 5.3 I<sup>2</sup>C/I3C coexistence in ASM330LHBG1](#) for details concerning the choice of the interface when powering up the device.

### 5.2.2 MIPI I3C<sup>SM</sup> CCC supported commands

The list of MIPI I3C<sup>SM</sup> CCC commands supported by the device is detailed in the following table.

**Table 16. MIPI I3C<sup>SM</sup> CCC commands**

Command	Command code	Default	Description
ENTDAA	0x07		DAA procedure
SETDASA	0x87		Assign dynamic address using static address 0x6B/0x6A depending on SDO pin
ENEC	0x80 / 0x00		Slave activity control (direct and broadcast)
DISEC	0x81/ 0x01		Slave activity control (direct and broadcast)
ENTAS0	0x82 / 0x02		Enter activity state (direct and broadcast)
ENTAS1	0x83 / 0x03		Enter activity state (direct and broadcast)
ENTAS2	0x84 / 0x04		Enter activity state (direct and broadcast)
ENTAS3	0x85 / 0x05		Enter activity state (direct and broadcast)
RSTDAA	0x86 / 0x06		Reset the assigned dynamic address (direct and broadcast)
SETMWL	0x89 / 0x08		Define maximum write length during private write (direct and broadcast)
SETMRL	0x8A / 0x09		Define maximum read length during private read (direct and broadcast)
SETNEWDA	0x88		Change dynamic address
GETMWL	0x8B	0x00 0x08 (2 byte)	Get maximum write length during private write
GETMRL	0x8C	0x00 0x10 0x09 (3 byte)	Get maximum read length during private read
GETPID	0x8D	0x02 0x08 0x00 0x6B 0x10 0x0B	Device ID register
GETBCR	0x8E	0x07 (1 byte)	Bus characteristics register
GETDCR	0x8F	0x00	MIPI I3C <sup>SM</sup> device characteristics register
GETSTATUS	0x90	0x00 0x00 (2 byte)	Status register
GETMXDS	0x94	0x00 0x38 (2 byte)	Return max data speed <sup>(1)</sup>

1. Bits[5:3] are set to "111" which indicates that  $T_{sco}$  is greater than 12 nsec. To calculate the effective bus frequency,  $T_{sco}$  should be used together with line capacitance, number of slaves and stubs (if present).

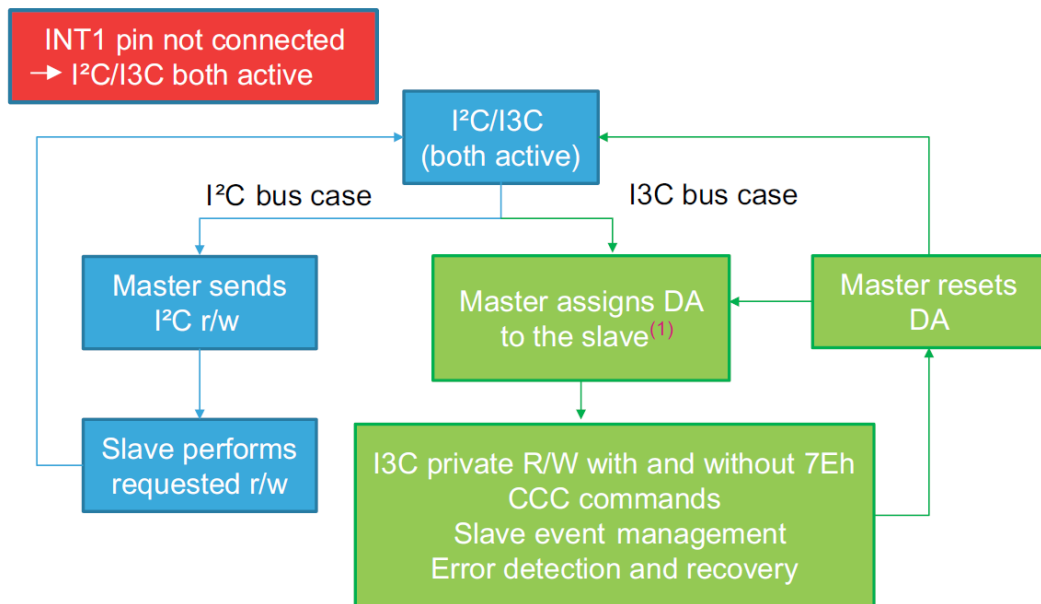
### 5.3 I<sup>2</sup>C/I<sup>3</sup>C coexistence in ASM330LHBG1

In the ASM330LHBG1, the SDA and SCL lines are common to both I<sup>2</sup>C and I<sup>3</sup>C. The I<sup>2</sup>C bus requires anti-spike filters on the SDA and SCL pins that are not compatible with I<sup>3</sup>C timing.

The device can be connected to both I<sup>2</sup>C and I<sup>3</sup>C or only to the I<sup>3</sup>C bus depending on the connection of the INT1 pin when the device is powered up:

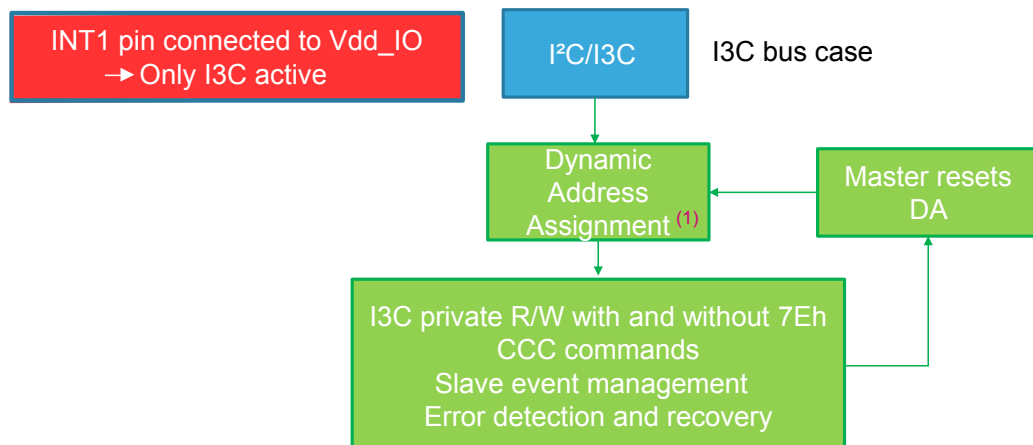
- INT1 pin floating (internal pull-down): I<sup>2</sup>C/I<sup>3</sup>C both active, see Figure 15
- INT1 pin connected to Vdd\_IO: only I<sup>3</sup>C active, see Figure 16

**Figure 15. I<sup>2</sup>C and I<sup>3</sup>C both active (INT1 pin not connected)**



1. Address assignment (DAA or ENTDA) must be performed with I<sup>2</sup>C fast mode plus timing. When the slave is addressed, the I<sup>2</sup>C slave is disabled and the timing is compatible with I<sup>3</sup>C specifications.

**Figure 16. Only I<sup>3</sup>C active (INT1 pin connected to Vdd\_IO)**



1. When the slave is I<sup>3</sup>C only, the I<sup>2</sup>C slave is always disabled. The address can be assigned using I<sup>3</sup>C SDR timing.

## 6 Functionality

### 6.1 Operating modes

In the ASM330LHBG1, the accelerometer and the gyroscope can be turned on/off independently of each other and are allowed to have different ODRs and power modes.

The ASM330LHBG1 has three operating modes available:

- Only accelerometer active and gyroscope in power-down or sleep mode
- Only gyroscope active and accelerometer in power-down
- Both accelerometer and gyroscope sensors active with independent ODR

The accelerometer is activated from power-down by writing ODR\_XL[3:0] in [CTRL1\\_XL \(10h\)](#) while the gyroscope is activated from power-down by writing ODR\_G[3:0] in [CTRL2\\_G \(11h\)](#). For combo mode the ODRs are totally independent.

*Note:* *If the accelerometer is to be activated in high-performance operating mode while the gyroscope is already running (that is, the gyroscope is not in power-down mode), proceed as follows:*

1. *Disable the accelerometer high-performance operating mode (set the XL\_HM\_MODE bit to 1 in the [CTRL6\\_C \(15h\)](#) register).*
2. *Write the [CTRL1\\_XL \(10h\)](#) register to 50h.*
3. *Read the [OUTZ\\_H\\_A \(2Dh\)](#) register to clear the XLDA bit in the [STATUS\\_REG \(1Eh\)](#) register.*
4. *Wait for 1/ODR\_XL time period or wait until the XLDA bit in the [STATUS\\_REG \(1Eh\)](#) register becomes equal to 1.*
5. *Enable the accelerometer high-performance operating mode (set the XL\_HM\_MODE bit to 0 in the [CTRL6\\_C \(15h\)](#) register).*
6. *Write the [CTRL1\\_XL \(10h\)](#) register to the desired value.*

### 6.2 Gyroscope power modes

In the ASM330LHBG1, the gyroscope can be configured in two different operating modes: low-power and high-performance mode. The operating mode selected depends on the value of the G\_HM\_MODE bit in [CTRL7\\_G \(16h\)](#). If G\_HM\_MODE is set to 0, high-performance mode is valid for all ODRs (from 12.5 Hz up to 1.67 kHz).

To enable low-power mode, the G\_HM\_MODE bit has to be set to 1. Low-power mode is available for ODRs equal to 12.5 Hz, 26 Hz, 52 Hz, 104 Hz and 208 Hz.

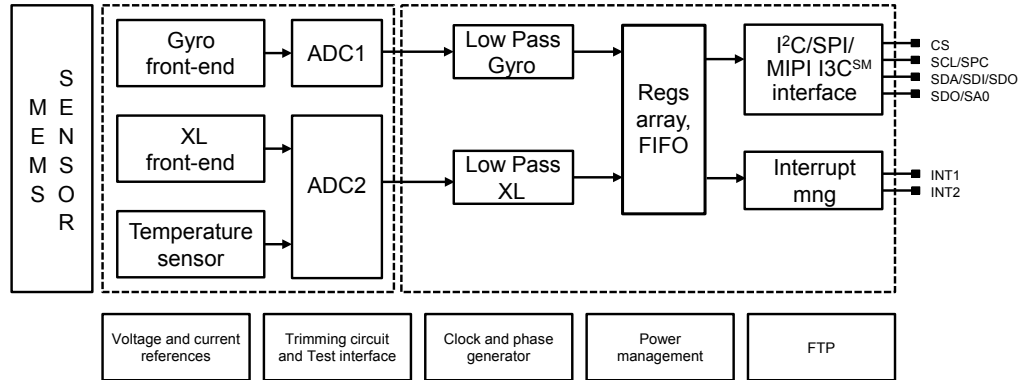
### 6.3 Accelerometer power modes

In the ASM330LHBG1, the accelerometer can be configured in two different operating modes: low-power and high-performance mode. The operating mode selected depends on the value of the XL\_HM\_MODE bit in [CTRL6\\_C \(15h\)](#). If XL\_HM\_MODE is set to 0, high-performance mode is valid for all ODRs (from 12.5 Hz up to 1.67 kHz).

To enable low-power mode, the XL\_HM\_MODE bit has to be set to 1. Low-power mode is available for ODRs equal to 1.6 Hz, 12.5 Hz, 26 Hz, 52 Hz, 104 Hz and 208 Hz.

## 6.4 Block diagram of filters

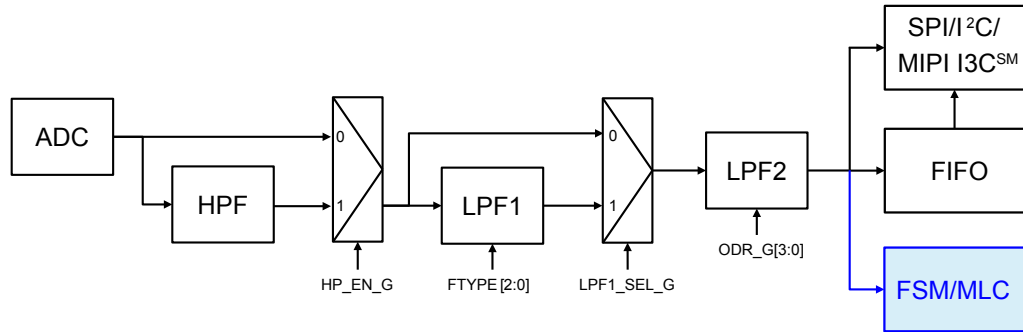
Figure 17. Block diagram of filters



### 6.4.1 Block diagram of the gyroscope filter

The gyroscope filtering chain appears below.

**Figure 18. Gyroscope filtering chain**



The gyroscope ODR is selectable from 12.5 Hz up to 1.67 kHz. A low-pass filter (LPF1) is available, for more details about the filter characteristics see [Table 58. Gyroscope LPF1 bandwidth selection](#). The digital LPF2 filter cannot be configured by the user and its cutoff frequency depends on the selected gyroscope ODR, as indicated in the following table.

Data can be acquired from the output registers and FIFO.

**Table 17. Gyroscope LPF2 bandwidth selection**

Gyroscope ODR [Hz]	LPF2 cutoff [Hz]
12.5	4.3
26	8.3
52	16.7
104	33
208	67
417	133
833	267
1667	539

### 6.4.2 Block diagrams of the accelerometer filters

In the ASM330LHBG1, the filtering chain for the accelerometer part is composed of the following:

- Digital filter (LPF1)
- Composite filter

Details of the block diagram appear in the following figure.

Figure 19. Accelerometer chain

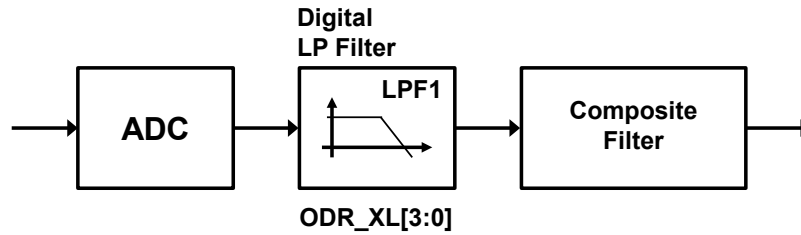
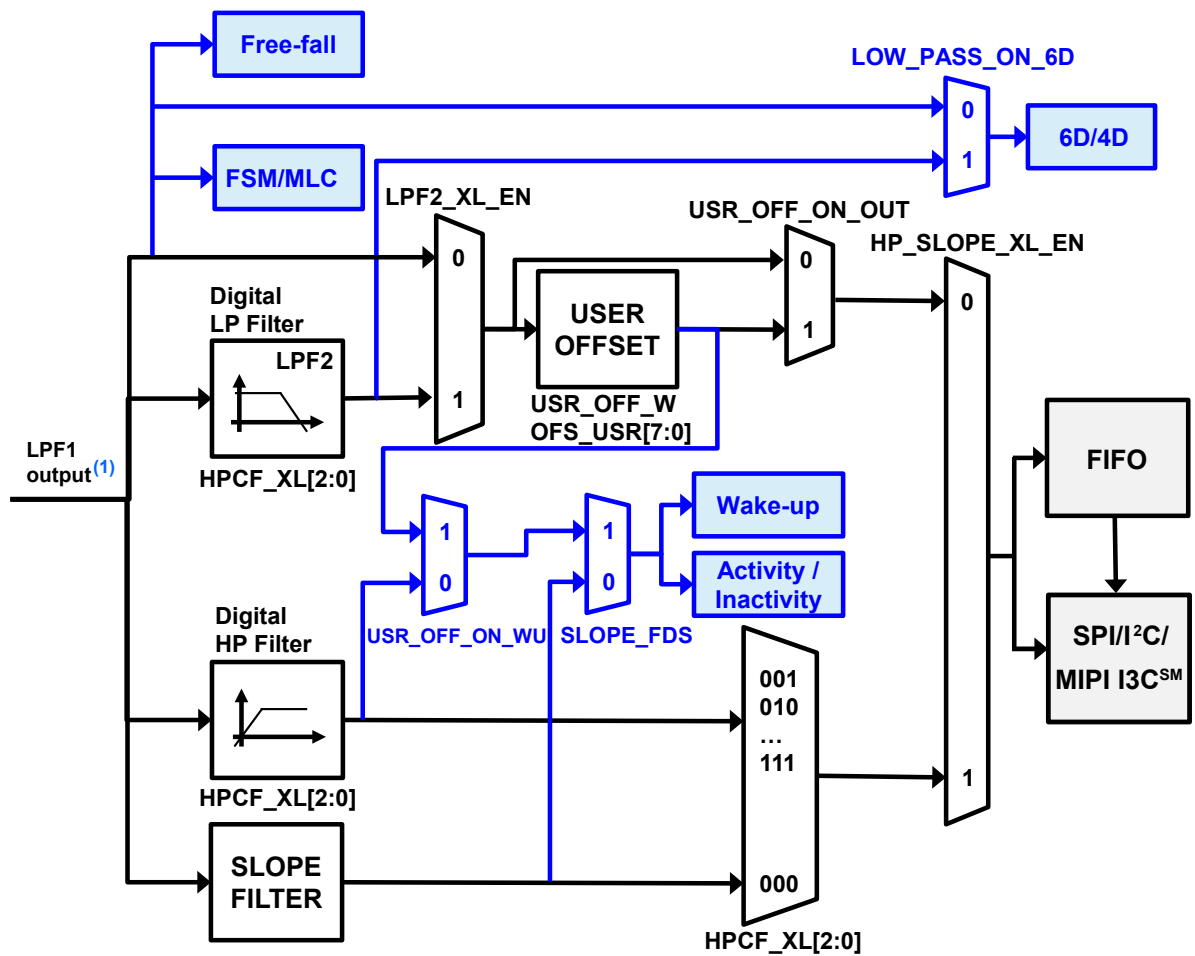


Figure 20. Accelerometer composite filter



1. The cutoff value of the LPF1 output is  $ODR/2$  when the accelerometer is in high-performance mode and  $ODR$  up to 833 Hz. This value is equal to 780 Hz when the accelerometer is in low-power mode.



## 6.5 FIFO

The presence of a FIFO allows consistent power saving for the system since the host processor does not need continuously poll data from the sensor, but it can wake up only when needed and burst the significant data out from the FIFO.

The ASM330LHBG1 embeds 3 KB of data in FIFO to store the following data:

- Gyroscope
- Accelerometer
- Timestamp
- Temperature

Writing data in the FIFO is triggered by the accelerometer / gyroscope data-ready signal.

The applications have maximum flexibility in choosing the rate of batching for physical sensors with FIFO-dedicated configurations: accelerometer, gyroscope and temperature sensor batch rates can be selected by the user. It is possible to select decimation for timestamp batching in FIFO with a factor of 1, 8, or 32.

The reconstruction of a FIFO stream is a simple task thanks to the FIFO\_DATA\_OUT\_TAG byte that allows recognizing the meaning of a word in FIFO.

FIFO allows correct reconstruction of the timestamp information for each sensor stored in FIFO. If a change in the ODR or BDR (batch data rate) configuration is performed, the application can correctly reconstruct the timestamp and know exactly when the change was applied without disabling FIFO batching. FIFO stores information of the new configuration and timestamp in which the change was applied in the device.

The programmable FIFO watermark threshold can be set in FIFO\_CTRL1 (07h) and FIFO\_CTRL2 (08h) using the WTM[8:0] bits. To monitor the FIFO status, dedicated registers (FIFO\_STATUS1 (3Ah), FIFO\_STATUS2 (3Bh)) can be read to detect FIFO overrun events, FIFO full status, FIFO empty status, FIFO watermark status and the number of unread samples stored in the FIFO. To generate dedicated interrupts on the INT1 and INT2 pins of these status events, the configuration can be set in INT1\_CTRL (0Dh) and INT2\_CTRL (0Eh).

The FIFO buffer can be configured according to six different modes:

- Bypass mode
- FIFO mode
- Continuous mode
- Continuous-to-FIFO mode
- Bypass-to-continuous mode
- Bypass-to-FIFO mode

Each mode is selected by the FIFO\_MODE\_[2:0] bits in the FIFO\_CTRL4 (0Ah) register.

### 6.5.1 Bypass mode

In bypass mode (FIFO\_CTRL4 (0Ah)(FIFO\_MODE\_[2:0] = 000), the FIFO is not operational and it remains empty. Bypass mode is also used to reset the FIFO when in FIFO mode.

### 6.5.2 FIFO mode

In FIFO mode (**FIFO\_CTRL4 (0Ah)**(**FIFO\_MODE\_[2:0] = 001**) data from the output channels are stored in the FIFO until it is full.

To reset FIFO content, bypass mode should be selected by writing **FIFO\_CTRL4 (0Ah)**(**FIFO\_MODE\_[2:0]**) to 000. After this reset command, it is possible to restart FIFO mode by writing **FIFO\_CTRL4 (0Ah)** (**FIFO\_MODE\_[2:0]**) to 001.

The FIFO buffer memorizes up to 3 KB of data but the depth of the FIFO can be resized by setting the **WTM[8:0]** bits in **FIFO\_CTRL1 (07h)** and **FIFO\_CTRL2 (08h)**. If the **STOP\_ON\_WTM** bit in **FIFO\_CTRL2 (08h)** is set to 1, FIFO depth is limited up to the **WTM[8:0]** bits in **FIFO\_CTRL1 (07h)** and **FIFO\_CTRL2 (08h)**.

### 6.5.3 Continuous mode

Continuous mode (**FIFO\_CTRL4 (0Ah)**(**FIFO\_MODE\_[2:0] = 110**) provides a continuous FIFO update: as new data arrives, the older data is discarded.

A FIFO threshold flag **FIFO\_STATUS2 (3Bh)**(**FIFO\_WTM\_IA**) is asserted when the number of unread samples in FIFO is greater than or equal to **FIFO\_CTRL1 (07h)** and **FIFO\_CTRL2 (08h)** (**WTM[8:0]**).

It is possible to route the **FIFO\_WTM\_IA** flag to the **INT1** pin by writing in register **INT1\_CTRL (0Dh)** (**INT1\_FIFO\_TH**) = 1 or to the **INT2** pin by writing in register **INT2\_CTRL (0Eh)**(**INT2\_FIFO\_TH**) = 1.

A full-flag interrupt can be enabled, **INT1\_CTRL (0Dh)**(**INT1\_FIFO\_FULL**) = 1 or **INT2\_CTRL (0Eh)** (**INT2\_FIFO\_FULL**) = 1, in order to indicate FIFO saturation and eventually read its content all at once.

If an overrun occurs, at least one of the oldest samples in FIFO has been overwritten and the **FIFO\_OVR\_IA** flag in **FIFO\_STATUS2 (3Bh)** is asserted.

In order to empty the FIFO before it is full, it is also possible to pull from FIFO the number of unread samples available in **FIFO\_STATUS1 (3Ah)** and **FIFO\_STATUS2 (3Bh)**(**DIFF\_FIFO\_[9:0]**).

### 6.5.4 Continuous-to-FIFO mode

In continuous-to-FIFO mode (**FIFO\_CTRL4 (0Ah)**(**FIFO\_MODE\_[2:0] = 011**), FIFO behavior changes according to the trigger event detected in one of the following interrupt events:

- Wake-up
- Free-fall
- D6D

When the selected trigger bit is equal to 1, FIFO operates in FIFO mode.

When the selected trigger bit is equal to 0, FIFO operates in continuous mode.

### 6.5.5 Bypass-to-continuous mode

In bypass-to-continuous mode (**FIFO\_CTRL4 (0Ah)**(**FIFO\_MODE\_[2:0] = 100**), data measurement storage inside FIFO operates in continuous mode when selected triggers are equal to 1, otherwise FIFO content is reset (bypass mode).

FIFO behavior changes according to the trigger event detected in one of the following interrupt events:

- Wake-up
- Free-fall
- D6D

### 6.5.6 Bypass-to-FIFO mode

In bypass-to-FIFO mode (**FIFO\_CTRL4 (0Ah)**(**FIFO\_MODE\_[2:0] = 111**), data measurement storage inside FIFO operates in FIFO mode when selected triggers are equal to 1, otherwise FIFO content is reset (bypass mode).

FIFO behavior changes according to the trigger event detected in one of the following interrupt events:

- Wake-up
- Free-fall
- D6D

### 6.5.7 FIFO reading procedure

The data stored in FIFO are accessible from dedicated registers and each FIFO word is composed of 7 bytes: one tag byte (`FIFO_DATA_OUT_TAG` (78h)), in order to identify the sensor, and 6 bytes of fixed data (`FIFO_DATA_OUT` registers from (79h) to (7Eh)).

The `DIFF_FIFO_[9:0]` field in the `FIFO_STATUS1` (3Ah) and `FIFO_STATUS2` (3Bh) registers contains the number of words (1 byte TAG + 6 bytes DATA) collected in FIFO.

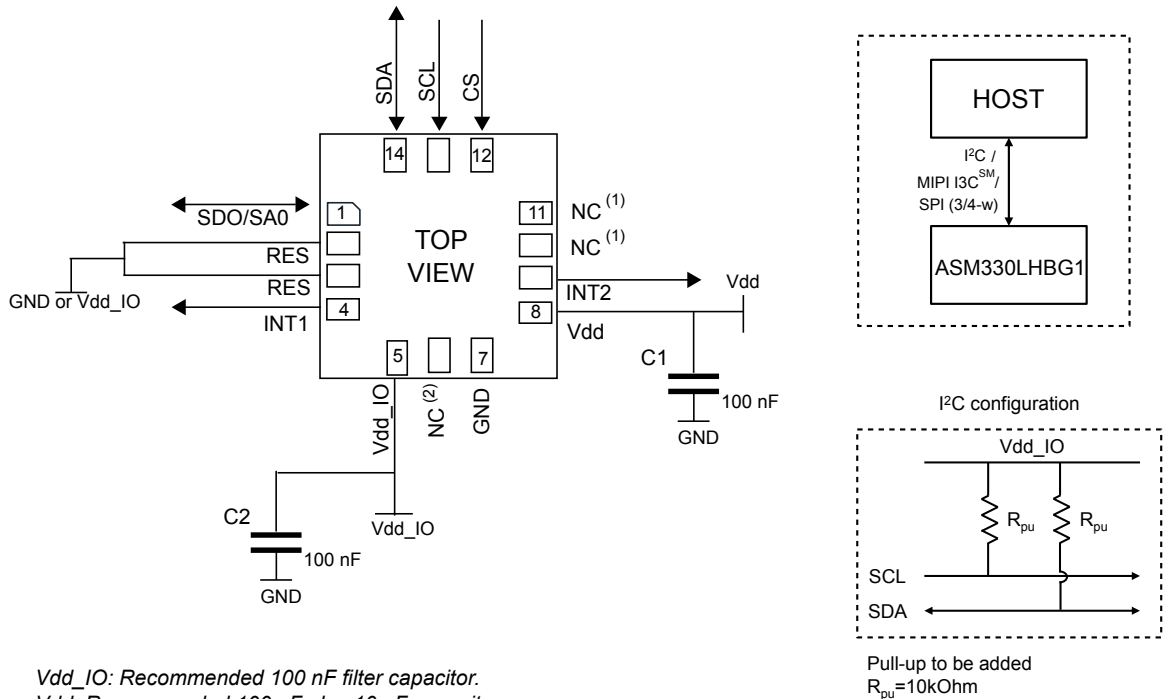
In addition, it is possible to configure a counter of the batch events of accelerometer or gyroscope sensors. The flag `COUNTER_BDR_IA` in `FIFO_STATUS2` (3Bh) alerts that the counter reaches a selectable threshold (`CNT_BDR_TH_[10:0]` field in `COUNTER_BDR_REG1` (0Bh) and `COUNTER_BDR_REG2` (0Ch)). This allows triggering the reading of FIFO with the desired latency of one single sensor. The sensor is selectable using the `TRIG_COUNTER_BDR` bit in `COUNTER_BDR_REG1` (0Bh). As for the other FIFO status events, the flag `COUNTER_BDR_IA` can be routed to the INT1 or INT2 pins by asserting the corresponding bits (`INT1_CNT_BDR` of `INT1_CTRL` (0Dh) and `INT2_CNT_BDR` of `INT2_CTRL` (0Eh)).

Meta information about accelerometer and gyroscope sensor configuration changes can be managed by enabling the `ODR_CHG_EN` bit in `FIFO_CTRL2` (08h).

## 7 Application hints

### 7.1 ASM330LHBG1 electrical connections

Figure 21. ASM330LHBG1 electrical connections



1. Leave pin electrically unconnected and soldered to PCB.
2. Connect to Vdd\_IO or GND or leave unconnected and soldered to PCB.

The device core is supplied through the Vdd line. Power supply decoupling capacitors (C1, C2 = 100 nF ceramic) should be placed as near as possible to the supply pin of the device (common design practice).

The functionality of the device and the measured acceleration/angular rate data is selectable and accessible through the SPI/I<sup>2</sup>C/MIPI I3C<sup>SM</sup> primary interface.

The functions, the threshold and the timing of the two interrupt pins for each sensor can be completely programmed by the user through the SPI/I<sup>2</sup>C/MIPI I3C<sup>SM</sup> primary interface.

**Table 18. Internal pin status**

Pin #	Name	Pin function	Pin status
1	SDO	SPI 4-wire interface serial data output (SDO)	Default: input without pull-up Pull-up is enabled if bit SDO_PU_EN = 1 in register PIN_CTRL (02h).
	SA0	I <sup>2</sup> C least significant bit of the device address (SA0) MIPI I3C <sup>SM</sup> least significant bit of the static address (SA0)	
2	RES	Connect to Vdd_IO or GND	
3	RES	Connect to Vdd_IO or GND	
4	INT1	Programmable interrupt 1. If device is used as MIPI I3C <sup>SM</sup> pure slave, this pin must be set to 1.	Default: input with pull-down <sup>(1)</sup> Pull-down is disabled if bit PD_DIS_INT1 = 1 in register I3C_BUS_AVB (62h).
5	Vdd_IO	Power supply for I/O pins	
6	NC	Connect to Vdd_IO or GND or leave unconnected	
7	GND	0 V supply	
8	Vdd	Power supply	
9	INT2	Programmable interrupt 2 (INT2) / data enabled (DEN)	Default: output forced to ground
10	NC	Leave unconnected	
11	NC	Leave unconnected	
12	CS	I <sup>2</sup> C and MIPI I3C <sup>SM</sup> /SPI mode selection (1:SPI idle mode / I <sup>2</sup> C and MIPI I3C <sup>SM</sup> communication enabled; 0: SPI communication mode / I <sup>2</sup> C and MIPI I3C <sup>SM</sup> disabled)	Default: input with pull-up Pull-up is disabled if bit I2C_disable = 1 in register CTRL4_C (13h) and I3C_disable = 1 in register CTRL9_XL (18h).
13	SCL	I <sup>2</sup> C/MIPI I3C <sup>SM</sup> serial clock (SCL) / SPI serial port clock (SPC)	Default: input without pull-up
14	SDA	I <sup>2</sup> C/MIPI I3C <sup>SM</sup> serial data (SDA) / SPI serial data input (SDI) / 3-wire interface serial data output (SDO)	Default: input without pull-up

1. INT1 must be set to 0 or left unconnected during power-on if the I<sup>2</sup>C/SPI interfaces are used.

Internal pull-up value is from 30 kΩ to 50 kΩ, depending on Vdd\_IO.

Note:

The procedure to enable the pull-up on pins 2 and 3 is as follows:

1. From the primary I<sup>2</sup>C/I3C/SPI interface: write 40h in register at address 01h
2. From the primary I<sup>2</sup>C/I3C/SPI interface: write 08h in register at address 14h (enable the pull-up on pins 2 and 3)
3. From the primary I<sup>2</sup>C/I3C/SPI interface: write 00h in register at address 01h

## 8 Register map

The table given below provides a list of the 8/16-bit registers embedded in the device and the corresponding addresses.

**Table 19. Registers address map**

Name	Type	Register address		Default	Comment
		Hex	Binary		
FUNC_CFG_ACCESS	R/W	01	00000001	00000000	
PIN_CTRL	R/W	02	00000010	00111111	
RESERVED	-	03-06			Reserved
FIFO_CTRL1	R/W	07	00000111	00000000	
FIFO_CTRL2	R/W	08	00001000	00000000	
FIFO_CTRL3	R/W	09	00001001	00000000	
FIFO_CTRL4	R/W	0A	00001010	00000000	
COUNTER_BDR_REG1	R/W	0B	00001011	00000000	
COUNTER_BDR_REG2	R/W	0C	00001100	00000000	
INT1_CTRL	R/W	0D	00001101	00000000	
INT2_CTRL	R/W	0E	00001110	00000000	
WHO_AM_I	R	0F	00001111	01101011	
CTRL1_XL	R/W	10	00010000	00000000	
CTRL2_G	R/W	11	00010001	00000000	
CTRL3_C	R/W	12	00010010	00000100	
CTRL4_C	R/W	13	00010011	00000000	
CTRL5_C	R/W	14	00010100	00000000	
CTRL6_C	R/W	15	00010101	00000000	
CTRL7_G	R/W	16	00010110	00000000	
CTRL8_XL	R/W	17	00010111	00000000	
CTRL9_XL	R/W	18	00011000	11100000	
CTRL10_C	R/W	19	00011001	00000000	
ALL_INT_SRC	R	1A	00011010	output	
WAKE_UP_SRC	R	1B	00011011	output	
RESERVED	-	1C			Reserved
D6D_SRC	R	1D	00011101	output	
STATUS_REG	R	1E	00011110	output	
RESERVED	-	1F			Reserved
OUT_TEMP_L	R	20	00100000	output	
OUT_TEMP_H	R	21	00100001	output	
OUTX_L_G	R	22	00100010	output	
OUTX_H_G	R	23	00100011	output	
OUTY_L_G	R	24	00100100	output	
OUTY_H_G	R	25	00100101	output	
OUTZ_L_G	R	26	00100110	output	

Name	Type	Register address		Default	Comment
		Hex	Binary		
OUTZ_H_G	R	27	00100111	output	
OUTX_L_A	R	28	00101000	output	
OUTX_H_A	R	29	00101001	output	
OUTY_L_A	R	2A	00101010	output	
OUTY_H_A	R	2B	00101011	output	
OUTZ_L_A	R	2C	00101100	output	
OUTZ_H_A	R	2D	00101101	output	
RESERVED	-	2E-34			Reserved
EMB_FUNC_STATUS_MAINPAGE	R	35	00110101	output	
FSM_STATUS_A_MAINPAGE	R	36	00110110	output	
FSM_STATUS_B_MAINPAGE	R	37	00110111	output	
MLC_STATUS_MAINPAGE	R	38	00111000	output	
RESERVED	-	39			Reserved
FIFO_STATUS1	R	3A	00111010	output	
FIFO_STATUS2	R	3B	00111011	output	
RESERVED	-	3C-3F			Reserved
TIMESTAMP0_REG	R	40	01000000	output	
TIMESTAMP1_REG	R	41	01000001	output	
TIMESTAMP2_REG	R	42	01000010	output	
TIMESTAMP3_REG	R	43	01000011	output	
RESERVED	-	44-55			Reserved
INT_CFG0	R/W	56	01010110	00000000	
RESERVED	-	57			Reserved
INT_CFG1	R/W	58	01011000	00000000	
THS_6D	R/W	59	01011001	00000000	
RESERVED	-	5A			Reserved
WAKE_UP_THS	R/W	5B	01011011	00000000	
WAKE_UP_DUR	R/W	5C	01011100	00000000	
FREE_FALL	R/W	5D	01011101	00000000	
MD1_CFG	R/W	5E	01011110	00000000	
MD2_CFG	R/W	5F	01011111	00000000	
RESERVED	-	60-61		00000000	Reserved
I3C_BUS_AVB	R/W	62	01100010	00000000	
INTERNAL_FREQ_FINE	R	63	01100011	output	
RESERVED	-	64-72			Reserved
X_OFS_USR	R/W	73	01110011	00000000	
Y_OFS_USR	R/W	74	01110100	00000000	
Z_OFS_USR	R/W	75	01110101	00000000	
RESERVED	-	76-77			Reserved
FIFO_DATA_OUT_TAG	R	78	01111000	output	

Name	Type	Register address		Default	Comment
		Hex	Binary		
FIFO_DATA_OUT_X_L	R	79	01111001	output	
FIFO_DATA_OUT_X_H	R	7A	01111010	output	
FIFO_DATA_OUT_Y_L	R	7B	01111011	output	
FIFO_DATA_OUT_Y_H	R	7C	01111100	output	
FIFO_DATA_OUT_Z_L	R	7D	01111101	output	
FIFO_DATA_OUT_Z_H	R	7E	01111110	output	

Reserved registers must not be changed. Writing to those registers may cause permanent damage to the device. The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.



## 9 Register description

The device contains a set of registers which are used to control its behavior and to retrieve linear acceleration, angular rate and temperature data. The register addresses, made up of 7 bits, are used to identify them and to write data through the serial interface.

### 9.1 FUNC\_CFG\_ACCESS (01h)

Enable embedded functions register (R/W)

**Table 20. FUNC\_CFG\_ACCESS register**

FUNC_CFG_ACCESS	0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>
-----------------	------------------	------------------	------------------	------------------	------------------	------------------	------------------

1. This bit must be set to 0 for the correct operation of the device.

**Table 21. FUNC\_CFG\_ACCESS register description**

FUNC_CFG_ACCESS	Enables access to the embedded functions configuration registers. Default value: 0 <sup>(1)</sup>
-----------------	---

1. Details concerning the embedded functions configuration registers are available in [Section 10 Embedded functions register mapping](#) and [Section 11 Embedded functions register description](#).

### 9.2 PIN\_CTRL (02h)

Enable/disable SDO pin pull-up register (R/W)

**Table 22. PIN\_CTRL register**

0 <sup>(1)</sup>	SDO_PU_EN	1 <sup>(2)</sup>	1 <sup>(2)</sup>	1 <sup>(2)</sup>	1 <sup>(2)</sup>	1 <sup>(2)</sup>	1 <sup>(2)</sup>
------------------	-----------	------------------	------------------	------------------	------------------	------------------	------------------

1. This bit must be set to 0 for the correct operation of the device.
2. This bit must be set to 1 for the correct operation of the device.

**Table 23. PIN\_CTRL register description**

SDO_PU_EN	Enables pull-up on SDO pin. Default value: 0 (0: SDO pin pull-up disconnected (default); 1: SDO pin with pull-up)
-----------	--

### 9.3 FIFO\_CTRL1 (07h)

FIFO control register 1 (R/W)

**Table 24. FIFO\_CTRL1 register**

WTM7	WTM6	WTM5	WTM4	WTM3	WTM2	WTM1	WTM0
------	------	------	------	------	------	------	------

**Table 25. FIFO\_CTRL1 register description**

WTM[7:0]	FIFO watermark threshold, in conjunction with WTM8 in <a href="#">FIFO_CTRL2 (08h)</a> 1 LSB = 1 sensor (6 bytes) + TAG (1 byte) written in FIFO Watermark flag rises when the number of bytes written in the FIFO is greater than or equal to the threshold level.
----------	---

### 9.4 FIFO\_CTRL2 (08h)

FIFO control register 2 (R/W)

**Table 26. FIFO\_CTRL2 register**

STOP_ON_WTM	0 <sup>(1)</sup>	0 <sup>(1)</sup>	ODRCHG_EN	0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>	WTM8
-------------	------------------	------------------	-----------	------------------	------------------	------------------	------

1. This bit must be set to 0 for the correct operation of the device.

**Table 27. FIFO\_CTRL2 register**

STOP_ON_WTM	Sensing chain FIFO stop values memorization at threshold level (0: FIFO depth is not limited (default); 1: FIFO depth is limited to the threshold level, defined in <a href="#">FIFO_CTRL1 (07h)</a> and <a href="#">FIFO_CTRL2 (08h)</a>
ODRCHG_EN	Enables ODR CHANGE virtual sensor to be batched in FIFO
WTM8	FIFO watermark threshold, in conjunction with WTM[7:0] in <a href="#">FIFO_CTRL1 (07h)</a> 1 LSB = 1 sensor (6 bytes) + TAG (1 byte) written in FIFO Watermark flag rises when the number of bytes written in FIFO is greater than or equal to the threshold level.

## 9.5 FIFO\_CTRL3 (09h)

FIFO control register 3 (R/W)

**Table 28. FIFO\_CTRL3 register**

BDR_GY_3	BDR_GY_2	BDR_GY_1	BDR_GY_0	BDR_XL_3	BDR_XL_2	BDR_XL_1	BDR_XL_0
----------	----------	----------	----------	----------	----------	----------	----------

**Table 29. FIFO\_CTRL3 register description**

BDR_GY_[3:0]	<p>Selects batch data rate (write frequency in FIFO) for gyroscope data.</p> <p>(0000: gyroscope not batched in FIFO (default);</p> <p>0001: 12.5 Hz;</p> <p>0010: 26 Hz;</p> <p>0011: 52 Hz;</p> <p>0100: 104 Hz;</p> <p>0101: 208 Hz;</p> <p>0110: 417 Hz;</p> <p>0111: 833 Hz;</p> <p>1000: 1667 Hz;</p> <p>1001: reserved;</p> <p>1010: reserved;</p> <p>1011: 6.5 Hz;</p> <p>1100-1111: reserved)</p>
BDR_XL_[3:0]	<p>Selects batch data rate (write frequency in FIFO) for accelerometer data.</p> <p>(0000: accelerometer not batched in FIFO (default);</p> <p>0001: 12.5 Hz;</p> <p>0010: 26 Hz;</p> <p>0011: 52 Hz;</p> <p>0100: 104 Hz;</p> <p>0101: 208 Hz;</p> <p>0110: 417 Hz;</p> <p>0111: 833 Hz;</p> <p>1000: 1667 Hz;</p> <p>1001: reserved;</p> <p>1010: reserved;</p> <p>1011: 1.6 Hz;</p> <p>1100-1111: reserved)</p>

## 9.6 FIFO\_CTRL4 (0Ah)

FIFO control register 4 (R/W)

**Table 30. FIFO\_CTRL4 register**

DEC_TS_BATCH_1	DEC_TS_BATCH_0	ODR_T_BATCH_1	ODR_T_BATCH_0	0 <sup>(1)</sup>	FIFO_MODE2	FIFO_MODE1	FIFO_MODE0
----------------	----------------	---------------	---------------	------------------	------------	------------	------------

1. This bit must be set to 0 for the correct operation of the device.

**Table 31. FIFO\_CTRL4 register description**

DEC_TS_BATCH_[1:0]	Selects decimation for timestamp batching in FIFO. The write rate is the maximum rate between the accelerometer and gyroscope BDR divided by decimation decoder. (00: timestamp not batched in FIFO (default); 01: decimation 1: $\max(\text{BDR\_XL}[\text{Hz}], \text{BDR\_GY}[\text{Hz}])$ [Hz]; 10: decimation 8: $\max(\text{BDR\_XL}[\text{Hz}], \text{BDR\_GY}[\text{Hz}])/8$ [Hz]; 11: decimation 32: $\max(\text{BDR\_XL}[\text{Hz}], \text{BDR\_GY}[\text{Hz}])/32$ [Hz])
ODR_T_BATCH_[1:0]	Selects batch data rate (write frequency in FIFO) for temperature data (00: temperature not batched in FIFO (default); 01: 1.6 Hz; 10: 12.5 Hz; 11: 52 Hz)
FIFO_MODE[2:0]	FIFO mode selection (000: bypass mode: FIFO disabled; 001: FIFO mode: stops collecting data when FIFO is full; 010: reserved; 011: continuous-to-FIFO mode: continuous mode until trigger is deasserted, then FIFO mode; 100: bypass-to-continuous mode: bypass mode until trigger is deasserted, then continuous mode; 101: reserved; 110: continuous mode: if the FIFO is full, the new sample overwrites the older one; 111: bypass-to-FIFO mode: bypass mode until trigger is deasserted, then FIFO mode.)

## 9.7 COUNTER\_BDR\_REG1 (0Bh)

Counter batch data rate register 1 (R/W)

**Table 32. COUNTER\_BDR\_REG1 register**

dataready_pulsed	RST_COUNTER_BDR	TRIG_COUNTER_BDR	0 <sup>(1)</sup>	0 <sup>(1)</sup>	CNT_BDR_TH_10	CNT_BDR_TH_9	CNT_BDR_TH_8
------------------	-----------------	------------------	------------------	------------------	---------------	--------------	--------------

1. This bit must be set to 0 for the correct operation of the device.

**Table 33. COUNTER\_BDR\_REG1 register description**

dataready_pulsed	Enables pulsed data-ready mode (0: data-ready latched mode (returns to 0 only after an interface reading) (default); 1: data-ready pulsed mode (the data ready pulses are 75 µs long)
RST_COUNTER_BDR	Resets the internal counter of batch events for a single sensor. This bit is automatically reset to zero if it was set to 1.
TRIG_COUNTER_BDR	Selects the trigger for the internal counter of batch events between the accelerometer and gyroscope. (0: accelerometer batch event; 1: gyroscope batch event)
CNT_BDR_TH_[10:8]	In conjunction with CNT_BDR_TH_[7:0] in <a href="#">COUNTER_BDR_REG2 (0Ch)</a> , sets the threshold for the internal counter of batch events. When this counter reaches the threshold, the counter is reset and the COUNTER_BDR_IA flag in <a href="#">FIFO_STATUS2 (3Bh)</a> is set to 1.

## 9.8 COUNTER\_BDR\_REG2 (0Ch)

Counter batch data rate register 2 (R/W)

**Table 34. COUNTER\_BDR\_REG2 register**

CNT_BDR_TH_7	CNT_BDR_TH_6	CNT_BDR_TH_5	CNT_BDR_TH_4	CNT_BDR_TH_3	CNT_BDR_TH_2	CNT_BDR_TH_1	CNT_BDR_TH_0
--------------	--------------	--------------	--------------	--------------	--------------	--------------	--------------

**Table 35. COUNTER\_BDR\_REG2 register description**

CNT_BDR_TH_[7:0]	In conjunction with CNT_BDR_TH_[10:8] in <a href="#">COUNTER_BDR_REG1 (0Bh)</a> , sets the threshold for the internal counter of batch events. When this counter reaches the threshold, the counter is reset and the COUNTER_BDR_IA flag in <a href="#">FIFO_STATUS2 (3Bh)</a> is set to 1.
------------------	---

## 9.9 INT1\_CTRL (0Dh)

INT1 pin control register (R/W)

Each bit in this register enables a signal to be carried over INT1 when the MIPI I3C<sup>SM</sup> dynamic address is not assigned (I<sup>2</sup>C or SPI is used). Some bits can be also used to trigger an IBI (in-band interrupt) when the MIPI I3C<sup>SM</sup> interface is used. The output of the pad is the OR combination of the signals selected here and in register MD1\_CFG (5Eh).

**Table 36. INT1\_CTRL register**

DEN_DRDY_flag	INT1_CNT_BDR	INT1_FIFO_FULL	INT1_FIFO_OVR	INT1_FIFO_TH	INT1_BOOT	INT1_DRDY_G	INT1_DRDY_XL
---------------	--------------	----------------	---------------	--------------	-----------	-------------	--------------

**Table 37. INT1\_CTRL register description**

DEN_DRDY_flag	Sends DEN_DRDY (DEN stamped on sensor data flag) to the INT1 pin.
INT1_CNT_BDR	Enables COUNTER_BDR_IA interrupt on the INT1.
INT1_FIFO_FULL	Enables FIFO full flag interrupt on the INT1 pin. It can be also used to trigger an IBI when the MIPI I3C <sup>SM</sup> interface is used.
INT1_FIFO_OVR	Enables FIFO overrun interrupt on the INT1 pin. It can be also used to trigger an IBI when the MIPI I3C <sup>SM</sup> interface is used.
INT1_FIFO_TH	Enables FIFO threshold interrupt on the INT1 pin. It can be also used to trigger an IBI when the MIPI I3C <sup>SM</sup> interface is used.
INT1_BOOT	Enables boot status on the INT1 pin.
INT1_DRDY_G	Enables gyroscope data-ready interrupt on the INT1 pin. It can be also used to trigger an IBI when the MIPI I3C <sup>SM</sup> interface is used.
INT1_DRDY_XL	Enables accelerometer data-ready interrupt on the INT1 pin. It can be also used to trigger an IBI when the MIPI I3C <sup>SM</sup> interface is used.

## 9.10 INT2\_CTRL (0Eh)

INT2 pin control register (R/W)

Each bit in this register enables a signal to be carried over INT2 when the MIPI I3C<sup>SM</sup> dynamic address is not assigned (I<sup>2</sup>C or SPI is used). Some bits can be also used to trigger an IBI when the MIPI I3C<sup>SM</sup> interface is used.. The output of the pad is the OR combination of the signals selected here and in register MD2\_CFG (5Fh).

**Table 38. INT2\_CTRL register**

0 <sup>(1)</sup>	INT2_CNT_BDR	INT2_FIFO_FULL	INT2_FIFO_OVR	INT2_FIFO_TH	INT2_DRDY_TEMP	INT2_DRDY_G	INT2_DRDY_XL
------------------	--------------	----------------	---------------	--------------	----------------	-------------	--------------

1. This bit must be set to 0 for the correct operation of the device.

**Table 39. INT2\_CTRL register description**

INT2_CNT_BDR	Enables COUNTER_BDR_IA interrupt on the INT2 pin.
INT2_FIFO_FULL	Enables FIFO full flag interrupt on the INT2 pin.
INT2_FIFO_OVR	Enables FIFO overrun interrupt on the INT2 pin.
INT2_FIFO_TH	Enables FIFO threshold interrupt on the INT2 pin.
INT2_DRDY_TEMP	Enables temperature sensor data-ready interrupt on the INT2 pin. It can be also used to trigger an IBI when the MIPI I3C <sup>SM</sup> interface is used and INT2_ON_INT1 = 1 in CTRL4_C (13h).
INT2_DRDY_G	Enables gyroscope data-ready interrupt on the INT2 pin.
INT2_DRDY_XL	Enables accelerometer data-ready interrupt on the INT2 pin.

### 9.11 WHO\_AM\_I (0Fh)

WHO\_AM\_I register (R). This is a read-only register. Its value is fixed at 6Bh.

**Table 40. Who\_Am\_I register**

0	1	1	0	1	0	1	1
---	---	---	---	---	---	---	---

### 9.12 CTRL1\_XL (10h)

Accelerometer control register 1 (R/W)

**Table 41. CTRL1\_XL register**

ODR_XL3	ODR_XL2	ODR_XL1	ODR_XL0	FS1_XL	FS0_XL	LPF2_XL_EN	0 <sup>(1)</sup>
---------	---------	---------	---------	--------	--------	------------	------------------

1. This bit must be set to 0 for the correct operation of the device.

**Table 42. CTRL1\_XL register description**

ODR_XL[3:0]	Accelerometer ODR selection (see Table 43)
FS[1:0]_XL	Accelerometer full-scale selection. Default value: 00 (00: $\pm 2$ g; 01: $\pm 16$ g; 10: $\pm 4$ g; 11: $\pm 8$ g)
LPF2_XL_EN	Accelerometer high-resolution selection (0: output from first stage digital filtering selected (default); 1: output from LPF2 second filtering stage selected)

**Table 43. Accelerometer ODR register setting**

ODR_XL3	ODR_XL2	ODR_XL1	ODR_XL0	ODR selection [Hz] when XL_HM_MODE = 1 in CTRL6_C (15h)	ODR selection [Hz] when XL_HM_MODE = 0 in CTRL6_C (15h)
0	0	0	0	Power-down	Power-down
1	0	1	1	1.6 Hz (low power only)	N.A.
0	0	0	1	12.5 Hz (low power)	12.5 Hz (high performance)
0	0	1	0	26 Hz (low power)	26 Hz (high performance)
0	0	1	1	52 Hz (low power)	52 Hz (high performance)
0	1	0	0	104 Hz (low power)	104 Hz (high performance)
0	1	0	1	208 Hz (low power)	208 Hz (high performance)
0	1	1	0	416 Hz (high performance)	416 Hz (high performance)
0	1	1	1	833 Hz (high performance)	833 Hz (high performance)
1	0	0	0	1.67 kHz (high performance)	1.67 kHz (high performance)
1	0	0	1	Reserved	Reserved
1	0	1	0	Reserved	Reserved
1	1	x	x	Reserved	Reserved



## 9.13 CTRL2\_G (11h)

Gyroscope control register 2 (R/W)

**Table 44. CTRL2\_G register**

ODR_G3	ODR_G2	ODR_G1	ODR_G0	FS1_G	FS0_G	FS_125	FS_4000
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**Table 45. CTRL2\_G register description**

ODR_G[3:0]	Gyroscope output data rate selection. Default value: 0000 (Refer to Table 46)
FS[1:0]_G	Gyroscope chain full-scale selection (00: $\pm 250$ dps; 01: $\pm 500$ dps; 10: $\pm 1000$ dps; 11: $\pm 2000$ dps)
FS_125	Selects gyroscope chain full-scale $\pm 125$ dps (0: FS selected through bits FS[1:0]_G; 1: FS set to $\pm 125$ dps)
FS_4000	Selects gyroscope chain full-scale $\pm 4000$ dps (0: FS selected through bits FS[1:0]_G or FS_125; 1: FS set to $\pm 4000$ dps)

**Table 46. Gyroscope ODR configuration setting**

ODR_G3	ODR_G2	ODR_G1	ODR_G0	ODR selection [Hz] when G_HM_MODE = 1 in CTRL7_G (16h)	ODR selection [Hz] when G_HM_MODE = 0 in CTRL7_G (16h)
0	0	0	0	Power-down	Power-down
0	0	0	1	12.5 Hz (low power)	12.5 Hz (high performance)
0	0	1	0	26 Hz (low power)	26 Hz (high performance)
0	0	1	1	52 Hz (low power)	52 Hz (high performance)
0	1	0	0	104 Hz (low power)	104 Hz (high performance)
0	1	0	1	208 Hz (low power)	208 Hz (high performance)
0	1	1	0	416 Hz (high performance)	416 Hz (high performance)
0	1	1	1	833 Hz (high performance)	833 Hz (high performance)
1	0	0	0	1.67 kHz (high performance)	1.67 kHz (high performance)
1	0	0	1	Reserved	Reserved
1	0	1	0	Reserved	Reserved
1	0	1	1	Reserved	Reserved

## 9.14 CTRL3\_C (12h)

Control register 3 (R/W)

**Table 47. CTRL3\_C register**

BOOT	BDU	H_LACTIVE	PP_OD	SIM	IF_INC	0 <sup>(1)</sup>	SW_RESET
------	-----	-----------	-------	-----	--------	------------------	----------

1. This bit must be set to 0 for the correct operation of the device.

**Table 48. CTRL3\_C register description**

BOOT	Reboots memory content. Default value: 0 (0: normal mode; 1: reboot memory content) Note: the accelerometer must be ON. This bit is automatically cleared.
BDU	Block data update. Default value: 0 (0: continuous update; 1: output registers are not updated until MSB and LSB have been read)
H_LACTIVE	Interrupt activation level. Default value: 0 (0: interrupt output pins active high; 1: interrupt output pins active low)
PP_OD	Push-pull/open-drain selection on INT1 and INT2 pins. This bit must be set to 0 when H_LACTIVE is set to 1. Default value: 0 (0: push-pull mode; 1: open-drain mode)
SIM	SPI serial interface mode selection. Default value: 0 (0: 4-wire interface; 1: 3-wire interface)
IF_INC	Register address automatically incremented during a multiple byte access with a serial interface (I <sup>2</sup> C or SPI). Default value: 1 (0: disabled; 1: enabled)
SW_RESET	Software reset. Default value: 0 (0: normal mode; 1: reset device) This bit is automatically cleared.

## 9.15 CTRL4\_C (13h)

Control register 4 (R/W)

**Table 49. CTRL4\_C register**

0 <sup>(1)</sup>	SLEEP_G	INT2_on_INT1	0 <sup>(1)</sup>	DRDY_MASK	I2C_disable	LPF1_SEL_G	0 <sup>(1)</sup>
------------------	---------	--------------	------------------	-----------	-------------	------------	------------------

1. This bit must be set to 0 for the correct operation of the device.

**Table 50. CTRL4\_C register description**

SLEEP_G	Enables gyroscope sleep mode. Default value: 0 (0: disabled; 1: enabled)
INT2_on_INT1	All interrupt signals available on the INT1 pin enable. Default value: 0 (0: interrupt signals divided between the INT1 and INT2 pins; 1: all interrupt signals in logic or on the INT1 pin)
DRDY_MASK	Enables data available (0: disabled; 1: mask DRDY on pin (both accelerometer and gyroscope) until filter settling ends (accelerometer and gyroscope independently masked).
I2C_disable	Disables I <sup>2</sup> C interface. Default value: 0 (0: SPI, I <sup>2</sup> C and MIPI I3C <sup>SM</sup> interfaces enabled (default); 1: I <sup>2</sup> C interface disabled)
LPF1_SEL_G	Enables gyroscope digital LPF1; the bandwidth can be selected through FTYPE[2:0] in CTRL6_C (15h). (0: disabled; 1: enabled)

## 9.16 CTRL5\_C (14h)

Control register 5 (R/W)

**Table 51. CTRL5\_C register**

0 <sup>(1)</sup>	ROUNDING1	ROUNDING0	0 <sup>(1)</sup>	ST1_G	ST0_G	ST1_XL	ST0_XL
------------------	-----------	-----------	------------------	-------	-------	--------	--------

1. This bit must be set to 0 for the correct operation of the device.

**Table 52. CTRL5\_C register description**

ROUNDING[1:0]	Circular burst mode (wraparound) read of the output registers. Default value: 00 (00: no wraparound; 01: accelerometer only; 10: gyroscope only; 11: gyroscope + accelerometer)
ST[1:0]_G	Enables angular rate sensor self-test. Default value: 00 (00: self-test disabled; Other: refer to <a href="#">Table 53</a> )
ST[1:0]_XL	Enables linear acceleration sensor self-test. Default value: 00 (00: self-test disabled; Other: refer to <a href="#">Table 54</a> )

**Table 53. Angular rate sensor self-test mode selection**

ST1_G	ST0_G	Self-test mode
0	0	Normal mode
0	1	Positive sign self-test
1	0	Not allowed
1	1	Negative sign self-test

**Table 54. Linear acceleration sensor self-test mode selection**

ST1_XL	ST0_XL	Self-test mode
0	0	Normal mode
0	1	Positive sign self-test
1	0	Negative sign self-test
1	1	Not allowed

## 9.17 CTRL6\_C (15h)

Control register 6 (R/W)

**Table 55. CTRL6\_C register**

TRIG_EN	LVL1_EN	LVL2_EN	XL_HM_MODE	USR_OFF_W	FTYPE_2	FTYPE_1	FTYPE_0
---------	---------	---------	------------	-----------	---------	---------	---------

**Table 56. CTRL6\_C register description**

TRIG_EN	Enables DEN data edge-sensitive trigger mode. Refer to Table 57.
LVL1_EN	Enables DEN data level-sensitive trigger mode. Refer to Table 57.
LVL2_EN	Enables DEN level-sensitive latched mode. Refer to Table 57.
XL_HM_MODE	Disables high-performance operating mode for accelerometer. Default value: 0 (0: high-performance operating mode enabled; 1: high-performance operating mode disabled)
USR_OFF_W	Weight of XL user offset bits of registers X_OFS_USR (73h), Y_OFS_USR (74h), Z_OFS_USR (75h) (0: 2 <sup>-10</sup> g/LSB; 1: 2 <sup>-6</sup> g/LSB)
FTYPE[2:0]	Gyroscope low-pass filter (LPF1) bandwidth selection. Table 58 shows the selectable bandwidth values.

**Table 57. Trigger mode selection**

TRIG_EN, LVL1_EN, LVL2_EN	Trigger mode
100	Edge-sensitive trigger mode is selected
010	Level-sensitive trigger mode is selected
011	Level-sensitive latched mode is selected
110	Level-sensitive FIFO enable mode is selected

**Table 58. Gyroscope LPF1 bandwidth selection**

FTYPE[2:0]	12.5 Hz	26 Hz	52 Hz	104 Hz	208 Hz	416 Hz	833 Hz	1.67 kHz
000	4.3	8.3	16.7	33	67	133	222	274
001	4.3	8.3	16.7	33	67	128	186	212
010	4.3	8.3	16.7	33	67	112	140	150
011	4.3	8.3	16.7	33	67	134	260	390
100	4.3	8.3	16.7	34	62	86	96	99
101	4.3	8.3	16.9	31	43	48	49	50
110	4.3	8.3	13.4	19	23	24.6	25	25
111	4.3	8.3	9.8	11.6	12.2	12.4	12.6	12.6

## 9.18 CTRL7\_G (16h)

Control register 7 (R/W)

**Table 59. CTRL7\_G register**

G_HM_MODE	HP_EN_G	HPM1_G	HPM0_G	0 <sup>(1)</sup>	0 <sup>(1)</sup>	USR_OFF_ON_OUT	0 <sup>(1)</sup>
-----------	---------	--------	--------	------------------	------------------	----------------	------------------

1. This bit must be set to 0 for the correct operation of the device.

G_HM_MODE	Disables high-performance operating mode for gyroscope. Default: 0 (0: high-performance operating mode enabled; 1: high-performance operating mode disabled)
HP_EN_G	Enables gyroscope digital high-pass filter. The filter is enabled only if the gyroscope is in HP mode. Default value: 0 (0: HPF disabled; 1: HPF enabled)
HPM_G[1:0]	Gyroscope digital HP filter cutoff selection. Default: 00 (00: 16 mHz; 01: 65 mHz; 10: 260 mHz; 11: 1.04 Hz)
USR_OFF_ON_OUT	Enables accelerometer user offset correction block; it's valid for the low-pass path - see <a href="#">Figure 20</a> . Default value: 0 (0: accelerometer user offset correction block bypassed; 1: accelerometer user offset correction block enabled)

## 9.19 CTRL8\_XL (17h)

Control register 8 (R/W)

**Table 60. CTRL8\_XL register**

HPCF_XL_2	HPCF_XL_1	HPCF_XL_0	HP_REF_MODE_XL	FASTSETTL_MODE_XL	HP_SLOPE_XL_EN	0 <sup>(1)</sup>	LOW_PASS_ON_6D
-----------	-----------	-----------	----------------	-------------------	----------------	------------------	----------------

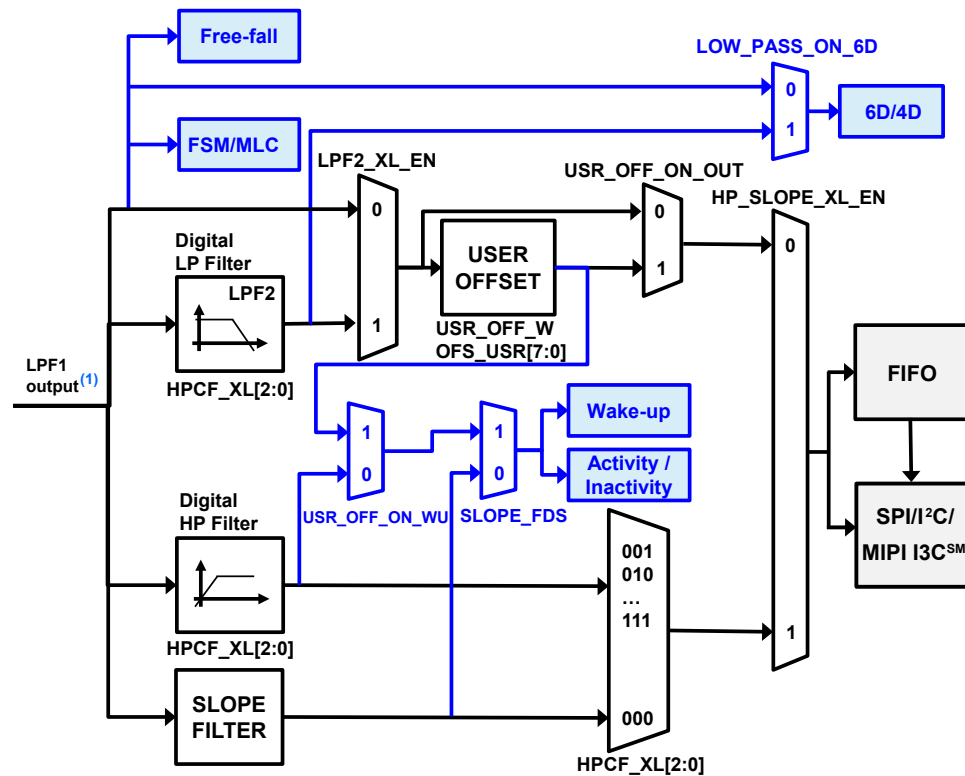
1. This bit must be set to 0 for the correct operation of the device.

HPCF_XL_[2:0]	Accelerometer LPF2 and HP filter configuration and cutoff setting. Refer to <a href="#">Table 61</a> .
HP_REF_MODE_XL	Enables accelerometer high-pass filter reference mode (valid for high-pass path - HP_SLOPE_XL_EN bit must be 1). Default value: 0 <sup>(1)</sup> (0: disabled, 1: enabled)
FASTSETTL_MODE_XL	Enables accelerometer LPF2 and HPF fast-settling mode. The filter sets the second samples after writing this bit. Active only during device exit from power-down mode. Default value: 0 (0: disabled, 1: enabled)
HP_SLOPE_XL_EN	Accelerometer slope filter / high-pass filter selection. Refer to <a href="#">Figure 22</a> .
LOW_PASS_ON_6D	LPF2 on 6D function selection. Refer to <a href="#">Figure 22</a> . Default value: 0 (0: ODR/2 low-pass filtered data sent to 6D interrupt function; 1: LPF2 output data sent to 6D interrupt function)

1. When enabled, the first output data have to be discarded.

**Table 61. Accelerometer bandwidth configurations**

Filter type	HP_SLOPE_XL_EN	LPF2_XL_EN	HPCF_XL_[2:0]	Bandwidth
Low pass	0	0	-	ODR/2
			000	ODR/4
		1	001	ODR/10
			010	ODR/20
			011	ODR/45
			100	ODR/100
			101	ODR/200
			110	ODR/400
			111	ODR/800
			High pass	1
001	ODR/10			
010	ODR/20			
011	ODR/45			
100	ODR/100			
101	ODR/200			
110	ODR/400			
111	ODR/800			

**Figure 22. Accelerometer block diagram**


1. The cutoff value of the LPF1 output is ODR/2 when the accelerometer is in high-performance mode and ODR up to 833 Hz. This value is equal to 780 Hz when the accelerometer is in low-power mode.

## 9.20 CTRL9\_XL (18h)

Control register 9 (R/W)

**Table 62. CTRL9\_XL register**

DEN_X	DEN_Y	DEN_Z	DEN_XL_G	DEN_XL_EN	DEN_LH	I3C_disable	0 <sup>(1)</sup>
-------	-------	-------	----------	-----------	--------	-------------	------------------

1. This bit must be set to 0 for the correct operation of the device.

**Table 63. CTRL9\_XL register description**

DEN_X	DEN value stored in LSB of X-axis. Default value: 1 (0: DEN not stored in X-axis LSB; 1: DEN stored in X-axis LSB)
DEN_Y	DEN value stored in LSB of Y-axis. Default value: 1 (0: DEN not stored in Y-axis LSB; 1: DEN stored in Y-axis LSB)
DEN_Z	DEN value stored in LSB of Z-axis. Default value: 1 (0: DEN not stored in Z-axis LSB; 1: DEN stored in Z-axis LSB)
DEN_XL_G	DEN stamping sensor selection. Default value: 0 (0: DEN pin info stamped in the gyroscope axis selected by bits [7:5]; 1: DEN pin info stamped in the accelerometer axis selected by bits [7:5])
DEN_XL_EN	Extends DEN functionality to accelerometer sensor. Default value: 0 (0: disabled; 1: enabled)
DEN_LH	DEN active level configuration. Default value: 0 (0: active low; 1: active high)
I3C_disable	Disables MIPI I3C <sup>SM</sup> communication protocol <sup>(1)</sup> (0: SPI, I <sup>2</sup> C, MIPI I3C <sup>SM</sup> interfaces enabled (default); 1: MIPI I3C <sup>SM</sup> interface disabled)

1. It is recommended to set this bit to 1 during the initial device configuration phase, when the I3C interface is not used.

## 9.21 CTRL10\_C (19h)

Control register 10 (R/W)

**Table 64. CTRL10\_C register**

0 <sup>(1)</sup>	0 <sup>(1)</sup>	TIMESTAMP_EN	0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>
------------------	------------------	--------------	------------------	------------------	------------------	------------------	------------------

1. This bit must be set to 0 for the correct operation of the device.

**Table 65. CTRL10\_C register description**

TIMESTAMP_EN	Enables timestamp counter. Default value: 0 (0: disabled; 1: enabled)  The counter is readable in <b>TIMESTAMP0</b> (40h), <b>TIMESTAMP1</b> (41h), <b>TIMESTAMP2</b> (42h), and <b>TIMESTAMP3</b> (43h).
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## 9.22 ALL\_INT\_SRC (1Ah)

Source register for all interrupts (R)

**Table 66. ALL\_INT\_SRC register**

TIMESTAMP_ENDCOUNT	0	SLEEP_CHANGE_IA	D6D_IA	0	0	WU_IA	FF_IA
--------------------	---	-----------------	--------	---	---	-------	-------

**Table 67. ALL\_INT\_SRC register description**

TIMESTAMP_ENDCOUNT	Alerts timestamp overflow within 6.4 ms
SLEEP_CHANGE_IA	Detects change event in activity/inactivity status. Default value: 0 (0: change status not detected; 1: change status detected)
D6D_IA	Interrupt active for change in position of portrait, landscape, face-up, face-down. Default value: 0 (0: change in position not detected; 1: change in position detected)
WU_IA	Wake-up event status. Default value: 0 (0: event not detected, 1: event detected)
FF_IA	Free-fall event status. Default value: 0 (0: event not detected, 1: event detected)

## 9.23 WAKE\_UP\_SRC (1Bh)

Wake-up interrupt source register (R)

**Table 68. WAKE\_UP\_SRC register**

0	SLEEP_CHANGE_IA	FF_IA	SLEEP_STATE	WU_IA	X_WU	Y_WU	Z_WU
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**Table 69. WAKE\_UP\_SRC register description**

SLEEP_CHANGE_IA	Detects change event in activity/inactivity status. Default value: 0 (0: change status not detected; 1: change status detected)
FF_IA	Free-fall event detection status. Default: 0 (0: free-fall event not detected; 1: free-fall event detected)
SLEEP_STATE	Sleep event status. Default value: 0 (0: sleep event not detected; 1: sleep event detected)
WU_IA	Wake-up event detection status. Default value: 0 (0: wake-up event not detected; 1: wake-up event detected.)
X_WU	Wake-up event detection status on X-axis. Default value: 0 (0: wake-up event on X-axis not detected; 1: wake-up event on X-axis detected)
Y_WU	Wake-up event detection status on Y-axis. Default value: 0 (0: wake-up event on Y-axis not detected; 1: wake-up event on Y-axis detected)
Z_WU	Wake-up event detection status on Z-axis. Default value: 0 (0: wake-up event on Z-axis not detected; 1: wake-up event on Z-axis detected)

## 9.24 DRD\_SRC (1Dh)

Portrait, landscape, face-up and face-down source register (R)

**Table 70. D6D\_SRC register**

DEN_DRDY	D6D_IA	ZH	ZL	YH	YL	XH	XL
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**Table 71. D6D\_SRC register description**

DEN_DRDY	DEN data-ready signal. It is set high when data output is related to the data coming from a DEN active condition. <sup>(1)</sup>
D6D_IA	Interrupt active for change position portrait, landscape, face-up, face-down. Default value: 0 (0: change position not detected; 1: change position detected)
ZH	Z-axis high event (over threshold). Default value: 0 (0: event not detected; 1: event (over threshold) detected)
ZL	Z-axis low event (under threshold). Default value: 0 (0: event not detected; 1: event (under threshold) detected)
YH	Y-axis high event (over threshold). Default value: 0 (0: event not detected; 1: event (over threshold) detected)
YL	Y-axis low event (under threshold). Default value: 0 (0: event not detected; 1: event (under threshold) detected)
XH	X-axis high event (over threshold). Default value: 0 (0: event not detected; 1: event (over threshold) detected)
XL	X-axis low event (under threshold). Default value: 0 (0: event not detected; 1: event (under threshold) detected)

1. The DEN data-ready signal can be latched or pulsed depending on the value of the `dataready_pulsed` bit of the `COUNTER_BDR_REG1 (0Bh)` register.

## 9.25 STATUS\_REG (1Eh)

Status register (R)

**Table 72. STATUS\_REG register**

0	0	0	0	BOOT_CHECK_FAIL	TDA	GDA	XLDA
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**Table 73. STATUS\_REG register description**

BOOT_CHECK_FAIL	Embedded CRC check status after boot/reboot. Default value: 0 (0: boot check passed; 1: boot check failed)
TDA	Temperature new data available. Default: 0 (0: no set of data is available at temperature sensor output; 1: a new set of data is available at temperature sensor output)
GDA	Gyroscope new data available. Default value: 0 (0: no set of data available at gyroscope output; 1: a new set of data is available at gyroscope output)
XLDA	Accelerometer new data available. Default value: 0 (0: no set of data available at accelerometer output; 1: a new set of data is available at accelerometer output)

## 9.26 OUT\_TEMP\_L (20h), OUT\_TEMP\_H (21h)

Temperature data output register (R). L and H registers together express a 16-bit word in two's complement.

**Table 74. OUT\_TEMP\_L register**

Temp7	Temp6	Temp5	Temp4	Temp3	Temp2	Temp1	Temp0
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**Table 75. OUT\_TEMP\_H register**

Temp15	Temp14	Temp13	Temp12	Temp11	Temp10	Temp9	Temp8
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**Table 76. OUT\_TEMP register description**

Temp[15:0]	Temperature sensor output data The value is expressed as two's complement sign extended on the MSB.
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### 9.27 OUTX\_H\_G (23h), OUTX\_L\_G (22h)

Angular rate sensor pitch axis (X) angular rate output register (R). The value is expressed as a 16-bit word in two's complement.

**Table 77. OUTX\_H\_G register**

D15	D14	D13	D12	D11	D10	D9	D8
-----	-----	-----	-----	-----	-----	----	----

**Table 78. OUTX\_L\_G register**

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

**Table 79. OUTX\_H\_G, OUTX\_L\_G register description**

D[15:0]	Gyroscope pitch axis output expressed in two's complement
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### 9.28 OUTY\_H\_G (25h), OUTY\_L\_G (24h)

Angular rate sensor roll axis (Y) angular rate output register (R). The value is expressed as a 16-bit word in two's complement.

**Table 80. OUTY\_H\_G register**

D15	D14	D13	D12	D11	D10	D9	D8
-----	-----	-----	-----	-----	-----	----	----

**Table 81. OUTY\_L\_G register**

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

**Table 82. OUTY\_H\_G, OUTY\_L\_G register description**

D[15:0]	Gyroscope roll axis output expressed in two's complement
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### 9.29 OUTZ\_H\_G (27h), OUTZ\_L\_G (26h)

Angular rate sensor pitch yaw (Z) angular rate output register (R). The value is expressed as a 16-bit word in two's complement.

**Table 83. OUTZ\_H\_G register**

D15	D14	D13	D12	D11	D10	D9	D8
-----	-----	-----	-----	-----	-----	----	----

**Table 84. OUTZ\_L\_G register**

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

**Table 85. OUTZ\_H\_G, OUTZ\_L\_G register description**

D[15:0]	Gyroscope yaw axis output expressed in two's complement
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### 9.30 OUTX\_H\_A (29h), OUTX\_L\_A (28h)

Linear acceleration sensor X-axis output register (R). The value is expressed as a 16-bit word in two's complement.

**Table 86. OUTX\_H\_A register**

D15	D14	D13	D12	D11	D10	D9	D8
-----	-----	-----	-----	-----	-----	----	----

**Table 87. OUTX\_L\_A register**

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

**Table 88. OUTX\_H\_A, OUTX\_L\_A register description**

D[15:0]	Accelerometer X-axis output expressed as two's complement
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### 9.31 OUTY\_H\_A (2Bh), OUTY\_L\_A (2Ah)

Linear acceleration sensor Y-axis output register (R). The value is expressed as a 16-bit word in two's complement.

**Table 89. OUTY\_H\_A register**

D15	D14	D13	D12	D11	D10	D9	D8
-----	-----	-----	-----	-----	-----	----	----

**Table 90. OUTY\_L\_A register**

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

**Table 91. OUTY\_H\_A, OUTY\_L\_A register description**

D[15:0]	Accelerometer Y-axis output expressed as two's complement
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### 9.32 OUTZ\_H\_A (2Dh), OUTZ\_L\_A (2Ch)

Linear acceleration sensor Z-axis output register (R). The value is expressed as a 16-bit word in two's complement.

**Table 92. OUTZ\_H\_A register**

D15	D14	D13	D12	D11	D10	D9	D8
-----	-----	-----	-----	-----	-----	----	----

**Table 93. OUTZ\_L\_A register**

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

**Table 94. OUTZ\_H\_A, OUTZ\_L\_A register description**

D[15:0]	Accelerometer Z-axis output expressed as two's complement
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### 9.33 EMB\_FUNC\_STATUS\_MAINPAGE (35h)

Embedded function status register (R)

**Table 95. EMB\_FUNC\_STATUS\_MAINPAGE register**

IS_FSM_LC	0	0	0	0	0	0	0
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**Table 96. EMB\_FUNC\_STATUS\_MAINPAGE register description**

IS_FSM_LC	Interrupt status bit for FSM long counter timeout interrupt event. (1: interrupt detected; 0: no interrupt)
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### 9.34 FSM\_STATUS\_A\_MAINPAGE (36h)

Finite state machine status register (R)

**Table 97. FSM\_STATUS\_A\_MAINPAGE register**

IS_FSM8	IS_FSM7	IS_FSM6	IS_FSM5	IS_FSM4	IS_FSM3	IS_FSM2	IS_FSM1
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**Table 98. FSM\_STATUS\_A\_MAINPAGE register description**

IS_FSM8	Interrupt status bit for FSM8 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM7	Interrupt status bit for FSM7 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM6	Interrupt status bit for FSM6 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM5	Interrupt status bit for FSM5 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM4	Interrupt status bit for FSM4 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM3	Interrupt status bit for FSM3 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM2	Interrupt status bit for FSM2 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM1	Interrupt status bit for FSM1 interrupt event. (1: interrupt detected; 0: no interrupt)

### 9.35 FSM\_STATUS\_B\_MAINPAGE (37h)

Finite state machine status register (R)

**Table 99. FSM\_STATUS\_B\_MAINPAGE register**

IS_FSM16	IS_FSM15	IS_FSM14	IS_FSM13	IS_FSM12	IS_FSM11	IS_FSM10	IS_FSM9
----------	----------	----------	----------	----------	----------	----------	---------

**Table 100. FSM\_STATUS\_B\_MAINPAGE register description**

IS_FSM16	Interrupt status bit for FSM16 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM15	Interrupt status bit for FSM15 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM14	Interrupt status bit for FSM14 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM13	Interrupt status bit for FSM13 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM12	Interrupt status bit for FSM12 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM11	Interrupt status bit for FSM11 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM10	Interrupt status bit for FSM10 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM9	Interrupt status bit for FSM9 interrupt event. (1: interrupt detected; 0: no interrupt)

### 9.36 MLC\_STATUS\_MAINPAGE (38h)

Machine learning core status register (R)

**Table 101. MLC\_STATUS\_MAINPAGE register**

IS_MLC8	IS_MLC7	IS_MLC6	IS_MLC5	IS_MLC4	IS_MLC3	IS_MLC2	IS_MLC1
---------	---------	---------	---------	---------	---------	---------	---------

**Table 102. MLC\_STATUS\_MAINPAGE register description**

IS_MLC8	Interrupt status bit for MLC8 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_MLC7	Interrupt status bit for MLC7 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_MLC6	Interrupt status bit for MLC6 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_MLC5	Interrupt status bit for MLC5 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_MLC4	Interrupt status bit for MLC4 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_MLC3	Interrupt status bit for MLC3 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_MLC2	Interrupt status bit for MLC2 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_MLC1	Interrupt status bit for MLC1 interrupt event. (1: interrupt detected; 0: no interrupt)

### 9.37 FIFO\_STATUS1 (3Ah)

FIFO status register 1 (R)

**Table 103. FIFO\_STATUS1 register**

DIFF_FIFO_7	DIFF_FIFO_6	DIFF_FIFO_5	DIFF_FIFO_4	DIFF_FIFO_3	DIFF_FIFO_2	DIFF_FIFO_1	DIFF_FIFO_0
-------------	-------------	-------------	-------------	-------------	-------------	-------------	-------------

**Table 104. FIFO\_STATUS1 register description**

DIFF_FIFO_[7:0]	Number of unread sensor data (TAG + 6 bytes) stored in FIFO In conjunction with DIFF_FIFO[9:8] in FIFO_STATUS2 (3Bh).
-----------------	--

### 9.38 FIFO\_STATUS2 (3Bh)

FIFO status register 2 (R)

**Table 105. FIFO\_STATUS2 register**

FIFO_WTM_IA	FIFO_OVR_IA	FIFO_FULL_IA	COUNTER_BDR_IA	FIFO_OVR_LATCHED	0	DIFF_FIFO_9	DIFF_FIFO_8
-------------	-------------	--------------	----------------	------------------	---	-------------	-------------

**Table 106. FIFO\_STATUS2 register description**

FIFO_WTM_IA	FIFO watermark status. Default value: 0 (0: FIFO filling is lower than WTM; 1: FIFO filling is equal to or greater than WTM) Watermark is set through bits WTM[8:0] in FIFO_CTRL2 (08h) and FIFO_CTRL1 (07h).
FIFO_OVR_IA	FIFO overrun status. Default value: 0 (0: FIFO is not completely filled; 1: FIFO is completely filled)
FIFO_FULL_IA	Smart FIFO full status. Default value: 0 (0: FIFO is not full; 1: FIFO will be full at the next ODR)
COUNTER_BDR_IA	Counter BDR reaches the CNT_BDR_TH_[10:0] threshold set in COUNTER_BDR_REG1 (0Bh) and COUNTER_BDR_REG2 (0Ch). Default value: 0 This bit is reset when these registers are read.
FIFO_OVR_LATCHED	Latched FIFO overrun status. Default value: 0 This bit is reset when this register is read.
DIFF_FIFO_[9:8]	Number of unread sensor data (TAG + 6 bytes) stored in FIFO. Default value: 00 In conjunction with DIFF_FIFO[7:0] in FIFO_STATUS1 (3Ah)



### 9.39 **TIMESTAMP0 (40h), TIMESTAMP1 (41h), TIMESTAMP2 (42h), and TIMESTAMP3 (43h)**

Timestamp first data output register (R). The value is expressed as a 32-bit word and the bit resolution is 25 μs.

**Table 107. TIMESTAMP3 register**

D31	D30	D29	D28	D27	D26	D25	D24
-----	-----	-----	-----	-----	-----	-----	-----

**Table 108. TIMESTAMP2 register**

D23	D22	D21	D20	D19	D18	D17	D16
-----	-----	-----	-----	-----	-----	-----	-----

**Table 109. TIMESTAMP1 register**

D15	D14	D13	D12	D11	D10	D9	D8
-----	-----	-----	-----	-----	-----	----	----

**Table 110. TIMESTAMP0 register**

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

D[31:0]	Timestamp output registers: 1LSB = 25 μs
---------	--

The formula below can be used to calculate a better estimation of the actual timestamp resolution:

$$TS\_Res = 1 / (40000 + (0.0015 * INTERNAL\_FREQ\_FINE * 40000))$$

where INTERNAL\_FREQ\_FINE is the content of [INTERNAL\\_FREQ\\_FINE \(63h\)](#).

## 9.40 INT\_CFG0 (56h)

Activity/inactivity functions, configuration of filtering, and interrupt latch mode configuration (R/W)

**Table 111. INT\_CFG0 register**

0 <sup>(1)</sup>	INT_CLR_ON_READ	SLEEP_STATUS_ON_INT	SLOPE_FDS	0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>	LIR
------------------	-----------------	---------------------	-----------	------------------	------------------	------------------	-----

1. This bit must be set to 0 for the correct operation of the device.

**Table 112. INT\_CFG0 register description**

INT_CLR_ON_READ	This bit allows immediately clearing the latched interrupts of an event detection upon the read of the corresponding status register. It must be set to 1 together with LIR. Default value: 0 (0: latched interrupt signal cleared at the end of the ODR period; 1: latched interrupt signal immediately cleared)
SLEEP_STATUS_ON_INT	Activity/inactivity interrupt mode configuration. If INT1_SLEEP_CHANGE or INT2_SLEEP_CHANGE bits are enabled, drives the sleep status or sleep change on INT pins. Default value: 0 (0: sleep change notification on INT pins; 1: sleep status reported on INT pins)
SLOPE_FDS	HPF or SLOPE filter selection on wake-up and activity/inactivity functions. Default value: 0 (0: SLOPE filter applied; 1: HPF applied)
LIR	Latched interrupt. Default value: 0 (0: interrupt request not latched; 1: interrupt request latched)

## 9.41 INT\_CFG1 (58h)

Enable interrupt function register (R/W)

**Table 113. INT\_CFG1 register**

INTERRUPTS_ENABLE	INACT_EN1	INACT_EN0	0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>
-------------------	-----------	-----------	------------------	------------------	------------------	------------------	------------------

1. This bit must be set to 0 for the correct operation of the device.

**Table 114. INT\_CFG1 register description**

INTERRUPTS_ENABLE	Enables hardcoded functions
INACT_EN[1:0]	Enables activity/inactivity (sleep) function. Default value: 00 (00: stationary/motion-only interrupts generated, accelerometer and gyroscope do not change; 01: sets accelerometer ODR to 12.5 Hz (low-power mode), gyroscope does not change; 10: sets accelerometer ODR to 12.5 Hz (low-power mode), gyroscope to sleep mode; 11: sets accelerometer ODR to 12.5 Hz (low-power mode), gyroscope to power-down mode)

## 9.42 THS\_6D (59h)

Portrait/landscape position register (R/W)

**Table 115. THS\_6D register**

D4D_EN	SIXD_THS1	SIXD_THS0	0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>
--------	-----------	-----------	------------------	------------------	------------------	------------------	------------------

1. This bit must be set to 0 for the correct operation of the device.

**Table 116. THS\_6D register description**

D4D_EN	Enables detection of 4D orientation. Z-axis position detection is disabled. Default value: 0 (0: disabled; 1: enabled)
SIXD_THS[1:0]	Threshold for 4D/6D function (00: 80 degrees (default); 01: 70 degrees; 10: 60 degrees; 11: 50 degrees)

## 9.43 WAKE\_UP\_THS (5Bh)

Wake-up configuration register (R/W)

**Table 117. WAKE\_UP\_THS register**

0 <sup>(1)</sup>	USR_OFF_ON_WU	WK_THS5	WK_THS4	WK_THS3	WK_THS2	WK_THS1	WK_THS0
------------------	---------------	---------	---------	---------	---------	---------	---------

1. This bit must be set to 0 for the correct operation of the device.

**Table 118. WAKE\_UP\_THS register description**

USR_OFF_ON_WU	Sends the low-pass filtered data with user offset correction (instead of high-pass filtered data) to the wake-up and the activity/inactivity functions. Default value: 0
WK_THS[5:0]	Threshold for wake-up: 1 LSB weight depends on WAKE_THS_W in WAKE_UP_DUR (5Ch). Default value: 000000

## 9.44 WAKE\_UP\_DUR (5Ch)

Free-fall, wake-up and sleep mode functions duration setting register (R/W)

**Table 119. WAKE\_UP\_DUR register**

FF_DUR5	WAKE_DUR1	WAKE_DUR0	WAKE_THS_W	SLEEP_DUR3	SLEEP_DUR2	SLEEP_DUR1	SLEEP_DUR0
---------	-----------	-----------	------------	------------	------------	------------	------------

**Table 120. WAKE\_UP\_DUR register description**

FF_DUR5	Free-fall duration event. Default: 0 For the complete configuration of the free-fall duration, refer to FF_DUR[4:0] in <a href="#">FREE_FALL (5Dh)</a> configuration. 1 LSB = 1 ODR_time
WAKE_DUR[1:0]	Wake-up duration event. Default: 00 1LSB = 1 ODR_time
WAKE_THS_W	Weight of 1 LSB of wake-up threshold. Default: 0 (0: 1 LSB = FS_XL / (2 <sup>6</sup> ); 1: 1 LSB = FS_XL / (2 <sup>8</sup> ))
SLEEP_DUR[3:0]	Duration to go in sleep mode. Default value: 0000 (this corresponds to 16 ODR) 1 LSB = 512 ODR

## 9.45 FREE\_FALL (5Dh)

Free-fall function duration setting register (R/W)

**Table 121. FREE\_FALL register**

FF_DUR4	FF_DUR3	FF_DUR2	FF_DUR1	FF_DUR0	FF_THS2	FF_THS1	FF_THS0
---------	---------	---------	---------	---------	---------	---------	---------

**Table 122. FREE\_FALL register description**

FF_DUR[4:0]	Free-fall duration event. Default: 0 For the complete configuration of the free fall duration, refer to FF_DUR5 in <a href="#">WAKE_UP_DUR (5Ch)</a> configuration
FF_THS[2:0]	Free-fall threshold setting (000: 156 mg (default); 001: 219 mg; 010: 250 mg; 011: 312 mg; 100: 344 mg; 101: 406 mg; 110: 469 mg; 111: 500 mg)

## 9.46 MD1\_CFG (5Eh)

Functions routing to INT1 pin register (R/W)

**Table 123. MD1\_CFG register**

INT1_SLEEP_CHANGE	0 <sup>(1)</sup>	INT1_WU	INT1_FF	0 <sup>(1)</sup>	INT1_6D	INT1_EMB_FUNC	0 <sup>(1)</sup>
-------------------	------------------	---------	---------	------------------	---------	---------------	------------------

1. This bit must be set to 0 for the correct operation of the device.

**Table 124. MD1\_CFG register description**

INT1_SLEEP_CHANGE <sup>(1)</sup>	Routing activity/inactivity recognition event to INT1. Default: 0 (0: routing activity/inactivity event to INT1 disabled; 1: routing activity/inactivity event to INT1 enabled)
INT1_WU	Routing wake-up event to INT1. Default value: 0 (0: routing wake-up event to INT1 disabled; 1: routing wake-up event to INT1 enabled)
INT1_FF	Routing free-fall event to INT1. Default value: 0 (0: routing free-fall event to INT1 disabled; 1: routing free-fall event to INT1 enabled)
INT1_6D	Routing 6D event to INT1. Default value: 0 (0: routing 6D event to INT1 disabled; 1: routing 6D event to INT1 enabled)
INT1_EMB_FUNC	Routing embedded functions event to INT1. Default value: 0 (0: routing embedded functions event to INT1 disabled; 1: routing embedded functions event to INT1 enabled)

1. Activity/inactivity interrupt mode (sleep change or sleep status) depends on the SLEEP\_STATUS\_ON\_INT bit in the INT\_CFG0 (56h) register.

## 9.47 MD2\_CFG (5Fh)

Functions routing to INT2 pin register (R/W)

**Table 125. MD2\_CFG register**

INT2_SLEEP_CHANGE	0 <sup>(1)</sup>	INT2_WU	INT2_FF	0 <sup>(1)</sup>	INT2_6D	INT2_EMB_FUNC	INT2_TIMESTAMP
-------------------	------------------	---------	---------	------------------	---------	---------------	----------------

1. This bit must be set to 0 for the correct operation of the device.

**Table 126. MD2\_CFG register description**

INT2_SLEEP_CHANGE <sup>(1)</sup>	Routing activity/inactivity recognition event to INT2. Default: 0 (0: routing activity/inactivity event to INT2 disabled; 1: routing activity/inactivity event to INT2 enabled)
INT2_WU	Routing wake-up event to INT2. Default value: 0 (0: routing wake-up event to INT2 disabled; 1: routing wake-up event to INT2 enabled)
INT2_FF	Routing free-fall event to INT2. Default value: 0 (0: routing free-fall event to INT2 disabled; 1: routing free-fall event to INT2 enabled)
INT2_6D	Routing 6D event to INT2. Default value: 0 (0: routing 6D event to INT2 disabled; 1: routing 6D event to INT2 enabled)
INT2_EMB_FUNC	Routing embedded functions event to INT2. Default value: 0 (0: routing embedded functions event to INT2 disabled; 1: routing embedded functions event to INT2 enabled)
INT2_TIMESTAMP	Enables routing the alert for timestamp overflow within 6.4 ms to the INT2 pin.

1. Activity/inactivity interrupt mode (sleep change or sleep status) depends on the SLEEP\_STATUS\_ON\_INT bit in the INT\_CFG0 (56h) register.

## 9.48 I3C\_BUS\_AVB (62h)

I3C\_BUS\_AVB register (R/W)

**Table 127. I3C\_BUS\_AVB register**

0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>	I3C_Bus_Avb_Sel1	I3C_Bus_Avb_Sel0	0 <sup>(1)</sup>	0 <sup>(1)</sup>	PD_DIS_INT1
------------------	------------------	------------------	------------------	------------------	------------------	------------------	-------------

1. This bit must be set to 0 for the correct operation of the device.

**Table 128. I3C\_BUS\_AVB register description**

I3C_Bus_Avb_Sel[1:0]	<p>These bits are used to select the bus available time when I3C IBI is used.</p> <p>Default value: 00</p> <p>(00: bus available time equal to 50 <math>\mu</math>s (default);</p> <p>01: bus available time equal to 2 <math>\mu</math>s;</p> <p>10: bus available time equal to 1 ms;</p> <p>11: bus available time equal to 25 ms)</p>
PD_DIS_INT1	<p>This bit allows disabling the INT1 pull-down.</p> <p>(0: Pull-down on INT1 enabled (pull-down is effectively connected only when no interrupts are routed to the INT1 pin or when the I3C dynamic address is assigned);</p> <p>1: Pull-down on INT1 disabled (pull-down not connected))</p>

**Note:** *The IBI (in-band interrupt) is continuously generated (each time a bus available condition is satisfied) until an interrupt is served. The master should execute the interrupt service routine (ISR) at a time lower than the configured bus available time, otherwise the master should disable the interrupt (I3C DISEC in order to disable the interrupt request) at a time lower than the bus available time.*

*If the master needs more time to analyze and start the correct ISR, then the master can change the bus available time from 50  $\mu$ s (default) to a higher time.*

## 9.49 INTERNAL\_FREQ\_FINE (63h)

Internal frequency register (R)

**Table 129. INTERNAL\_FREQ\_FINE register**

FREQ_FINE7	FREQ_FINE6	FREQ_FINE5	FREQ_FINE4	FREQ_FINE3	FREQ_FINE2	FREQ_FINE1	FREQ_FINE0
------------	------------	------------	------------	------------	------------	------------	------------

**Table 130. INTERNAL\_FREQ\_FINE register description**

FREQ_FINE[7:0]	Difference in percentage of the effective ODR (and timestamp rate) with respect to the typical. Step: 0.15%. 8-bit format, two's complement.
----------------	--

The formula below can be used to calculate a better estimation of the actual ODR:

$$\text{ODR\_Actual} = (6667 + ((0.0015 * \text{INTERNAL\_FREQ\_FINE}) * 6667)) / \text{ODR\_Coeff}$$

Selected_ODR	ODR_Coeff
12.5	512
26	256
52	128
104	64
208	32
416	16
833	8
1667	4

The Selected\_ODR parameter has to be derived from the ODR\_XL selection ([Table 42. CTRL1\\_XL register description](#)) in order to estimate the accelerometer ODR and from the ODR\_G selection ([Table 45. CTRL2\\_G register description](#)) in order to estimate the gyroscope ODR.



### 9.50 X\_OFS\_USR (73h)

Accelerometer X-axis user offset correction (R/W). The offset value set in the X\_OFS\_USR offset register is internally subtracted from the acceleration value measured on the X-axis.

**Table 131. X\_OFS\_USR register**

X_OFS_USR_7	X_OFS_USR_6	X_OFS_USR_5	X_OFS_USR_4	X_OFS_USR_3	X_OFS_USR_2	X_OFS_USR_1	X_OFS_USR_0
-------------	-------------	-------------	-------------	-------------	-------------	-------------	-------------

**Table 132. X\_OFS\_USR register description**

X_OFS_USR_[7:0]	Accelerometer X-axis user offset correction expressed in two's complement, weight depends on USR_OFF_W in CTRL6_C (15h). The value must be in the range [-127 127].
-----------------	---

### 9.51 Y\_OFS\_USR (74h)

Accelerometer Y-axis user offset correction (R/W). The offset value set in the Y\_OFS\_USR offset register is internally subtracted from the acceleration value measured on the Y-axis.

**Table 133. Y\_OFS\_USR register**

Y_OFS_USR_7	Y_OFS_USR_6	Y_OFS_USR_5	Y_OFS_USR_4	Y_OFS_USR_3	Y_OFS_USR_2	Y_OFS_USR_1	Y_OFS_USR_0
-------------	-------------	-------------	-------------	-------------	-------------	-------------	-------------

Y_OFS_USR_[7:0]	Accelerometer Y-axis user offset calibration expressed in two's complement, weight depends on USR_OFF_W in CTRL6_C (15h). The value must be in the range [-127, +127].
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### 9.52 Z\_OFS\_USR (75h)

Accelerometer Z-axis user offset correction (R/W). The offset value set in the Z\_OFS\_USR offset register is internally subtracted from the acceleration value measured on the Z-axis.

**Table 134. Z\_OFS\_USR register**

Z_OFS_USR_7	Z_OFS_USR_6	Z_OFS_USR_5	Z_OFS_USR_4	Z_OFS_USR_3	Z_OFS_USR_2	Z_OFS_USR_1	Z_OFS_USR_0
-------------	-------------	-------------	-------------	-------------	-------------	-------------	-------------

**Table 135. Z\_OFS\_USR register description**

Z_OFS_USR_[7:0]	Accelerometer Z-axis user offset calibration expressed in two's complement, weight depends on USR_OFF_W in CTRL6_C (15h). The value must be in the range [-127, +127].
-----------------	--

## 9.53 FIFO\_DATA\_OUT\_TAG (78h)

FIFO tag register (R)

**Table 136. FIFO\_DATA\_OUT\_TAG register**

TAG_SENSOR_4	TAG_SENSOR_3	TAG_SENSOR_2	TAG_SENSOR_1	TAG_SENSOR_0	TAG_CNT_1	TAG_CNT_0	TAG_PARITY
--------------	--------------	--------------	--------------	--------------	-----------	-----------	------------

**Table 137. FIFO\_DATA\_OUT\_TAG register description**

TAG_SENSOR_[4:0]	Identifies the sensor in: FIFO_DATA_OUT_X_H (7Ah) and FIFO_DATA_OUT_X_L (79h), FIFO_DATA_OUT_Y_H (7Ch) and FIFO_DATA_OUT_Y_L (7Bh), and FIFO_DATA_OUT_Z_H (7Eh) and FIFO_DATA_OUT_Z_L (7Dh)
TAG_CNT_[1:0]	2-bit counter which identifies sensor time slot
TAG_PARITY	Parity check of TAG content

**Table 138. FIFO tag**

TAG_SENSOR_[4:0]	Sensor name
0x01	Gyroscope
0x02	Accelerometer
0x03	Temperature
0x04	Timestamp
0x05	CFG_Change

### 9.54 FIFO\_DATA\_OUT\_X\_H (7Ah) and FIFO\_DATA\_OUT\_X\_L (79h)

FIFO data output X (R)

**Table 139. FIFO\_DATA\_OUT\_X\_H register**

D15	D14	D13	D12	D11	D10	D9	D8
-----	-----	-----	-----	-----	-----	----	----

**Table 140. FIFO\_DATA\_OUT\_X\_L register**

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

**Table 141. FIFO\_DATA\_OUT\_X\_H, FIFO\_DATA\_OUT\_X\_L register description**

D[15:0]	FIFO X-axis output
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### 9.55 FIFO\_DATA\_OUT\_Y\_H (7Ch) and FIFO\_DATA\_OUT\_Y\_L (7Bh)

FIFO data output Y (R)

**Table 142. FIFO\_DATA\_OUT\_Y\_H register**

D15	D14	D13	D12	D11	D10	D9	D8
-----	-----	-----	-----	-----	-----	----	----

**Table 143. FIFO\_DATA\_OUT\_Y\_L register**

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

**Table 144. FIFO\_DATA\_OUT\_Y\_H, FIFO\_DATA\_OUT\_Y\_L register description**

D[15:0]	FIFO Y-axis output
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### 9.56 FIFO\_DATA\_OUT\_Z\_H (7Eh) and FIFO\_DATA\_OUT\_Z\_L (7Dh)

FIFO data output Z (R)

**Table 145. FIFO\_DATA\_OUT\_Z\_H register**

D15	D14	D13	D12	D11	D10	D9	D8
-----	-----	-----	-----	-----	-----	----	----

**Table 146. FIFO\_DATA\_OUT\_Z\_L register**

D7	D6	D5	D4	D3	D2	D1	D0
----	----	----	----	----	----	----	----

**Table 147. FIFO\_DATA\_OUT\_Z\_H, FIFO\_DATA\_OUT\_Z\_L register description**

D[15:0]	FIFO Z-axis output
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## 10 Embedded functions register mapping

The table given below provides a list of the registers for the embedded functions available in the device and the corresponding addresses. Embedded functions registers are accessible when FUNC\_CFG\_EN is set to 1 in FUNC\_CFG\_ACCESS (01h).

**Table 148. Register address map - embedded functions**

Name	Type	Register address		Default	Comment
		Hex	Binary		
PAGE_SEL	R/W	02	00000010	00000001	
RESERVED	-	03-04			Reserved
EMB_FUNC_EN_B	R/W	05	00000101	00000000	
PAGE_ADDRESS	R/W	08	00001000	00000000	
PAGE_VALUE	R/W	09	00001001	00000000	
EMB_FUNC_INT1	R/W	0A	00001010	00000000	
FSM_INT1_A	R/W	0B	00001011	00000000	
FSM_INT1_B	R/W	0C	00001100	00000000	
MLC_INT1	R/W	0D	00001101	00000000	
EMB_FUNC_INT2	R/W	0E	00001110	00000000	
FSM_INT2_A	R	0F	00001111	01101011	
FSM_INT2_B	R/W	10	00010000	00000000	
MLC_INT2	R/W	11	00010001	00000000	
EMB_FUNC_STATUS	R	12	00010010	output	
FSM_STATUS_A	R	13	00010011	output	
FSM_STATUS_B	R	14	00010100	output	
MLC_STATUS	R	15	00010101	output	
PAGE_RW	R/W	17	00010111	00000000	
RESERVED	-	18-45			Reserved
FSM_ENABLE_A	R/W	46	01000110	00000000	
FSM_ENABLE_B	R/W	47	01000111	00000000	
FSM_LONG_COUNTER_L	R/W	48	01001000	00000000	
FSM_LONG_COUNTER_H	R/W	49	01001001	00000000	
FSM_LONG_COUNTER_CLEAR	R/W	4A	01001010	00000000	
FSM_OUTS1	R	4C	01001100	output	
FSM_OUTS2	R	4D	01001101	output	
FSM_OUTS3	R	4E	01001110	output	
FSM_OUTS4	R	4F	01001111	output	
FSM_OUTS5	R	50	01010000	output	
FSM_OUTS6	R	51	01010001	output	
FSM_OUTS7	R	52	01010010	output	
FSM_OUTS8	R	53	01010011	output	
FSM_OUTS9	R	54	01010100	output	
FSM_OUTS10	R	55	01010101	output	

Name	Type	Register address		Default	Comment
		Hex	Binary		
FSM_OUTS11	R	56	01010110	output	
FSM_OUTS12	R	57	01010111	output	
FSM_OUTS13	R	58	01011000	output	
FSM_OUTS14	R	59	01011001	output	
FSM_OUTS15	R	5A	01011010	output	
FSM_OUTS16	R	5B	01011011	output	
RESERVED	-	5C-5E			Reserved
EMB_FUNC_ODR_CFG_B	R/W	5F	01011111	01001011	
EMB_FUNC_ODR_CFG_C	R/W	60	01100000	00010101	
RESERVED	-	61-66			Reserved
EMB_FUNC_INIT_B	R/W	67	01100111	00000000	
MLC0_SRC	R	70	01110000	output	
MLC1_SRC	R	71	01110001	output	
MLC2_SRC	R	72	01110010	output	
MLC3_SRC	R	73	01110011	output	
MLC4_SRC	R	74	01110100	output	
MLC5_SRC	R	75	01110101	output	
MLC6_SRC	R	76	01110110	output	
MLC7_SRC	R	77	01110111	output	

Reserved registers must not be changed. Writing to those registers may cause permanent damage to the device. The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

## 11 Embedded functions register description

### 11.1 PAGE\_SEL (02h)

Enable advanced features dedicated page (R/W)

**Table 149. PAGE\_SEL register**

PAGE_SEL3	PAGE_SEL2	PAGE_SEL1	PAGE_SEL0	0 <sup>(1)</sup>	0 <sup>(1)</sup>	EMB_FUNC_CLK_DIS	1 <sup>(2)</sup>
-----------	-----------	-----------	-----------	------------------	------------------	------------------	------------------

1. This bit must be set to 0 for the correct operation of the device.
2. This bit must be set to 1 for the correct operation of the device.

**Table 150. PAGE\_SEL register description**

PAGE_SEL[3:0]	Selects the advanced features dedicated page. Default value: 0000
EMB_FUNC_CLK_DIS	Disables the embedded functions clock. Default value: 0 (0: clock enabled; 1: clock disabled)

### 11.2 EMB\_FUNC\_EN\_B (05h)

Enable embedded functions register (R/W)

**Table 151. EMB\_FUNC\_EN\_B register**

0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>	MLC_EN	0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>	FSM_EN
------------------	------------------	------------------	--------	------------------	------------------	------------------	--------

1. This bit must be set to 0 for the correct operation of the device.

**Table 152. EMB\_FUNC\_EN\_B register description**

MLC_EN	Enables machine learning core feature. Default value: 0 (0: machine learning core feature disabled; 1: machine learning core feature enabled)
FSM_EN	Enables finite state machine (FSM) feature. Default value: 0 (0: FSM feature disabled; 1: FSM feature enabled)

### 11.3 PAGE\_ADDRESS (08h)

Page address register (R/W)

**Table 153. PAGE\_ADDRESS register**

PAGE_ADDR7	PAGE_ADDR6	PAGE_ADDR5	PAGE_ADDR4	PAGE_ADDR3	PAGE_ADDR2	PAGE_ADDR1	PAGE_ADDR0
------------	------------	------------	------------	------------	------------	------------	------------

**Table 154. PAGE\_ADDRESS register description**

PAGE_ADDR[7:0]	After setting the bit PAGE_WRITE / PAGE_READ in register PAGE_RW (17h), this register is used to set the address of the register to be written/read in the advanced features page selected through the bits PAGE_SEL[3:0] in register PAGE_SEL (02h).
----------------	---

## 11.4 PAGE\_VALUE (09h)

Page value register (R/W)

**Table 155. PAGE\_VALUE register**

PAGE_VALUE7	PAGE_VALUE6	PAGE_VALUE5	PAGE_VALUE4	PAGE_VALUE3	PAGE_VALUE2	PAGE_VALUE1	PAGE_VALUE0
-------------	-------------	-------------	-------------	-------------	-------------	-------------	-------------

**Table 156. PAGE\_VALUE register description**

PAGE_VALUE[7:0]	These bits are used to write (if the bit PAGE_WRITE = 1 in register <a href="#">PAGE_RW (17h)</a> ) or read (if the bit PAGE_READ = 1 in register <a href="#">PAGE_RW (17h)</a> ) the data at the address PAGE_ADDR[7:0] of the selected advanced features page.
-----------------	--

## 11.5 EMB\_FUNC\_INT1 (0Ah)

INT1 pin control register (R/W)

Each bit in this register enables a signal to be carried over INT1. The pin's output supplies the OR combination of the selected signals.

**Table 157. EMB\_FUNC\_INT1 register**

INT1_FSM_LC	0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>
-------------	------------------	------------------	------------------	------------------	------------------	------------------	------------------

1. This bit must be set to 0 for the correct operation of the device.

**Table 158. EMB\_FUNC\_INT1 register description**

INT1_FSM_LC <sup>(1)</sup>	Routing FSM long counter timeout interrupt event to INT1. Default value: 0 (0: routing to INT1 disabled; 1: routing to INT1 enabled)
----------------------------	---

1. This bit is activated if the INT1\_EMB\_FUNC bit of [MD1\\_CFG \(5Eh\)](#) is set to 1.

## 11.6 FSM\_INT1\_A (0Bh)

INT1 pin control register (R/W)

Each bit in this register enables a signal to be carried over INT1. The pin's output supplies the OR combination of the selected signals.

**Table 159. FSM\_INT1\_A register**

INT1_FSM8	INT1_FSM7	INT1_FSM6	INT1_FSM5	INT1_FSM4	INT1_FSM3	INT1_FSM2	INT1_FSM1
-----------	-----------	-----------	-----------	-----------	-----------	-----------	-----------

**Table 160. FSM\_INT1\_A register description**

INT1_FSM8 <sup>(1)</sup>	Routing FSM8 interrupt event to INT1. Default value: 0 (0: routing to INT1 disabled; 1: routing to INT1 enabled)
INT1_FSM7 <sup>(1)</sup>	Routing FSM7 interrupt event to INT1. Default value: 0 (0: routing to INT1 disabled; 1: routing to INT1 enabled)
INT1_FSM6 <sup>(1)</sup>	Routing FSM6 interrupt event to INT1. Default value: 0 (0: routing to INT1 disabled; 1: routing to INT1 enabled)
INT1_FSM5 <sup>(1)</sup>	Routing FSM5 interrupt event to INT1. Default value: 0 (0: routing to INT1 disabled; 1: routing to INT1 enabled)
INT1_FSM4 <sup>(1)</sup>	Routing FSM4 interrupt event to INT1. Default value: 0 (0: routing to INT1 disabled; 1: routing to INT1 enabled)
INT1_FSM3 <sup>(1)</sup>	Routing FSM3 interrupt event to INT1. Default value: 0 (0: routing to INT1 disabled; 1: routing to INT1 enabled)
INT1_FSM2 <sup>(1)</sup>	Routing FSM2 interrupt event to INT1. Default value: 0 (0: routing to INT1 disabled; 1: routing to INT1 enabled)
INT1_FSM1 <sup>(1)</sup>	Routing FSM1 interrupt event to INT1. Default value: 0 (0: routing to INT1 disabled; 1: routing to INT1 enabled)

1. This bit is activated if the INT1\_EMB\_FUNC bit of MD1\_CFG (5Eh) is set to 1.



## 11.7 FSM\_INT1\_B (0Ch)

INT1 pin control register (R/W)

Each bit in this register enables a signal to be carried over INT1. The pin's output supplies the OR combination of the selected signals.

**Table 161. FSM\_INT1\_B register**

INT1_FSM16	INT1_FSM15	INT1_FSM14	INT1_FSM13	INT1_FSM12	INT1_FSM11	INT1_FSM10	INT1_FSM9
------------	------------	------------	------------	------------	------------	------------	-----------

**Table 162. FSM\_INT1\_B register description**

INT1_FSM16 <sup>(1)</sup>	Routing FSM16 interrupt event to INT1. Default value: 0 (0: routing to INT1 disabled; 1: routing to INT1 enabled)
INT1_FSM15 <sup>(1)</sup>	Routing FSM15 interrupt event to INT1. Default value: 0 (0: routing to INT1 disabled; 1: routing to INT1 enabled)
INT1_FSM14 <sup>(1)</sup>	Routing FSM14 interrupt event to INT1. Default value: 0 (0: routing to INT1 disabled; 1: routing to INT1 enabled)
INT1_FSM13 <sup>(1)</sup>	Routing FSM13 interrupt event to INT1. Default value: 0 (0: routing to INT1 disabled; 1: routing to INT1 enabled)
INT1_FSM12 <sup>(1)</sup>	Routing FSM12 interrupt event to INT1. Default value: 0 (0: routing to INT1 disabled; 1: routing to INT1 enabled)
INT1_FSM11 <sup>(1)</sup>	Routing FSM11 interrupt event to INT1. Default value: 0 (0: routing to INT1 disabled; 1: routing to INT1 enabled)
INT1_FSM10 <sup>(1)</sup>	Routing FSM10 interrupt event to INT1. Default value: 0 (0: routing to INT1 disabled; 1: routing to INT1 enabled)
INT1_FSM9 <sup>(1)</sup>	Routing FSM9 interrupt event to INT1. Default value: 0 (0: routing to INT1 disabled; 1: routing to INT1 enabled)

1. This bit is activated if the INT1\_EMB\_FUNC bit of MD1\_CFG (5Eh) is set to 1.

## 11.8 MLC\_INT1 (0Dh)

INT1 pin control register (R/W)

Each bit in this register enables a signal to be carried over INT1. The pin's output supplies the OR combination of the selected signals.

**Table 163. MLC\_INT1 register**

INT1_MLC8	INT1_MLC7	INT1_MLC6	INT1_MLC5	INT1_MLC4	INT1_MLC3	INT1_MLC2	INT1_MLC1
-----------	-----------	-----------	-----------	-----------	-----------	-----------	-----------

**Table 164. MLC\_INT1 register description**

INT1_MLC8	Routing MLC8 interrupt event to INT1. Default value: 0 (0: routing to INT1 disabled; 1: routing to INT1 enabled)
INT1_MLC7	Routing MLC7 interrupt event to INT1. Default value: 0 (0: routing to INT1 disabled; 1: routing to INT1 enabled)
INT1_MLC6	Routing MLC6 interrupt event to INT1. Default value: 0 (0: routing to INT1 disabled; 1: routing to INT1 enabled)
INT1_MLC5	Routing MLC5 interrupt event to INT1. Default value: 0 (0: routing to INT1 disabled; 1: routing to INT1 enabled)
INT1_MLC4	Routing MLC4 interrupt event to INT1. Default value: 0 (0: routing to INT1 disabled; 1: routing to INT1 enabled)
INT1_MLC3	Routing MLC3 interrupt event to INT1. Default value: 0 (0: routing to INT1 disabled; 1: routing to INT1 enabled)
INT1_MLC2	Routing MLC2 interrupt event to INT1. Default value: 0 (0: routing to INT1 disabled; 1: routing to INT1 enabled)
INT1_MLC1	Routing MLC1 interrupt event to INT1. Default value: 0 (0: routing to INT1 disabled; 1: routing to INT1 enabled)

## 11.9 EMB\_FUNC\_INT2 (0Eh)

INT2 pin control register (R/W)

Each bit in this register enables a signal to be carried over INT2. The pin's output supplies the OR combination of the selected signals.

**Table 165. EMB\_FUNC\_INT2 register**

INT2_FSM_LC	0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>
-------------	------------------	------------------	------------------	------------------	------------------	------------------	------------------

1. This bit must be set to 0 for the correct operation of the device.

**Table 166. EMB\_FUNC\_INT2 register description**

INT2_FSM_LC <sup>(1)</sup>	Routing FSM long counter timeout interrupt event to INT2. Default value: 0 (0: routing to INT2 disabled; 1: routing to INT2 enabled)
----------------------------	---

1. This bit is activated if the INT2\_EMB\_FUNC bit of MD2\_CFG (5Fh) is set to 1.

## 11.10 FSM\_INT2\_A (0Fh)

INT2 pin control register (R/W)

Each bit in this register enables a signal to be carried over INT2. The pin's output supplies the OR combination of the selected signals.

**Table 167. FSM\_INT2\_A register**

INT2_FSM8	INT2_FSM7	INT2_FSM6	INT2_FSM5	INT2_FSM4	INT2_FSM3	INT2_FSM2	INT2_FSM1
-----------	-----------	-----------	-----------	-----------	-----------	-----------	-----------

**Table 168. FSM\_INT2\_A register description**

INT2_FSM8 <sup>(1)</sup>	Routing FSM8 interrupt event to INT2. Default value: 0 (0: routing to INT2 disabled; 1: routing to INT2 enabled)
INT2_FSM7 <sup>(1)</sup>	Routing FSM7 interrupt event to INT2. Default value: 0 (0: routing to INT2 disabled; 1: routing to INT2 enabled)
INT2_FSM6 <sup>(1)</sup>	Routing FSM6 interrupt event to INT2. Default value: 0 (0: routing to INT2 disabled; 1: routing to INT2 enabled)
INT2_FSM5 <sup>(1)</sup>	Routing FSM5 interrupt event to INT2. Default value: 0 (0: routing to INT2 disabled; 1: routing to INT2 enabled)
INT2_FSM4 <sup>(1)</sup>	Routing FSM4 interrupt event to INT2. Default value: 0 (0: routing to INT2 disabled; 1: routing to INT2 enabled)
INT2_FSM3 <sup>(1)</sup>	Routing FSM3 interrupt event to INT2. Default value: 0 (0: routing to INT2 disabled; 1: routing to INT2 enabled) (0: routing to INT1 disabled; 1: routing to INT1 enabled)
INT2_FSM2 <sup>(1)</sup>	Routing FSM2 interrupt event to INT2. Default value: 0 (0: routing to INT2 disabled; 1: routing to INT2 enabled)
INT2_FSM1 <sup>(1)</sup>	Routing FSM1 interrupt event to INT2. Default value: 0 (0: routing to INT2 disabled; 1: routing to INT2 enabled)

1. This bit is activated if the INT2\_EMB\_FUNC bit of MD2\_CFG (5Fh) is set to 1.

## 11.11 FSM\_INT2\_B (10h)

INT2 pin control register (R/W)

Each bit in this register enables a signal to be carried over INT2. The pin's output supplies the OR combination of the selected signals.

**Table 169. FSM\_INT2\_B register**

INT2_FSM16	INT2_FSM15	INT2_FSM14	INT2_FSM13	INT2_FSM12	INT2_FSM11	INT2_FSM10	INT2_FSM9
------------	------------	------------	------------	------------	------------	------------	-----------

**Table 170. FSM\_INT2\_B register description**

INT2_FSM16 <sup>(1)</sup>	Routing FSM16 interrupt event to INT2. Default value: 0 (0: routing to INT2 disabled; 1: routing to INT2 enabled)
INT2_FSM15 <sup>(1)</sup>	Routing FSM15 interrupt event to INT2. Default value: 0 (0: routing to INT2 disabled; 1: routing to INT2 enabled)
INT2_FSM14 <sup>(1)</sup>	Routing FSM14 interrupt event to INT2. Default value: 0 (0: routing to INT2 disabled; 1: routing to INT2 enabled)
INT2_FSM13 <sup>(1)</sup>	Routing FSM13 interrupt event to INT2. Default value: 0 (0: routing to INT2 disabled; 1: routing to INT2 enabled)
INT2_FSM12 <sup>(1)</sup>	Routing FSM12 interrupt event to INT2. Default value: 0 (0: routing to INT2 disabled; 1: routing to INT2 enabled)
INT2_FSM11 <sup>(1)</sup>	Routing FSM11 interrupt event to INT2. Default value: 0 (0: routing to INT2 disabled; 1: routing to INT2 enabled)
INT2_FSM10 <sup>(1)</sup>	Routing FSM10 interrupt event to INT2. Default value: 0 (0: routing to INT2 disabled; 1: routing to INT2 enabled)
INT2_FSM9 <sup>(1)</sup>	Routing FSM9 interrupt event to INT2. Default value: 0 (0: routing to INT2 disabled; 1: routing to INT2 enabled)

1. This bit is activated if the INT2\_EMB\_FUNC bit of MD2\_CFG (5Fh) is set to 1.

## 11.12 MLC\_INT2 (11h)

INT2 pin control register (R/W)

Each bit in this register enables a signal to be carried over INT2. The pin's output supplies the OR combination of the selected signals.

**Table 171. MLC\_INT2 register**

INT2_MLC8	INT2_MLC7	INT2_MLC6	INT2_MLC5	INT2_MLC4	INT2_MLC3	INT2_MLC2	INT2_MLC1
-----------	-----------	-----------	-----------	-----------	-----------	-----------	-----------

**Table 172. MLC\_INT2 register description**

INT2_MLC8	Routing MLC8 interrupt event to INT2. Default value: 0 (0: routing to INT2 disabled; 1: routing to INT2 enabled)
INT2_MLC7	Routing MLC7 interrupt event to INT2. Default value: 0 (0: routing to INT2 disabled; 1: routing to INT2 enabled)
INT2_MLC6	Routing MLC6 interrupt event to INT2. Default value: 0 (0: routing to INT2 disabled; 1: routing to INT2 enabled)
INT2_MLC5	Routing MLC5 interrupt event to INT2. Default value: 0 (0: routing to INT2 disabled; 1: routing to INT2 enabled)
INT2_MLC4	Routing MLC4 interrupt event to INT2. Default value: 0 (0: routing to INT2 disabled; 1: routing to INT2 enabled)
INT2_MLC3	Routing MLC3 interrupt event on INT2. Default value: 0 (0: routing to INT2 disabled; 1: routing to INT2 enabled)
INT2_MLC2	Routing MLC2 interrupt event to INT2. Default value: 0 (0: routing to INT2 disabled; 1: routing to INT2 enabled)
INT2_MLC1	Routing MLC1 interrupt event to INT2. Default value: 0 (0: routing to INT2 disabled; 1: routing to INT2 enabled)

## 11.13 EMB\_FUNC\_STATUS (12h)

Embedded function status register (R)

**Table 173. EMB\_FUNC\_STATUS register**

IS_FSM_LC	0	0	0	0	0	0	0
-----------	---	---	---	---	---	---	---

**Table 174. EMB\_FUNC\_STATUS register description**

IS_FSM_LC	Interrupt status bit for FSM long counter timeout interrupt event. (1: interrupt detected; 0: no interrupt)
-----------	--

## 11.14 FSM\_STATUS\_A (13h)

Finite state machine status register (R)

**Table 175. FSM\_STATUS\_A register**

IS_FSM8	IS_FSM7	IS_FSM6	IS_FSM5	IS_FSM4	IS_FSM3	IS_FSM2	IS_FSM1
---------	---------	---------	---------	---------	---------	---------	---------

**Table 176. FSM\_STATUS\_A register description**

IS_FSM8	Interrupt status bit for FSM8 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM7	Interrupt status bit for FSM7 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM6	Interrupt status bit for FSM6 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM5	Interrupt status bit for FSM5 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM4	Interrupt status bit for FSM4 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM3	Interrupt status bit for FSM3 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM2	Interrupt status bit for FSM2 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM1	Interrupt status bit for FSM1 interrupt event. (1: interrupt detected; 0: no interrupt)

## 11.15 FSM\_STATUS\_B (14h)

Finite state machine status register (R)

**Table 177. FSM\_STATUS\_B register**

IS_FSM16	IS_FSM15	IS_FSM14	IS_FSM13	IS_FSM12	IS_FSM11	IS_FSM10	IS_FSM9
----------	----------	----------	----------	----------	----------	----------	---------

**Table 178. FSM\_STATUS\_B register description**

IS_FSM16	Interrupt status bit for FSM16 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM15	Interrupt status bit for FSM15 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM14	Interrupt status bit for FSM14 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM13	Interrupt status bit for FSM13 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM12	Interrupt status bit for FSM12 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM11	Interrupt status bit for FSM11 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM10	Interrupt status bit for FSM10 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_FSM9	Interrupt status bit for FSM9 interrupt event. (1: interrupt detected; 0: no interrupt)

## 11.16 MLC\_STATUS (15h)

Machine learning core status register (R)

**Table 179. MLC\_STATUS register**

IS_MLC8	IS_MLC7	IS_MLC6	IS_MLC5	IS_MLC4	IS_MLC3	IS_MLC2	IS_MLC1
---------	---------	---------	---------	---------	---------	---------	---------

**Table 180. MLC\_STATUS register description**

IS_MLC8	Interrupt status bit for MLC8 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_MLC7	Interrupt status bit for MLC7 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_MLC6	Interrupt status bit for MLC6 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_MLC5	Interrupt status bit for MLC5 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_MLC4	Interrupt status bit for MLC4 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_MLC3	Interrupt status bit for MLC3 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_MLC2	Interrupt status bit for MLC2 interrupt event. (1: interrupt detected; 0: no interrupt)
IS_MLC1	Interrupt status bit for MLC1 interrupt event. (1: interrupt detected; 0: no interrupt)



## 11.17 PAGE\_RW (17h)

Enable read and write mode of advanced features dedicated page (R/W)

**Table 181. PAGE\_RW register**

EMB_FUNC_LIR	PAGE_WRITE	PAGE_READ	0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>
--------------	------------	-----------	------------------	------------------	------------------	------------------	------------------

1. This bit must be set to 0 for the correct operation of the device.

**Table 182. PAGE\_RW register description**

EMB_FUNC_LIR	Latched interrupt mode for embedded functions. Default value: 0 (0: embedded functions interrupt request not latched; 1: embedded functions interrupt request latched)
PAGE_WRITE	Enables writes to the selected advanced features dedicated page. <sup>(1)</sup> Default value: 0 (1: enable; 0: disable)
PAGE_READ	Enables reads from the selected advanced features dedicated page. <sup>(1)</sup> Default value: 0 (1: enable; 0: disable)

1. Page selected by PAGE\_SEL[3:0] in PAGE\_SEL (02h) register.

## 11.18 FSM\_ENABLE\_A (46h)

Enable FSM register (R/W)

**Table 183. FSM\_ENABLE\_A register**

FSM8_EN	FSM7_EN	FSM6_EN	FSM5_EN	FSM4_EN	FSM3_EN	FSM2_EN	FSM1_EN
---------	---------	---------	---------	---------	---------	---------	---------

**Table 184. FSM\_ENABLE\_A register description**

FSM8_EN	Enables FSM8. Default value: 0 (0: FSM8 disabled; 1: FSM8 enabled)
FSM7_EN	Enables FSM7. Default value: 0 (0: FSM7 disabled; 1: FSM7 enabled)
FSM6_EN	Enables FSM6. Default value: 0 (0: FSM6 disabled; 1: FSM6 enabled)
FSM5_EN	Enables FSM5. Default value: 0 (0: FSM5 disabled; 1: FSM5 enabled)
FSM4_EN	Enables FSM4. Default value: 0 (0: FSM4 disabled; 1: FSM4 enabled)
FSM3_EN	Enables FSM3. Default value: 0 (0: FSM3 disabled; 1: FSM3 enabled)
FSM2_EN	Enables FSM2. Default value: 0 (0: FSM2 disabled; 1: FSM2 enabled)
FSM1_EN	Enables FSM1. Default value: 0 (0: FSM1 disabled; 1: FSM1 enabled)

## 11.19 FSM\_ENABLE\_B (47h)

Enable FSM register (R/W)

**Table 185. FSM\_ENABLE\_B register**

FSM16_EN	FSM15_EN	FSM14_EN	FSM13_EN	FSM12_EN	FSM11_EN	FSM10_EN	FSM9_EN
----------	----------	----------	----------	----------	----------	----------	---------

**Table 186. FSM\_ENABLE\_B register description**

FSM16_EN	Enables FSM16. Default value: 0 (0: FSM16 disabled; 1: FSM16 enabled)
FSM15_EN	Enables FSM15. Default value: 0 (0: FSM15 disabled; 1: FSM15 enabled)
FSM14_EN	Enables FSM14. Default value: 0 (0: FSM14 disabled; 1: FSM14 enabled)
FSM13_EN	Enables FSM13. Default value: 0 (0: FSM13 disabled; 1: FSM13 enabled)
FSM12_EN	Enables FSM12. Default value: 0 (0: FSM12 disabled; 1: FSM12 enabled)
FSM11_EN	Enables FSM11. Default value: 0 (0: FSM11 disabled; 1: FSM11 enabled)
FSM10_EN	Enables FSM10. Default value: 0 (0: FSM10 disabled; 1: FSM10 enabled)
FSM9_EN	Enables FSM9. Default value: 0 (0: FSM9 disabled; 1: FSM9 enabled)

## 11.20 FSM\_LONG\_COUNTER\_L (48h) and FSM\_LONG\_COUNTER\_H (49h)

FSM long counter status register (R/W)

Long counter value is an unsigned integer value (16-bit format); this value can be reset using the LC\_CLEAR bit in FSM\_LONG\_COUNTER\_CLEAR (4Ah) register.

**Table 187. FSM\_LONG\_COUNTER\_L register**

FSM_LC_7	FSM_LC_6	FSM_LC_5	FSM_LC_4	FSM_LC_3	FSM_LC_2	FSM_LC_1	FSM_LC_0
----------	----------	----------	----------	----------	----------	----------	----------

**Table 188. FSM\_LONG\_COUNTER\_L register description**

FSM_LC_[7:0]	Long counter current value (LSbyte). Default value: 00000000
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**Table 189. FSM\_LONG\_COUNTER\_H register**

FSM_LC_15	FSM_LC_14	FSM_LC_13	FSM_LC_12	FSM_LC_11	FSM_LC_10	FSM_LC_9	FSM_LC_8
-----------	-----------	-----------	-----------	-----------	-----------	----------	----------

**Table 190. FSM\_LONG\_COUNTER\_H register description**

FSM_LC_[15:8]	Long counter current value (MSbyte). Default value: 00000000
---------------	--

## 11.21 FSM\_LONG\_COUNTER\_CLEAR (4Ah)

FSM long counter reset register (R/W)

**Table 191. FSM\_LONG\_COUNTER\_CLEAR register**

0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>	FSM_LC_CLEARED	FSM_LC_CLEAR
------------------	------------------	------------------	------------------	------------------	------------------	----------------	--------------

1. This bit must be set to 0 for the correct operation of the device.

**Table 192. FSM\_LONG\_COUNTER\_CLEAR register description**

FSM_LC_CLEARED	This read-only bit is automatically set to 1 when the long counter reset is done. Default value: 0
FSM_LC_CLEAR	Clear FSM long counter value. Default value: 0

## 11.22 FSM\_OUTS1 (4Ch)

FSM1 output register (R)

**Table 193. FSM\_OUTS1 register**

P_X	N_X	P_Y	N_Y	P_Z	N_Z	P_V	N_V
-----	-----	-----	-----	-----	-----	-----	-----

**Table 194. FSM\_OUTS1 register description**

P_X	FSM1 output: positive event detected on the X-axis. (0: event not detected; 1: event detected)
N_X	FSM1 output: negative event detected on the X-axis. (0: event not detected; 1: event detected)
P_Y	FSM1 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected)
N_Y	FSM1 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected)
P_Z	FSM1 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected)
N_Z	FSM1 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected)
P_V	FSM1 output: positive event detected on the vector. (0: event not detected; 1: event detected)
N_V	FSM1 output: negative event detected on the vector. (0: event not detected; 1: event detected)

**11.23 FSM\_OUTS2 (4Dh)**  
FSM2 output register (R)

**Table 195. FSM\_OUTS2 register**

P_X	N_X	P_Y	N_Y	P_Z	N_Z	P_V	N_V
-----	-----	-----	-----	-----	-----	-----	-----

**Table 196. FSM\_OUTS2 register description**

P_X	FSM2 output: positive event detected on the X-axis. (0: event not detected; 1: event detected)
N_X	FSM2 output: negative event detected on the X-axis. (0: event not detected; 1: event detected)
P_Y	FSM2 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected)
N_Y	FSM2 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected)
P_Z	FSM2 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected)
N_Z	FSM2 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected)
P_V	FSM2 output: positive event detected on the vector. (0: event not detected; 1: event detected)
N_V	FSM2 output: negative event detected on the vector. (0: event not detected; 1: event detected)

## 11.24 FSM\_OUTS3 (4Eh)

FSM3 output register (R)

**Table 197. FSM\_OUTS3 register**

P_X	N_X	P_Y	N_Y	P_Z	N_Z	P_V	N_V
-----	-----	-----	-----	-----	-----	-----	-----

**Table 198. FSM\_OUTS3 register description**

P_X	FSM3 output: positive event detected on the X-axis. (0: event not detected; 1: event detected)
N_X	FSM3 output: negative event detected on the X-axis. (0: event not detected; 1: event detected)
P_Y	FSM3 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected)
N_Y	FSM3 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected)
P_Z	FSM3 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected)
N_Z	FSM3 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected)
P_V	FSM3 output: positive event detected on the vector. (0: event not detected; 1: event detected)
N_V	FSM3 output: negative event detected on the vector. (0: event not detected; 1: event detected)

## 11.25 FSM\_OUTS4 (4Fh)

FSM4 output register (R)

**Table 199. FSM\_OUTS4 register**

P_X	N_X	P_Y	N_Y	P_Z	N_Z	P_V	N_V
-----	-----	-----	-----	-----	-----	-----	-----

**Table 200. FSM\_OUTS4 register description**

P_X	FSM4 output: positive event detected on the X-axis. (0: event not detected; 1: event detected)
N_X	FSM4 output: negative event detected on the X-axis. (0: event not detected; 1: event detected)
P_Y	FSM4 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected)
N_Y	FSM4 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected)
P_Z	FSM4 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected)
N_Z	FSM4 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected)
P_V	FSM4 output: positive event detected on the vector. (0: event not detected; 1: event detected)
N_V	FSM4 output: negative event detected on the vector. (0: event not detected; 1: event detected)

## 11.26 FSM\_OUTS5 (50h)

FSM5 output register (R)

**Table 201. FSM\_OUTS5 register**

P_X	N_X	P_Y	N_Y	P_Z	N_Z	P_V	N_V
-----	-----	-----	-----	-----	-----	-----	-----

**Table 202. FSM\_OUTS5 register description**

P_X	FSM5 output: positive event detected on the X-axis. (0: event not detected; 1: event detected)
N_X	FSM5 output: negative event detected on the X-axis. (0: event not detected; 1: event detected)
P_Y	FSM5 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected)
N_Y	FSM5 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected)
P_Z	FSM5 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected)
N_Z	FSM5 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected)
P_V	FSM5 output: positive event detected on the vector. (0: event not detected; 1: event detected)
N_V	FSM5 output: negative event detected on the vector. (0: event not detected; 1: event detected)



## 11.27 FSM\_OUTS6 (51h)

FSM6 output register (R)

**Table 203. FSM\_OUTS6 register**

P_X	N_X	P_Y	N_Y	P_Z	N_Z	P_V	N_V
-----	-----	-----	-----	-----	-----	-----	-----

**Table 204. FSM\_OUTS6 register description**

P_X	FSM6 output: positive event detected on the X-axis. (0: event not detected; 1: event detected)
N_X	FSM6 output: negative event detected on the X-axis. (0: event not detected; 1: event detected)
P_Y	FSM6 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected)
N_Y	FSM6 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected)
P_Z	FSM6 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected)
N_Z	FSM6 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected)
P_V	FSM6 output: positive event detected on the vector. (0: event not detected; 1: event detected)
N_V	FSM6 output: negative event detected on the vector. (0: event not detected; 1: event detected)

## 11.28 FSM\_OUTS7 (52h)

FSM7 output register (R)

**Table 205. FSM\_OUTS7 register**

P_X	N_X	P_Y	N_Y	P_Z	N_Z	P_V	N_V
-----	-----	-----	-----	-----	-----	-----	-----

**Table 206. FSM\_OUTS7 register description**

P_X	FSM7 output: positive event detected on the X-axis. (0: event not detected; 1: event detected)
N_X	FSM7 output: negative event detected on the X-axis. (0: event not detected; 1: event detected)
P_Y	FSM7 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected)
N_Y	FSM7 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected)
P_Z	FSM7 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected)
N_Z	FSM7 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected)
P_V	FSM7 output: positive event detected on the vector. (0: event not detected; 1: event detected)
N_V	FSM7 output: negative event detected on the vector. (0: event not detected; 1: event detected)

## 11.29 FSM\_OUTS8 (53h)

FSM8 output register (R)

**Table 207. FSM\_OUTS8 register**

P_X	N_X	P_Y	N_Y	P_Z	N_Z	P_V	N_V
-----	-----	-----	-----	-----	-----	-----	-----

**Table 208. FSM\_OUTS8 register description**

P_X	FSM8 output: positive event detected on the X-axis. (0: event not detected; 1: event detected)
N_X	FSM8 output: negative event detected on the X-axis. (0: event not detected; 1: event detected)
P_Y	FSM8 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected)
N_Y	FSM8 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected)
P_Z	FSM8 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected)
N_Z	FSM8 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected)
P_V	FSM8 output: positive event detected on the vector. (0: event not detected; 1: event detected)
N_V	FSM8 output: negative event detected on the vector. (0: event not detected; 1: event detected)

## 11.30 FSM\_OUTS9 (54h)

FSM9 output register (R)

**Table 209. FSM\_OUTS9 register**

P_X	N_X	P_Y	N_Y	P_Z	N_Z	P_V	N_V
-----	-----	-----	-----	-----	-----	-----	-----

**Table 210. FSM\_OUTS9 register description**

P_X	FSM9 output: positive event detected on the X-axis. (0: event not detected; 1: event detected)
N_X	FSM9 output: negative event detected on the X-axis. (0: event not detected; 1: event detected)
P_Y	FSM9 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected)
N_Y	FSM9 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected)
P_Z	FSM9 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected)
N_Z	FSM9 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected)
P_V	FSM9 output: positive event detected on the vector. (0: event not detected; 1: event detected)
N_V	FSM9 output: negative event detected on the vector. (0: event not detected; 1: event detected)

## 11.31 FSM\_OUTS10 (55h)

FSM10 output register (R)

**Table 211. FSM\_OUTS10 register**

P_X	N_X	P_Y	N_Y	P_Z	N_Z	P_V	N_V
-----	-----	-----	-----	-----	-----	-----	-----

**Table 212. FSM\_OUTS10 register description**

P_X	FSM10 output: positive event detected on the X-axis. (0: event not detected; 1: event detected)
N_X	FSM10 output: negative event detected on the X-axis. (0: event not detected; 1: event detected)
P_Y	FSM10 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected)
N_Y	FSM10 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected)
P_Z	FSM10 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected)
N_Z	FSM10 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected)
P_V	FSM10 output: positive event detected on the vector. (0: event not detected; 1: event detected)
N_V	FSM10 output: negative event detected on the vector. (0: event not detected; 1: event detected)

## 11.32 FSM\_OUTS11 (56h)

FSM11 output register (R)

**Table 213. FSM\_OUTS11 register**

P_X	N_X	P_Y	N_Y	P_Z	N_Z	P_V	N_V
-----	-----	-----	-----	-----	-----	-----	-----

**Table 214. FSM\_OUTS11 register description**

P_X	FSM11 output: positive event detected on the X-axis. (0: event not detected; 1: event detected)
N_X	FSM11 output: negative event detected on the X-axis. (0: event not detected; 1: event detected)
P_Y	FSM11 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected)
N_Y	FSM11 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected)
P_Z	FSM11 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected)
N_Z	FSM11 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected)
P_V	FSM11 output: positive event detected on the vector. (0: event not detected; 1: event detected)
N_V	FSM11 output: negative event detected on the vector. (0: event not detected; 1: event detected)

## 11.33 FSM\_OUTS12 (57h)

FSM12 output register (R)

**Table 215. FSM\_OUTS12 register**

P_X	N_X	P_Y	N_Y	P_Z	N_Z	P_V	N_V
-----	-----	-----	-----	-----	-----	-----	-----

**Table 216. FSM\_OUTS12 register description**

P_X	FSM12 output: positive event detected on the X-axis. (0: event not detected; 1: event detected)
N_X	FSM12 output: negative event detected on the X-axis. (0: event not detected; 1: event detected)
P_Y	FSM12 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected)
N_Y	FSM12 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected)
P_Z	FSM12 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected)
N_Z	FSM12 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected)
P_V	FSM12 output: positive event detected on the vector. (0: event not detected; 1: event detected)
N_V	FSM12 output: negative event detected on the vector. (0: event not detected; 1: event detected)

## 11.34 FSM\_OUTS13 (58h)

FSM13 output register (R)

**Table 217. FSM\_OUTS13 register**

P_X	N_X	P_Y	N_Y	P_Z	N_Z	P_V	N_V
-----	-----	-----	-----	-----	-----	-----	-----

**Table 218. FSM\_OUTS13 register description**

P_X	FSM13 output: positive event detected on the X-axis. (0: event not detected; 1: event detected)
N_X	FSM13 output: negative event detected on the X-axis. (0: event not detected; 1: event detected)
P_Y	FSM13 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected)
N_Y	FSM13 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected)
P_Z	FSM13 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected)
N_Z	FSM13 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected)
P_V	FSM13 output: positive event detected on the vector. (0: event not detected; 1: event detected)
N_V	FSM13 output: negative event detected on the vector. (0: event not detected; 1: event detected)



## 11.35 FSM\_OUTS14 (59h)

FSM14 output register (R)

**Table 219. FSM\_OUTS14 register**

P_X	N_X	P_Y	N_Y	P_Z	N_Z	P_V	N_V
-----	-----	-----	-----	-----	-----	-----	-----

**Table 220. FSM\_OUTS14 register description**

P_X	FSM14 output: positive event detected on the X-axis. (0: event not detected; 1: event detected)
N_X	FSM14 output: negative event detected on the X-axis. (0: event not detected; 1: event detected)
P_Y	FSM14 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected)
N_Y	FSM14 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected)
P_Z	FSM14 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected)
N_Z	FSM14 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected)
P_V	FSM14 output: positive event detected on the vector. (0: event not detected; 1: event detected)
N_V	FSM14 output: negative event detected on the vector. (0: event not detected; 1: event detected)

## 11.36 FSM\_OUTS15 (5Ah)

FSM15 output register (R)

**Table 221. FSM\_OUTS15 register**

P_X	N_X	P_Y	N_Y	P_Z	N_Z	P_V	N_V
-----	-----	-----	-----	-----	-----	-----	-----

**Table 222. FSM\_OUTS15 register description**

P_X	FSM15 output: positive event detected on the X-axis. (0: event not detected; 1: event detected)
N_X	FSM15 output: negative event detected on the X-axis. (0: event not detected; 1: event detected)
P_Y	FSM15 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected)
N_Y	FSM15 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected)
P_Z	FSM15 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected)
N_Z	FSM15 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected)
P_V	FSM15 output: positive event detected on the vector. (0: event not detected; 1: event detected)
N_V	FSM15 output: negative event detected on the vector. (0: event not detected; 1: event detected)

### 11.37 FSM\_OUTS16 (5Bh)

FSM16 output register (R)

**Table 223. FSM\_OUTS16 register**

P_X	N_X	P_Y	N_Y	P_Z	N_Z	P_V	N_V
-----	-----	-----	-----	-----	-----	-----	-----

**Table 224. FSM\_OUTS16 register description**

P_X	FSM16 output: positive event detected on the X-axis. (0: event not detected; 1: event detected)
N_X	FSM16 output: negative event detected on the X-axis. (0: event not detected; 1: event detected)
P_Y	FSM16 output: positive event detected on the Y-axis. (0: event not detected; 1: event detected)
N_Y	FSM16 output: negative event detected on the Y-axis. (0: event not detected; 1: event detected)
P_Z	FSM16 output: positive event detected on the Z-axis. (0: event not detected; 1: event detected)
N_Z	FSM16 output: negative event detected on the Z-axis. (0: event not detected; 1: event detected)
P_V	FSM16 output: positive event detected on the vector. (0: event not detected; 1: event detected)
N_V	FSM16 output: negative event detected on the vector. (0: event not detected; 1: event detected)

### 11.38 EMB\_FUNC\_ODR\_CFG\_B (5Fh)

Finite state machine output data rate configuration register (R/W)

**Table 225. EMB\_FUNC\_ODR\_CFG\_B register**

0 <sup>(1)</sup>	1 <sup>(2)</sup>	0 <sup>(1)</sup>	FSM_ODR1	FSM_ODR0	0 <sup>(1)</sup>	1 <sup>(2)</sup>	1 <sup>(2)</sup>
------------------	------------------	------------------	----------	----------	------------------	------------------	------------------

1. This bit must be set to 0 for the correct operation of the device.
2. This bit must be set to 1 for the correct operation of the device

**Table 226. EMB\_FUNC\_ODR\_CFG\_B register description**

FSM_ODR[1:0]	Finite state machine ODR configuration: (00: 12.5 Hz; 01: 26 Hz (default); 10: 52 Hz; 11: 104 Hz)
--------------	---

### 11.39 EMB\_FUNC\_ODR\_CFG\_C (60h)

Machine learning core output data rate configuration register (R/W)

**Table 227. EMB\_FUNC\_ODR\_CFG\_C register**

0 <sup>(1)</sup>	0 <sup>(1)</sup>	MLC_ODR1	MLC_ODR0	0 <sup>(1)</sup>	1 <sup>(2)</sup>	0 <sup>(1)</sup>	1 <sup>(2)</sup>
------------------	------------------	----------	----------	------------------	------------------	------------------	------------------

1. This bit must be set to 0 for the correct operation of the device.
2. This bit must be set to 1 for the correct operation of the device.

**Table 228. EMB\_FUNC\_ODR\_CFG\_C register description**

MLC_ODR[1:0]	Machine learning core ODR configuration: (00: 12.5 Hz; 01: 26 Hz (default); 10: 52 Hz; 11: 104 Hz)
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### 11.40 EMB\_FUNC\_INIT\_B (67h)

Embedded functions initialization register (R/W)

**Table 229. EMB\_FUNC\_INIT\_B register**

0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>	MLC_INIT	0 <sup>(1)</sup>	0 <sup>(1)</sup>	0 <sup>(1)</sup>	FSM_INIT
------------------	------------------	------------------	----------	------------------	------------------	------------------	----------

1. This bit must be set to 0 for the correct operation of the device.

**Table 230. EMB\_FUNC\_INIT\_B register description**

MLC_INIT	Machine learning core initialization request. Default value: 0
FSM_INIT	FSM initialization request. Default value: 0

### 11.41 MLC0\_SRC (70h)

Machine learning core source register (R)

**Table 231. MLC0\_SRC register**

MLC0_SRC_7	MLC0_SRC_6	MLC0_SRC_5	MLC0_SRC_4	MLC0_SRC_3	MLC0_SRC_2	MLC0_SRC_1	MLC0_SRC_0
------------	------------	------------	------------	------------	------------	------------	------------

**Table 232. MLC0\_SRC register description**

MLC0_SRC_[7:0]	Output value of MLC0 decision tree
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### 11.42 MLC1\_SRC (71h)

Machine learning core source register (R)

**Table 233. MLC1\_SRC register**

MLC1_SRC_7	MLC1_SRC_6	MLC1_SRC_5	MLC1_SRC_4	MLC1_SRC_3	MLC1_SRC_2	MLC1_SRC_1	MLC1_SRC_0
------------	------------	------------	------------	------------	------------	------------	------------

**Table 234. MLC1\_SRC register description**

MLC1_SRC_[7:0]	Output value of MLC1 decision tree
----------------	------------------------------------

### 11.43 MLC2\_SRC (72h)

Machine learning core source register (R)

**Table 235. MLC2\_SRC register**

MLC2_SRC_7	MLC2_SRC_6	MLC2_SRC_5	MLC2_SRC_4	MLC2_SRC_3	MLC2_SRC_2	MLC2_SRC_1	MLC2_SRC_0
------------	------------	------------	------------	------------	------------	------------	------------

**Table 236. MLC2\_SRC register description**

MLC2_SRC_[7:0]	Output value of MLC2 decision tree
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### 11.44 MLC3\_SRC (73h)

Machine learning core source register (R)

**Table 237. MLC3\_SRC register**

MLC3_SRC_7	MLC3_SRC_6	MLC3_SRC_5	MLC3_SRC_4	MLC3_SRC_3	MLC3_SRC_2	MLC3_SRC_1	MLC3_SRC_0
------------	------------	------------	------------	------------	------------	------------	------------

**Table 238. MLC3\_SRC register description**

MLC3_SRC_[7:0]	Output value of MLC3 decision tree
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### 11.45 MLC4\_SRC (74h)

Machine learning core source register (R)

**Table 239. MLC4\_SRC register**

MLC4_SRC_7	MLC4_SRC_6	MLC4_SRC_5	MLC4_SRC_4	MLC4_SRC_3	MLC4_SRC_2	MLC4_SRC_1	MLC4_SRC_0
------------	------------	------------	------------	------------	------------	------------	------------

**Table 240. MLC4\_SRC register description**

MLC4_SRC_[7:0]	Output value of MLC4 decision tree
----------------	------------------------------------

**11.46 MLC5\_SRC (75h)**

Machine learning core source register (R)

**Table 241. MLC5\_SRC register**

MLC5_SRC_7	MLC5_SRC_6	MLC5_SRC_5	MLC5_SRC_4	MLC5_SRC_3	MLC5_SRC_2	MLC5_SRC_1	MLC5_SRC_0
------------	------------	------------	------------	------------	------------	------------	------------

**Table 242. MLC5\_SRC register description**

MLC5_SRC_[7:0]	Output value of MLC5 decision tree
----------------	------------------------------------

**11.47 MLC6\_SRC (76h)**

Machine learning core source register (R)

**Table 243. MLC6\_SRC register**

MLC6_SRC_7	MLC6_SRC_6	MLC6_SRC_5	MLC6_SRC_4	MLC6_SRC_3	MLC6_SRC_2	MLC6_SRC_1	MLC6_SRC_0
------------	------------	------------	------------	------------	------------	------------	------------

**Table 244. MLC6\_SRC register description**

MLC6_SRC_[7:0]	Output value of MLC6 decision tree
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**11.48 MLC7\_SRC (77h)**

Machine learning core source register (R)

**Table 245. MLC7\_SRC register**

MLC7_SRC_7	MLC7_SRC_6	MLC7_SRC_5	MLC7_SRC_4	MLC7_SRC_3	MLC7_SRC_2	MLC7_SRC_1	MLC7_SRC_0
------------	------------	------------	------------	------------	------------	------------	------------

**Table 246. MLC7\_SRC register description**

MLC7_SRC_[7:0]	Output value of MLC7 decision tree
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## 12 Embedded advanced features

The following table provides a list of the registers for the embedded advanced features page 1. These registers are accessible when PAGE\_SEL[3:0] are set to 0001 in PAGE\_SEL (02h).

**Table 247. Register address map - embedded advanced features page 1**

Name	Type	Register address		Default	Comment
		Hex	Binary		
FSM_LC_TIMEOUT_L	R/W	7A	01111010	00000000	
FSM_LC_TIMEOUT_H	R/W	7B	01111011	00000000	
FSM_PROGRAMS	R/W	7C	01111100	00000000	
FSM_START_ADD_L	R/W	7E	01111110	00000000	
FSM_START_ADD_H	R/W	7F	01111111	00000000	

Reserved registers must not be changed. Writing to those registers may cause permanent damage to the device. The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

**Write procedure example:**

Example: write value 01h in register at address 7Ch (FSM\_PROGRAMS) in page 1

1. Write bit FUNC\_CFG\_EN = 1 in FUNC\_CFG\_ACCESS (01h) // Enable access to embedded functions registers
2. Write bit PAGE\_WRITE = 1 in PAGE\_RW (17h) // Select write operation mode
3. Write 0001 in the PAGE\_SEL[3:0] field of PAGE\_SEL (02h) // Select page 1
4. Write 7Ch in PAGE\_ADDRESS (08h) // Set address
5. Write 01h in PAGE\_VALUE (09h) // Set value to be written
6. Write bit PAGE\_WRITE = 0 in PAGE\_RW (17h) // Write operation disabled
7. Write bit FUNC\_CFG\_EN = 0 in FUNC\_CFG\_ACCESS (01h) // Disable access to embedded functions registers

**Read procedure example:**

Example: read value of register at address 7Ch (FSM\_PROGRAMS) in page 1

1. Write bit FUNC\_CFG\_EN = 1 in FUNC\_CFG\_ACCESS (01h) // Enable access to embedded functions registers
2. Write bit PAGE\_READ = 1 in PAGE\_RW (17h) // Select read operation mode
3. Write 0001 in the PAGE\_SEL[3:0] field of PAGE\_SEL (02h) // Select page 1
4. Write 7Ch in PAGE\_ADDRESS (08h) // Set address
5. Read value of PAGE\_VALUE (09h) // Get register value
6. Write bit PAGE\_READ = 0 in PAGE\_RW (17h) // Read operation disabled
7. Write bit FUNC\_CFG\_EN = 0 in FUNC\_CFG\_ACCESS (01h) // Disable access to embedded functions registers

*Note:* Steps 1 and 2 of both procedures are intended to be performed at the beginning of the procedure. Steps 6 and 7 of both procedures are intended to be performed at the end of the procedure. If the procedure involves multiple operations, only steps 3, 4 and 5 must be repeated for each operation. If, in particular, the multiple operations involve consecutive registers, only step 5 can be performed.

## 13 Embedded advanced features register description

### 13.1 Page 1 - Embedded advanced features registers

#### 13.1.1 FSM\_LC\_TIMEOUT\_L (7Ah) and FSM\_LC\_TIMEOUT\_H (7Bh)

FSM long counter timeout register (R/W)

The long counter timeout value is an unsigned integer value (16-bit format). When the long counter value reaches this value, the FSM generates an interrupt.

**Table 248. FSM\_LC\_TIMEOUT\_L register**

FSM_LC_TIMEOUT7	FSM_LC_TIMEOUT6	FSM_LC_TIMEOUT5	FSM_LC_TIMEOUT4	FSM_LC_TIMEOUT3	FSM_LC_TIMEOUT2	FSM_LC_TIMEOUT1	FSM_LC_TIMEOUT0
-----------------	-----------------	-----------------	-----------------	-----------------	-----------------	-----------------	-----------------

**Table 249. FSM\_LC\_TIMEOUT\_L register description**

FSM_LC_TIMEOUT[7:0]	FSM long counter timeout value (LSbyte). Default value: 00000000
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**Table 250. FSM\_LC\_TIMEOUT\_H register**

FSM_LC_TIMEOUT15	FSM_LC_TIMEOUT14	FSM_LC_TIMEOUT13	FSM_LC_TIMEOUT12	FSM_LC_TIMEOUT11	FSM_LC_TIMEOUT10	FSM_LC_TIMEOUT9	FSM_LC_TIMEOUT8
------------------	------------------	------------------	------------------	------------------	------------------	-----------------	-----------------

**Table 251. FSM\_LC\_TIMEOUT\_H register description**

FSM_LC_TIMEOUT[15:8]	FSM long counter timeout value (MSbyte). Default value: 00000000
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#### 13.1.2 FSM\_PROGRAMS (7Ch)

FSM number of programs register (R/W)

**Table 252. FSM\_PROGRAMS register**

FSM_N_PROG7	FSM_N_PROG6	FSM_N_PROG5	FSM_N_PROG4	FSM_N_PROG3	FSM_N_PROG2	FSM_N_PROG1	FSM_N_PROG0
-------------	-------------	-------------	-------------	-------------	-------------	-------------	-------------

**Table 253. FSM\_PROGRAMS register description**

FSM_N_PROG[7:0]	Number of FSM programs; must be less than or equal to 16. Default value: 00000000
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**13.1.3 FSM\_START\_ADD\_L (7Eh) and FSM\_START\_ADD\_H (7Fh)**

FSM start address register (R/W). First available address is 0x033C.

**Table 254. FSM\_START\_ADD\_L register**

FSM_START7	FSM_START6	FSM_START5	FSM_START4	FSM_START3	FSM_START2	FSM_START1	FSM_START0
------------	------------	------------	------------	------------	------------	------------	------------

**Table 255. FSM\_START\_ADD\_L register description**

FSM_START[7:0]	FSM start address value (LSbyte). Default value: 00000000
----------------	---

**Table 256. FSM\_START\_ADD\_H register**

FSM_START15	FSM_START14	FSM_START13	FSM_START12	FSM_START11	FSM_START10	FSM_START9	FSM_START8
-------------	-------------	-------------	-------------	-------------	-------------	------------	------------

**Table 257. FSM\_START\_ADD\_H register description**

FSM_START[15:8]	FSM start address value (MSbyte). Default value: 00000000
-----------------	---

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## 14 Soldering information

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The LGA package is compliant with the [ECOPACK](#) and RoHS standard.

It is qualified for soldering heat resistance according to JEDEC J-STD-020.

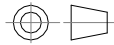
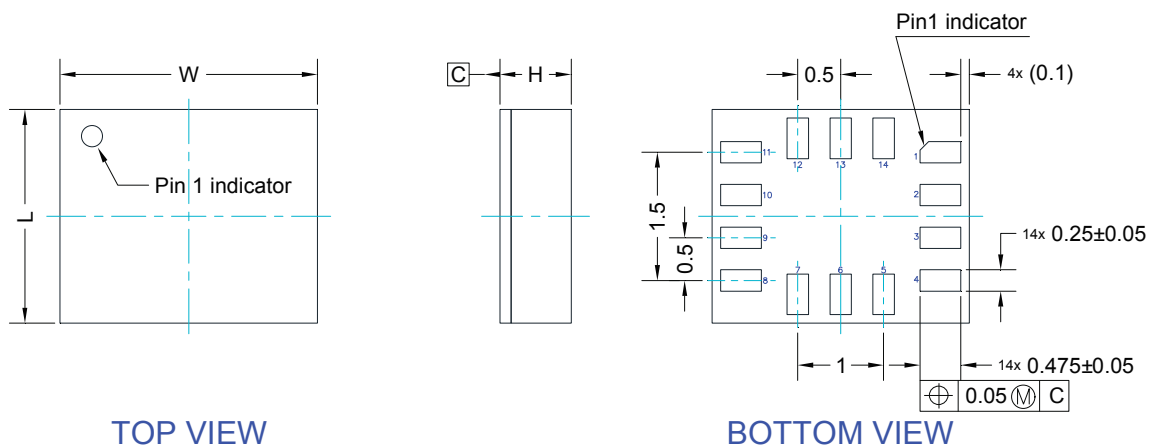
For land pattern and soldering recommendations, consult technical note [TN0018](#) available on [www.st.com](http://www.st.com).

## 15 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 15.1 LGA-14L package information

**Figure 23. LGA-14L 2.5 x 3.0 x 0.86 mm package outline and mechanical data**



Dimensions are in millimeter unless otherwise specified  
 General tolerance is  $\pm 0.1$  mm unless otherwise specified

#### OUTER DIMENSIONS

ITEM	DIMENSION [mm]	TOLERANCE [mm]
Length [L]	2.50	$\pm 0.1$
Width [W]	3.00	$\pm 0.1$
Height [H]	0.86	MAX

DM00249496\_5

## 15.2 LGA-14 packing information

Figure 24. Carrier tape information for LGA-14 package

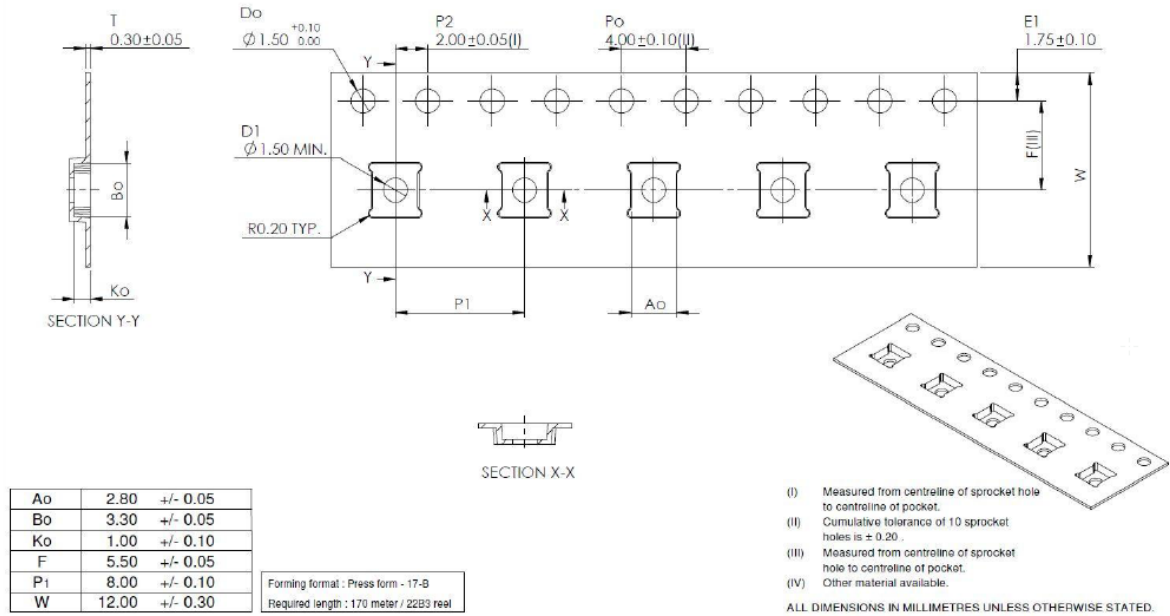
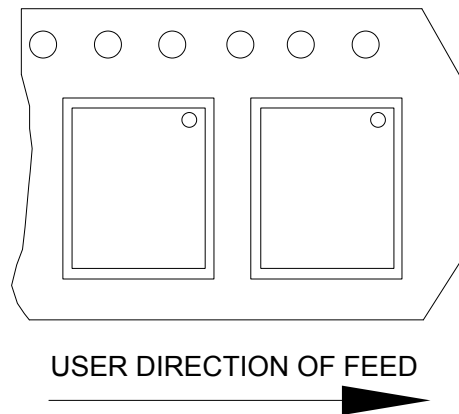
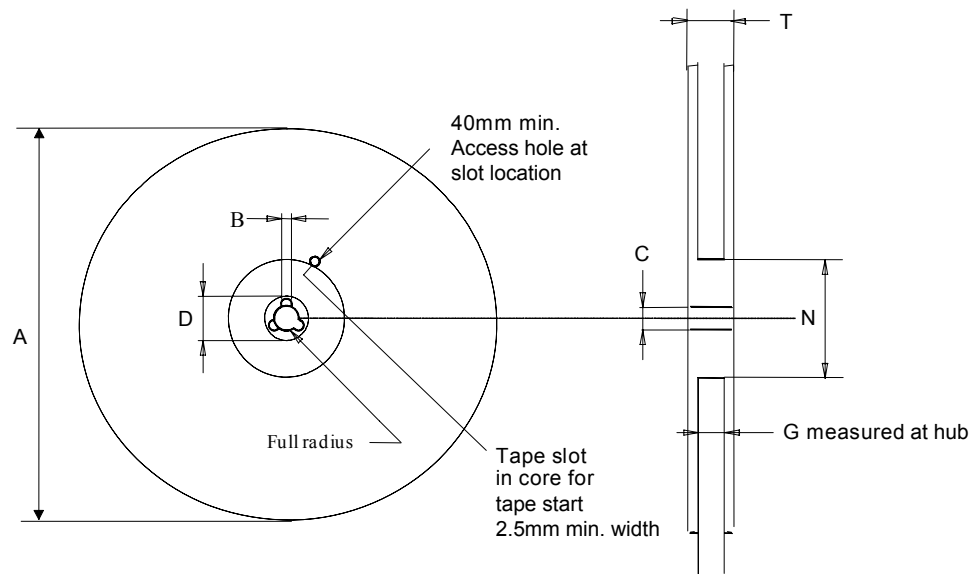


Figure 25. LGA-14 package orientation in carrier tape



**Figure 26. Reel information for carrier tape of LGA-14 package**

**Table 258. Reel dimensions for carrier tape of LGA-14 package**

Reel dimensions (mm)	
A (max)	330
B (min)	1.5
C	13 ±0.25
D (min)	20.2
N (min)	60
G	12.4 +2/-0
T (max)	18.4

## Revision history

Table 259. Document revision history

Date	Version	Changes
29-Nov-2023	1	Initial release

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