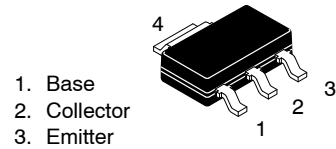


PNP Current Driver Transistor

NZT753

This device is designed for power amplifier, regulator and switching circuits where speed is important. Sourced from Process 5P.



- 1. Base
- 2. Collector
- 3. Emitter

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ABSOLUTE MAXIMUM RATINGS

($T_A = 25^\circ\text{C}$ unless otherwise noted.) (Notes 1, 2)

Symbol	Parameter	Value	Unit
V_{CEO}	Collector-Emitter Voltage	-100	V
V_{CBO}	Collector-Base Voltage	-120	V
V_{EBO}	Emitter-Base Voltage	-5.0	V
I_C	Collector Current - Continuous	-4.0	A
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- These ratings are based on a maximum junction temperature of 150°C .
- These are steady limits. The factory should be consulted on application involving pulsed or low duty cycle operations.

THERMAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$ unless otherwise noted.) (Note 3)

Symbol	Parameter	Max	Unit
P_D	Total Device Dissipation Derate above 25°C	1.2 9.7	W $\text{mW}/^\circ\text{C}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	103	$^\circ\text{C}/\text{W}$

- Device mounted on FR-4PCB $36\text{ mm} \times 18\text{ mm} \times 1.5\text{ mm}$; mounting pad for the collector lead min. 6 cm^2 .

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted.) (Note 4)

Symbol	Parameter	Test Conditions	Min	Max	Unit
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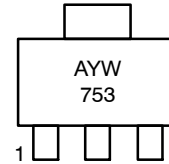
OFF CHARACTERISTICS

BV_{CEO}	Collector-Emitter Breakdown Voltage	$I_C = -10\text{ mA}, I_B = 0$	-100	-	V
BV_{CBO}	Collector-Base Breakdown Voltage	$I_C = -100\text{ }\mu\text{A}, I_E = 0$	-120	-	V
BV_{EBO}	Emitter-Base Breakdown Voltage	$I_E = -100\text{ }\mu\text{A}, I_C = 0$	-5.0	-	V
I_{CBO}	Collector-Base Cutoff Current	$V_{CB} = -100\text{ V}, I_E = 0$ $V_{CB} = -100\text{ V}, I_E = 0, T_A = 100^\circ\text{C}$	-	-0.1 -10	μA μA
I_{EBO}	Emitter-Base Cutoff Current	$V_{EB} = -4\text{ V}, I_C = 0$	-	-0.1	μA

ON CHARACTERISTICS (Note 4)

h_{FE}	DC Current Gain	$V_{CE} = -2.0\text{ V}, I_C = -50\text{ mA}$ $V_{CE} = -2.0\text{ V}, I_C = -500\text{ mA}$ $V_{CE} = -2.0\text{ V}, I_C = -1.0\text{ A}$	70 100 55	- 300 -	
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	$I_C = -1.0\text{ A}, I_B = -50\text{ mA}$		-0.3	V
$V_{BE(sat)}$	Base-Emitter Saturation Voltage	$I_C = -1.0\text{ A}, I_B = -100\text{ mA}$		-1.25	V

MARKING DIAGRAM



- A = Assembly Location
- Y = Year
- W = Work Week
- 753 = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping [†]
NZT753	SOT-223 (Pb-Free)	4,000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NZT753

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted.) (Note 4) (continued)

Symbol	Parameter	Test Conditions	Min	Max	Unit
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ON CHARACTERISTICS (Note 4)

$V_{BE(on)}$	Base-Emitter On Voltage	$V_{CE} = -2.0\text{ V}, I_C = -1.0\text{ A}$	-	-1.0	V
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SMALL SIGNAL CHARACTERISTICS

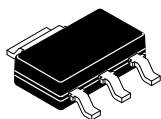
f_T	Transition Frequency	$V_{CE} = -5\text{ V}, I_C = -100\text{ mA}, f = 100\text{ MHz}$	75	-	MHz
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Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

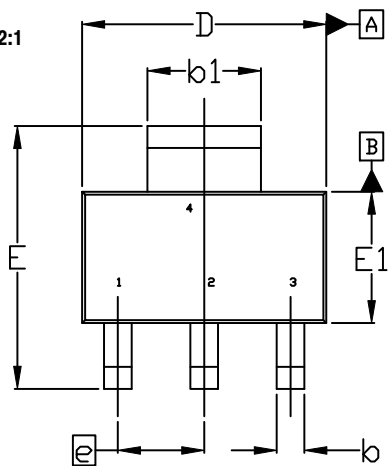
ON Semiconductor®



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ISSUE B

DATE 13 MAY 2020

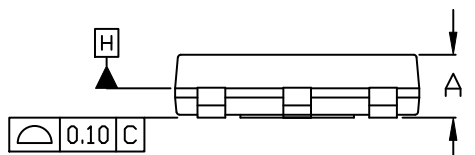
SCALE 2:1



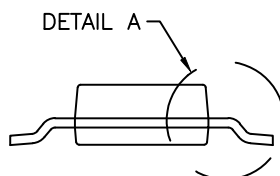
TOP VIEW

$\Phi 0.10 \text{ (M)}$ C A B

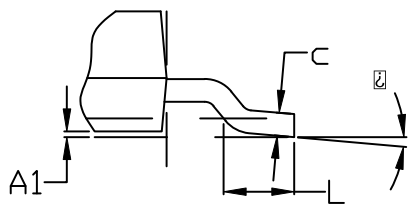
NOTE 7



SIDE VIEW



END VIEW

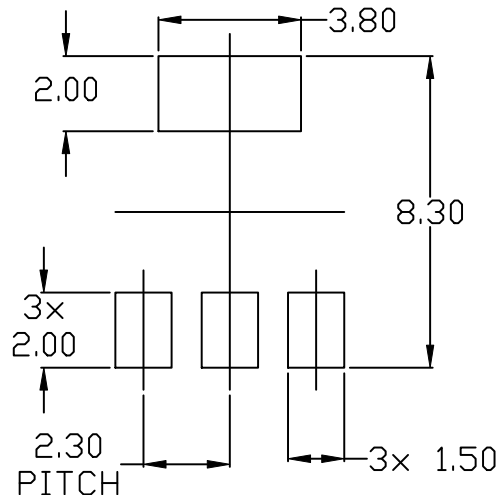


DETAIL A

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E1 ARE DETERMINED AT DATUM H. DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. SHALL NOT EXCEED 0.23mm PER SIDE.
4. LEAD DIMENSIONS b AND b1 DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS 0.08mm PER SIDE.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

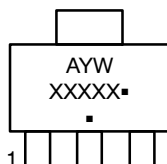
DIM	MILLIMETERS		
	MIN.	NDM.	MAX.
A	---	---	1.80
A1	0.02	0.06	0.11
b	0.60	0.74	0.88
b1	2.90	3.00	3.10
c	0.24	---	0.35
D	6.30	6.50	6.70
E	6.70	7.00	7.30
E1	3.30	3.50	3.70
e	2.30 BSC		
L	0.25	---	---
\square	0°	---	10°



RECOMMENDED MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

GENERIC MARKING DIAGRAM*



- A = Assembly Location
- Y = Year
- W = Work Week
- XXXXX = Specific Device Code
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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