# TPD1E10B09-Q1 Automotive 1-Channel ESD in 0402 Package With 10-pF Capacitance and 9-V Breakdown

## 1 Features

- AEC-Q101 qualified
- IEC 61000-4-2 level 4 ESD protection
  - ±20-kV Contact Discharge
  - ±20-kV Air-Gap Discharge
- ISO 10605 (330 pF, 330 Ω) ESD protection
  - ±8-kV Contact Discharge
  - ±15-kV Air-Gap Discharge
- IEC 61000-4-5 surge protection
  - 4.5 A (8/20 µs)
- I/O capacitance 10 pF (typical)
- $R_{DYN}$: 0.5 Ω (typical)
- DC breakdown voltage ±9.5 V (minimum)
- Ultra low leakage current 100 nA (maximum)
- 13-V clamping voltage (typical at $I_{PP}$ = 1 A)
- Industrial temperature range: –40°C to +125°C
- Space-saving 0402 footprint

## 2 Applications

- End equipment:
  - Head unit
  - Premium audio
  - External amplifier
  - Body control module
  - Gateway
  - Telematics
  - Camera module
- Interfaces:
  - Audio lines
  - Push-buttons
  - Memory interface
  - GPIO

## 3 Description

The TPD1E10B09-Q1 device is a bidirectional electrostatic discharge (ESD) transient voltage suppression (TVS) diode in a small 0402 industry standard package. This TVS protection diode is convenient for component placement in space-saving applications and features low $R_{DYN}$ and high IEC rating. The TPD1E10B09-Q1 is rated to dissipate ESD strikes above the maximum level specified in the IEC 61000-4-2 international standard (Level 4) offering ±20-kV contact discharge and ±20-kV IEC air-gap protection. ESD voltages can easily reach 5-kV and during extreme conditions these voltages can be significantly higher, causing damages to many integrated circuits. For example, in a low humidity environment voltages can exceed 20-kV.

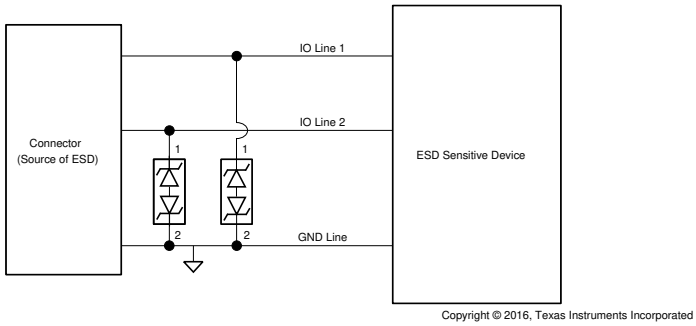
The low dynamic resistance (0.5 Ω) and low clamping voltage (13 V at 1-A IPP) allows for system level protection against transient events, providing robust protection on designs that are exposed to ESD events. This device also features a 10-pF IO capacitance making it an excellent choice for audio lines, push buttons, memory interfaces, or GPIOs.

This device is also available without automotive qualification: TPD1E10B09.

**Package Information**

| PART NUMBER | PACKAGE(1) | PACKAGE SIZE(2) |
|---|---|---|
| TPD1E10B09-Q1 | DPY (X1SON, 2) | 1 mm × 0.6 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

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**Application Schematic**

## Table of Contents



## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision A (September 2016) to Revision B (September 2023) | Page |
|---|---|
| • Changed the format of the *Package Information* table to include package lead size | 1 |
| • Changed the numbering format for tables, figures, and cross-references throughout the document | 1 |

| Changes from Revision * (August 2016) to Revision A (September 2016) | Page |
|---|---|
| • Changed device status from *Product Preview* to *Production Data* | 1 |


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# 5 Pin Configuration and Functions

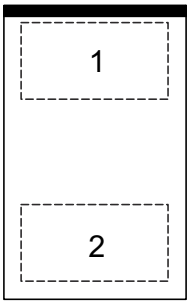


**Figure 5-1. DPY Package, 2-Pin X1SON (Top View)**

**Table 5-1. Pin Functions**

| PIN | | TYPE(1) | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 1 | IO | I/O | ESD protected I/O |
| 2 | GND | Ground | Ground. Connect to ground |

(1) I = input, O = output, GND = ground

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# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $I_{PP}$ | Peak pulse current (tp = 8/20 µs, positive) | | 5.5 | A |
| $I_{PP}$ | Peak pulse current (tp = 8/20 µs, negative) | | 4.5 | A |
| $P_{PP}$ | Peak pulse power (tp = 8/20 µs) | | 90 | W |
| P | Power Dissipation(2) | | 162 | mW |
| | Operating temperature | –40 | 125 | °C |
| $T_{stg}$ | Storage temperature | –65 | 155 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Max junction temperature: 125°C; power dissipation calculated at 25°C ambient temperature using JEDEC High K board Standard. Not to be used for steady state power dissipation in the breakdown region.

## 6.2 ESD Ratings—AEC Specification

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per AEC Q100-002(1) | ±2500 | V |
| | | Charged-device model (CDM), per AEC Q100-011 | ±1000 | |

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 6.3 ESD Ratings—IEC Specification

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | IEC 61000-4-2 Contact Discharge | ±20000 | V |
| | | IEC 61000-4-2 Air-Gap Discharge | ±20000 | |

## 6.4 ESD Ratings—ISO Specification

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | ISO 10605 (330 pF, 330 Ω) Contact Discharge | ±8000 | V |
| | | ISO 10605 (330 pF, 330 Ω) Air-Gap Discharge | ±15000 | |

## 6.5 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $T_A$ | Operating free-air temperature | | –40 | 125 | °C |
| | Operating voltage | Pin 1 to 2 or pin 2 to 1 | –9 | 9 | V |


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## 6.6 Thermal Information

| THERMAL METRIC[1] | | TPD1E10B09-Q1 DPY (X1SON) 2 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 615.5 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 404.8 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 493.3 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 127.7 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 493.3 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 6.7 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{RWM}$ | Reverse stand-off voltage | Pin 1 to 2 or pin 2 to 1 | | | 9 | V |
| $I_{LEAK}$ | Leakage current | Pin 1 = 5 V, pin 2 = 0 V | | | 100 | nA |
| VClamp1,2 | Clamp voltage with ESD strike on pin 1, pin 2 grounded | $I_{PP}$ = 1 A, tp = 8/20 µs[2] | | 13 | | V |
| | | $I_{PP}$ = 5 A, tp = 8/20 µs[2] | | 17 | | |
| VClamp2,1 | Clamp voltage with ESD strike on pin 2, pin 1 grounded | $I_{PP}$ = 1 A, tp = 8/20 µs[2] | | 13 | | V |
| | | $I_{PP}$ = 4.5 A, tp = 8/20 µs[2] | | 20 | | |
| $R_{DYN}$ | Dynamic resistance | Pin 1 to pin 2[1] | | 0.5 | | Ω |
| | | Pin 2 to pin 1[1] | | 0.5 | | |
| $C_{IO}$ | I/O capacitance | $V_{IO}$ = 2.5 V; *f* = 1 MHz | | 10 | | pF |
| $V_{BR1,2}$ | Break-down voltage, pin 1 to pin 2 | $I_{IO}$ = 1 mA | 9.5 | | | V |
| $V_{BR2,1}$ | Break-down voltage, pin 2 to pin 1 | $I_{IO}$ = 1 mA | 9.5 | | | V |

(1) Extraction of $R_{DYN}$ using least squares fit of TLP characteristics from $I_{PP}$ = 10 A to $I_{PP}$ = 20 A.
(2) Non-repetitive current pulse 8/20 µs exponentially decaying waveform according to IEC 61000-4-5.

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## 6.8 Typical Characteristics

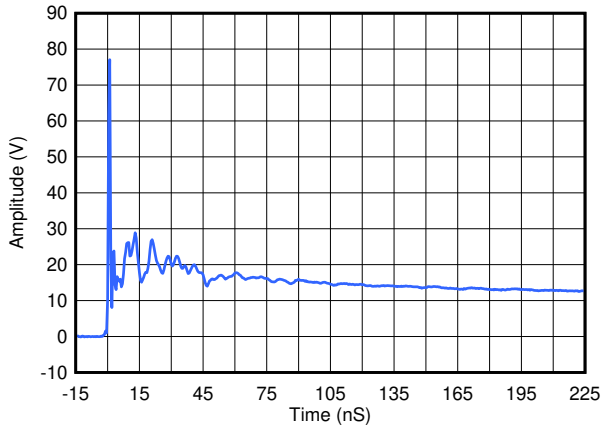


**Figure 6-1. ESD Clamp Voltage 8-kV Contact ESD**

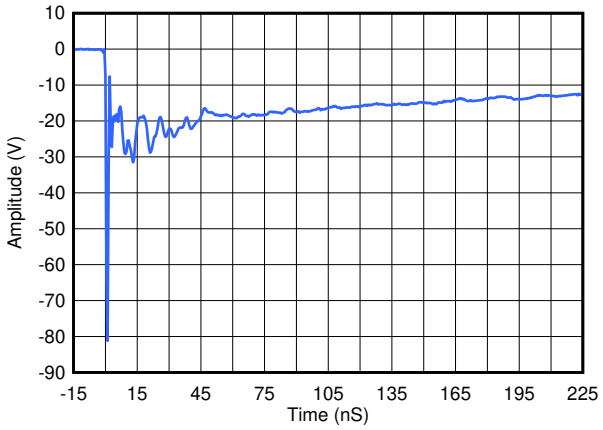


**Figure 6-2. ESD Clamp Voltage –8-kV Contact ESD**

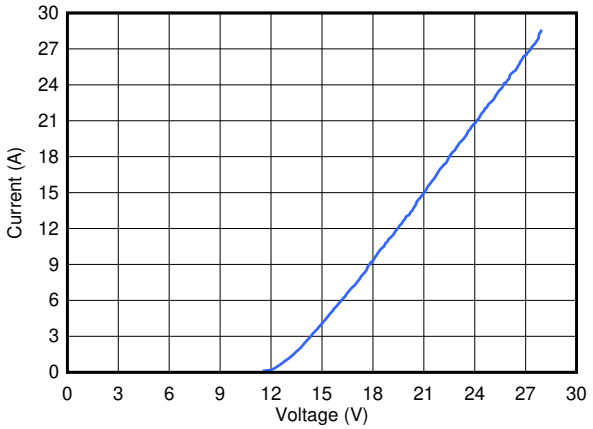


**Figure 6-3. Transmission Line Pulse (TLP) Waveform Pin 1 to Pin 2**

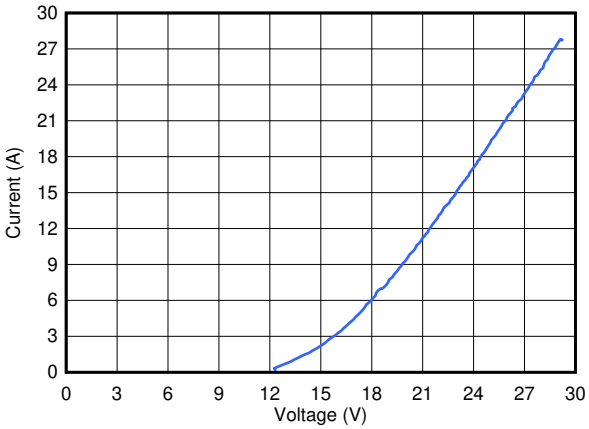


**Figure 6-4. Transmission Line Pulse (TLP) Waveform Pin 2 to Pin 1**

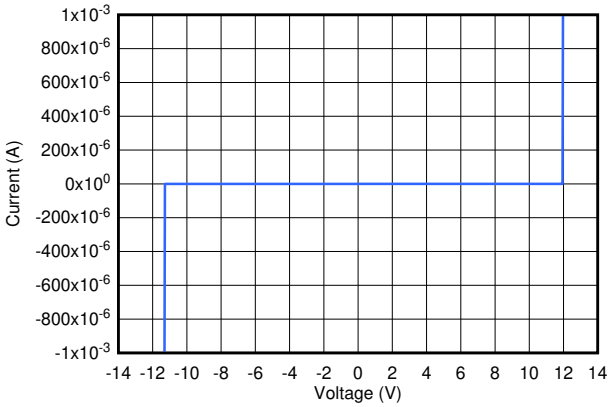


**Figure 6-5. IV Curve**

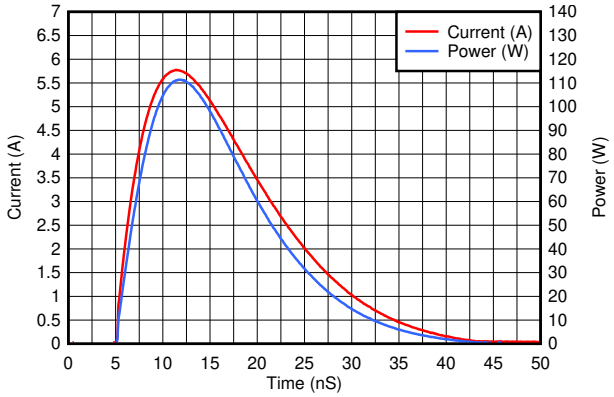


**Figure 6-6. Positive Surge Waveform 8/20 µs**


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## 6.8 Typical Characteristics (continued)

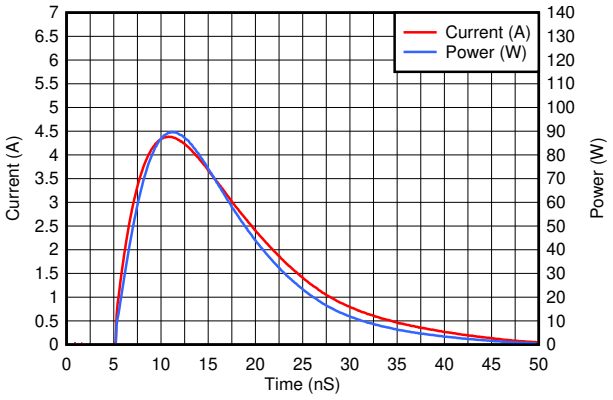



**Figure 6-7. Negative Surge Waveform 8/20 µs**

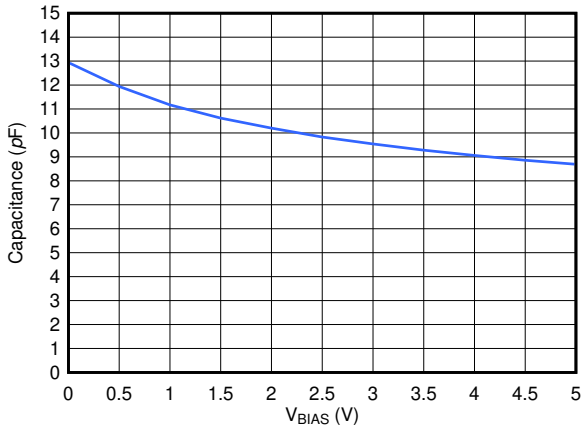



**Figure 6-8. Pin Capacitance Across $V_{BIAS}$**

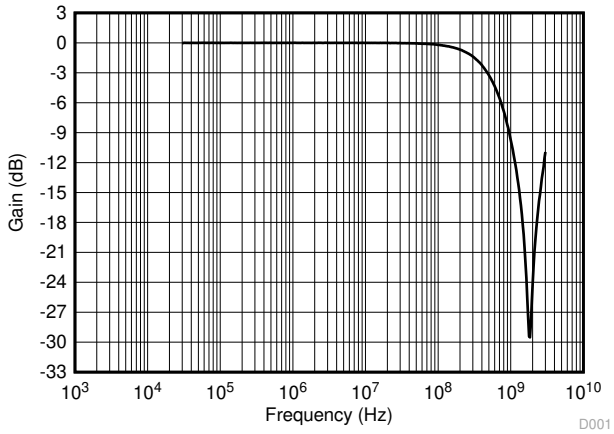


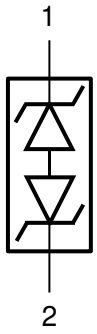

**Figure 6-9. Insertion Loss**

# 7 Detailed Description

## 7.1 Overview

The TPD1E10B09-Q1 is a single-channel ESD TVS that provides ±20-kV IEC 61000-4-2 (Level 4) contact and air-gap ESD protection. The 10-pF back-to-back diode architecture is suitable for signals that range from –9 V to 9 V and supports data rates up to 500 Mbps. The industry-standard 0402 package is convenient for placement in applications with limited space.

## 7.2 Functional Block Diagram

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## 7.3 Feature Description

The TPD1E10B09-Q1 is a bidirectional TVS with high ESD protection level. This device protects circuit from ESD strikes up to ±20-kV contact and ±20-kV air-gap specified in the IEC 61000-4-2 level 4 international standard. The device can also handle up to 4.5-A surge current (IEC 61000-4-5 8/20 µs). The I/O capacitance of 10 pF supports a data rate up to 500 Mbps. This clamping device has a small dynamic resistance of 0.5 Ω typically. This makes the clamping voltage low when the device is actively protecting other circuits. For example, the clamping voltage is only 13 V when the device is taking 1-A transient current. The breakdown is bidirectional so that this protection device is a good fit for GPIO, especially audio lines which carry bidirectional signals. Low leakage allows the diode to conserve power when working below the $V_{RWM}$. The industrial temperature range of –40°C to +125°C makes this ESD device work at extensive temperatures in most environments. The space-saving 0402 package can fit into small electronic devices like mobile equipment and wearables.

### 7.3.1 AEC-Q101 Qualified

This device is qualified to AEC-Q101 standards and is qualified to operate from –40°C to +125°C.

### 7.3.2 IEC 61000-4-2 ESD Protection

The I/O pins can withstand ESD events up to ±20-kV contact and ±20-kV air according to the IEC 61000-4-2 standard. An ESD-surge clamp diverts the current to ground.

### 7.3.3 ISO 10605 ESD Protection

The I/O pins can withstand ESD events at least ±8-kV contact and ±15-kV air according to the ISO 10605 (330 pF, 330 Ω) standard. An ESD-surge clamp diverts the current to ground.

### 7.3.4 IEC 61000-4-5 Surge Protection

The IO pins can withstand surge events up to 5.5 A positive and 4.5 A negative (8/20 µs waveform). An ESD-surge clamp diverts this current to ground.

### 7.3.5 IO Capacitance

The capacitance between the I/O pins 10 pF. This capacitance support data rates up to 500 Mbps.


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### 7.3.6 Dynamic Resistance

The IO pins feature an ESD clamp that has a low $R_{DYN}$ of 0.50 Ω which prevents system damage during ESD events.

### 7.3.7 DC Breakdown Voltage

The DC breakdown voltage between the IO pins is a minimum of 9.5 V, which protects sensitive equipment from surges above the reverse standoff voltage of 9 V.

### 7.3.8 Ultra Low Leakage Current

The IO pins feature an ultra-low leakage current of 100 nA (maximum) with a bias of 5 V.

### 7.3.9 Clamping Voltage

The IO pins feature an ESD clamp that is capable of clamping the voltage to 13 V ($I_{PP}$ = 1 A) and 17 V ($I_{PP}$ = 5 A).

### 7.3.10 Industrial Temperature Range

This device features an industrial operating range of –40°C to +125°C.

### 7.3.11 Space-Saving Footprint

This device features a space-saving, industry standard 0402 footprint.

## 7.4 Device Functional Modes

The TPD1E10B09-Q1 is a passive clamp that has low leakage during normal operation when the voltage between pin 1 and pin 2 is below $V_{RWM}$ and activates when the voltage between pin 1 and pin 2 goes above $V_{BR}$. During IEC ESD events, transient voltages as high as ±20 kV can be clamped between the two pins. When the voltages on the protected lines fall below the trigger voltage, the device reverts back to the low leakage passive state.

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# 8 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 8.1 Application Information

The TPD1E10B09-Q1 is a single-channel back-to-back diode that protects one bidirectional signal line from electrostatic discharge and surge pulses. Because the diode is bidirectional, the TPD1E10B09-Q1 protects signals that have positive or negative polarity. During normal operation, the diode behaves as a 10-pF capacitance to ground. Board layout is critical for optimal performance of any diode.

Placement: The diode must be placed very close to the external connector for optimal performance. Ideally, the diode must be placed on the line that it is protecting.

Layout: Pin 1 of the diode must be right over the protected signal line. There must a thick and short trace from pin 2 to ground. An example is shown in the *Layout* section.

## 8.2 Typical Application

A system with a human interface is vulnerable to large system-level ESD strikes that standard ICs cannot survive. TVS ESD protection diodes are typically used to suppress ESD at these connectors. The TPD1E10B09-Q1 is a single-channel ESD protection device containing back-to-back TVS diodes, which is typically used to provide a path to ground for dissipating ESD events on bidirectional signal lines between a human interface connector and a system. As the current from ESD passes through the device, only a small voltage drop is present across the diode structure. This is the voltage presented to the protected IC. The low $R_{DYN}$ of the triggered TVS holds this voltage, $V_{CLAMP}$, to a tolerable level to the protected IC.

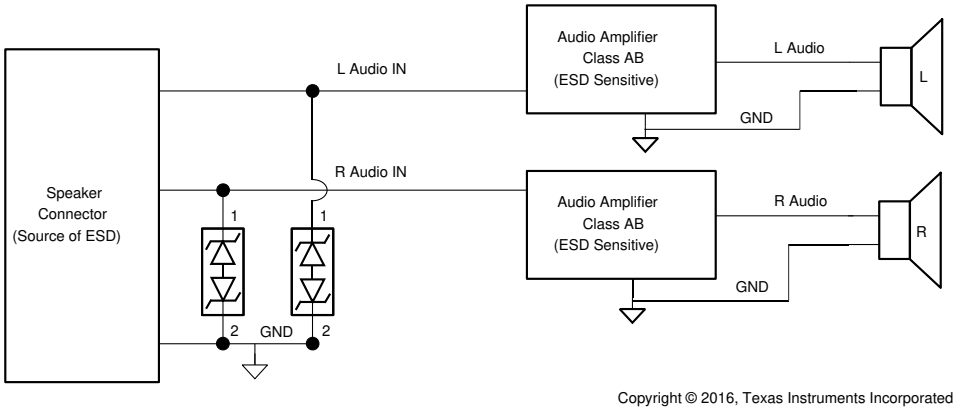

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**Figure 8-1. Typical Application Schematic**


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### 8.2.1 Design Requirements

For this design example, two TPD1E10B09-Q1s are used to protect left and right audio channels. Table 8-1 lists the known system parameters for this audio application.

**Table 8-1. Design Parameters**

| DESIGN PARAMETER | VALUE |
|---|---|
| Audio amplifier class | AB |
| Audio signal voltage range | –8 V to 8 V |
| Audio frequency content | 20 Hz to 20 kHz |
| Required IEC 61000-4-2 ESD protection | ±15-kV Contact, ±15-kV Air-Gap |

### 8.2.2 Detailed Design Procedure

To begin the design process, some parameters must be decided upon; the designer must make sure:

- The voltage range on the protected line does not exceed the reverse standoff voltage of the TVS diode(s) ($V_{RWM}$).
- The operating frequency is supported by the I/O capacitance, $C_{IO}$, of the TVS diode.
- The IEC 61000-4-2 protection requirement is covered by the IEC performance of the TVS diode.

For this application, the audio signal voltage range is –8 V to 8 V. The $V_{RWM}$ for the TVS is –9.5 V to 9.5 V; therefore, the bidirectional TVS does not break down during normal operation, and normal operation of the audio signal is not affected due to the signal voltage range. In this application, a bidirectional TVS like the TPD1E10B09-Q1 is required.

Next, consider the frequency content of this audio signal. In this application with the class AB amplifier, the frequency content is from 20 Hz to 20 kHz; ensure that the TVS I/O capacitance does not distort this signal by filtering it. With the TPD1E10B09-Q1 typical capacitance of 10 pF, which leads to a typical cutoff frequency of just under 500 MHz, this diode has sufficient bandwidth to pass the audio signal without distorting it.

Finally, the human interface in this application requires protection for ±15-kV Contact and ±15-kV Air-Gap ESD, which is above the standard Level 4 IEC 61000-4-2 system-level ESD protection. A standard TVS cannot survive this level of IEC ESD stress. However, the TPD1E10B09-Q1 can survive at least ±20-kV Contact and ±20-kV Air-Gap ESD. Therefore, the device can provide sufficient ESD protection for the interface, even though the requirements are stringent. For any TVS diode to provide its full range of ESD protection capabilities, as well as to minimize the noise and EMI disturbances the board will see during ESD events, it is crucial that a system designer uses proper board layout of their TVS ESD protection diodes. See the *Layout* section for instructions on properly laying out the TPD1E10B09-Q1.

### 8.2.3 Application Curves

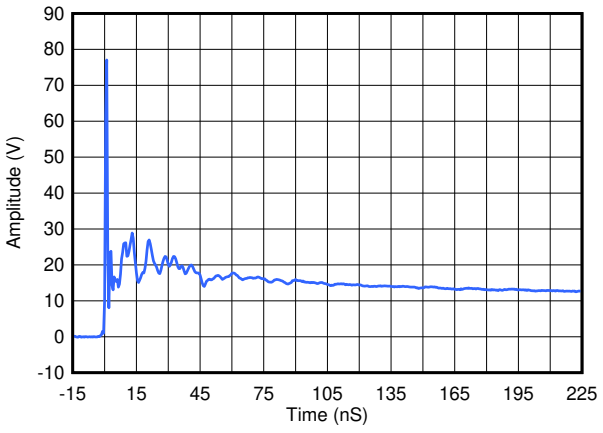


**Figure 8-2. ESD Clamp Voltage 8-kV Contact ESD**

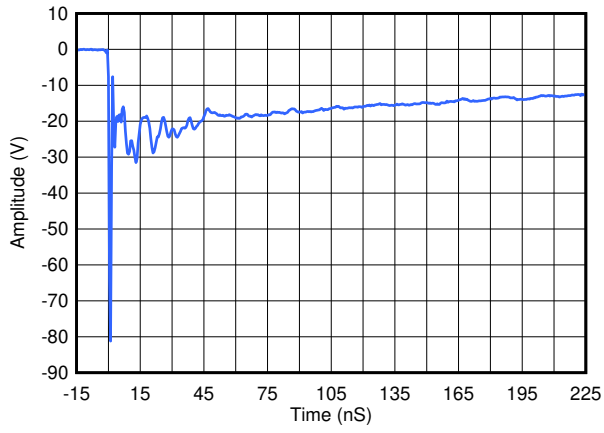


**Figure 8-3. ESD Clamp Voltage –8-kV Contact ESD**

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## 8.3 Power Supply Recommendations

This device is a passive TVS diode-based ESD protection device, so there is no need to power it. Do not violate the maximum specifications for each pin.

## 8.4 Layout

### 8.4.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Use rounded corners with the largest radii possible on the protected traces between the TVS and the connector, thus eliminating any sharp corners.
  - Electric fields tend to build up on corners, increasing EMI coupling.
- If pin 1 or pin 2 is connected to ground, use a thick and short trace for this return path.

### 8.4.2 Layout Example

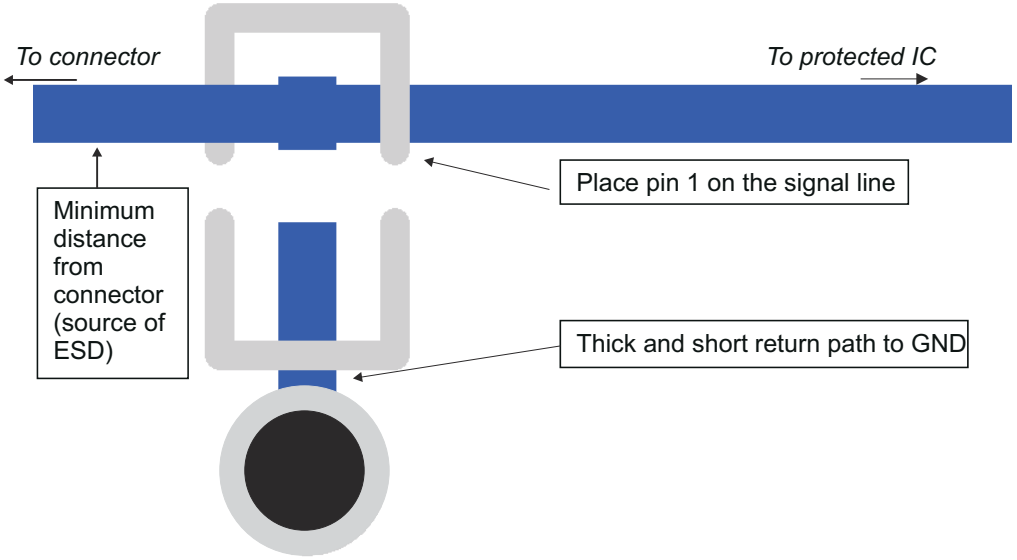


**Figure 8-4. Layout Example**


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# 9 Device and Documentation Support

## 9.1 Documentation Support

### 9.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TPD1E10B09-Q1 Evaluation Module*
- Texas Instruments, *Reading and Understanding an ESD Protection Data Sheet*
- Texas Instruments, *ESD Layout Guide*
- Texas Instruments, *ESD PROTECTION DIODES EVM*

## 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

## 9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 9.6 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

# 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPD1E10B09QDPYRQ1 | ACTIVE | X1SON | DPY | 2 | 10000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 4N | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF TPD1E10B09-Q1 :**

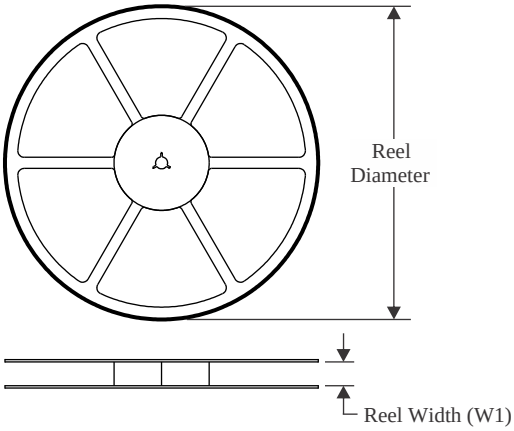
- Catalog : TPD1E10B09

NOTE: Qualified Version Definitions:

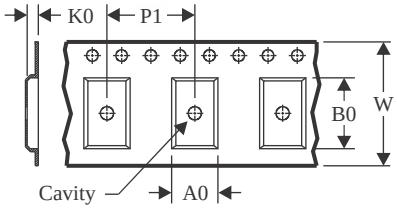
- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

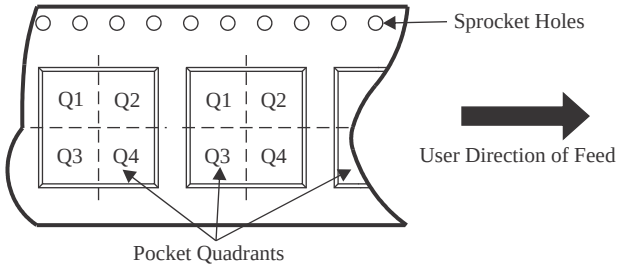



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

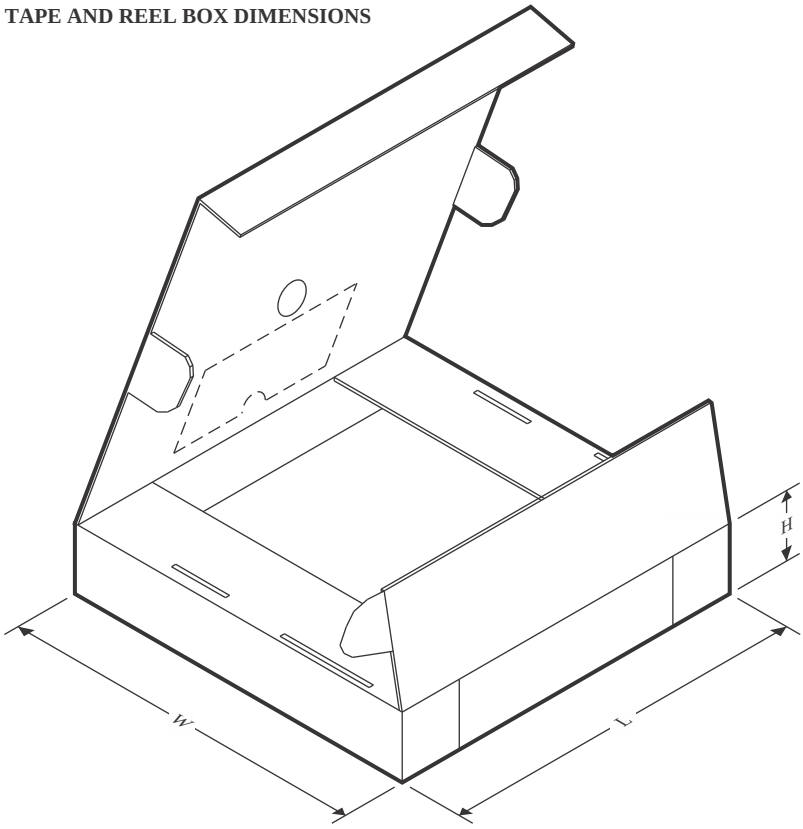
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPD1E10B09QDPYRQ1 | X1SON | DPY | 2 | 10000 | 180.0 | 9.5 | 0.73 | 1.13 | 0.5 | 2.0 | 8.0 | Q1 |

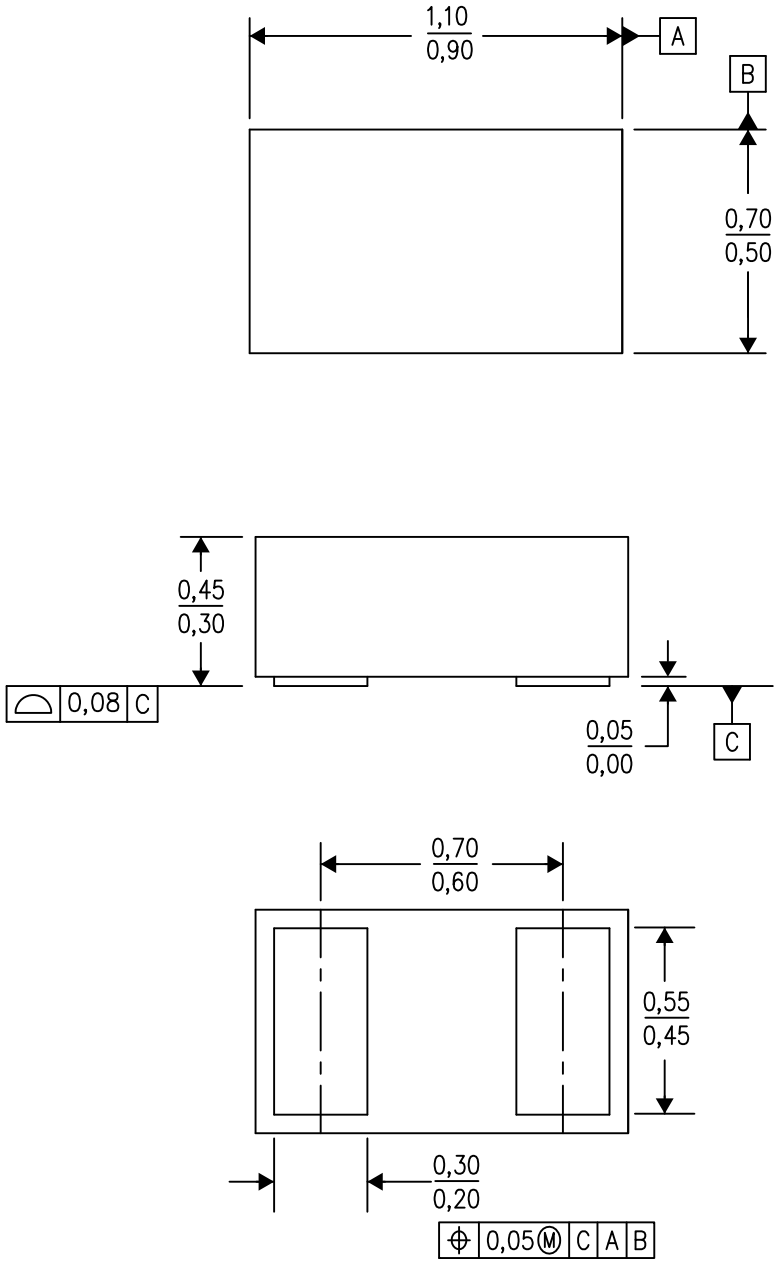
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPD1E10B09QDPYRQ1 | X1SON | DPY | 2 | 10000 | 189.0 | 185.0 | 36.0 |

DPY (R–PX1SON–N2) PLASTIC SMALL OUTLINE NO–LEAD




4211012/D 08/14

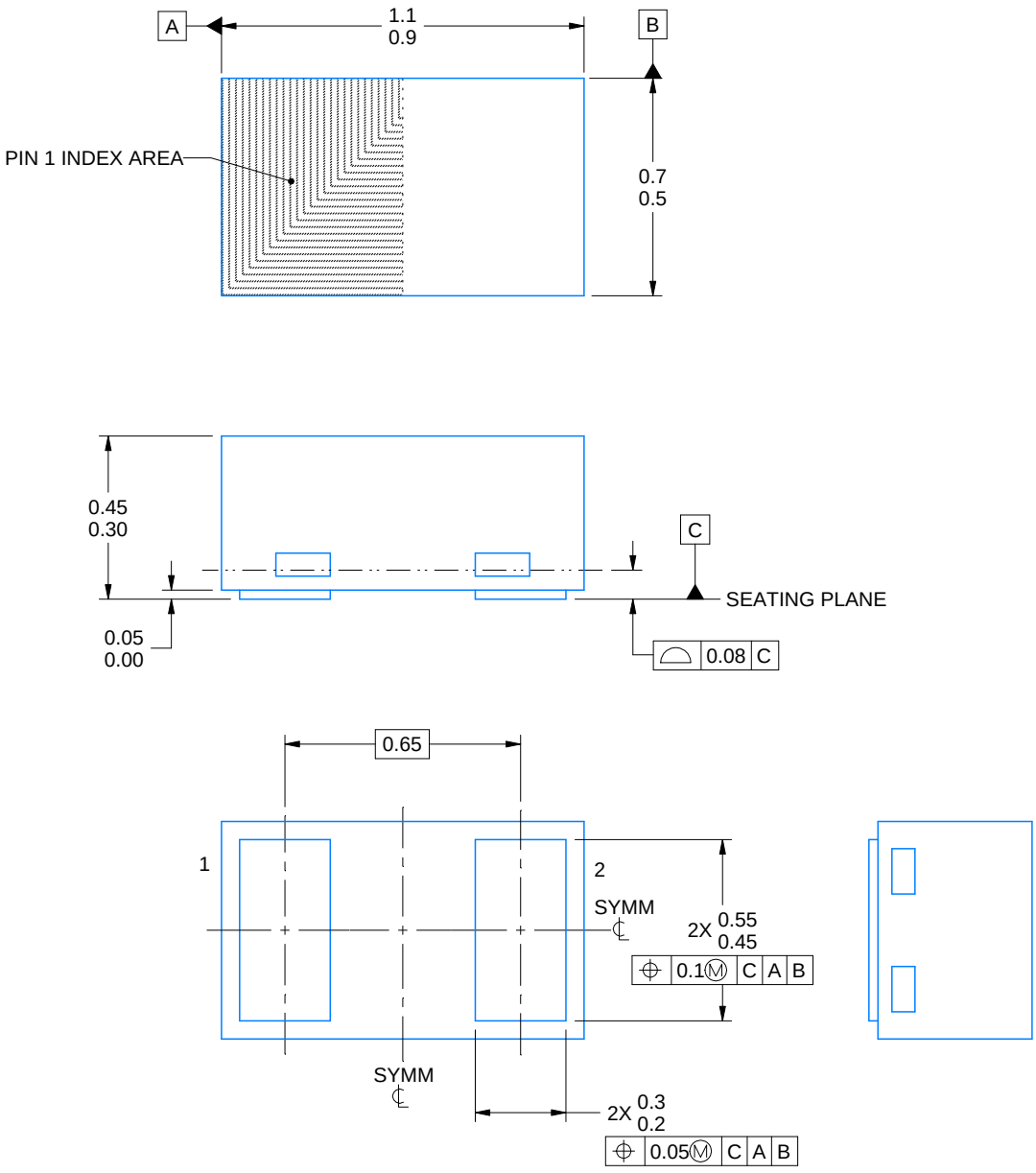
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.

# PACKAGE OUTLINE

## DPY0002A

## X1SON - 0.45 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

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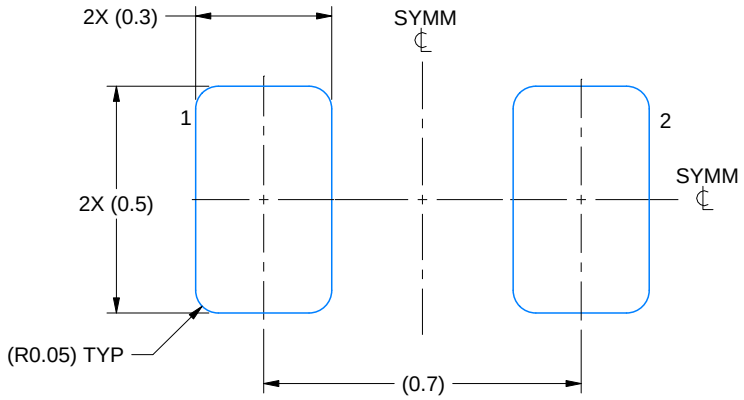
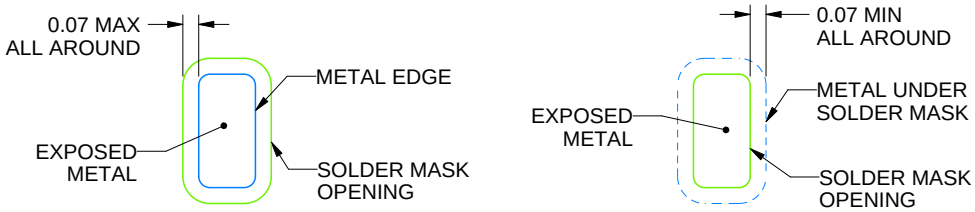
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M
2. This drawing is subject to change without notice.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:60X




SOLDER MASK DETAILS

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NOTES: (continued)

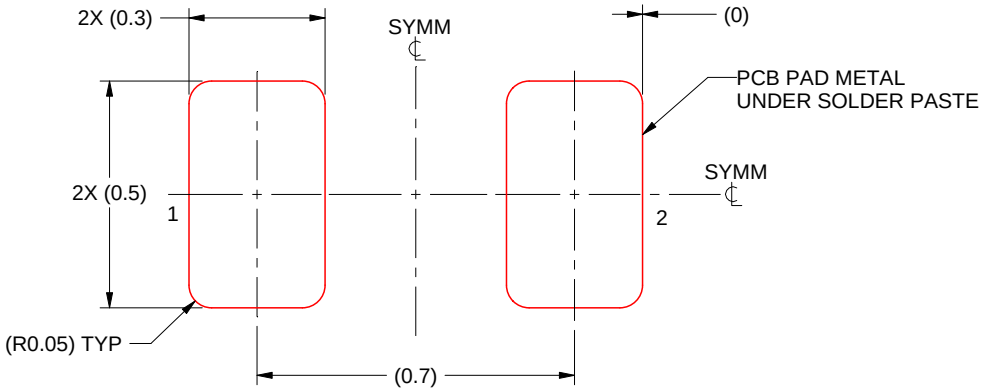
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

## DPY0002A

## X1SON - 0.45 mm max height

PLASTIC SMALL OUTLINE - NO LEAD




SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:60X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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