TPD4S009 4-Channel ESD Solution for High-Speed Differential Interface

1 Features

- IEC 61000-4-2 Level 4 ESD Protection
  - ±8-kV Contact Discharge
- IEC 61000-4-5 Surge Protection
  - 2.5A (8/20µs)
- I/O Capacitance: 0.8 pF (Typical)
- Low Leakage Current: 10 nA (Typical)
- Supports High-Speed Differential Data Rates (3-dB Bandwidth > 4 GHz)
- Ultra-low Matching Capacitance Between Differential Signal Pairs
- I_{off} Feature for the TPD4S009
- Industrial Temperature Range: –40°C to 85°C
- Easy Straight through Routing, Space-Saving Package Options

2 Applications

- End Equipment
  - Set-Top Boxes
  - DTVs
  - Laptop/Desktop
  - Electronic Point of Sale (EPOS)
- Interfaces
  - USB 2.0
  - HDMI 1.4
  - LVDS
  - SATA
  - Ethernet
  - FireWire

3 Description

The TPD4S009 and TPD4S010 are four-channel TVS diode arrays for electrostatic discharge (ESD) protection. TPD4S009 and TPD4S010 are rated to dissipate contact ESD strikes at the maximum level specified in the IEC 61000-4-2 international standard (Level 4), with ±8-kV contact discharge ESD protection. The low capacitance (0.8-pF) of these devices, coupled with the excellent matching between differential signal pairs (0.05-pF line-line capacitance for the TPD4S009DRY) enables this device to provide transient voltage suppression circuit protection for high-speed differential data rates (3-dB bandwidth > 4 GHz).

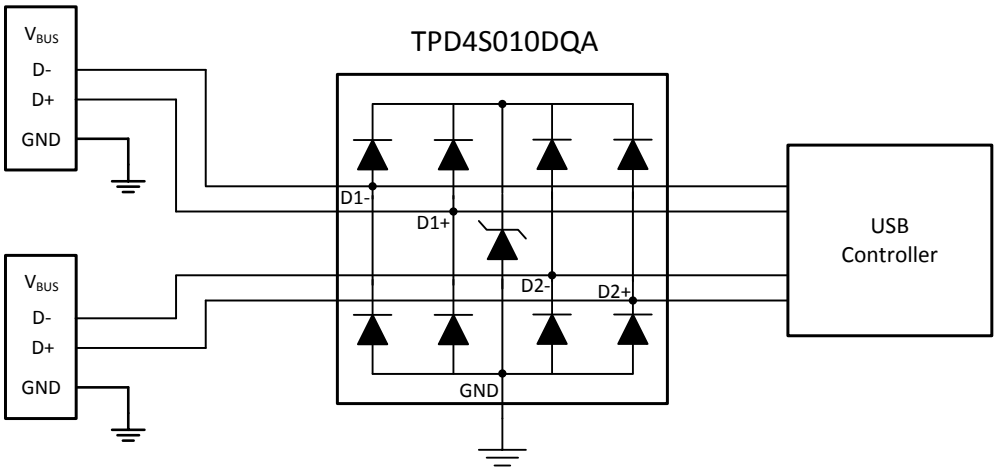
The TPD4S009 is offered in DBV, DCK, DGS, and DRY packages. The TPD4S009DRYR is the most space saving package option available for dual pair high-speed differential lines. The TPD4S010 is offered in the industry standard DQA package. The TPD4S009DGSR and TPD4S010DQAR offer flow-through board layout options to reduce signal glitches normally caused by routing mismatches between the D+ and D- signal pair. See also TPD4E05U06DQAR which is P2P compatible with TPD4S010DQAR. This device offers higher IEC ESD protection, lower capacitance, lower R_{DYN}, lower DC breakdown voltage, and lower clamping voltage.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPD4S009	SOT (6)	2.90 mm × 1.60 mm
		2.00 mm × 1.25 mm
	VSSOP (10)	3.00 mm × 3.00 mm
	USON (6)	1.45 mm × 1.00 mm
TPD4S010	USON (10)	2.50 mm × 1.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (August 2013) to Revision G — **Page**

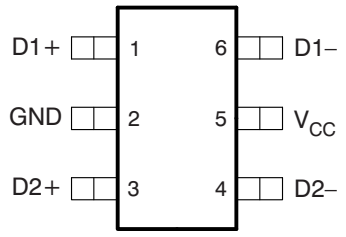
- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision E (December 2011) to Revision F — **Page**

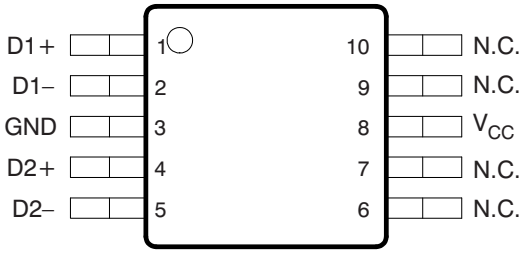
- Removed Ordering Information table. ... 5

5 Pin Configuration and Functions

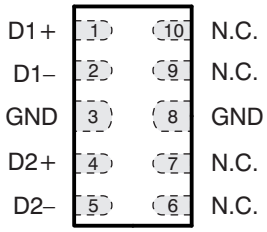
TPD4S009 DBV OR DCK PACKAGE
6-PIN SOT
TOP VIEW



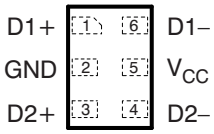
TPD4S009 DGS PACKAGE
10-PIN VSSOP
TOP VIEW



TPD4S010 DQA PACKAGE
10-PIN USON
TOP VIEW



TPD4S009 DRY PACKAGE
6-PIN USON
TOP VIEW



Pin Functions

PIN				I/O	DESCRIPTION
NAME	SOT or USON	VSSOP	USON		
D1+	1	1	1	ESD port	High-speed ESD clamp provides ESD protection to the high-speed differential data lines.
D1–	6	2	2		
D2+	3	4	4		
D2–	4	5	5		

Pin Functions (continued)

PIN				I/O	DESCRIPTION
NAME	SOT or USON	VSSOP	USON		
GND	2	3	3, 8	GND	Ground
N.C.	–	6, 7, 9, 10	6, 7, 9, 10	–	Not internally connected
V_{CC}	5	8	–	Power	Supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range for TPD4S009	–0.3	6	V
V_{IO}	IO signal voltage range	0	V_{CC}	V
T_A	Characterized free-air operating temperature range	–40	85	°C
	Lead temperature, 1.6 mm (1/16 in) from case for 10 s)		260	°C
	Peak pulse power (t_p = 8/20 µs)		25	W
	Peak pulse current (t_p = 8/20 µs)		2.5	A
T_{stg}	Storage temperature range	–65	125	°C

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1500	
		IEC 61000-4-2 Contact Discharge	±8000	
		IEC 61000-4-2 Air-Gap Discharge	±9000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
T_A Operating free-air Temperature Range		-40		85	°C
Operating Voltage	V_{CC} Pin	0.9		5.5	V
	IOx Pin (TPD4S009)	0		V_{CC}	
	IOx Pin (TPD4S010)	0		5.5	

6.4 Thermal Information

THERMAL METRIC[1]		TPD4S009				TPD4S010	UNIT
		DBV (SOT)	DCK (SOT)	DGS (VSSOP)	DRY (USON)	DQA (USON)	
		6 PINS	6 PINS	10 PINS	6 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	201.7	254.4	205.0	380.55	265.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	175.0	123.9	76.1	229.07	129.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	47.6	94.0	126.0	235.57	189.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	52.8	14.5	9.4	56.76	31.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	47.1	92.3	124.3	232.80	189.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	91.03	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{RWM}	Reverse standoff voltage	Any IO pin to ground				5.5	V
V_{BR}	Breakdown voltage	I_{IO} = 1 mA	Any IO pin to ground	9			V
I_{IO}	IO port current	V_{IO} = 3.3 V, V_{CC} = 5 V	Any IO pin		0.01	0.1	µA
I_{off}	Current from IO port to supply pins	V_{IO} = 3.3 V, V_{CC} = 5 V	Any IO pin		0.01	0.1	µA
V_D	Diode forward voltage	I_{IO} = 8 mA	Lower clamp diode	0.6	0.8	0.95	V
R_{DYN}	Dynamic resistance	I = 1 A	Any IO pin		1.1		Ω
C_{IO}	IO capacitance	V_{CC} = 5 V, V_{IO} = 2.5 V	Any IO pin		0.8		pF
I_{CC}	Operating supply current	V_{IO} = Open, V_{CC} = 5 V	V_{CC} pin		0.1	1	µA

6.6 Typical Characteristics

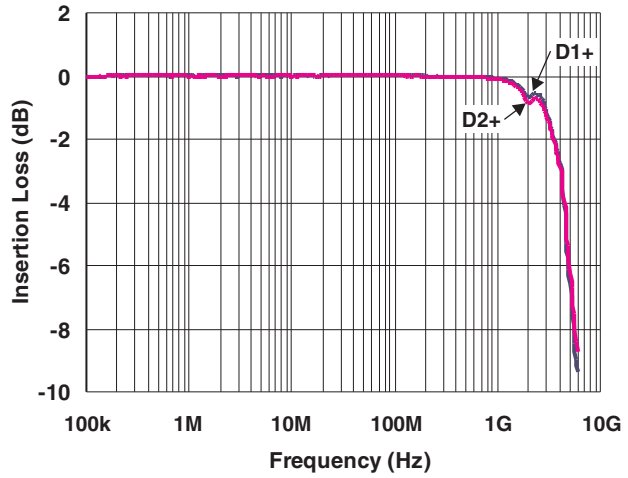
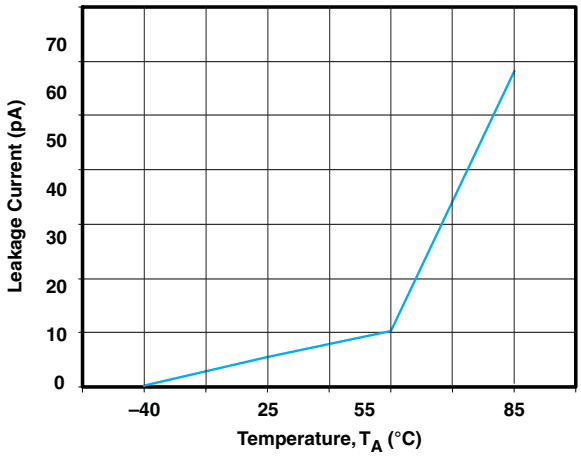
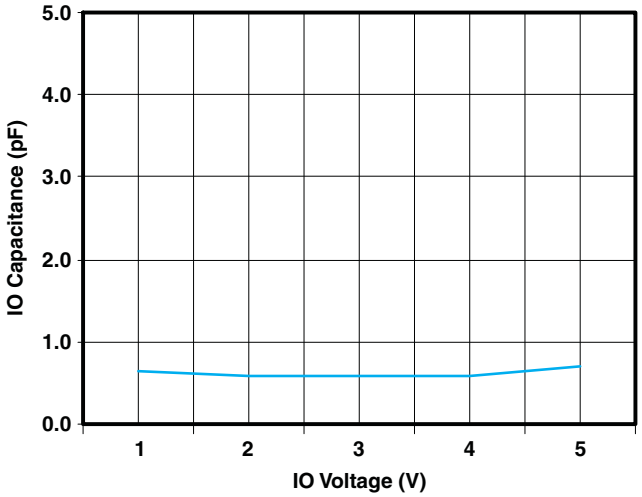


Figure 1. Insertion Loss S21 – I/O to GND



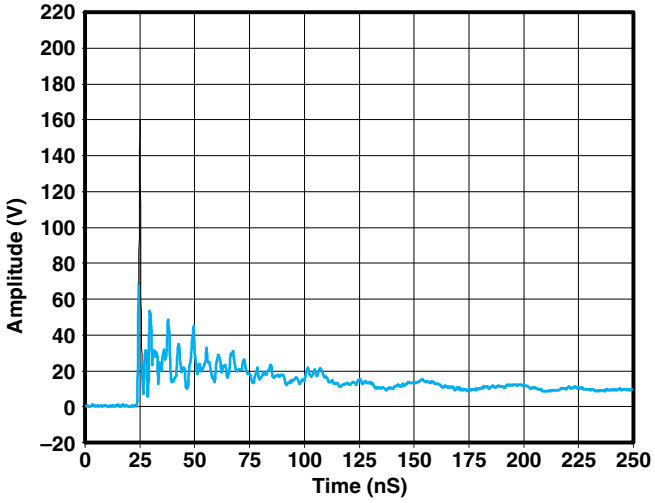
V_{IO} = 2.5 V

Figure 2. Leakage Current vs Temperature



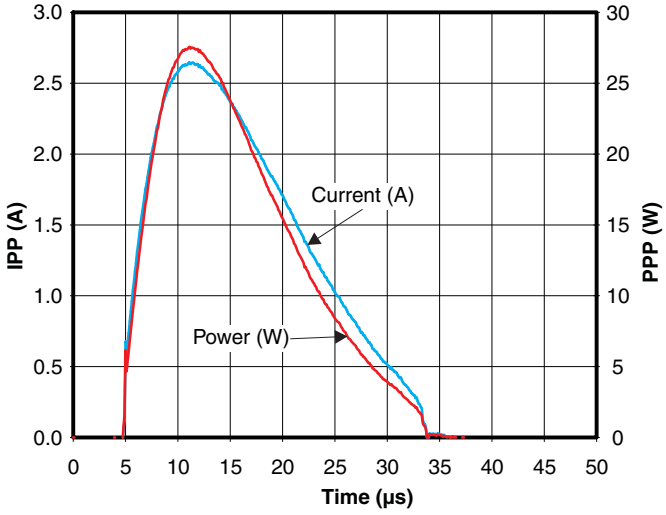
V_{CC} = 5 V

Figure 3. IO Capacitance vs Input Voltage



8-kV Contact, Average of Ten Waveforms

Figure 4. IEC Clamping Waveforms



8/20 µs Pulse

Figure 5. Pulse Waveform

7 Detailed Description

7.1 Overview

The TPD4S009 and TPD4S010 are four-channel TVS diode arrays for electrostatic discharge (ESD) protection. TPD4S009 and TPD4S010 are rated to dissipate contact ESD strikes at the maximum level specified in the IEC 61000-4-2 international standard (Level 4), with ±8-kV contact discharge ESD protection. The low 0.8 pF capacitance of these devices, coupled with the excellent matching between differential signal pairs (0.05-pF line-line capacitance for the TPD4S009DRY) enables this device to operate at high-speed differential data rates (3-dB bandwidth > 4 GHz).

The TPD4S009 offers an optional V_{CC} supply pin which can be connected to system supply plane. There is a blocking diode at the V_{CC} pin to enable the Ioff feature for the TPD4S009. The TPD4S009 can handle live signal at the D+, D- pins when the V_{CC} pin is connected to zero volt. The V_{CC} pin allows all the internal circuit nodes of the TPD4S009 to be at known potential during start up time. However, connecting the optional V_{CC} pin to board supply plane doesn't affect the system level ESD performance of the TPD4S009. The TPD4S010 does not offer the V_{CC} pin.

7.2 Functional Block Diagram

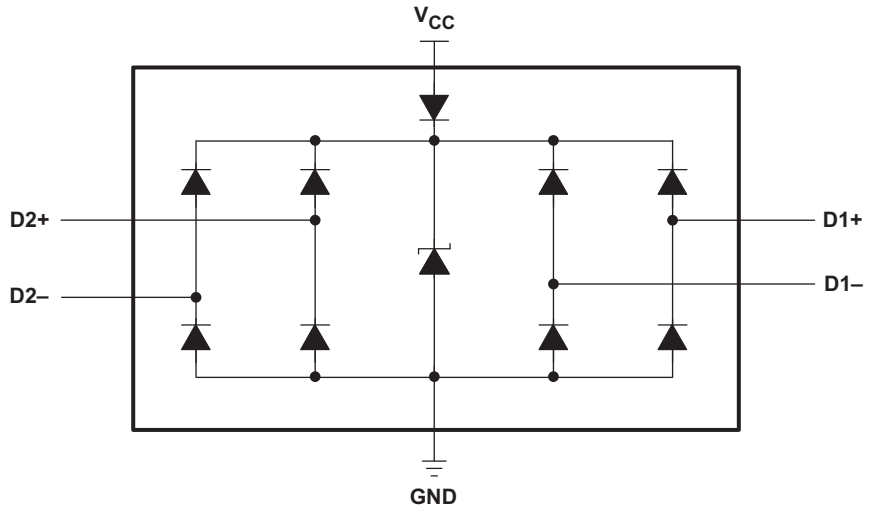


Figure 6. TPD4S009

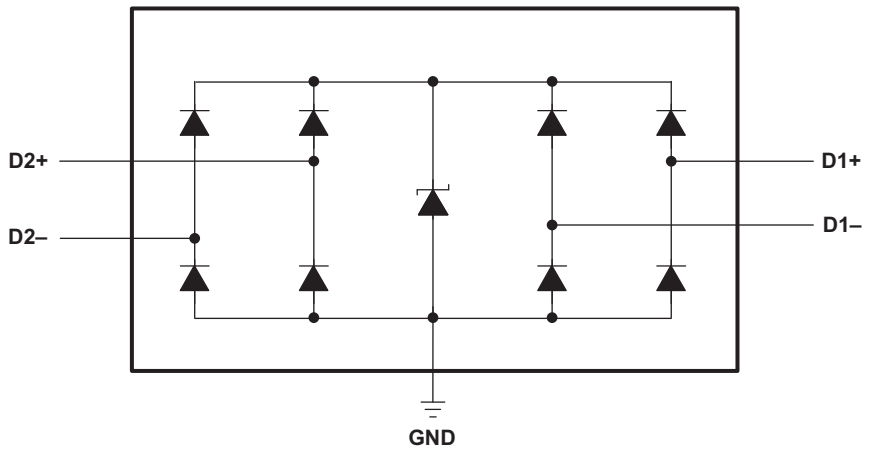


Figure 7. TPD4S010

7.3 Feature Description

7.3.1 ±8-kV IEC61000-4-2 Level 4 Contact ESD Protection

The I/O pins can withstand ESD events up to ±8-kV contact and ±9-kV air. An ESD/surge clamp diverts the current to ground.

7.3.2 IEC61000-4-5 Surge Protection

The I/O pins can withstand surge events up to 2.5 A and 25 W (8/20 µs waveform). An ESD/surge clamp diverts this current to ground.

7.3.3 I/O Capacitance

The capacitance between each I/O pin to ground is 0.8 pF (typical) for both TPD4S009 and TPD4S010. These devices support data rates up to 3.4 Gbps.

7.3.4 Low Leakage Current

The I/O pins feature a low leakage current of 10 nA (typical) with an IO bias of 3.3 V and V_{CC} bias of 5V.

7.3.5 Supports High-Speed Differential Data Rates

The I/O pins low capacitance of 0.8 pF (typical) gives them a typical –3 dB bandwidth > 4GHz. This allows TPD4S009 and TPD4S010 to protect interfaces with high speed signals like HDMI 1.4.

7.3.6 Ultra-low Matching Capacitance Between Differential Signal Pairs

The monolithic silicon technology allows matching between the differential signal pairs. The excellent matching between the differential pair signal lines (0.05-pF line-line capacitance for the TPD4S009DRY) enables this device to operate at high-speed differential data rates (3-dB bandwidth > 4 GHz). Excellent matching capacitance between differential signal pairs is also crucial to minimize the inter-pair and intra-pair skew between differential signals, which is crucial for many high-speed signal interfaces like HDMI 1.4.

7.3.7 I_{off} Feature for the TPD4S009

The TPD4S009 offers an optional V_{CC} supply pin which can be connected to system supply plane. There is a blocking diode at the V_{CC} pin which makes it so the TPD4S009 can handle live signal at the D+, D- pins when the V_{CC} pin is connected to zero volt. This is the I_{off} feature, which is crucial for HDMI, as a live signal can be put on the IO pins when the system is powered off. The TPD4S010 does not offer the V_{CC} pin.

7.3.8 Industrial Temperature Range

This device features an industrial operating range of –40°C to 85°C.

7.3.9 Easy Flow-Through Routing

The layout of this device makes it simple and easy to add protection to an existing layout. The packages offers flow-through routing, requiring minimal modification to an existing layout. Flow-through routing also allows the PCB designer to optimize the signal integrity of any high-speed signals being protected.

7.4 Device Functional Modes

TPD4S009 and TPD4S010 are passive integrated circuits that trigger when voltages are above V_{BR} or below the lower diodes V_f (–0.6 V). During ESD events, voltages as high as ±8 kV (contact) can be directed to ground via the internal diode network. Once the voltages on the protected line fall below the trigger levels of TPD4S009 or TPD4S010 (usually within 10's of nano-seconds) the device reverts back to its high-impedance state.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

TPD4S009 and TPD4S010 are four-channel TVS diode arrays which are used to provide IEC 61000-4-2 system level ESD protection for a human interface connector. TPD4S009 and TPD4S010 provide a path to ground for dissipating ESD events on hi-speed signal lines between the human interface connector and the system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP}, to a safe level for the protected IC.

8.2 Typical Application

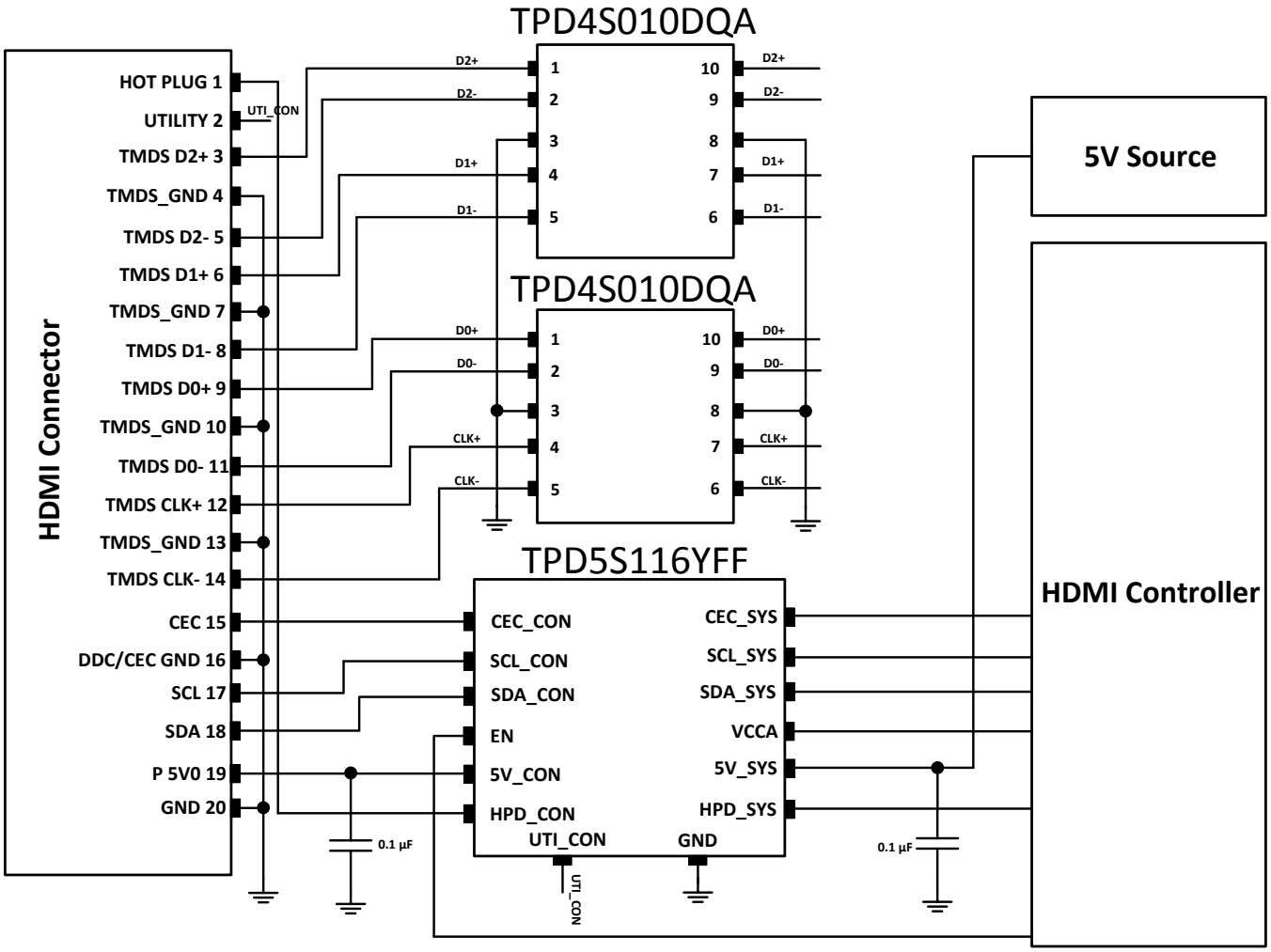


Figure 8. Typical Application Schematic

Typical Application (continued)

8.2.1 Design Requirements

For this design example, two TPD4S010 devices, and one TPD5S116 are being used in an HDMI 1.4 application. This will provide a complete port protection scheme.

Given the HDMI 1.4 application, the following parameters are known.

DESIGN PARAMETER	VALUE
Signal range on Pins 1, 2, 4, or 5	0 V to 3.6 V
Operating Frequency	1.7 GHz

8.2.2 Detailed Design Procedure

To begin the design process, some parameters must be decided upon; the designer needs to know the following:

- Signal range on all the protected lines
- Operating frequency

8.2.2.1 Signal Range on Pin 1, 2, 4, or 5

TPD4S010 has 4 identical protection channels for signal lines. The symmetry of the device provides flexibility when selecting which of the 4 I/O channels will protect which signal lines. Any I/O will support a signal range of 0 to 5.5 V. Therefore, this device will support the HDMI 1.4 signal swing.

8.2.2.2 Bandwidth on Pin 1, 2, 4, or 5

Each pin of the TPD4S010 has a typical –3 dB bandwidth of 4GHz. Therefore, this device can handle HDMI 1.4 data rate of 3.4 Gbps with operating frequency of 1.7 GHz.

8.2.3 Application Curves

Figure 9 and Figure 10 are HDMI eye diagram measurements for the TPD4S009. The same eye diagram performance is expected for the TPD4S010.

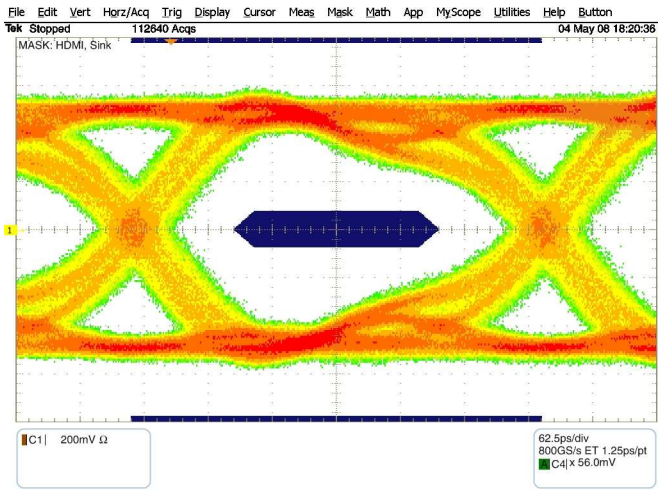


Figure 9. Eye Diagram Without TPD4S009

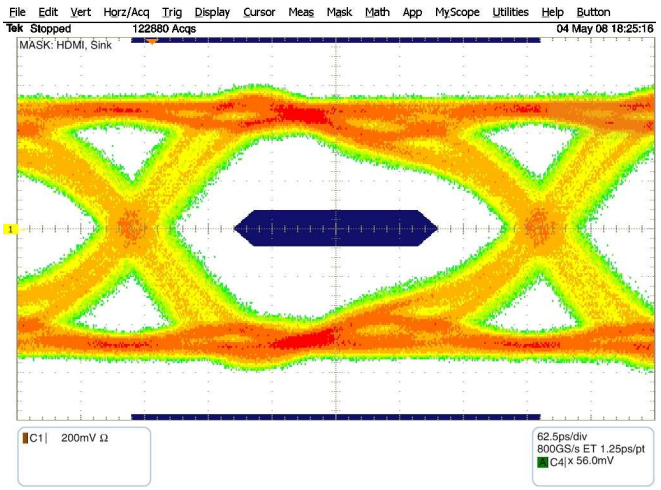


Figure 10. Eye Diagram With TPD4S009

9 Power Supply Recommendations

TPD4S009 and TPD4S010 are passive TVS diodes and so there is no requirement to power them. They are fully functional without any power supply. However, TPD4S009 does provide an option to apply a DC voltage to its V_{CC} pin, whose purpose is to bias the internal central clamp and insure a known voltage on all internal nodes during startup time. This feature is optional, and whether or not a DC voltage is applied to V_{CC} does not affect the ESD performance of this device.

10 Layout

10.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer needs to minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

10.2 Layout Example

This is a layout example for TPD4S010 being used to protect HDMI TMDS Lines.

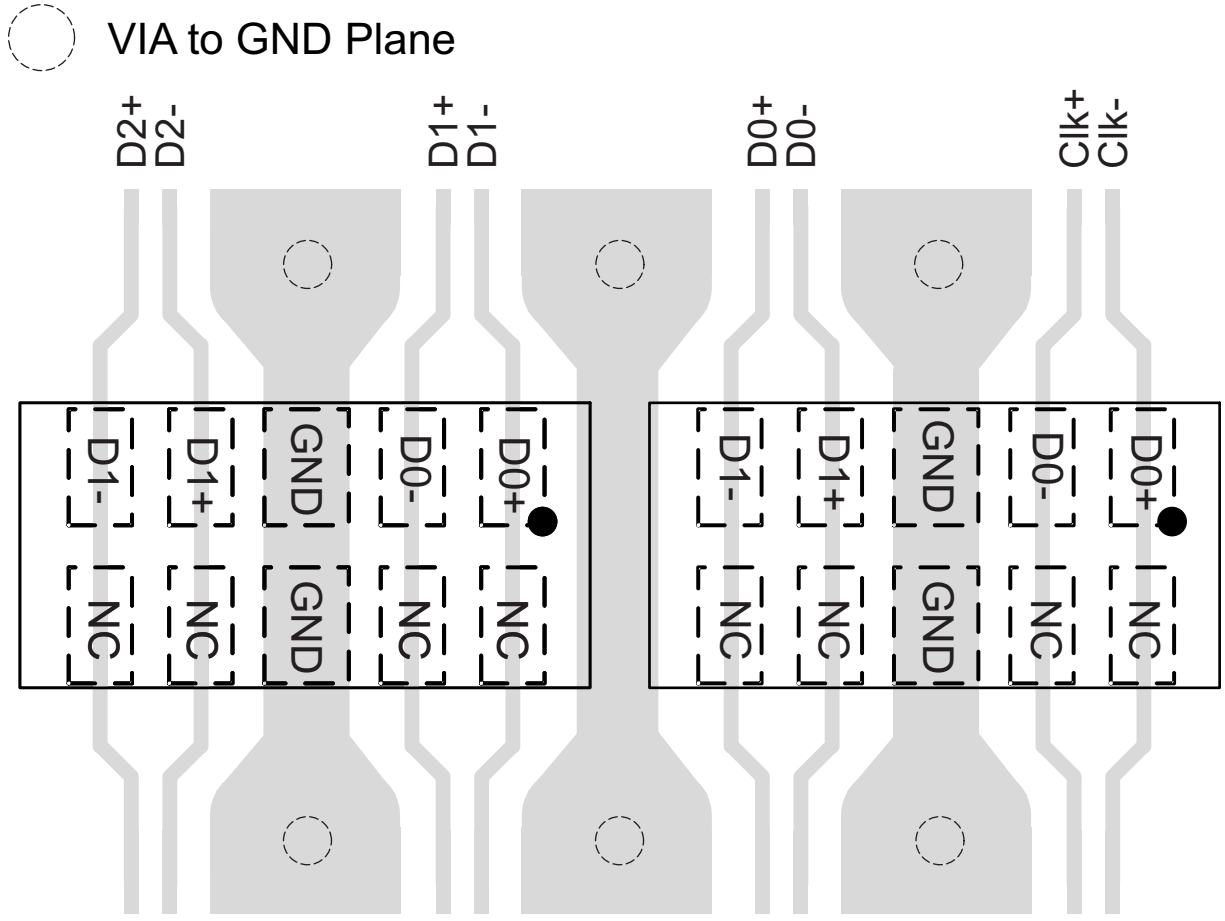


Figure 11. TPD4S010 Layout

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related information see, SLVSBO7

11.2 Trademarks

All trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD4S009DBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	NFJF	Samples
TPD4S009DBVRG4	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	NFJF	Samples
TPD4S009DCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3HR	Samples
TPD4S009DCKRG4	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3HR	Samples
TPD4S009DGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3HR	Samples
TPD4S009DRYR	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3H	Samples
TPD4S010DQAR	ACTIVE	USON	DQA	10	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(4U7, 4UO, 4UR, 4U V, BOR)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

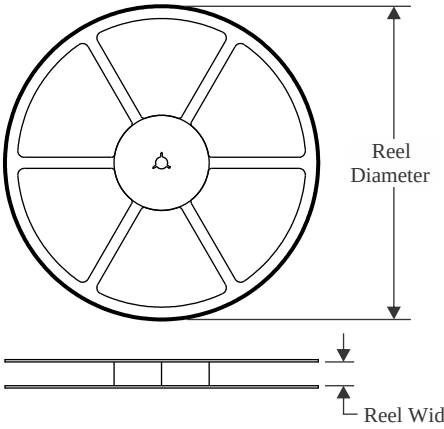
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

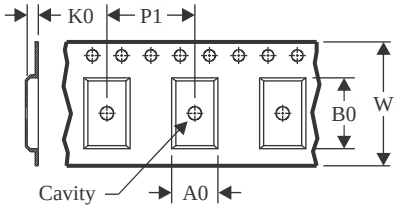
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

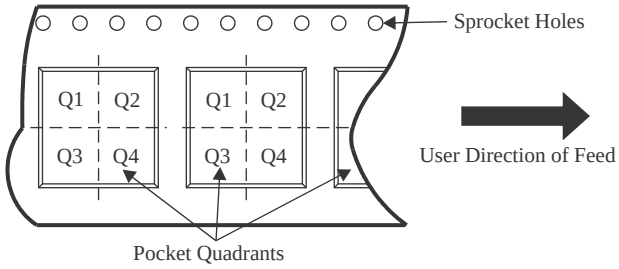


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

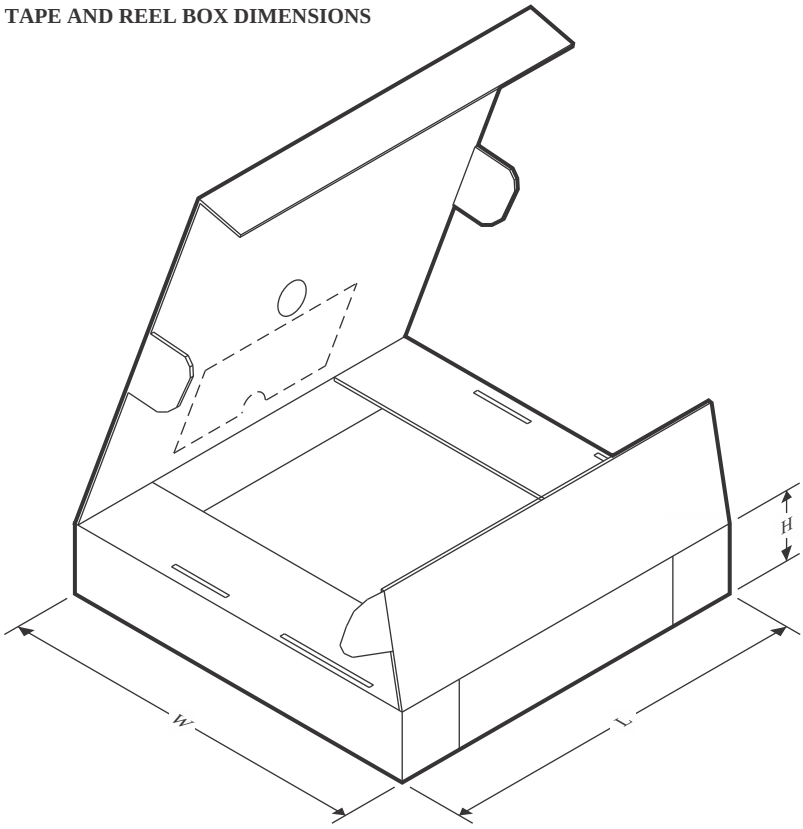
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD4S009DBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPD4S009DCKR	SC70	DCK	6	3000	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
TPD4S009DRYR	SON	DRY	6	5000	180.0	9.5	1.2	1.65	0.7	4.0	8.0	Q1
TPD4S010DQAR	USON	DQA	10	3000	180.0	9.5	1.18	2.68	0.72	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

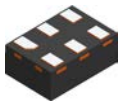
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD4S009DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
TPD4S009DCKR	SC70	DCK	6	3000	183.0	183.0	20.0
TPD4S009DRYR	SON	DRY	6	5000	189.0	185.0	36.0
TPD4S010DQAR	USON	DQA	10	3000	189.0	185.0	36.0

DRY 6 USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

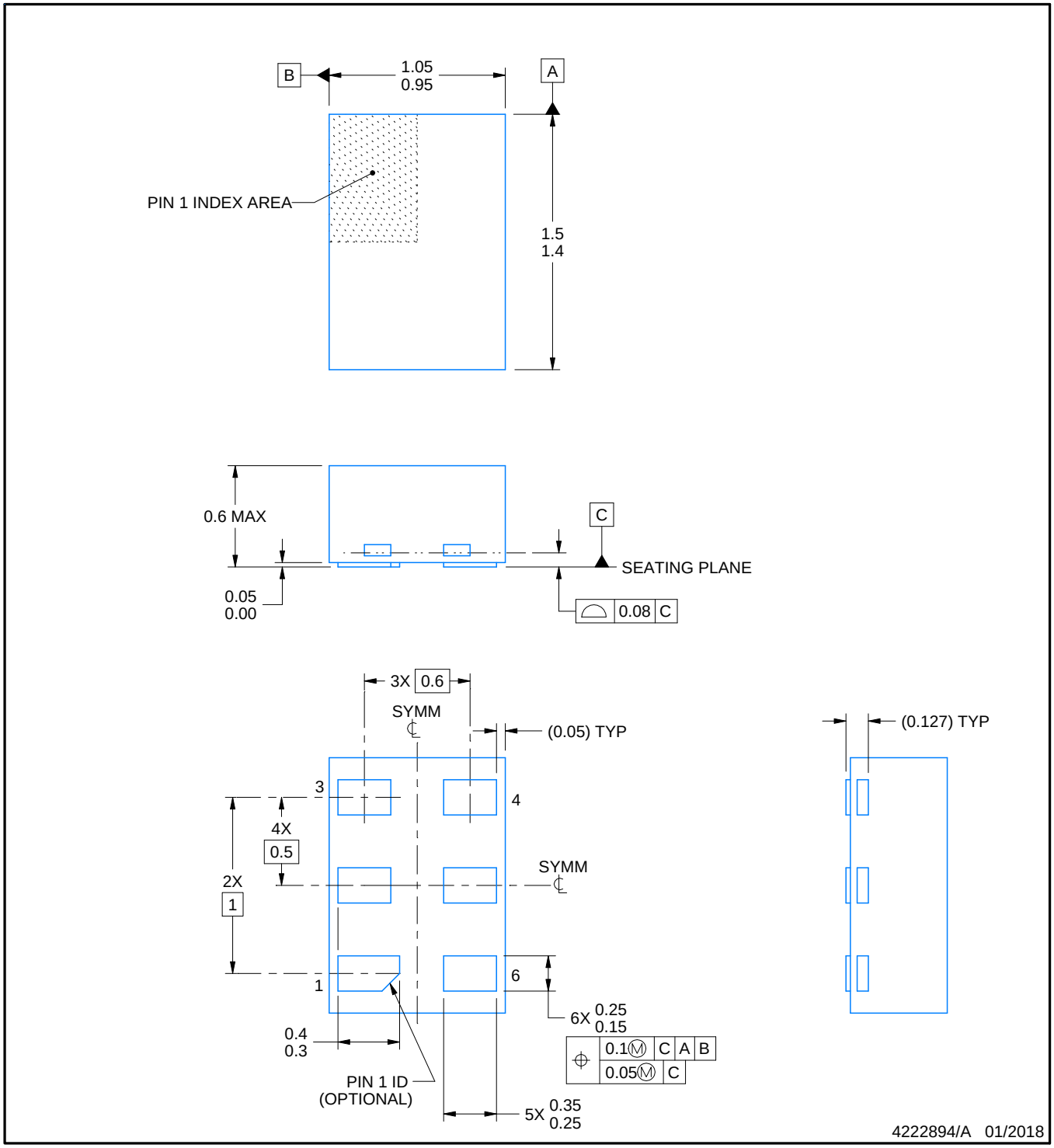
DRY0006A



PACKAGE OUTLINE

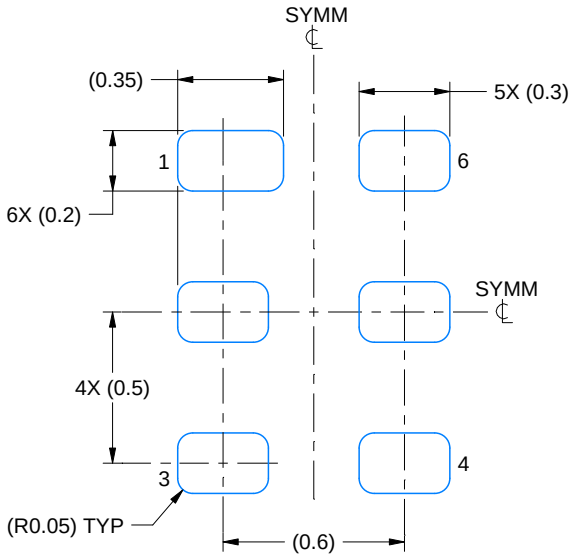
USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

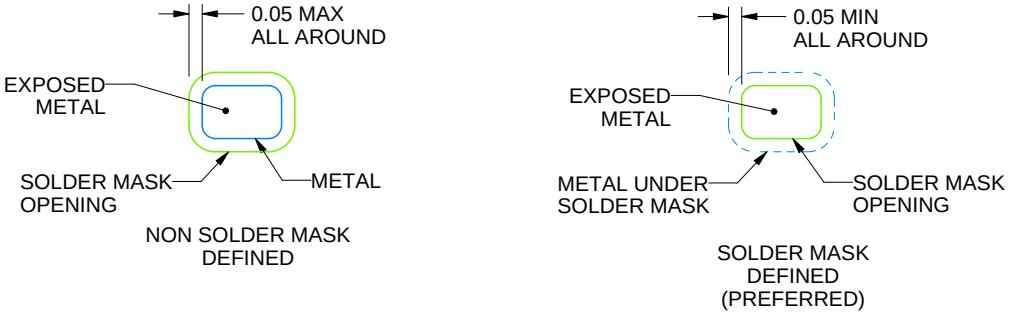


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4222894/A 01/2018

NOTES: (continued)

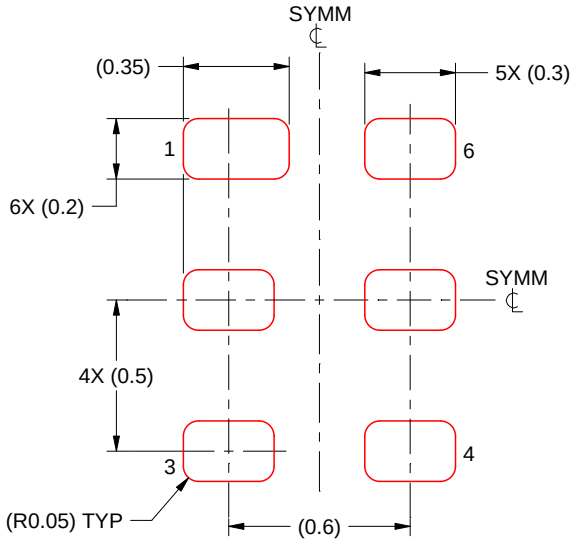
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

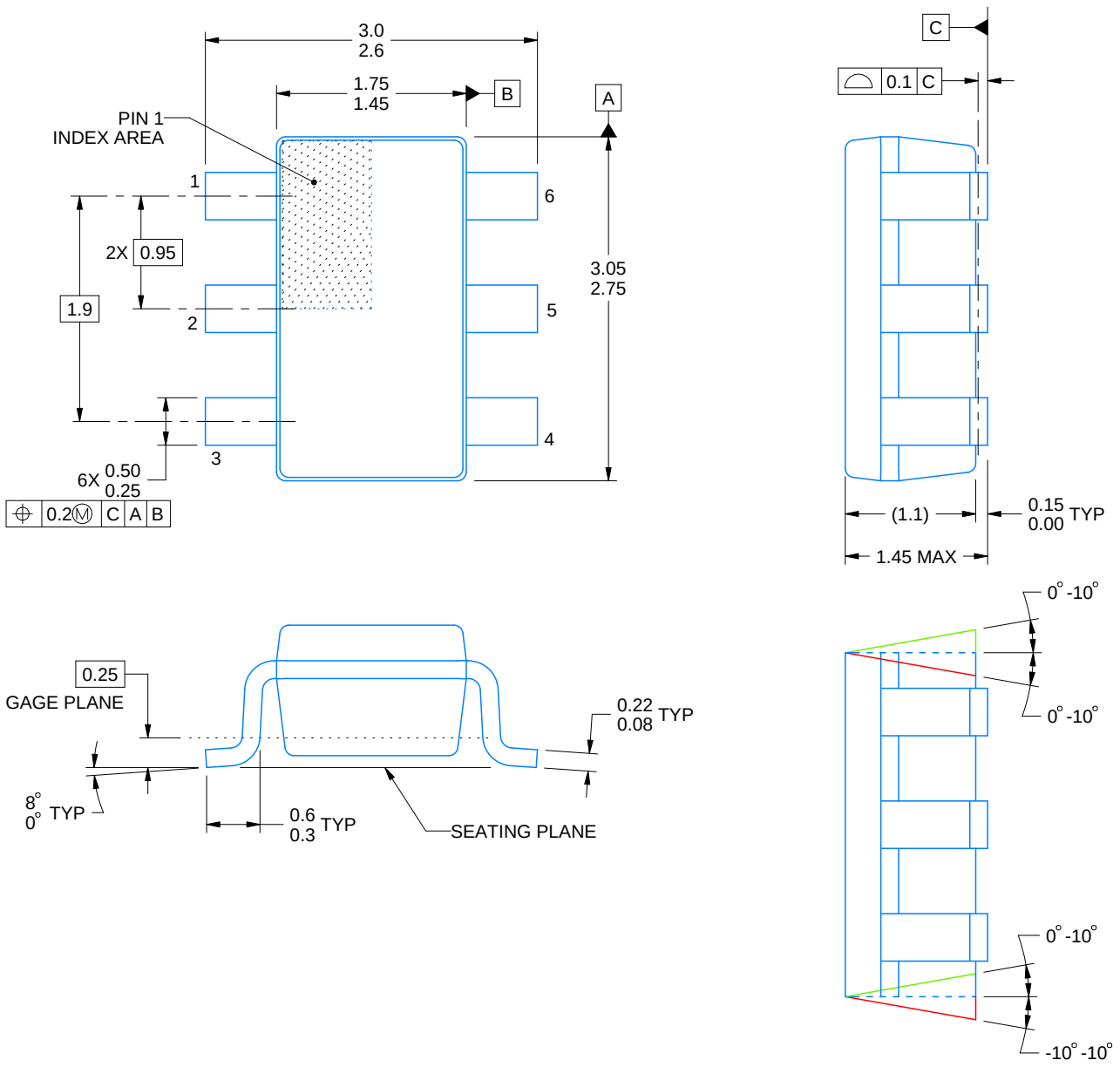
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

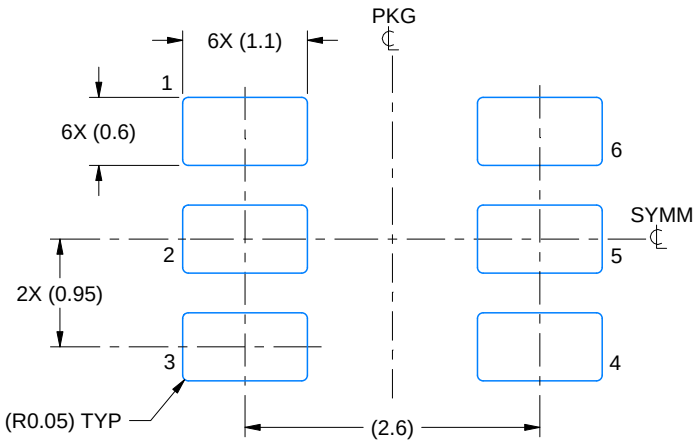


ALTERNATIVE PACKAGE SINGULATION VIEW

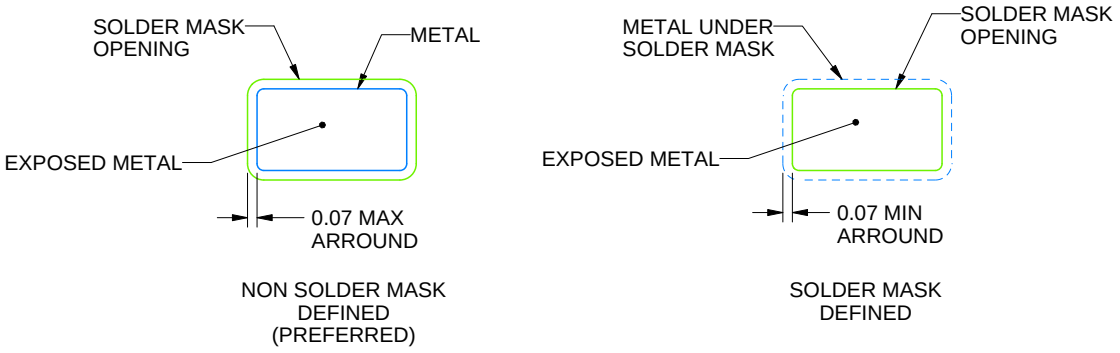
4214840/D 09/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

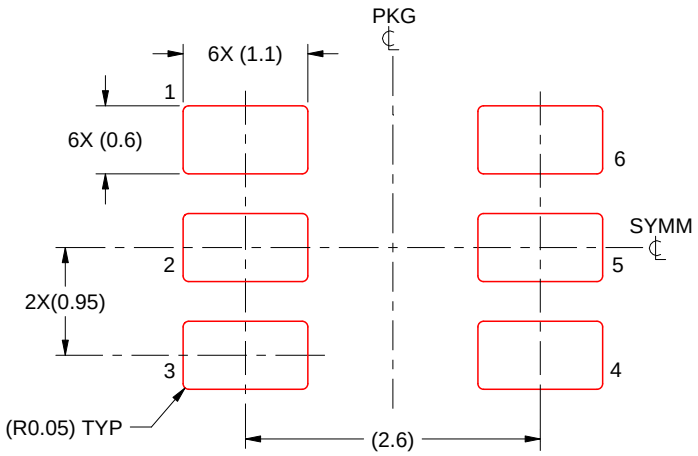


SOLDER MASK DETAILS

4214840/D 09/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/D 09/2023

NOTES: (continued)

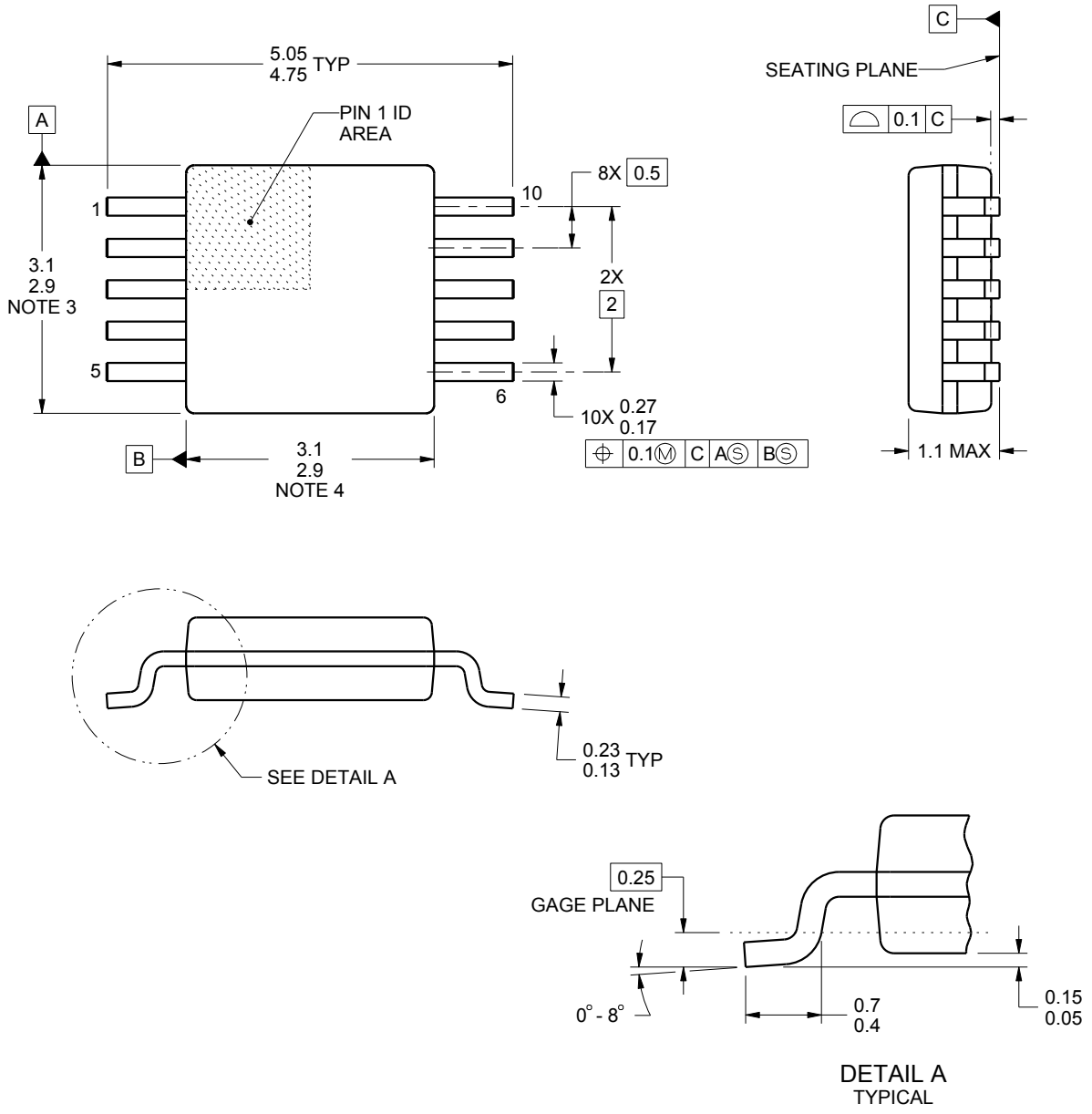
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGS0010A

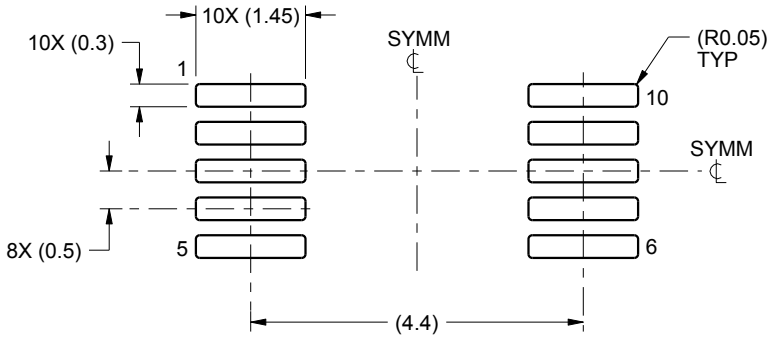
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

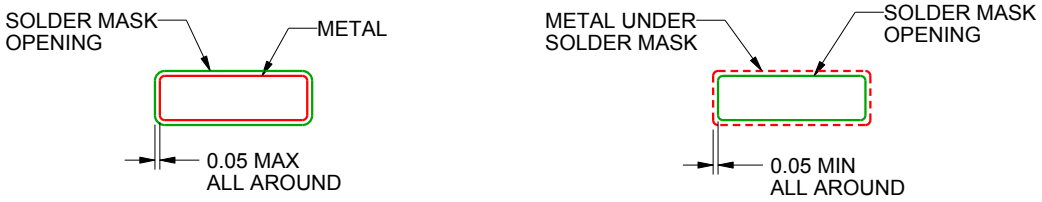


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

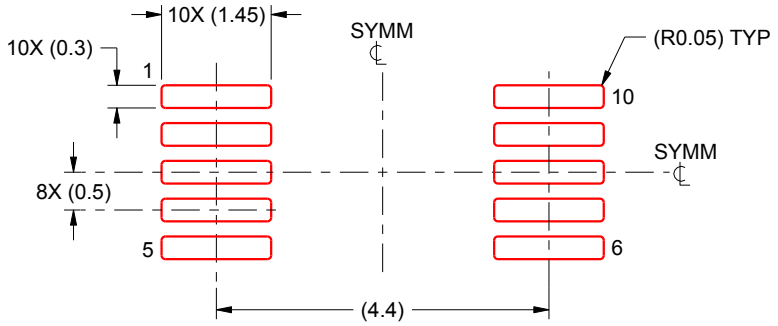


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



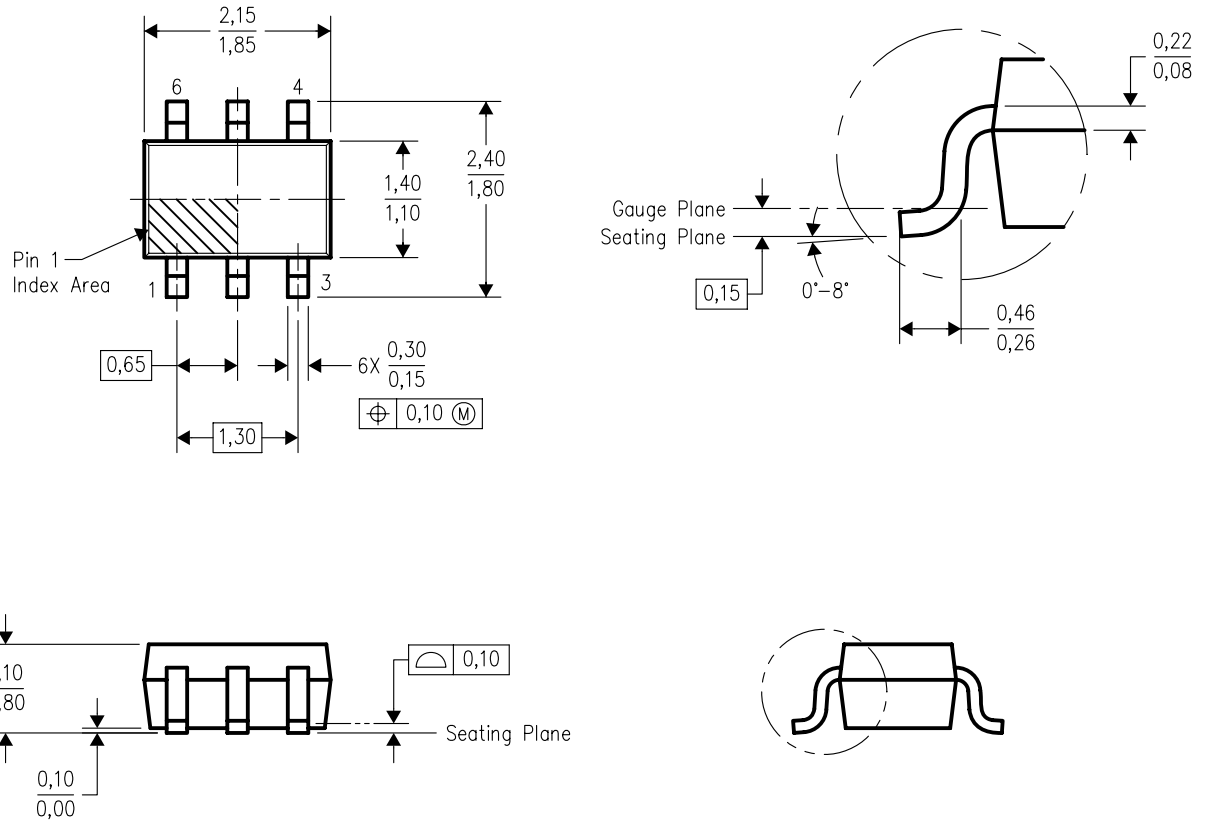
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

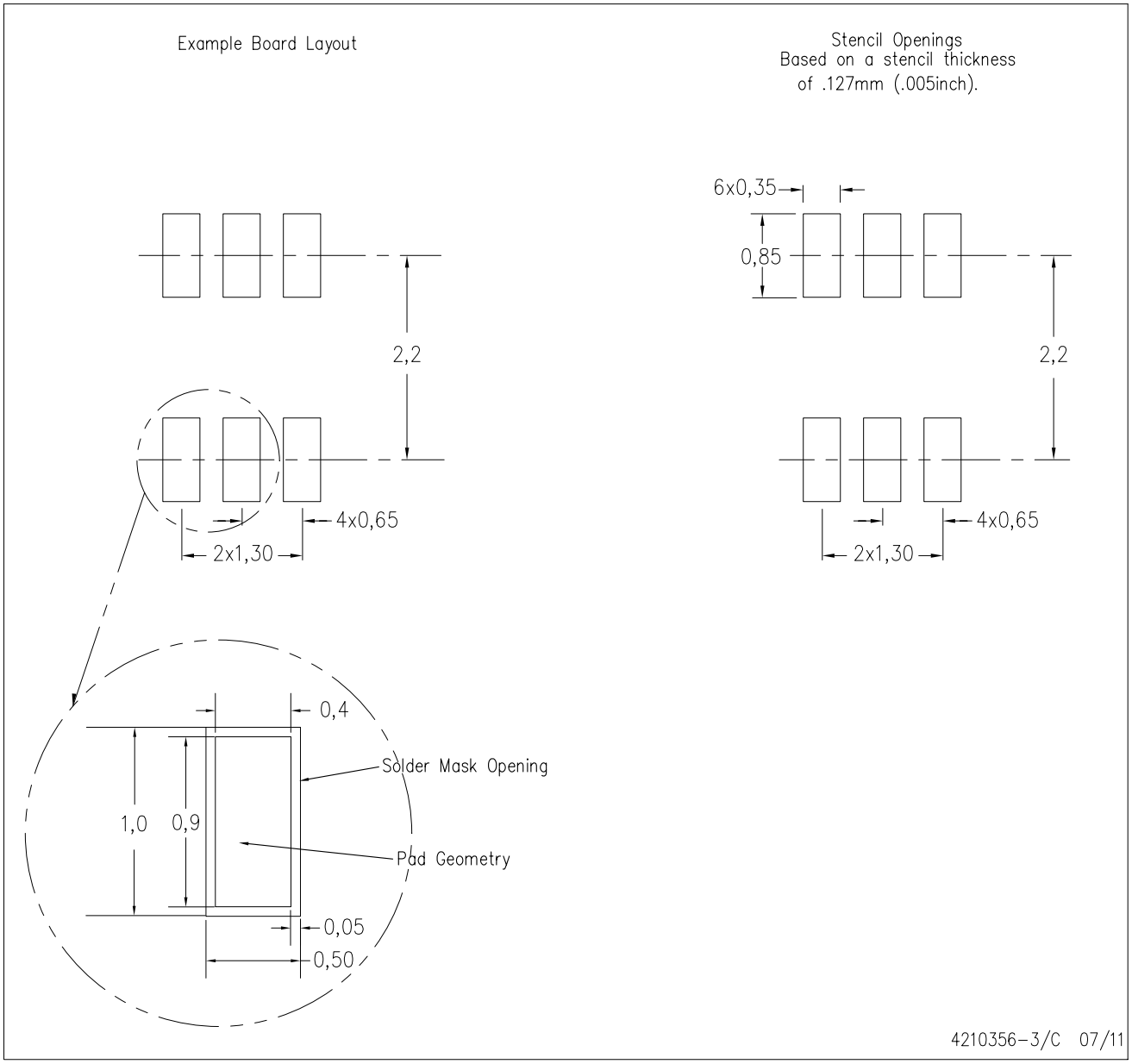
DCK (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



4093553–4/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AB.

DCK (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

GENERIC PACKAGE VIEW

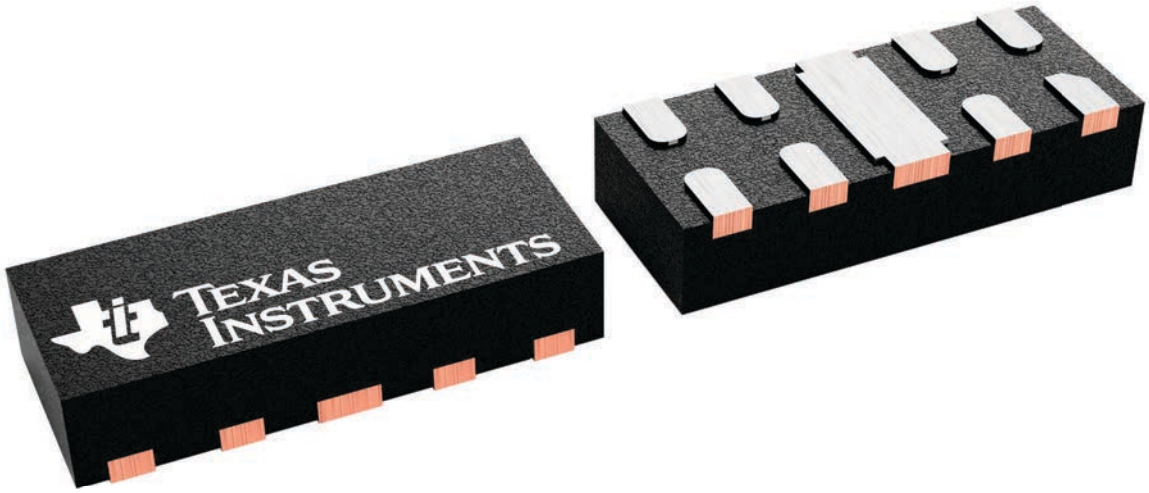
DQA 10

USON - 0.55 mm max height

1 x 2.5, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



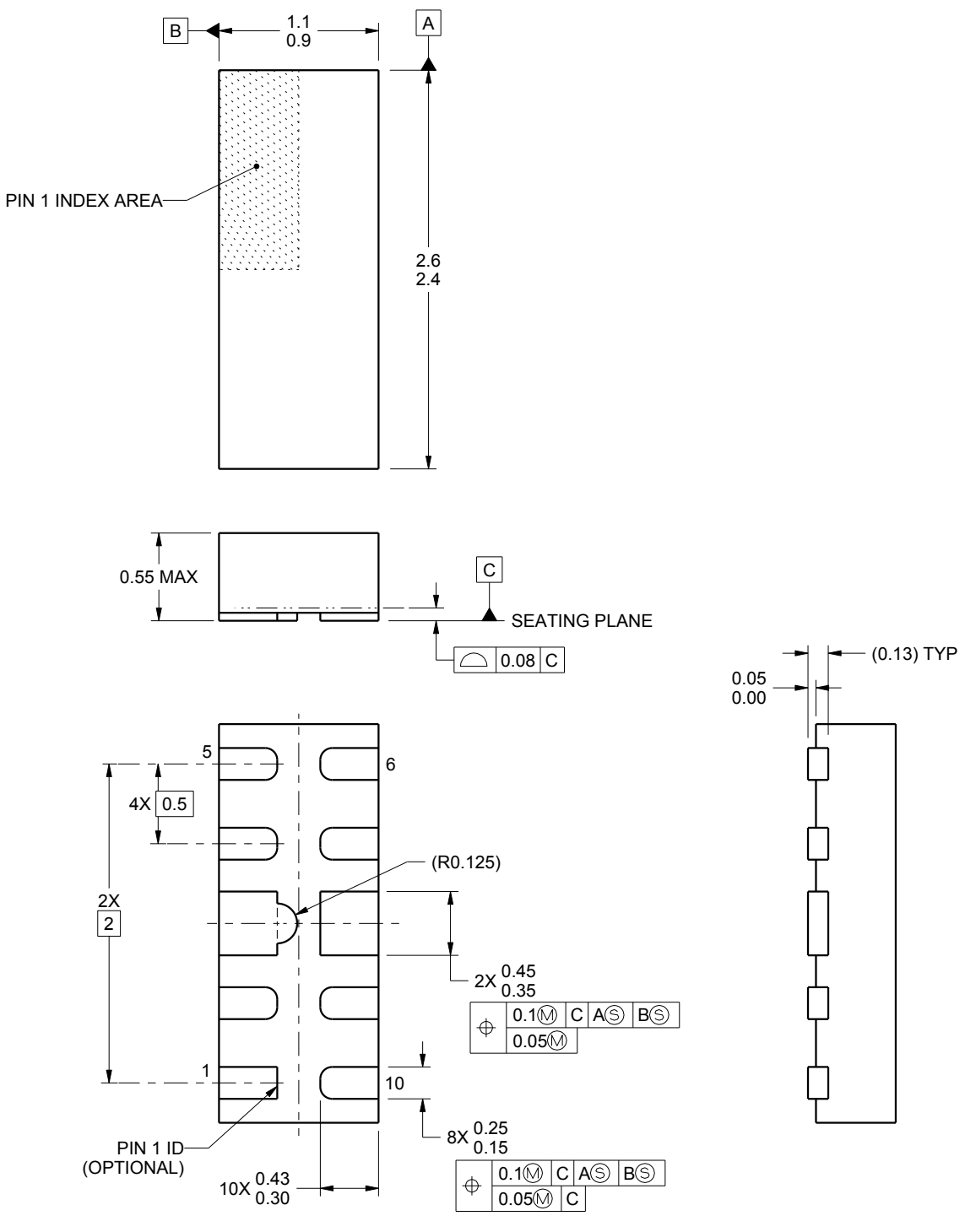
4230320/A

PACKAGE OUTLINE

DQA0010A

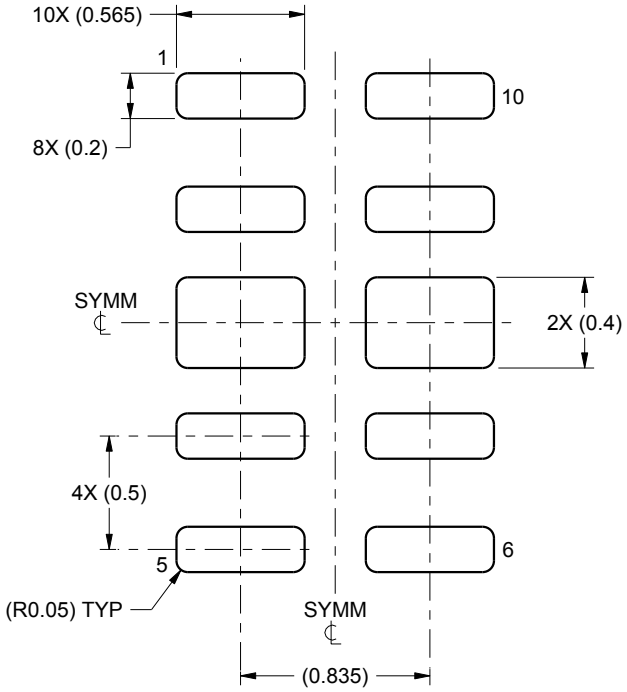
USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

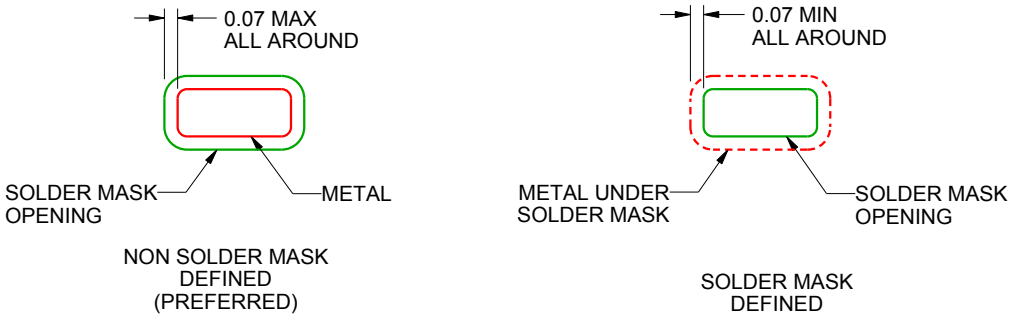


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:30X



SOLDER MASK DETAILS

4220328/A 12/2015

NOTES: (continued)

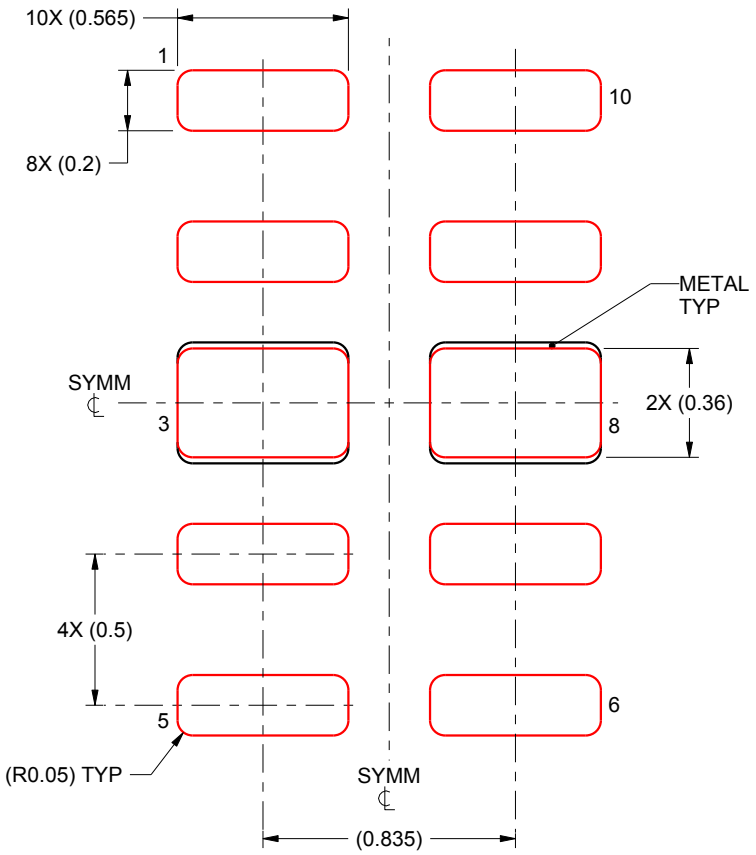
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DQA0010A

USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PADS 3 & 8:
90% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:40X

4220328/A 12/2015

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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