# SN75ALS197 Quadruple Differential Line Receiver

## 1 Features

- Meets or exceeds the requirements of ITU recommendations V.10, V.11, X.26, and X.27
- Designed for multipoint bus transmission on long bus lines in noisy environments
- Designed to operate Up to 20 Mbaud
- 3-State outputs
- Common-mode input voltage Range: − 7 V to 7 V
- Input sensitivity: ±300 mV
- Input hysteresis: 120 mV typical
- High-input impedance: 12 kΩ minimum
- Operates from single 5-V supply
- Low supply-current requirement 35 mA maximum
- Improved speed and power consumption compared to AM26LS32A

## 2 Applications

- Motor drives
- Factory automation and control

## 3 Description

The SN75ALSI97 is a monolithic, quadruple line receiver with 3-state outputs designed using advanced, low-power, Schottky technology. This technology provides combined improvements in bar design, tooling production, and wafer fabrication. This, in turn, provides significantly lower power requirements and permits much higher data throughput than other designs. The device meets the specifications of ITU Recommendations V.10, V.11, X.26, and X.27. The 3-state outputs feature permits direct connection to a bus-organized system with a fail-safe design that makes sure the outputs is always high if the inputs are open.

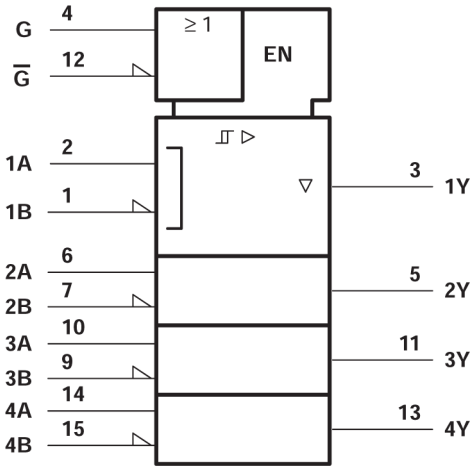
The device is optimized for balanced, multipoint bus transmission at rates up to 20 megabits per second. The input features high-input impedance, input hysteresis for increased noise immunity, and an input sensitivity of ±300 mV over a common-mode input voltage range of −7 V to 7 V. The device also features active-high and active-low enable functions that are common to the four channels. The device is designed for optimum performance when used with the SN75ALS192 quadruple differential line driver.

The SN75ALS197 is characterized for operation from 0°C to 70°C.

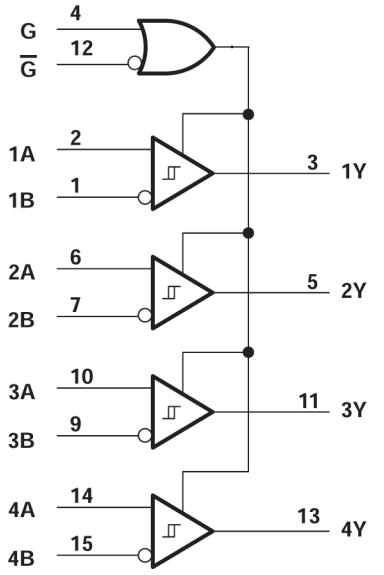
**Package Information**

| PART NUMBER | PACKAGE(1) | PACKAGE SIZE(2) |
|---|---|---|
| SN75ALS197 | SOIC (D, 16) | 9.9 mm × 6 mm |
| | PDIP (N, 16) | 19.3 mm × 9.4 mm |
| | SO (NS, 16) | 10 mm × 7.8 mm |

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.




**Logic Symbol†**




**Logic Diagram (Positive Logic)**

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

# Table of Contents

# 4 Pin Configuration and Functions

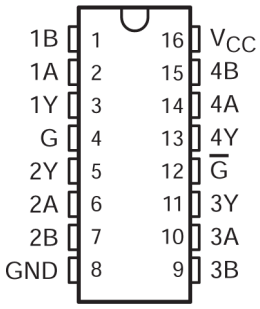



**Figure 4-1. D or N Package (Top View)**

**Table 4-1. Pin Functions**

| PIN | | TYPE[1] | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| 1B | 1 | I | Channel 1 Differential Receiver Inverting Input |
| 1A | 2 | I | Channel 1 Differential Receiver Non-Inverting Input |
| 1Y | 3 | O | Channel 1 Single Ended Output |
| G | 4 | I | Active High Enable |
| 2Y | 5 | O | Channel 2 Single Ended Output |
| 2A | 6 | I | Channel 2 Differential Receiver Non-Inverting Input |
| 2B | 7 | I | Channel 2 Differential Receiver Inverting Input |
| GND | 8 | GND | Device GND |
| 3B | 9 | I | Channel 3 Differential Receiver Inverting Input |
| 3A | 10 | I | Channel 3 Differential Receiver Non-Inverting Input |
| 3Y | 11 | O | Channel 3 Single Ended Output |
| $\overline{G}$ | 12 | I | Active Low Enable |
| 4Y | 13 | O | Channel 4 Single Ended Output |
| 4A | 14 | I | Channel 4 Differential Receiver Non-Inverting Input |
| 4B | 15 | I | Channel 4 Differential Receiver Inverting Input |
| $V_{CC}$ | 16 | PWR | Device VCC (4.75 V to 5.25 V) |

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage, see note(2) | | 7 | V |
| $V_I$ | Input voltage, A or B inputs | | ±15 | V |
| $V_{ID}$ | Differential input voltage, see note(3) | | ±15 | V |
| $V_I$ | Enable input voltage | | 7 | V |
| $I_{OL}$ | Low-level output current | | 50 | mA |
| | Continuous total dissipation | See Dissipation Rating Table | | |
| $T_A$ | Operating free-air temperature range | 0 | 70 | °C |
| $T_{stg}$ | Storage temperature range | − 65 | 150 | °C |
| | Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | | 260 | °C |

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential input voltage, are with respect to network ground terminal.
(3) Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.

## 5.2 Dissipation Ratings

| PACKAGE | $T_A \le 25°C$ POWER RATING | DERATING FACTOR | $T_A = 70°C$ POWER RATING |
|---|---|---|---|
| D | 950 mW | 7.6 mW/°C | 608 mW |
| N | 1150 mW | 9.2 mW/°C | 736 mW |

## 5.3 Recommended Operating Conditions

| | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage, $V_{CC}$ | 4.75 | 5 | 5.25 | V |
| Common-mode input voltage, $V_{IC}$ | | | ±7 | V |
| Differential input voltage, $V_{ID}$ | | | ±12 | V |
| High-level input voltage, $V_{IH}$ | 2 | | | V |
| Low-level input voltage, $V_{IL}$ | | | 0.8 | V |
| High-level output current, $I_{OH}$ | | | −400 | µA |
| Low-level output current, $I_{OL}$ | | | 16 | mA |
| Operating free-air temperature, $T_A$ | 0 | | 70 | °C |

## 5.4 Thermal Information

| THERMAL METRIC(1) | | N (PDIP) 16 Pins | D (SOIC) 16 Pins | UNIT |
|---|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 60.6 | 84.6 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 48.1 | 43.5 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 40.6 | 43.2 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 27.5 | 10.4 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 40.3 | 42.8 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

## 5.5 Electrical Characteristics

over recommended range of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP[1] | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IT+}$ | Positive-going input threshold voltage | | | | | 300 | mV |
| $V_{IT-}$ | Negative-going input threshold voltage | | | −300[1] | | | mV |
| $V_{hys}$ | Hysteresis voltage ($V_{IT+} - V_{IT-}$) | See Figure 5-1 | | | 120 | | mV |
| $V_{IK}$ | Enable-input clamp voltage | $I_I$ = −18 mA | | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | $V_{ID}$ = 300 mV, | $I_{OH}$ = − 400 µA | 2.7 | 1.6 | | V |
| $V_{OL}$ | Low-level output voltage | $V_{ID}$ = −300 mV | $I_{OL}$ = 8 mA | | | 0.45 | V |
| | | | $I_{OL}$ = 16 mA | | | 0.5 | |
| $I_{OZ}$ | High-impedance-state output current | $V_{CC}$ = 5.25 V | $V_O$ = 2.4 V | | | 20 | µA |
| | | | $V_{OH}$ = 0.4 V | | | −20 | |
| $I_I$ | Line input current | Other input at 0 V, See Note 3 | $V_I$ = 15 V | | 0.7 | 1.2 | µA |
| | | | $V_I$ = −15 V | | −1.0 | −1.7 | |
| $I_H$ | High-level enable-input current | | $V_{IH}$ = 2.7 V | | | 20 | µA |
| | | | $V_{IH}$ = 5.25 V | | | 100 | |
| $I_{IL}$ | Low-level enable-input current | $V_{IL}$ = 0.4 V | | | | −100 | µA |
| | Input resistance | | | 12 | 18 | | kΩ |
| $I_{OS}$ | Short-circuit output current[2] | $V_{ID}$ = 3 V, | $V_O$ = 0 | −15 | −78 | −130 | mA |
| $I_{CC}$ | Supply current | Outputs disabled | | | 22 | 35 | mA |

(1) The algebraic convention, in which the less positive limit is designated minimum, is used in this data sheet for threshold voltage levels only.
(2) Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
(3) Refer to ANSI Standard EIA/TIA-422-B and EIA/TIA-423-B for exact conditions.

## 5.6 Switching Characteristics

$V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low- to high-level output | $V_{ID}$ = −2.5 V to 2.5 V, See Figure 6-2 | $C_L$ = 15 pF | | 15 | 22 | ns |
| $t_{PHL}$ | Propagation delay time, high- to low-level output | | | | 15 | 22 | ns |
| $t_{PZH}$ | Output enable time to high level | $C_L$ = 15 pF, | See Figure 6-3 | | 13 | 25 | ns |
| $t_{PZL}$ | Output enable time to low level | | | | 11 | 25 | |
| $t_{PHZ}$ | Output disable time from high level | $C_L$ = 15 pF, | See Figure 6-3 | | 13 | 25 | ns |
| $t_{PLZ}$ | Output disable time from low level | | | | 15 | 22 | |

## 5.7 Typical Characteristics

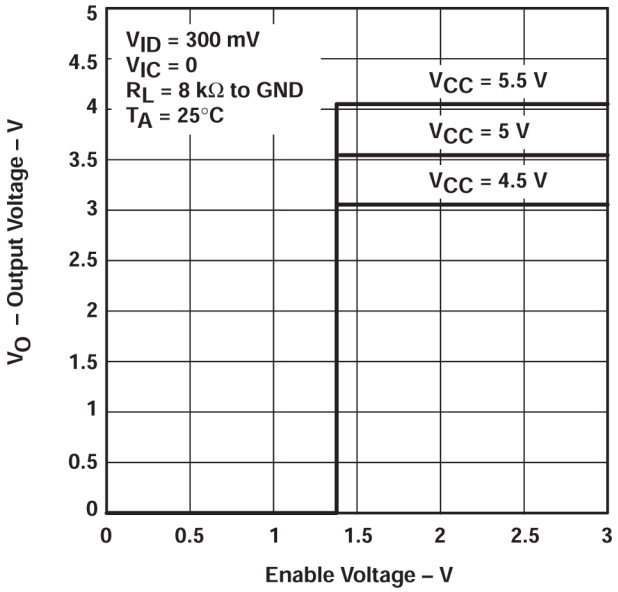



**Figure 5-1. Output Voltage vs Enable Voltage**

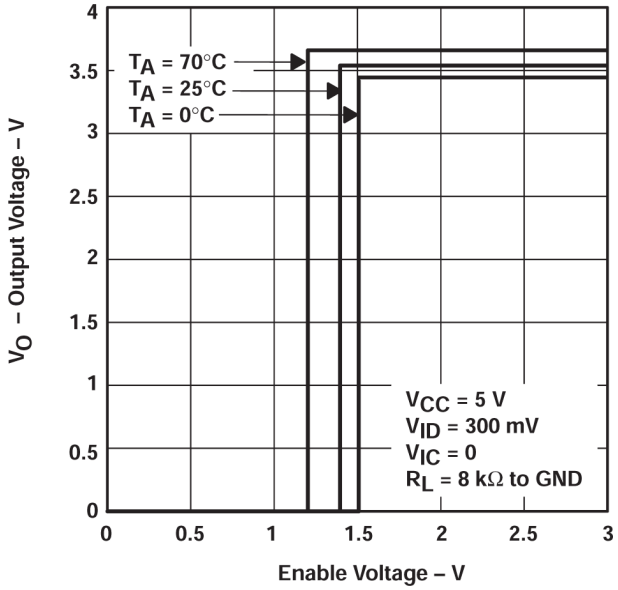



**Figure 5-2. Output Voltage vs Enable Voltage**

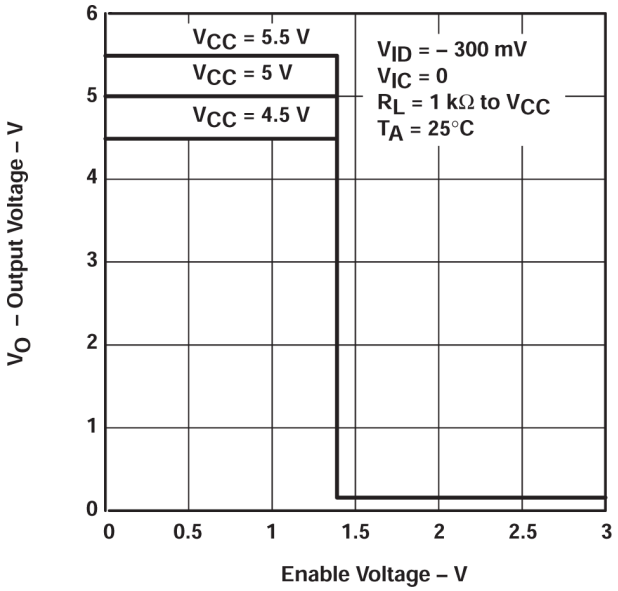



**Figure 5-3. Output Voltage vs Enable Voltage**

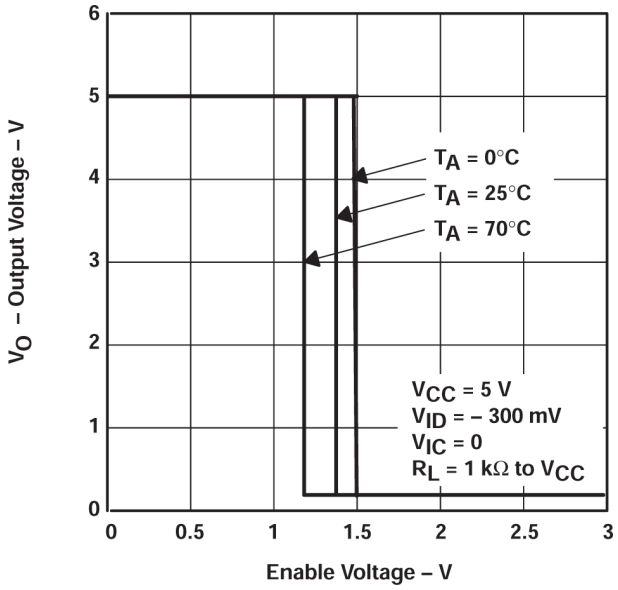



**Figure 5-4. Output Voltage vs Enable Voltage**

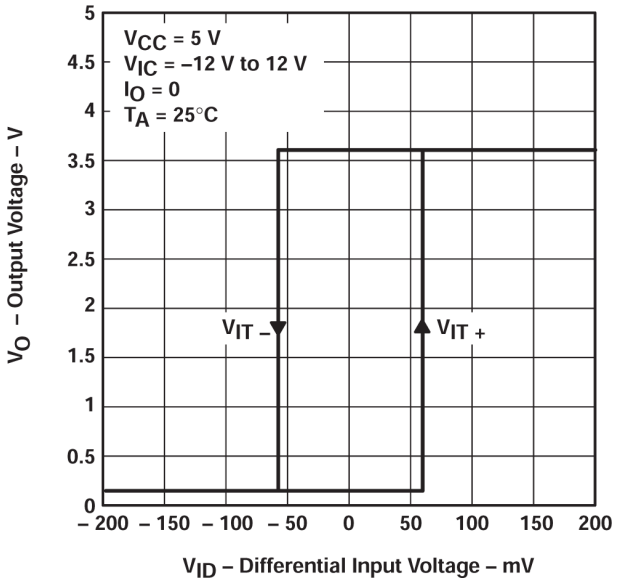



**Figure 5-5. Output Voltage vs Differential Input Voltage**

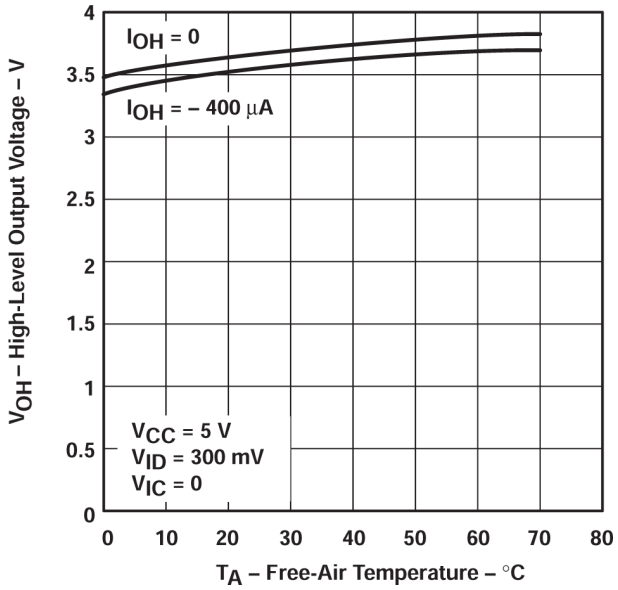



**Figure 5-6. High-level Output Voltage vs Free-air Temperature**

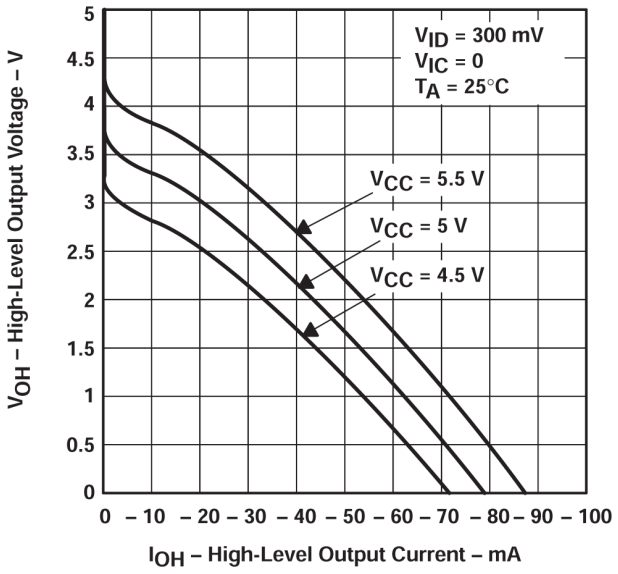



**Figure 5-7. High-level Output Voltage vs High-level Output Current**

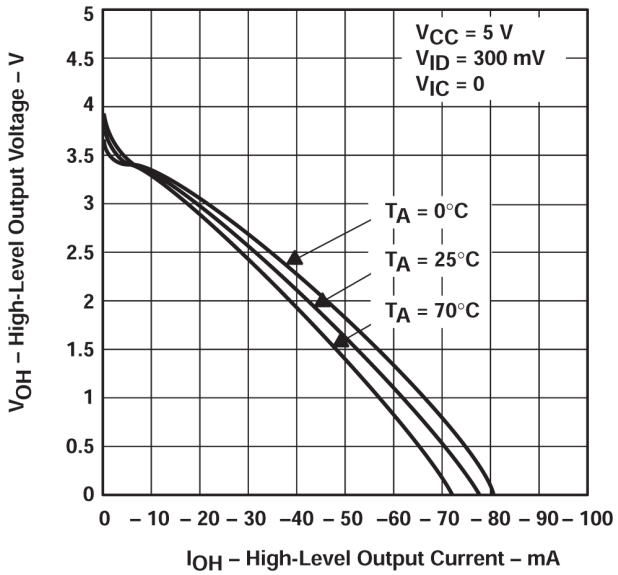



**Figure 5-8. High-level Output Voltage vs High-level Output Current**

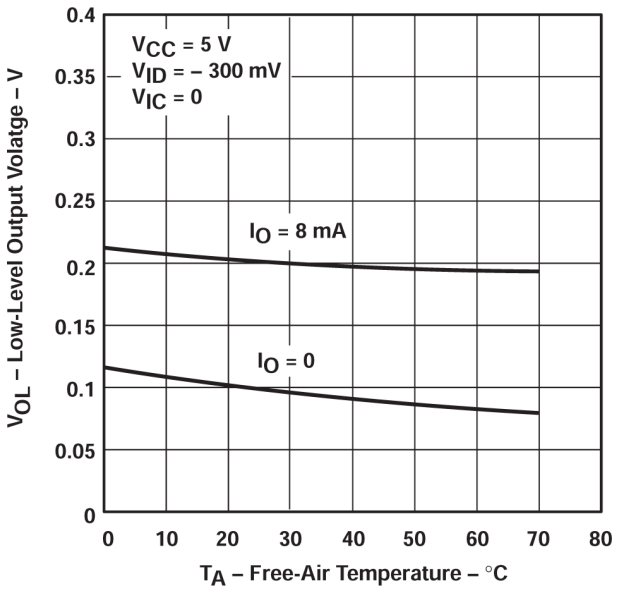



**Figure 5-9. Low-level Output Voltage vs Free-air Temperature**

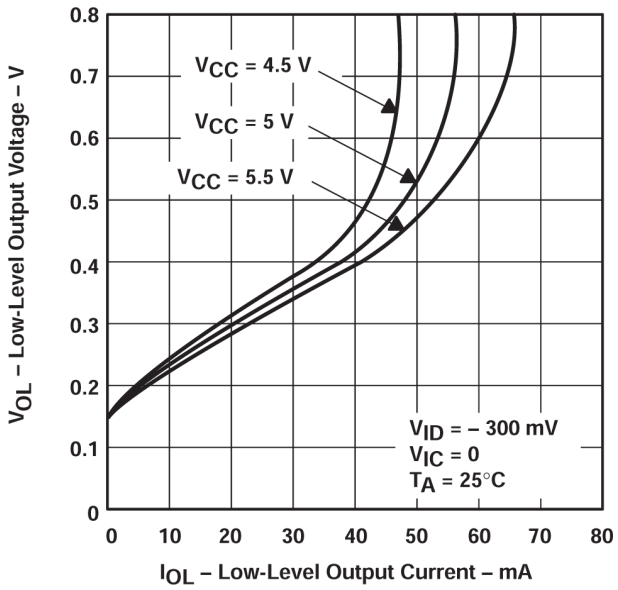



**Figure 5-10. Low-level Output Voltage vs Low-level Output Current**

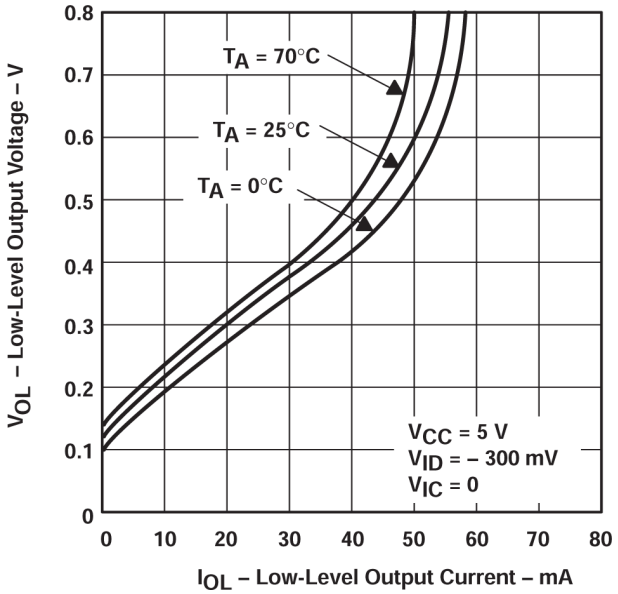



**Figure 5-11. Low-level Output Voltage vs Low-level Output Current**

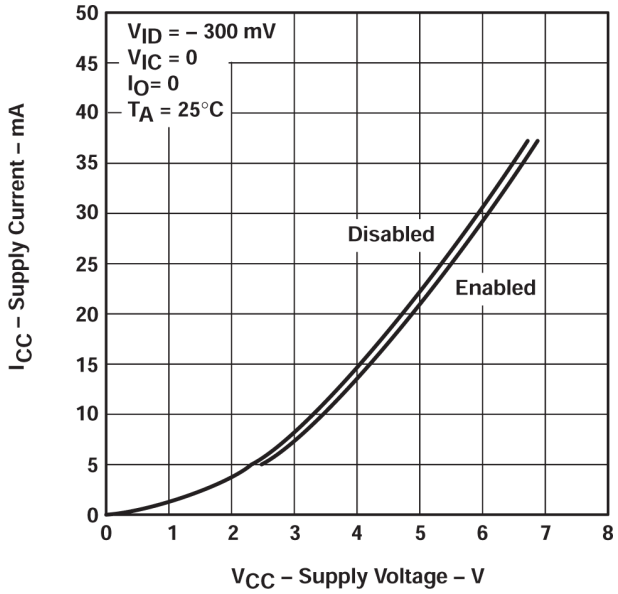



**Figure 5-12. Supply Current vs Supply Voltage**

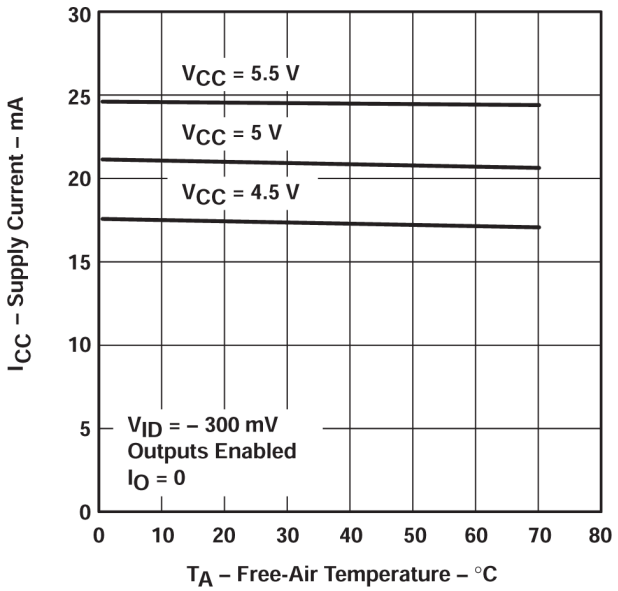



**Figure 5-13. Supply Current vs Free-air Temperature**

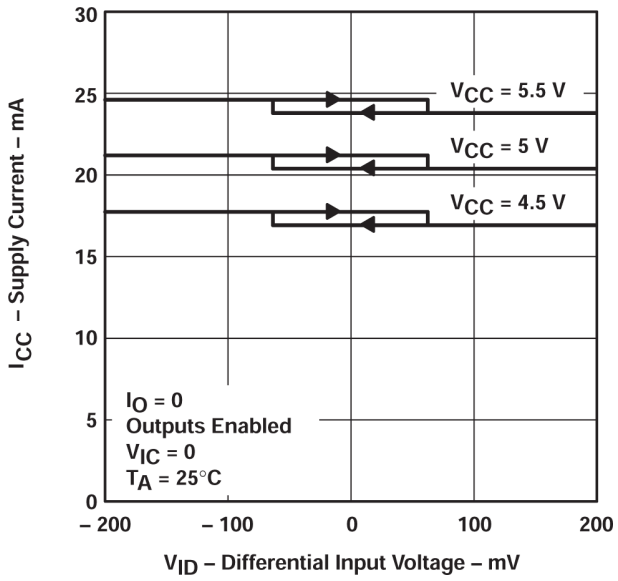



**Figure 5-14. Supply Current vs Differential Input Voltage**

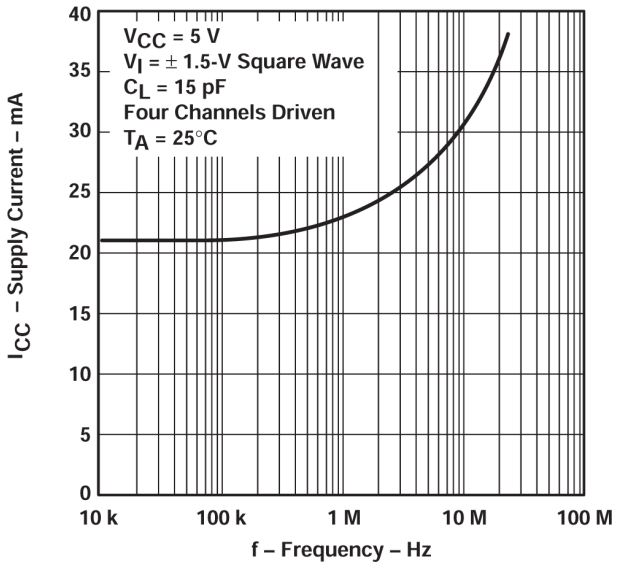



**Figure 5-15. Supply Current vs Frequency**

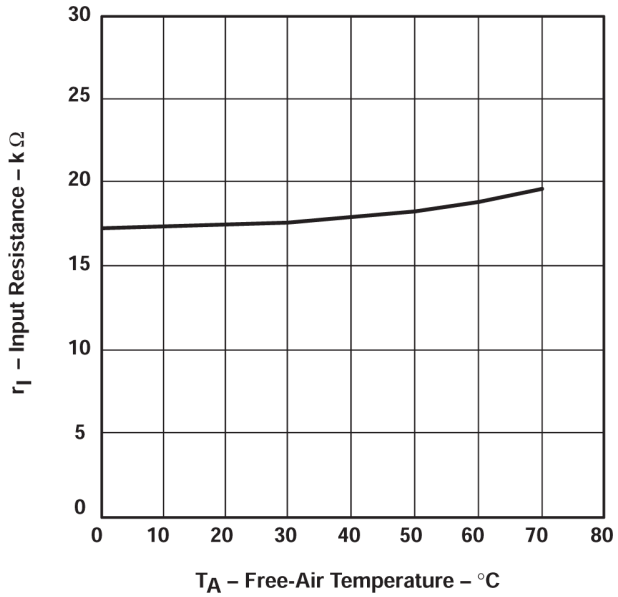



**Figure 5-16. Input Resistance vs Free-air Temperature**

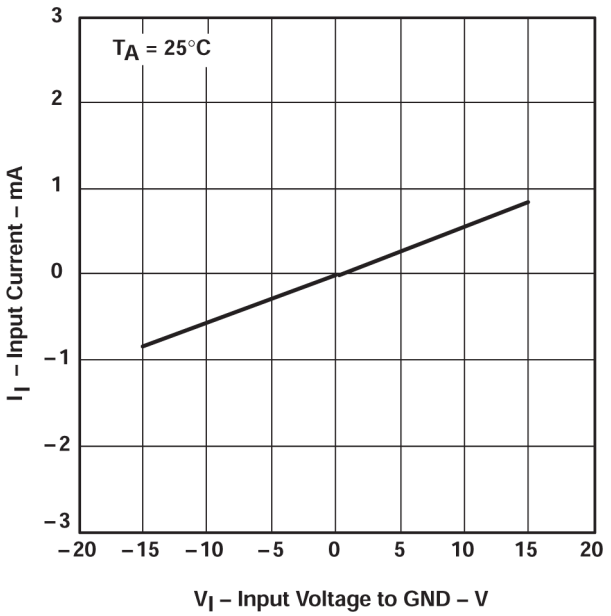



**Figure 5-17. Input Current vs Input Voltage to Gnd**

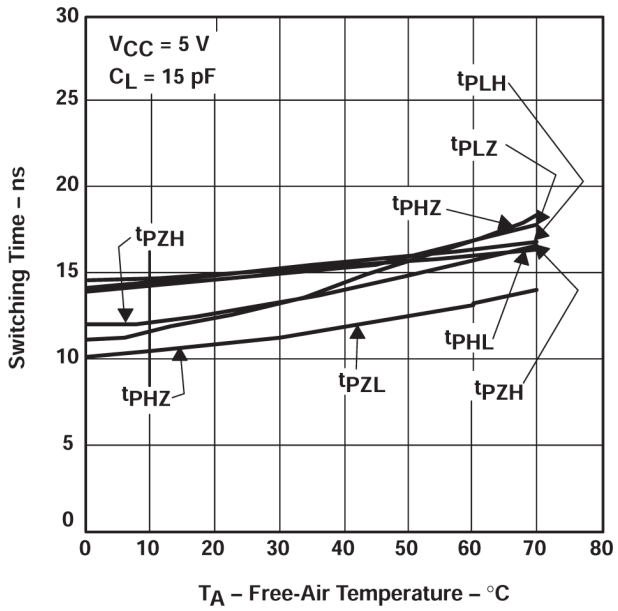



**Figure 5-18. Switching Time vs Free-air Temperature**

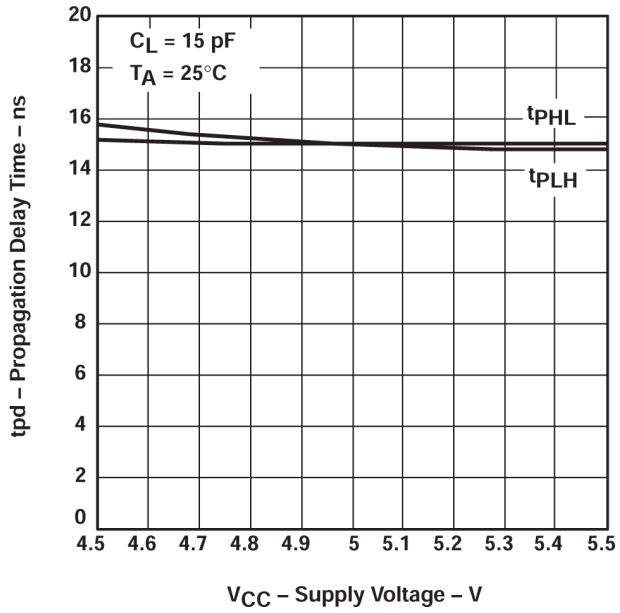



**Figure 5-19. Propagation Delay Time vs Supply Voltage**

## 6 Parameter Measurement Information

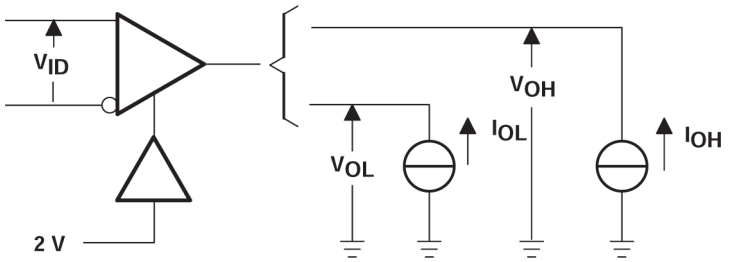
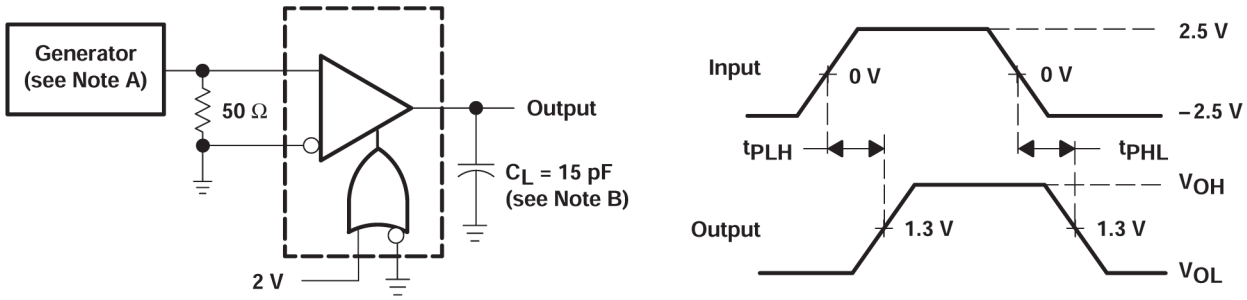


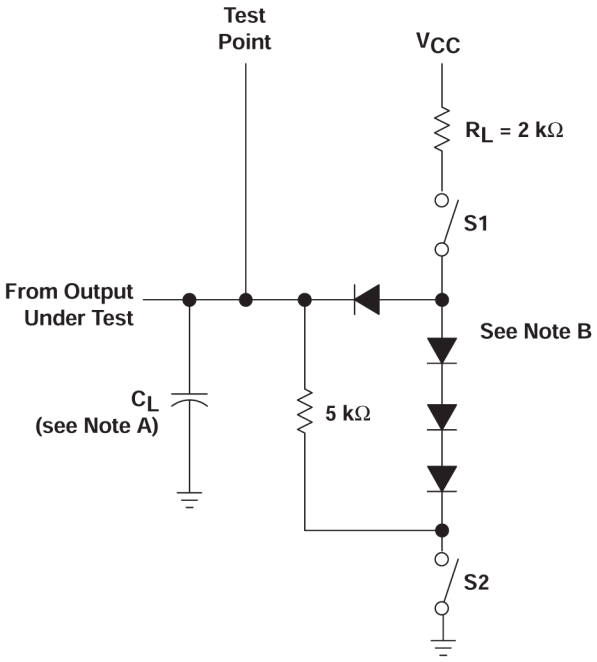

**Figure 6-1. $V_{OH}$ and $V_{OL}$ Test Circuit**



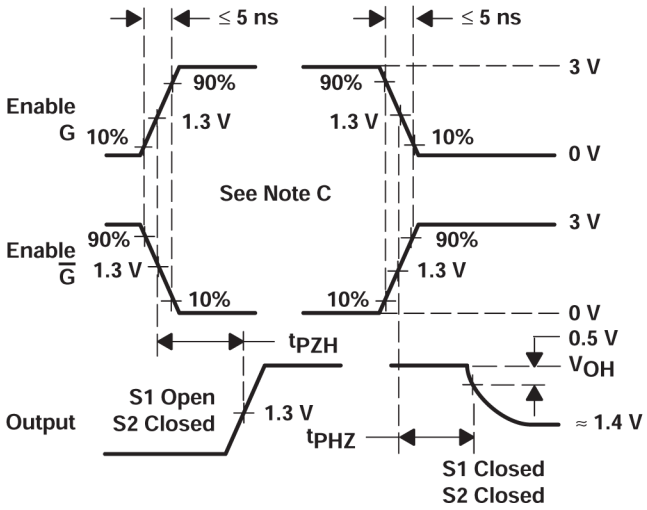

A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_O$ = 50 Ω, $t_r$ ≤ 6 ns, $t_f$ ≤ 6 ns.

B. $C_L$ includes probe and jig capacitance.

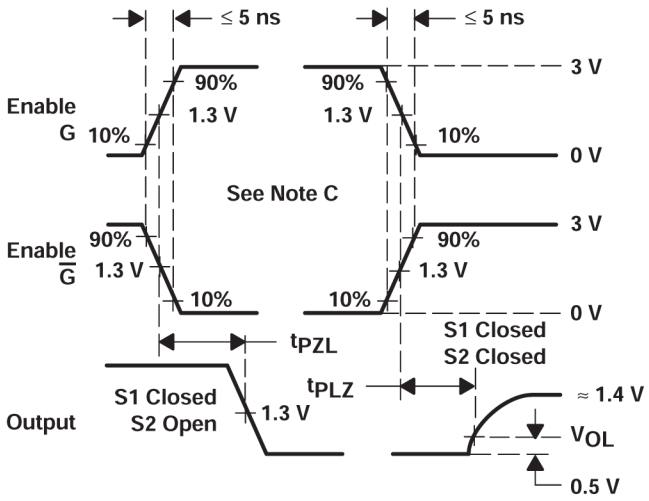
**Figure 6-2. $t_{PLH}$ And $T_{PHL}$ Test Circuit and Voltage Waveforms**




LOAD CIRCUIT




VOLTAGE WAVEFORMS FOR $t_{PHZ}$ and $t_{PZH}$




VOLTAGE WAVEFORMS FOR $t_{PLZ}$ and $t_{PZL}$

NOTES: A. $C_L$ includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. Enable G is tested with $\overline{G}$ high; $\overline{G}$ is tested with G low.

A. $C_L$ includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. Enable G is tested with $\overline{G}$ high; $\overline{G}$ is tested with G low.

**Figure 6-3. $t_{PHZ}$, $T_{PZH}$, $T_{PLZ}$, and $T_{PZL}$ Load Circuit and Voltage Waveforms**

# 7 Detailed Description

## 7.1 Device Functional Modes

**Table 7-1. Function Table (each receiver)**

| DIFFERENTIAL INPUTS A–B | ENABLES(1) | | OUTPUT Y |
|---|---|---|---|
| | G | $\overline{G}$ | |
| $V_{ID} \geq 0.3$ V | H | X | H |
| | X | L | H |
| $-0.3$ V $< V_{ID} < 0.3$ V | H | X | ? |
| | X | L | ? |
| $V_{ID} \leq -0.3$ V | H | X | L |
| | X | L | L |
| X | L | H | Z |
| Open | H | X | H |
| | X | L | H |

(1) H = high level, L = low level, X = irrelevant, ? = indeterminate, Z = high impedance (off)

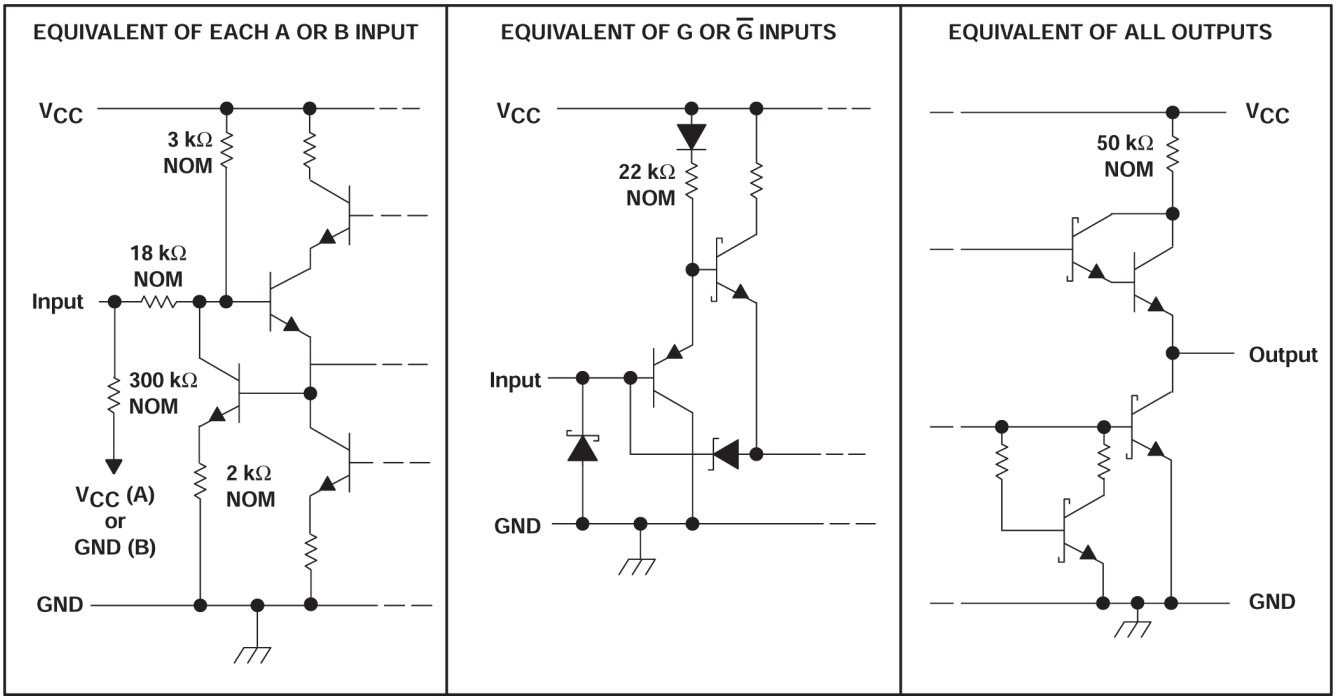



**Figure 7-1. Schematics of Inputs and Outputs**

# 8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

## 8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 8.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 8.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

## 8.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 8.5 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

# 9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision B (May 1995) to Revision C (October 2023) | Page |
|---|---|
| • Changed the numbering format for tables, figures, and cross-references throughout the document | 1 |

# 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN75ALS197D | LIFEBUY | SOIC | D | 16 | 40 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 75ALS197 | |
| SN75ALS197DR | ACTIVE | SOIC | D | 16 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 75ALS197 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

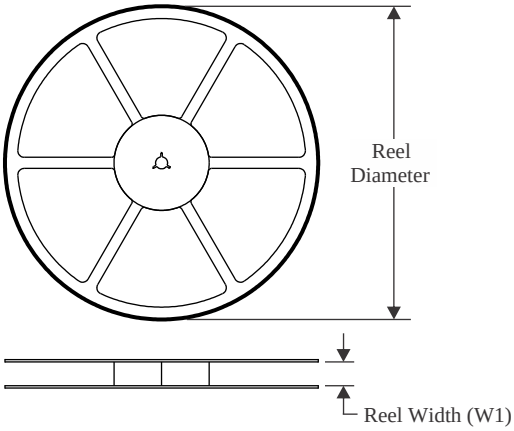
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

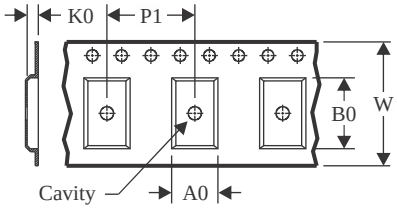
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

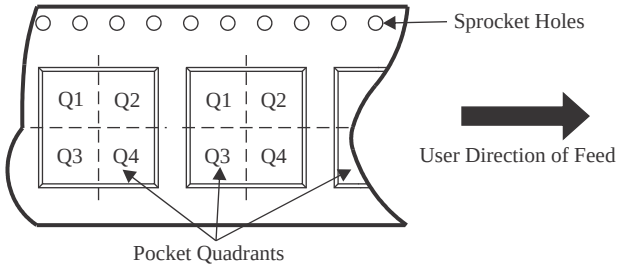



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

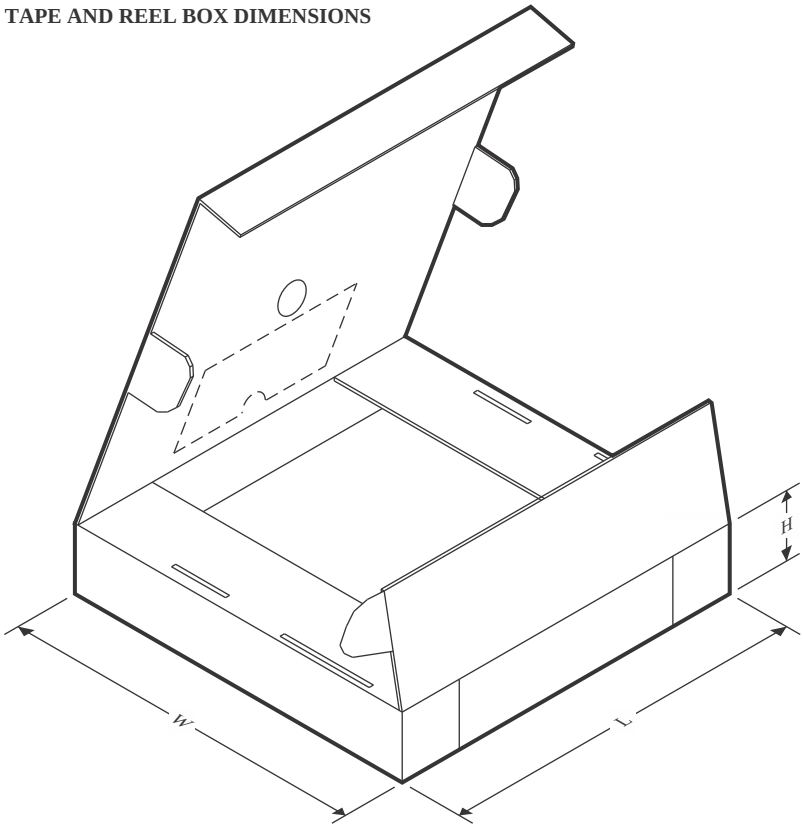
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN75ALS197DR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |

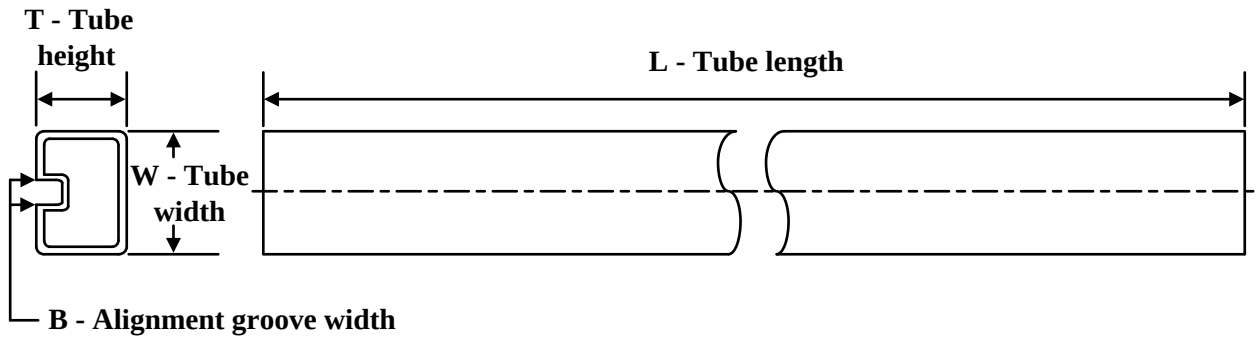
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN75ALS197DR | SOIC | D | 16 | 2500 | 340.5 | 336.1 | 32.0 |

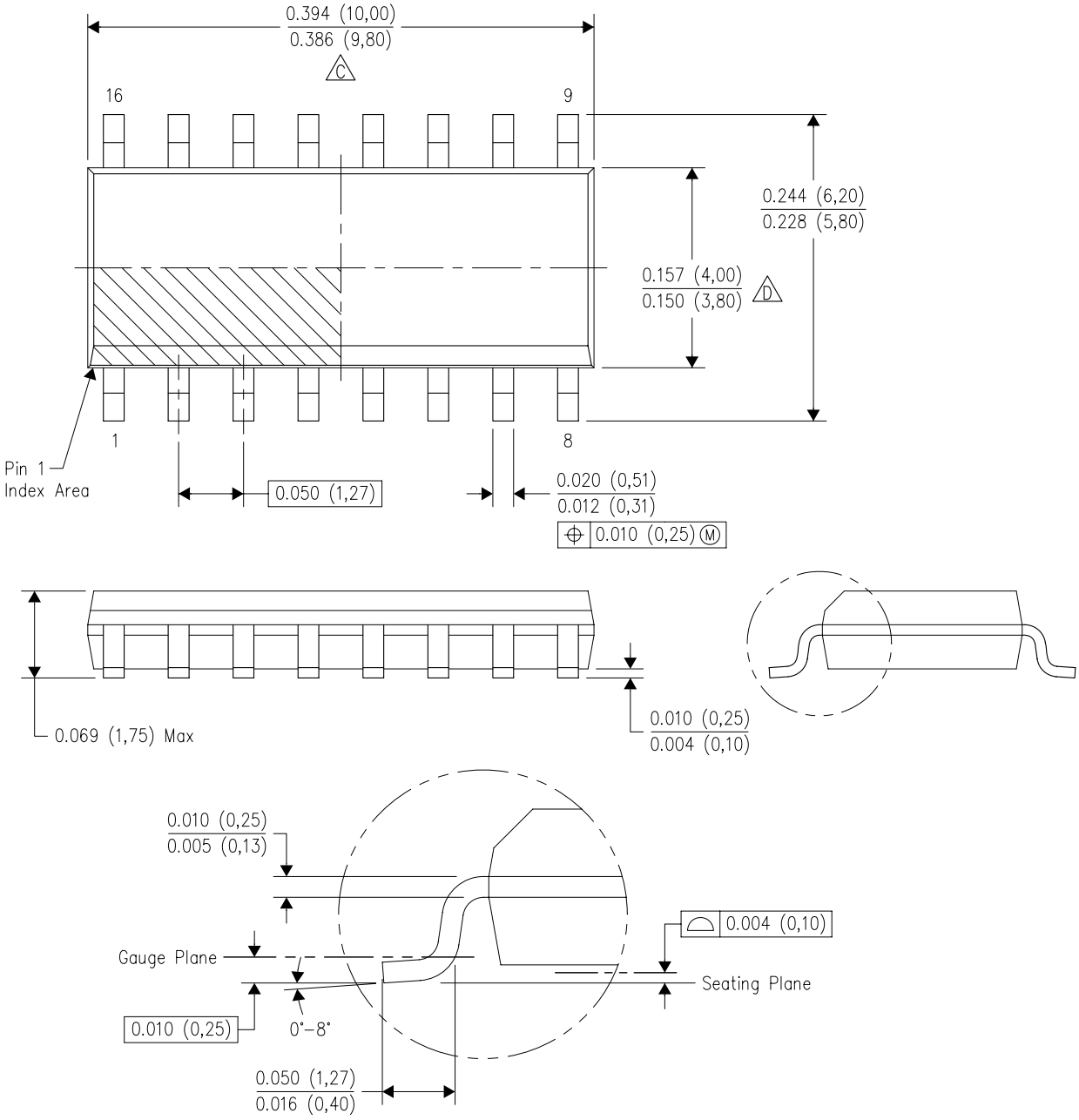
## TUBE




*All dimensions are nominal

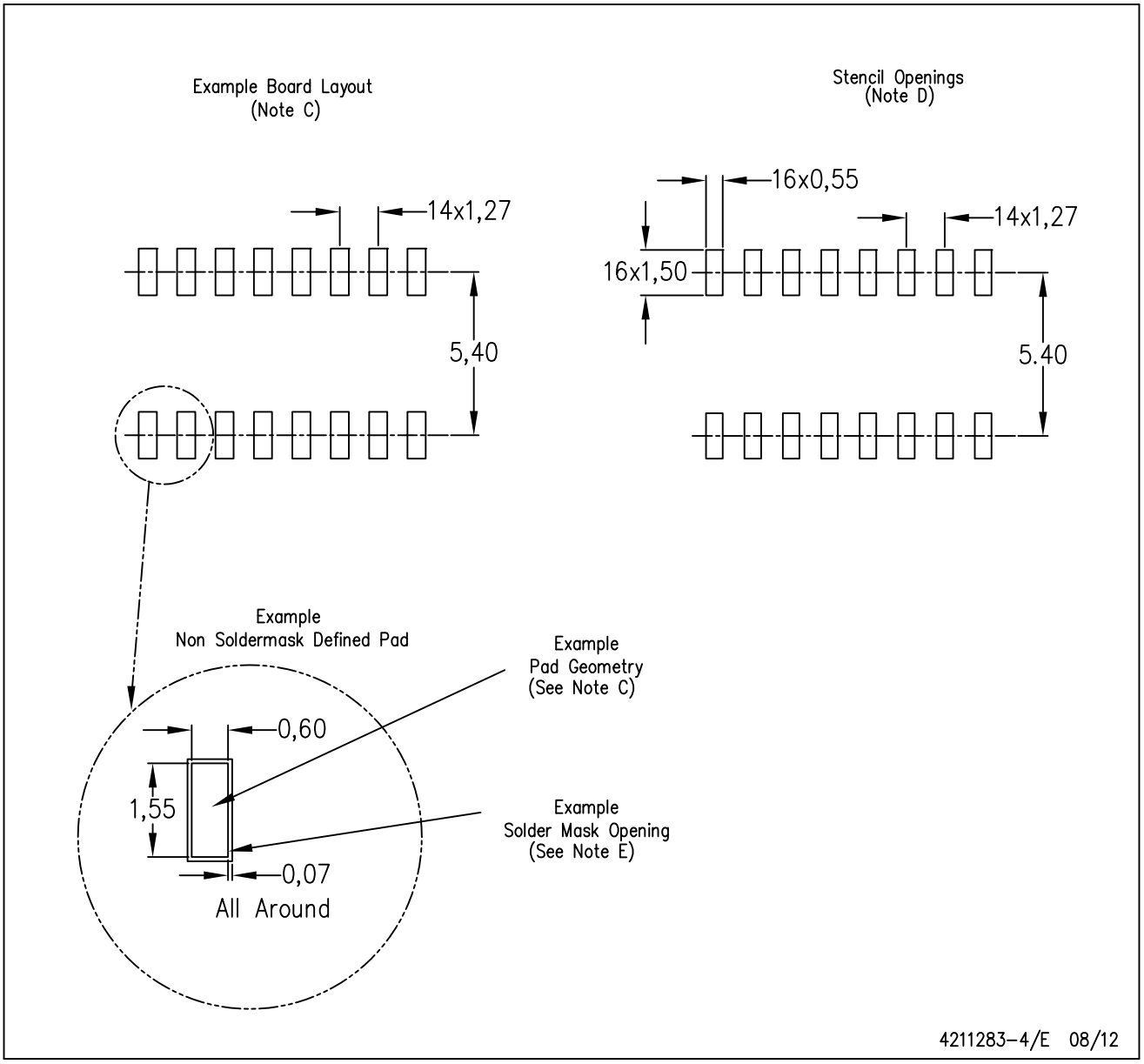
| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| SN75ALS197D | D | SOIC | 16 | 40 | 507 | 8 | 3940 | 4.32 |

D (R–PDSO–G16) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265