3-V to 5.5-V Multichannel RS-232 Line Driver and Receiver with ±15-kV ESD Protection

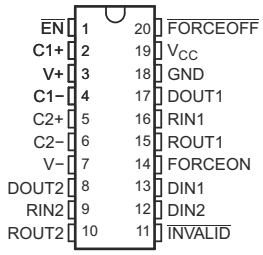
1 Features

- ESD protection for RS-232 bus pins
  - ±15-kV Human-body model (HBM)
  - ±8-kV IEC 61000-4-2, contact discharge
  - ±15-kV IEC 61000-4-2, Air-gap discharge
- Meets or exceeds the requirements of TIA/EIA-232-F and ITU v.28 standards
- Operates with 3-V to 5.5-V V_{CC} supply
- Operates up to 1000 kbit/s
- Two drivers and two receivers
- Low standby current: 1 µA Typical
- External capacitors: 4 × 0.1 µF
- Accepts 5-V logic input with 3.3-V supply

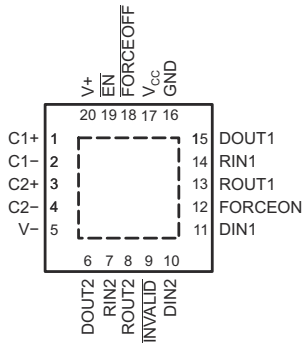
2 Applications

- Battery-powered systems
- PDAs
- Notebooks
- Laptops
- Palmtop PCs
- Hand-held equipment

DB, DW, OR PW PACKAGE
(TOP VIEW)



RGW PACKAGE
(TOP VIEW)



3 Description

The TRSF3223E consists of two line drivers, two line receivers, and a dual charge-pump circuit with ±15-kV ESD protection pin to pin (serial-port connection pins, including GND). This device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. The TRSF3223E operates at typical data signaling rates up to 1000 kbits.

Flexible control options for power management are available when the serial port is inactive. The auto-powerdown feature functions when FORCEON is low and $\overline{\text{FORCEOFF}}$ is high. During this mode of operation, if the device does not sense a valid RS-232 signal, the driver outputs are disabled. If $\overline{\text{FORCEOFF}}$ is set low and EN is high, both drivers and receivers are shut off, and the supply current is reduced to 1 mA. Disconnecting the serial port or turning off the peripheral drivers causes auto-powerdown to occur. Auto-powerdown can be disabled when FORCEON and $\overline{\text{FORCEOFF}}$ are high. With auto-powerdown enabled, the device is automatically activated when a valid signal is applied to any receiver input. The $\overline{\text{INVALID}}$ output is used to notify the user if an RS-232 signal is present at any receiver input. $\overline{\text{INVALID}}$ is high (valid data) if any receiver input voltage is greater than 2.7 V or less than –2.7 V, or has been between –0.3 V and 0.3 V for less than 30 µs. $\overline{\text{INVALID}}$ is low (invalid data) if the receiver input voltage is between –0.3 V and 0.3 V for more than 30 µs. Refer to Figure 5-4 for receiver input levels.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TRSF3223E	SOIC (DW, 20)	12.8 mm × 10.3 mm
	SSOP (DB, 20)	7.2 mm × 7.8 mm
	TSSOP (PW, 20)	6.5 mm x 6.4 mm
	VQFN (RGW, 20)	5 mm x 5mm

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

Table of Contents

4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.3	6	V
V+	Positive-output supply voltage range(2)		–0.3	7	V
V–	Negative-output supply voltage range(2)		0.3	–7	V
V+ – V–	Supply voltage difference(2)			13	V
V_I	Input voltage range	Driver ($\overline{\text{FORCEOFF}}$, FORCEON, $\overline{\text{EN}}$)	–0.3	6	V
		Receiver	–25	25	
V_O	Output voltage range	Driver	–13.2	13.2	V
		Receiver ($\overline{\text{INVALID}}$)	–0.3	V_{CC} + 0.3	
T_J	Operating virtual junction temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network GND.

4.2 Recommended Operating Conditions

See Figure 7-1 and (1)

				MIN	NOM	MAX	UNIT
	Supply voltage		V_{CC} = 3.3 V	3	3.3	3.6	V
			V_{CC} = 5 V	4.5	5	5.5	
V_{IH}	Driver and control high-level input voltage	DIN, $\overline{\text{EN}}$, $\overline{\text{FORCEOFF}}$, FORCEON	V_{CC} = 3.3 V	2			V
			V_{CC} = 5 V	2.4			
V_{IL}	Driver and control low-level input voltage	DIN, $\overline{\text{EN}}$, $\overline{\text{FORCEOFF}}$, FORCEON				0.8	V
V_I	Driver and control input voltage	DIN, $\overline{\text{EN}}$, $\overline{\text{FORCEOFF}}$, FORCEON		0		5.5	V
	Receiver input voltage			–25		25	
T_A	Operating free-air temperature		TRSF3223EC	0		70	°C
			TRSF3223EI	–40		85	

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.

4.3 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	All pins except RIN1, RIN2, DOUT1 and DOUT2 pins	±3000	V
			RIN1, RIN2, DOUT1 and DOUT2 pins to GND	±15000	
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	All pins	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

4.4 ESD Ratings - IEC Specifications

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 Contact Discharge (1)	RIN1, RIN2, DOUT1 and DOUT2 pins	±8,000	V
		IEC 61000-4-2 Air-gap Discharge (1)		±15,000	

(1) A minimum of 1-µF capacitor between V_{CC} and GND is required to meet the specified IEC 61000-4-2 rating.

4.5 Thermal Information

THERMAL METRIC(1)		DB (SOIC)	DW (SOIC)	PW (TSSOP)	RGW (VQFN)	UNIT
		20 PINS	20 PINS	20 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	76.2	76.8	89.7	32.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	36.8	39.6	29.0	23.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	33.9	41.5	41.9	11.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.7	12.6	1.9	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	33.6	40.9	41.3	11.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	2.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

4.6 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS(1)	MIN	TYP(2)	MAX	UNIT
I_I	Input leakage current	$\overline{EN}$, $\overline{FORCEOFF}$, FORCEON			±0.01	±1	µA
I_{CC}	Supply current	Auto-powerdown disabled	V_{CC} = 3.3 V or 5 V, T_A = 25°C, No load, $\overline{FORCEOFF}$ and FORCEON at V_{CC}		0.3	1.3	mA
		Powered off	No load, $\overline{FORCEOFF}$ at GND		1	10	µA
		Auto-powerdown enabled	No load, $\overline{FORCEOFF}$ at V_{CC}, FORCEON at GND, All RIN are open or grounded		1	10	

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

4.7 Electrical Characteristics, Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)	MIN	TYP(2)	MAX	UNIT
V_{OH}	High-level output voltage	DOUT at R_L = 3 kΩ to GND	5	5.4		V
V_{OL}	Low-level output voltage	DOUT at R_L = 3 kΩ to GND	–5	–5.4		V
I_{IH}	High-level input current	$V_I = V_{CC}$		±0.01	±1	μA
I_{IL}	Low-level input current	V_I at GND		±0.01	±1	μA
I_{OS}	Short-circuit output current(3)	V_{CC} = 3.6 V, V_O = 0 V		±35	±60	mA
		V_{CC} = 5.5 V, V_O = 0 V				
r_o	Output resistance	V_{CC}, V+, and V– = 0 V, V_O = ±2 V	300	10M		Ω
I_{OZ}	Output leakage current	$\overline{\text{FORCEOFF}}$ = GND, V_{CC} = 3 V to 3.6 V, V_O = ±12 V			±25	μA
		$\overline{\text{FORCEOFF}}$ = GND, V_{CC} = 4.5 V to 5.5 V, V_O = ±12 V			±25	

(1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(3) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

4.8 Switching Characteristics, Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)			MIN	TYP(2)	MAX	UNIT
	Maximum data rate (seeFigure 5-1)	R_L = 3 kΩ, One DOUT switching	C_L = 1000 pF		250			kbit/s
			C_L = 250 pF,	V_{CC} = 3 V to 4.5 V	1000			
			C_L = 1000 pF,	V_{CC} = 4.5 V to 5.5 V	1000			
$t_{sk(p)}$	Pulse skew(3)	C_L = 150 pF to 2500 pF,	R_L = 3 kΩ to 7 kΩ,	See Figure 5-2		300		ns
SR(tr)	Slew rate, transition region (see Figure 5-1)	R_L = 7 kΩ,	C_L = 150 pF to 1000 pF		8		90	V/μs
		R_L = 3 kΩ	C_L = 1000 pF		12		60	
			C_L = 150 pF to 250 pF		24		150	

(1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(3) Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.

4.9 Electrical Characteristics, Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)	MIN	TYP(2)	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –1 mA	V_{CC} – 0.6	V_{CC} – 0.1		V
V_{OL}	Low-level output voltage	I_{OL} = 1.6 mA			0.4	V
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 3.3 V		1.6	2.4	V
		V_{CC} = 5 V		1.9	2.4	
$V_{IT–}$	Negative-going input threshold voltage	V_{CC} = 3.3 V	0.6	1.1		V
		V_{CC} = 5 V	0.6	1.4		
V_{hys}	Input hysteresis (V_{IT+} – $V_{IT–}$)			0.5		V
I_{OZ}	Output leakage current	$\overline{EN}$ = V_{CC}		±0.05		µA
r_i	Input resistance	V_I = ±3 V to ±25 V	3	5		kΩ

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

4.10 Switching Characteristics, Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)	TYP(2)	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 150 pF, See Figure 5-3	150	ns
t_{PHL}	Propagation delay time, high- to low-level output	C_L = 150 pF, See Figure 5-3	150	ns
t_{en}	Output enable time	C_L = 150 pF, R_L = 3 kΩ, See Figure 5-4	200	ns
t_{dis}	Output disable time	C_L = 150 pF, R_L = 3 kΩ, See Figure 5-4	200	ns
$t_{sk(p)}$	Pulse skew(3)	See Figure 5-3	50	ns

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(3) Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.

4.11 Electrical Characteristics, Auto-Powerdown

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5-5)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
$V_{T+(valid)}$	Receiver input threshold for $\overline{INVALID}$ high-level output voltage	FORCEON = GND,	$\overline{FORCEOFF}$ = V_{CC}		2.7	V
$V_{T-(valid)}$	Receiver input threshold for $\overline{INVALID}$ high-level output voltage	FORCEON = GND,	$\overline{FORCEOFF}$ = V_{CC}	–2.7		V
$V_{T(invalid)}$	Receiver input threshold for $\overline{INVALID}$ low-level output voltage	FORCEON = GND,	$\overline{FORCEOFF}$ = V_{CC}	–0.3	0.3	V
V_{OH}	$\overline{INVALID}$ high-level output voltage	I_{OH} = 1 mA, $\overline{FORCEOFF}$ = V_{CC}	FORCEON = GND,	V_{CC} – 0.6		V
V_{OL}	$\overline{INVALID}$ low-level output voltage	I_{OL} = 1.6 mA, $\overline{FORCEOFF}$ = V_{CC}	FORCEON = GND,		0.4	V

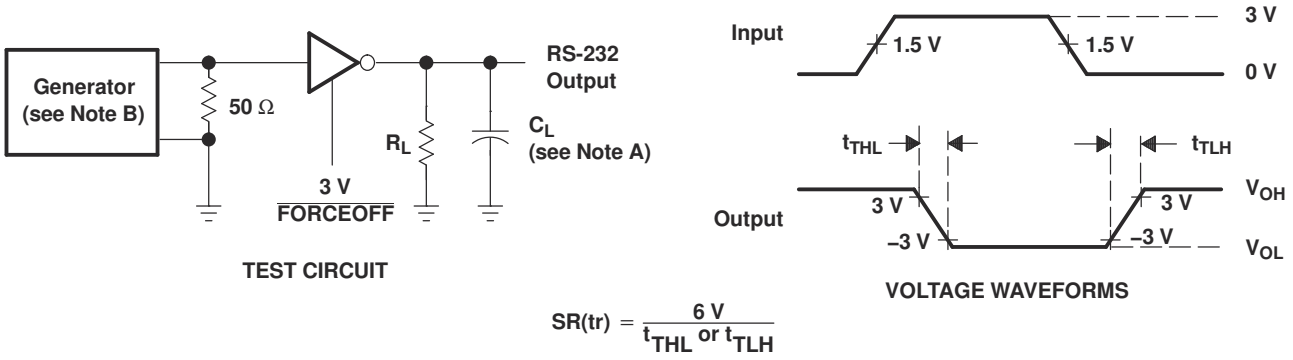
4.12 Switching Characteristics, Auto-Powerdown

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5-5)

PARAMETER		TYP(1)	UNIT
t_{valid}	Propagation delay time, low- to high-level output	1	µs
$t_{invalid}$	Propagation delay time, high- to low-level output	30	µs
t_{en}	Supply enable time	100	µs

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

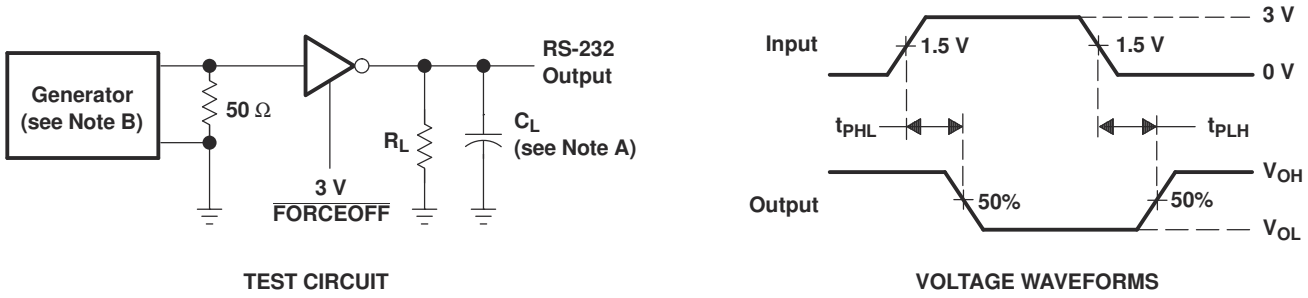
5 Parameter Measurement Information



A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 250 kbit/s, Z_O = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.

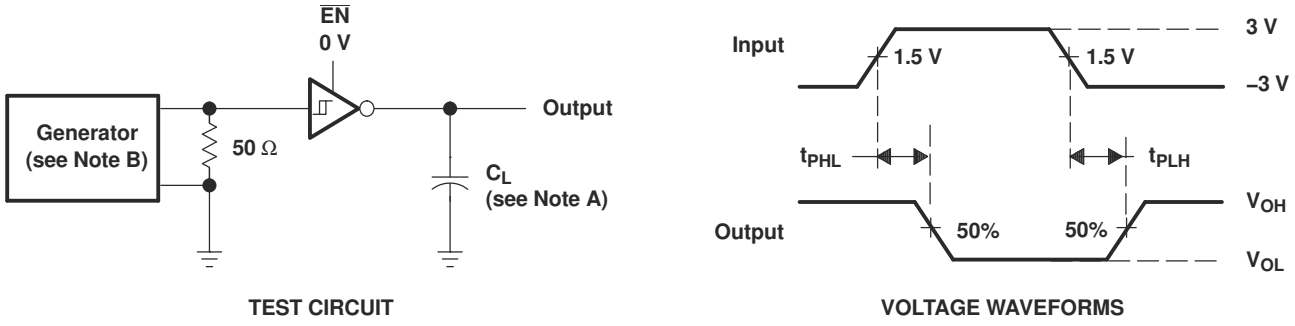
Figure 5-1. Driver Slew Rate



A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 250 kbit/s, Z_O = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.

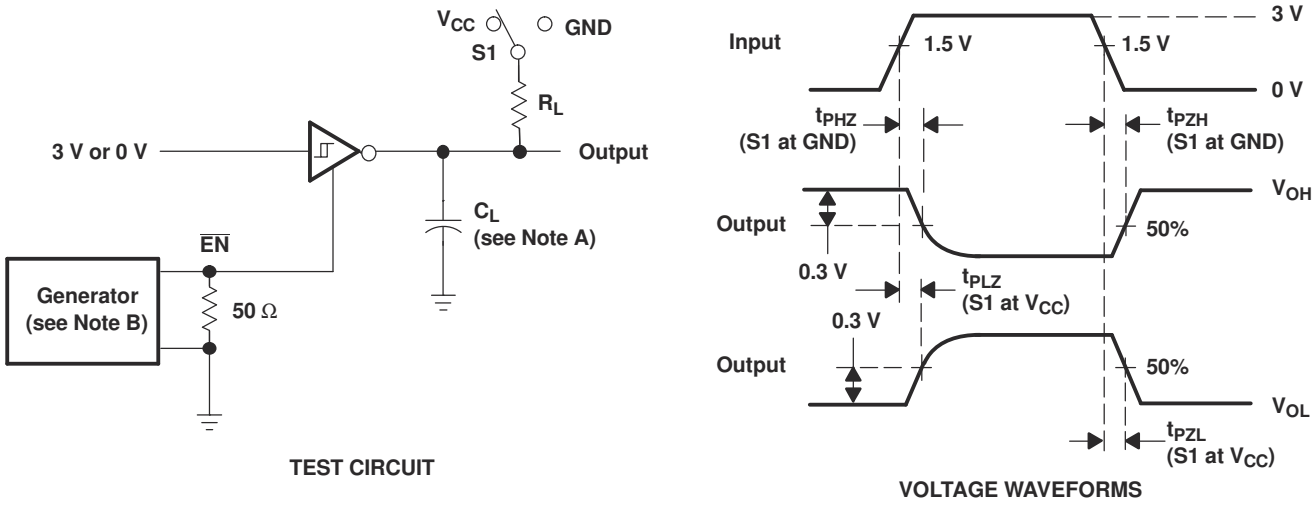
Figure 5-2. Driver Pulse Skew



A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.

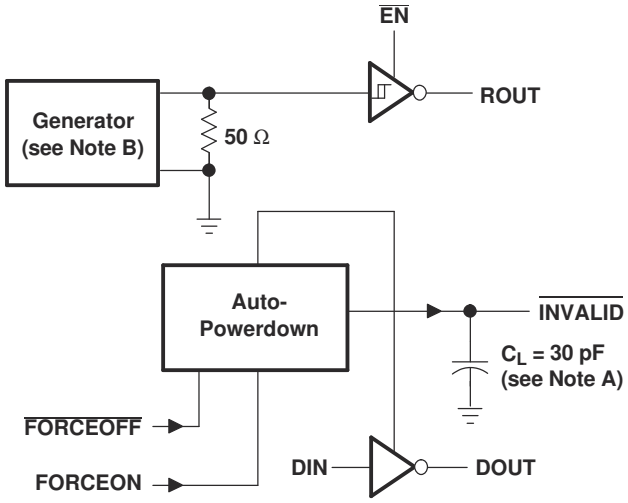
Figure 5-3. Receiver Propagation Delay Times



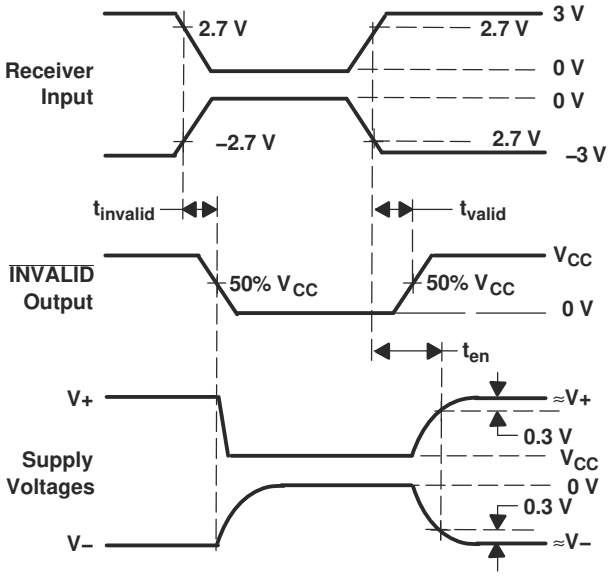
A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.

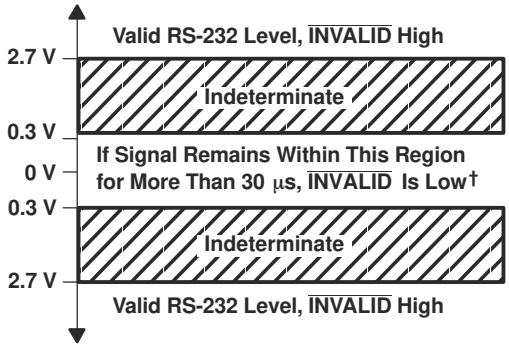
Figure 5-4. Receiver Enable and Disable Times



TEST CIRCUIT



VOLTAGE WAVEFORMS



† Auto-powerdown disables drivers and reduces supply current to 1 μA

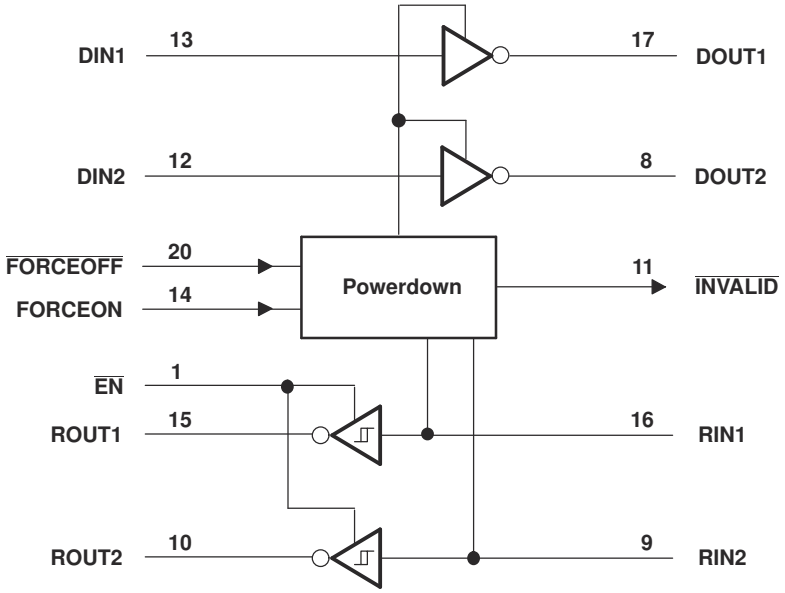
A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 250 kbit/s, Z_O = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.

Figure 5-5. $\overline{\text{INVALID}}$ Propagation Delay Times and Supply Enabling Time

6 Detailed Description

6.1 Functional Block Diagram



Pin numbers are for the DB, DW, and PW packages.

Figure 6-1. Logic Diagram (Positive Logic)

6.2 Device Functional Modes

Function Tables (Each Driver)

INPUTS(1)				OUTPUT DOUT	DRIVER STATUS
DIN	FORCEON	$\overline{\text{FORCEOFF}}$	VALID RIN RS-232 LEVEL		
X	X	L	X	Z	Powered off
L	H	H	X	H	Normal operation with auto-powerdown disabled
H	H	H	X	L	
L	L	H	Yes	H	Normal operation with auto-powerdown enabled
H	L	H	Yes	L	
L	L	H	No	Z	Powered off by auto-powerdown feature
H	L	H	No	Z	

(1) H = high level, L = low level, X = irrelevant, Z = high impedance

Function Tables (Each Receiver)

INPUTS(1)			OUTPUT ROUT
RIN	$\overline{\text{EN}}$	VALID RIN RS-232 LEVEL	
L	L	X	H
H	L	X	L
X	H	X	Z
Open	L	No	H

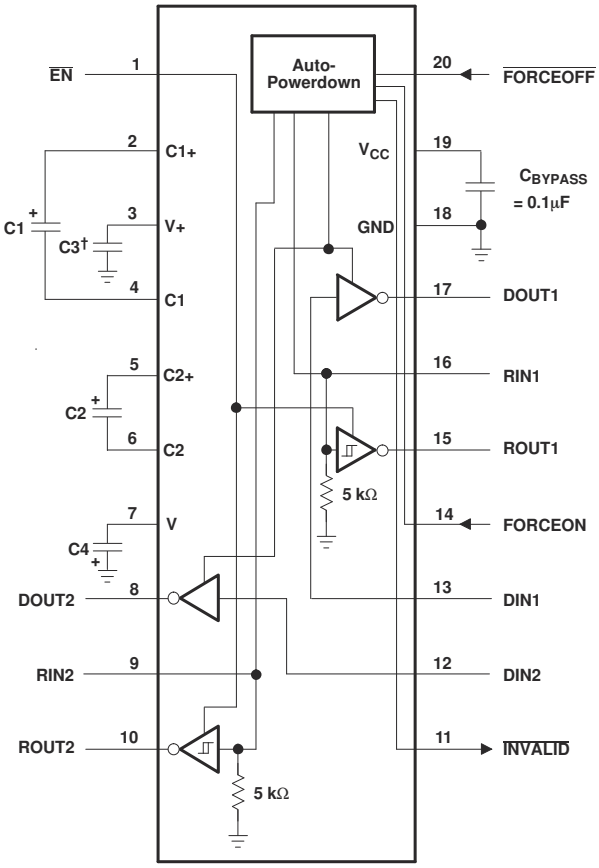
(1) H = high level, L = low level, X = irrelevant,
Z = high impedance (off),
Open = input disconnected or connected driver off

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Typical Application



† C3 can be connected to V_{CC} or GND.

NOTES: A. Resistor values shown are nominal.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

V_{CC} vs CAPACITOR VALUES

V_{CC}	C1	C2, C3, and C4
3.3 V ± 0.3 V	0.1 µF	0.1 µF
5 V ± 0.5 V	0.047 µF	0.33 µF
3 V to 5.5 V	0.1 µF	0.47 µF

Figure 7-1. Typical Operating Circuit and Capacitor Values

7.1.1 Detailed Design Procedure

TRSF3223E has integrated charge-pump that generates positive and negative rails needed for RS-232 signal levels. Main design requirement is that charge-pump capacitor terminals must be connected with recommended capacitor values. Charge-pump rail voltages and device supply pin must be properly bypassed with ceramic capacitors.

8 Device and Documentation Support

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (September 2011) to Revision B (December 2023)	Page
• Changed the numbering format for tables, figures, and cross-references throughout the document	1
• Added the *ESD Ratings* tables	3
• Added the *Thermal Information* table	4
• Changed the I_{CC} Auto-powerdown disabled max value from 1 mA to 1.3 mA in the *Electrical Characteristics*	4

Changes from Revision * (August 2007) to Revision A (September 2011)	Page
• Added the RGW package to the datasheet.	1
• Deleted the RHL package from the datasheet.	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TRSF3223EIDBR	LIFEBUY	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RT23EI	
TRSF3223EIDWR	LIFEBUY	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRSF3223EI	
TRSF3223EIPWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RT23EI	Samples
TRSF3223EIRGWR	ACTIVE	VQFN	RGW	20	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	RT23EI	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

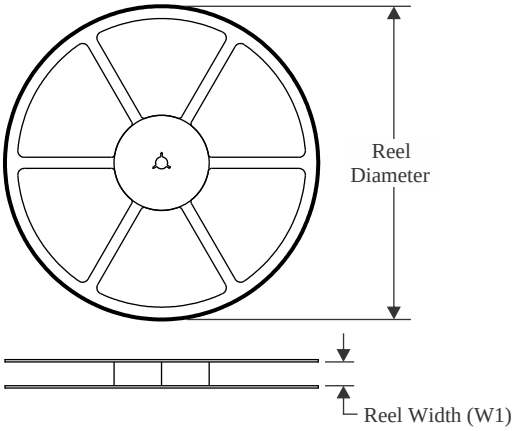
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

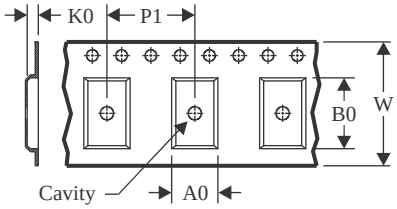
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

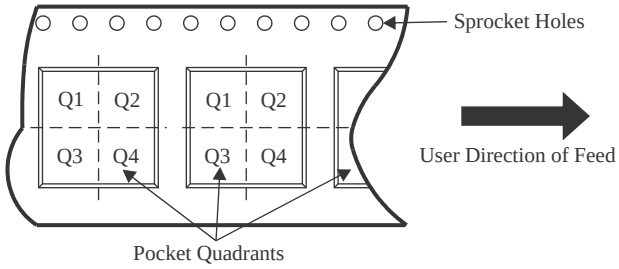


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

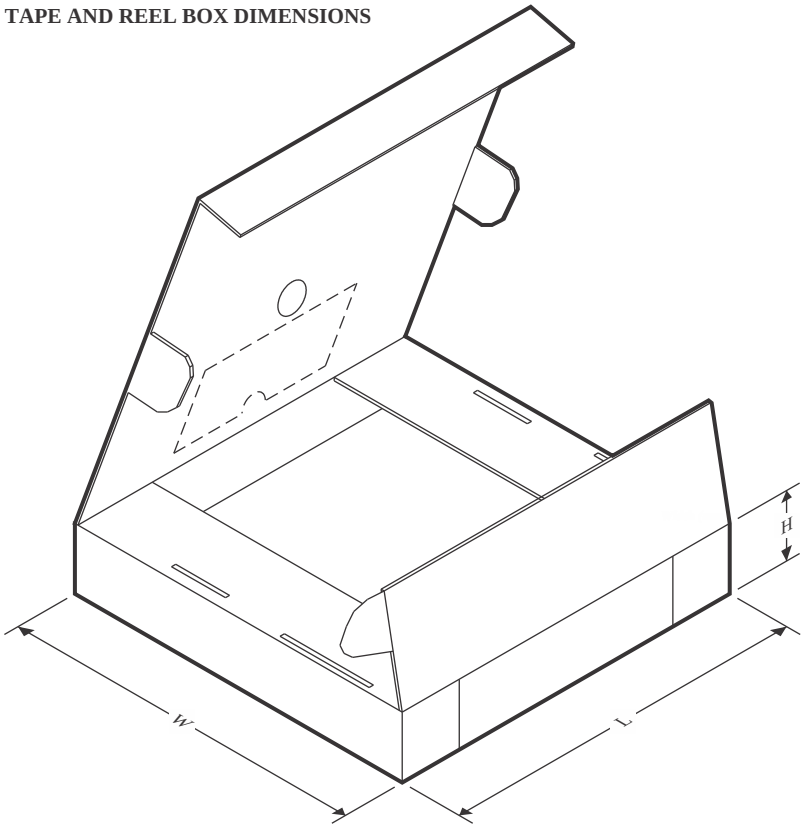
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRSF3223EIDBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
TRSF3223EIDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
TRSF3223EIPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TRSF3223EIRGWR	VQFN	RGW	20	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

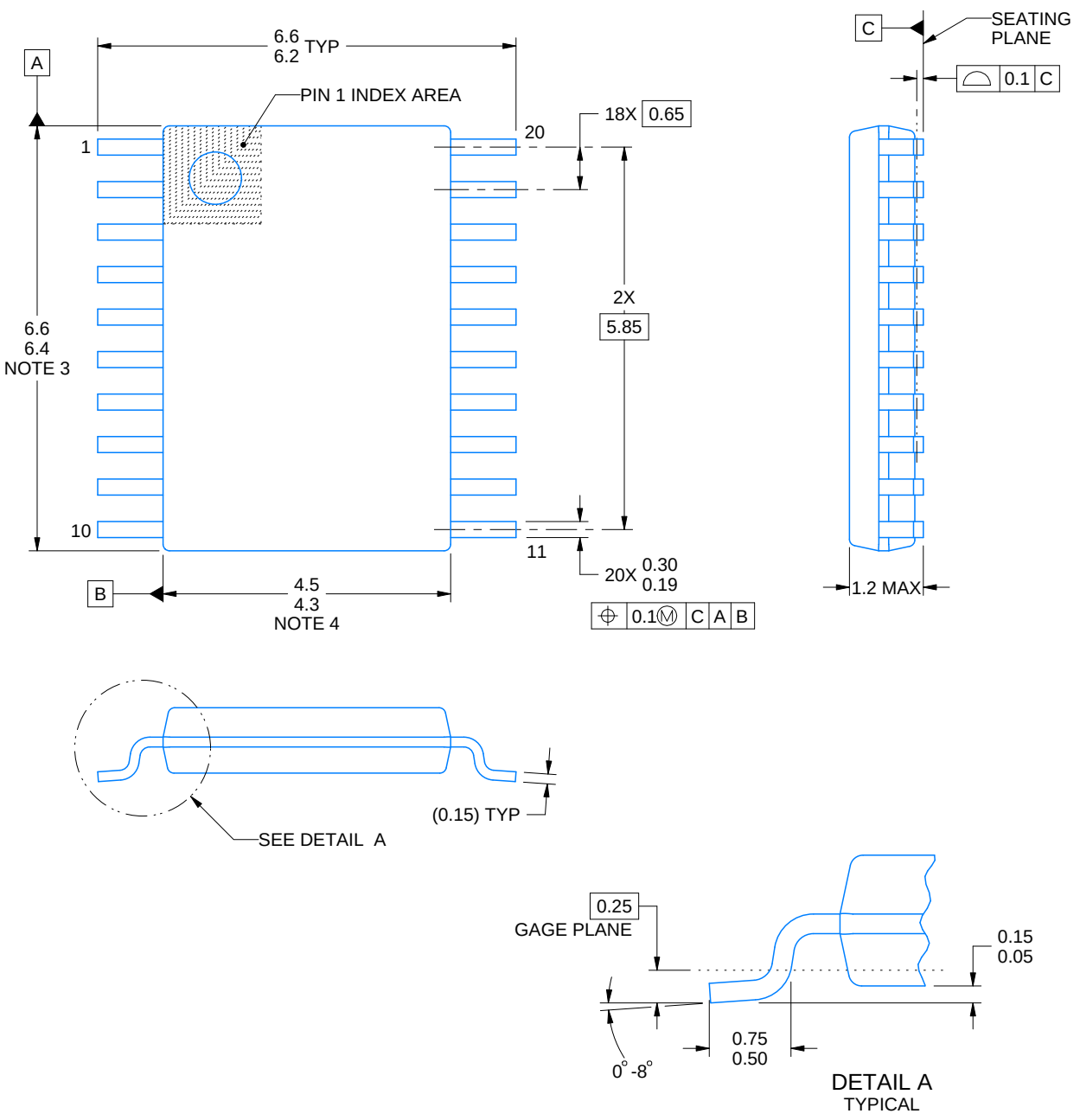
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRSF3223EIDBR	SSOP	DB	20	2000	356.0	356.0	35.0
TRSF3223EIDWR	SOIC	DW	20	2000	367.0	367.0	45.0
TRSF3223EIPWR	TSSOP	PW	20	2000	356.0	356.0	35.0
TRSF3223EIRGWR	VQFN	RGW	20	3000	356.0	356.0	35.0

PACKAGE OUTLINE

PW0020A

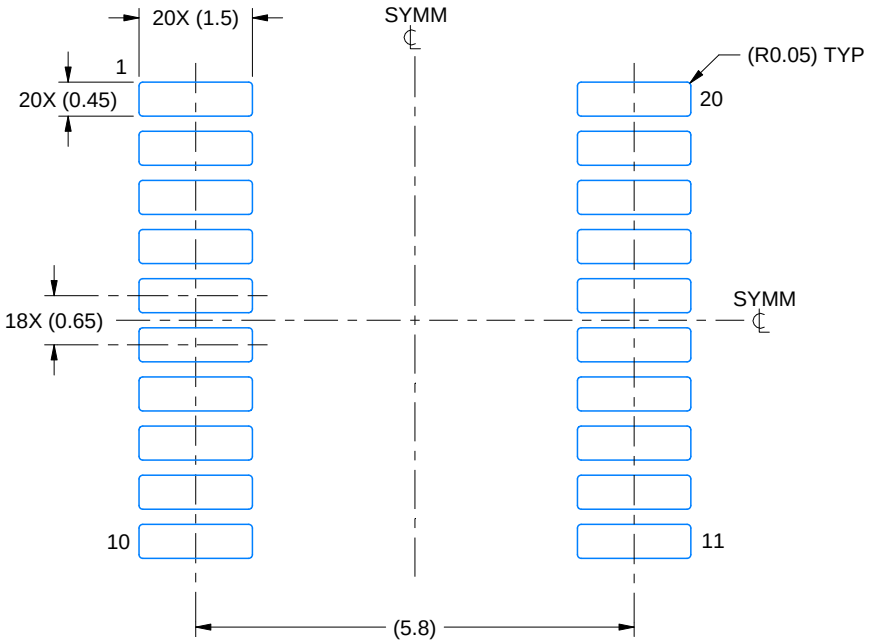
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



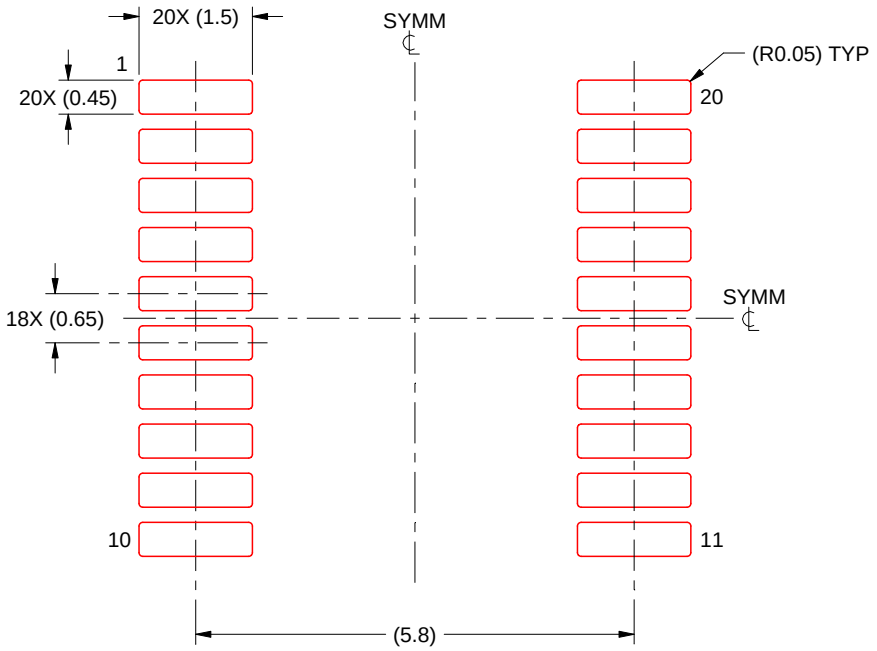
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



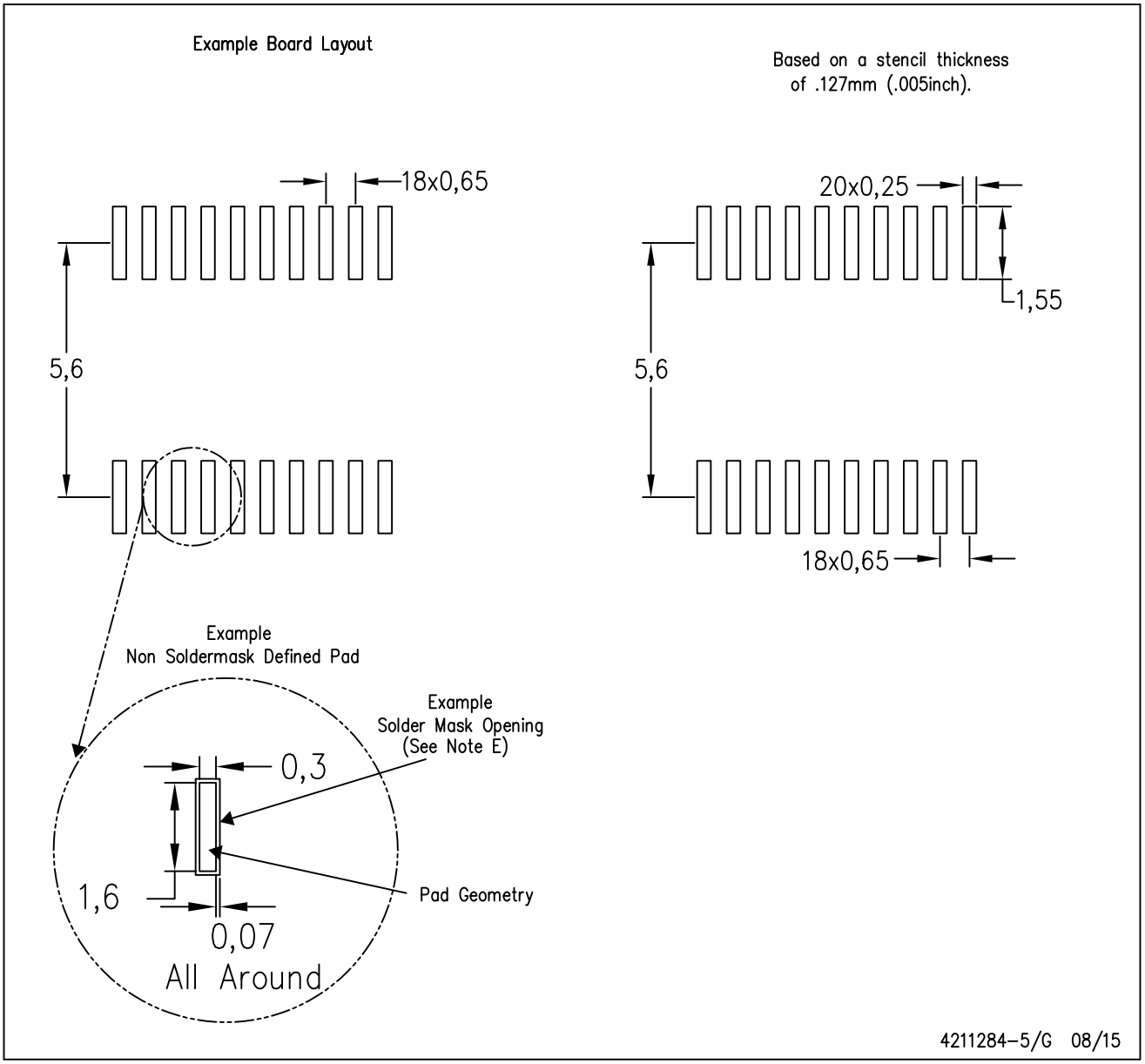
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



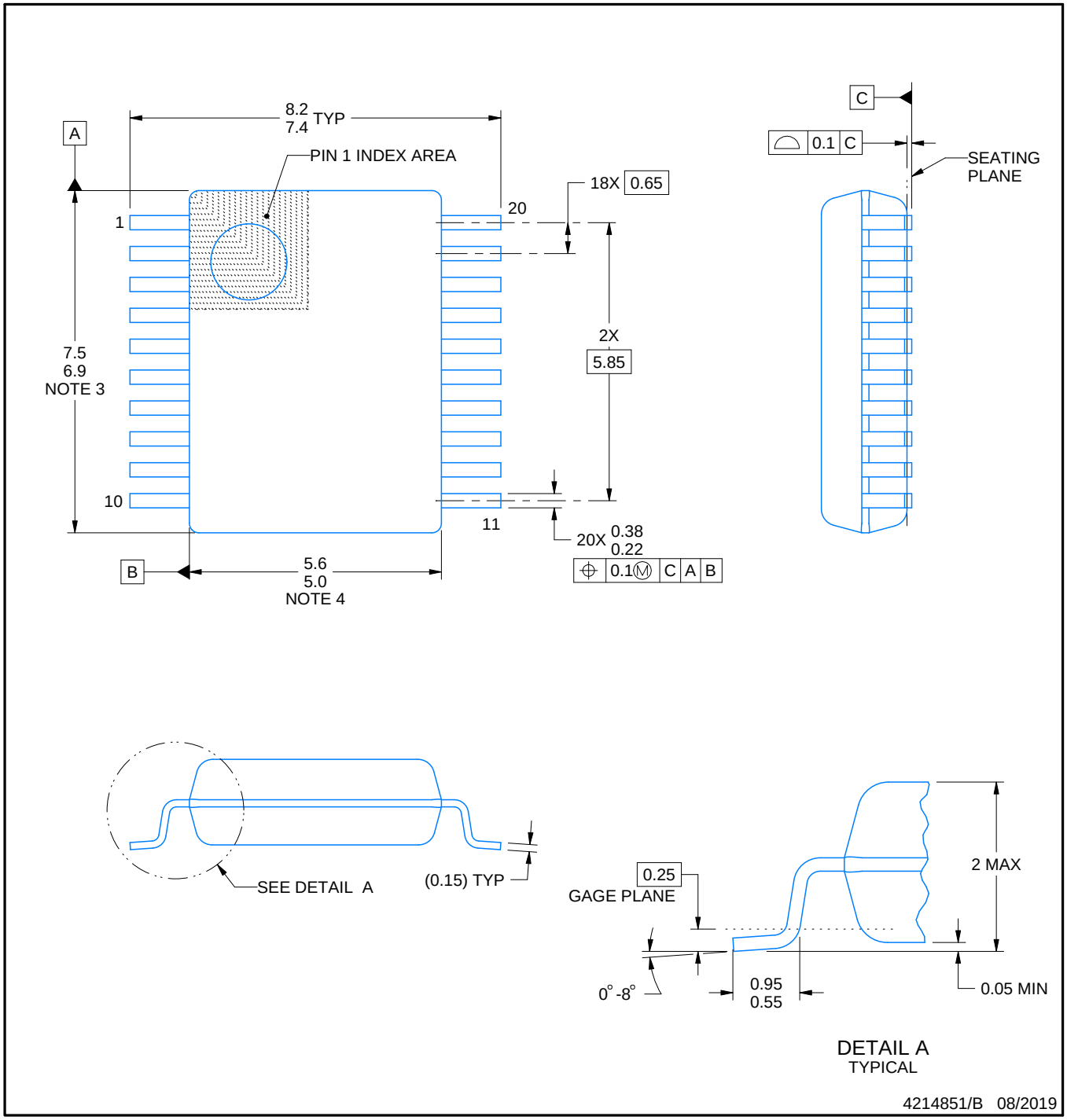
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

DB0020A

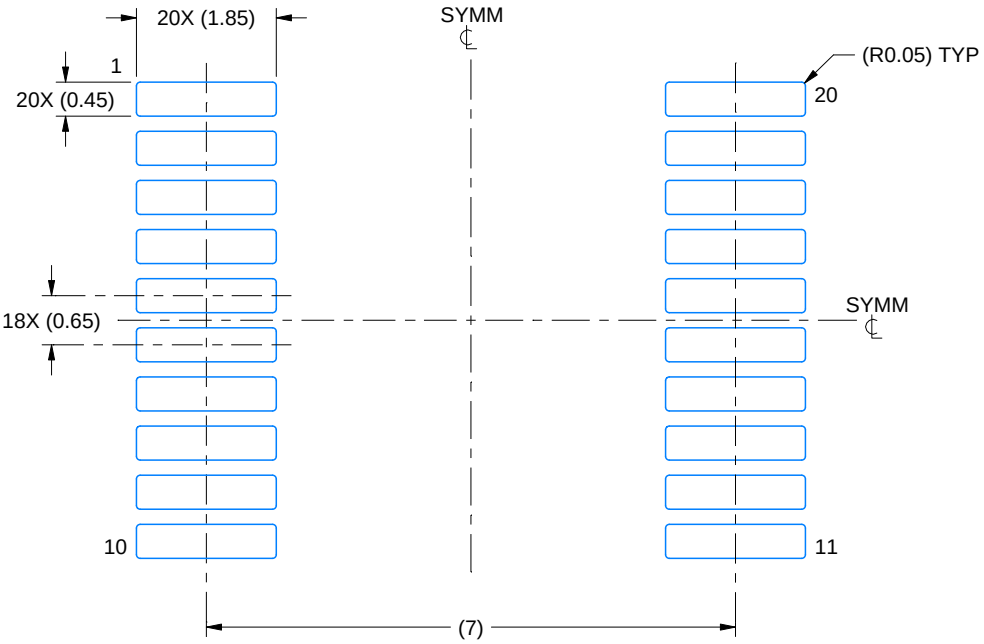
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

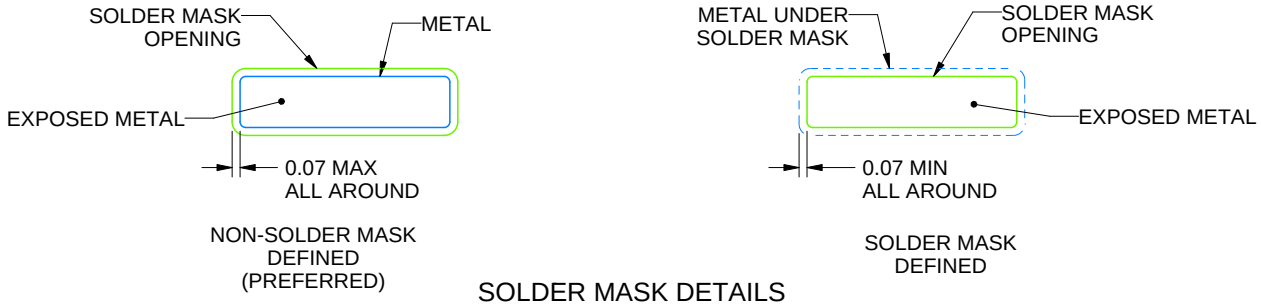


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

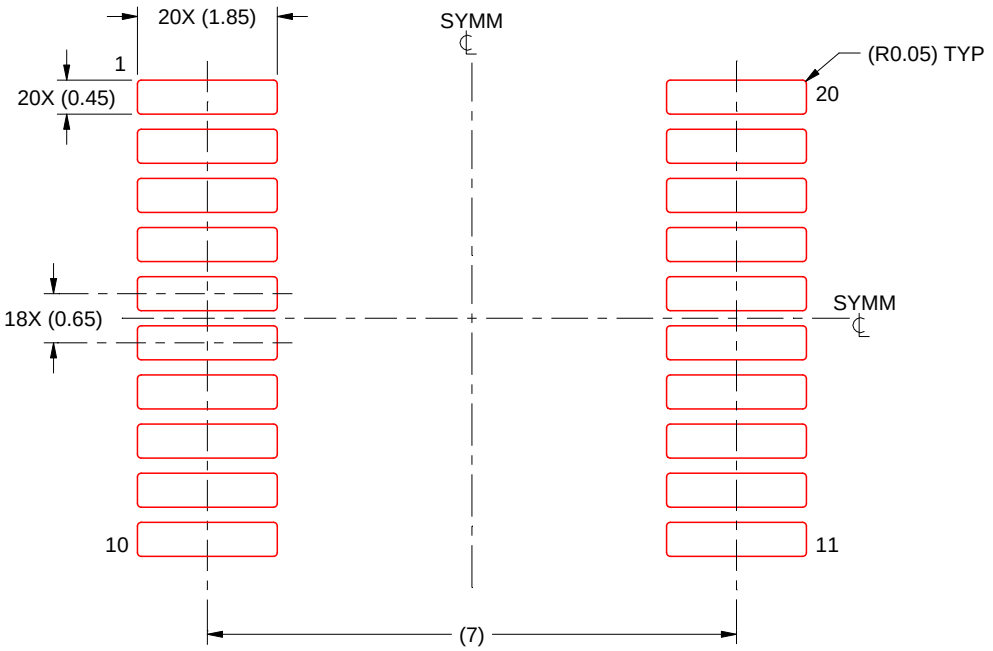
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

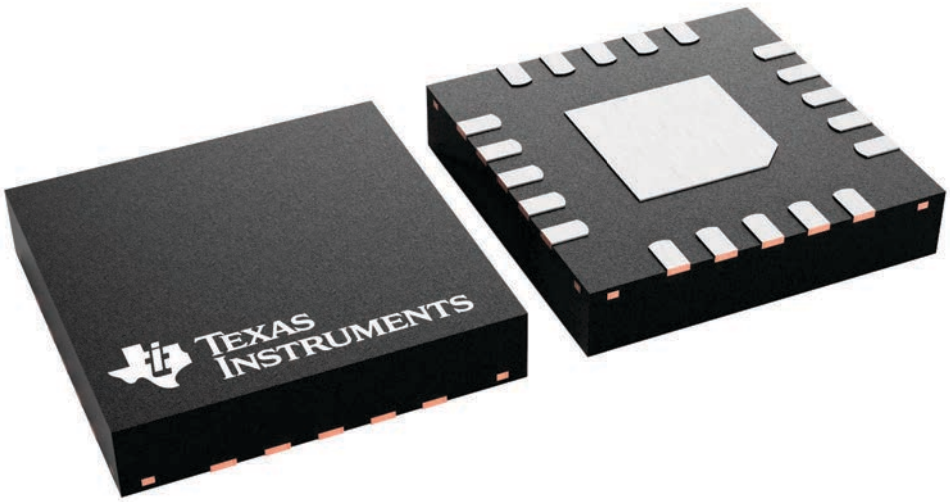
RGW 20

VQFN - 1 mm max height

5 x 5, 0.65 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



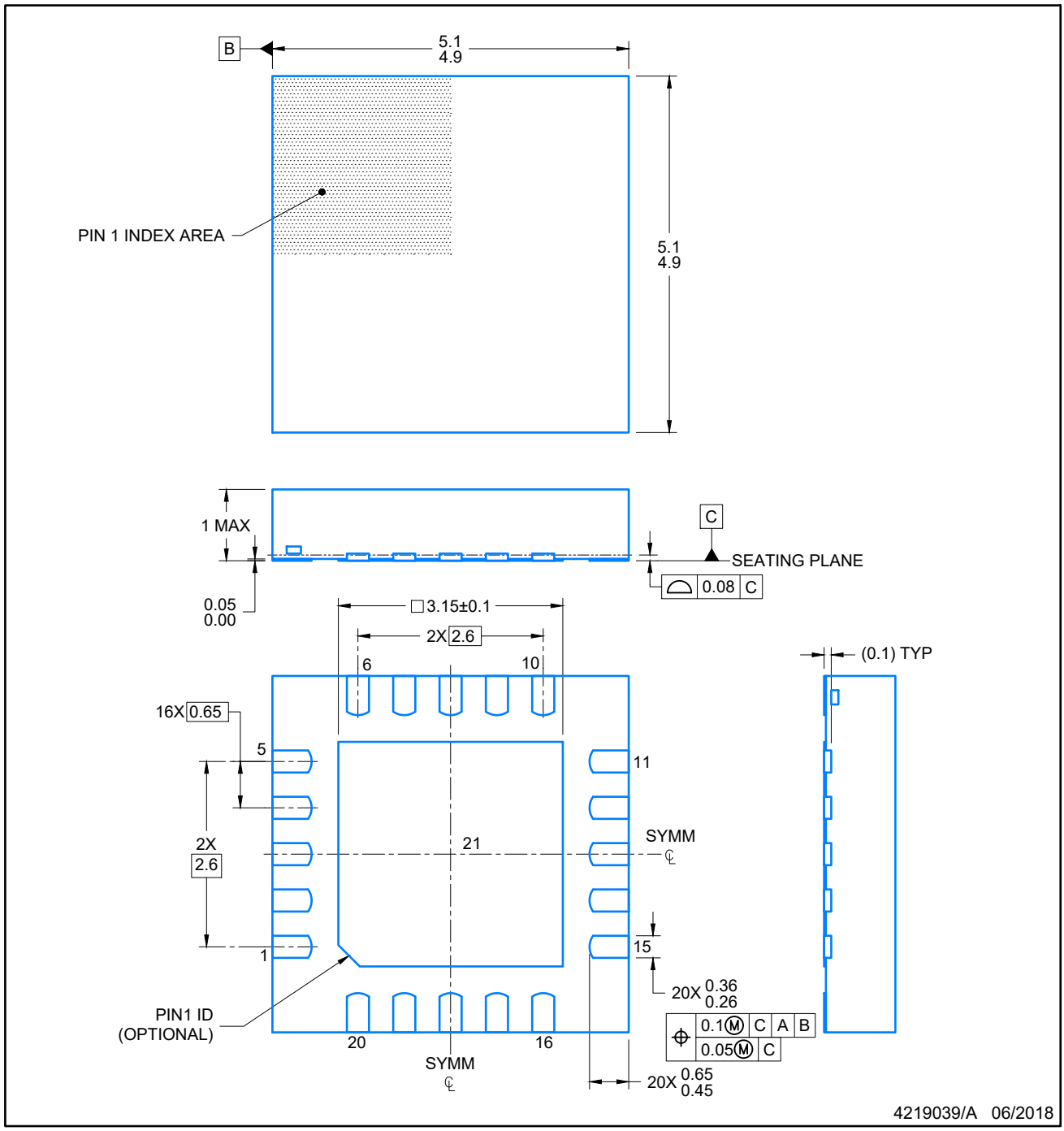
4227157/A

PACKAGE OUTLINE

RGW0020A

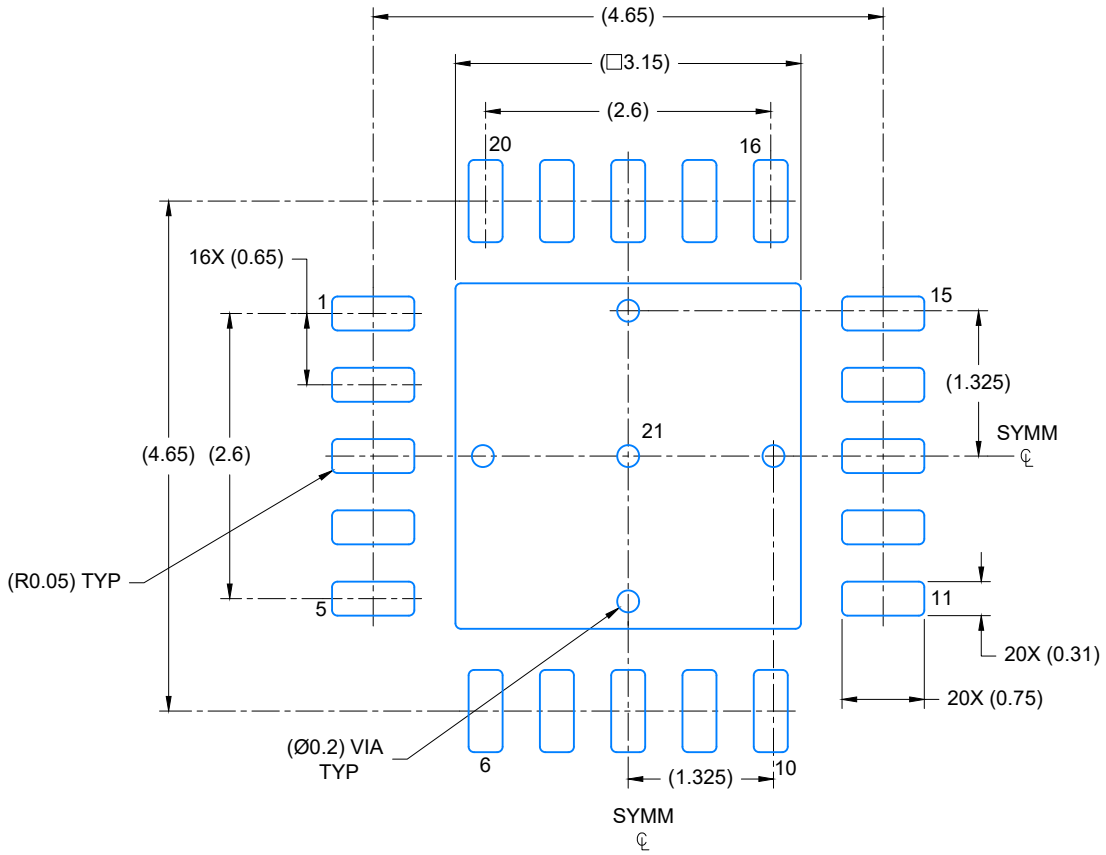
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



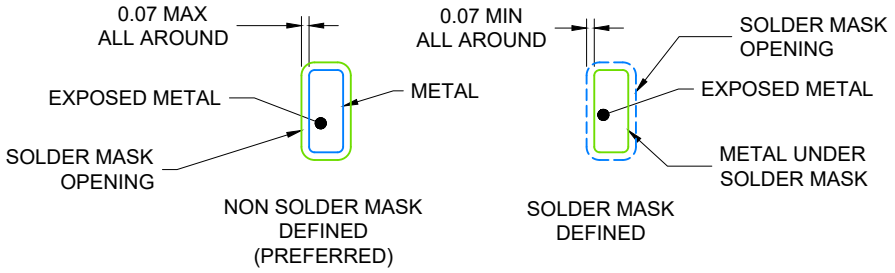
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE

SCALE: 15X

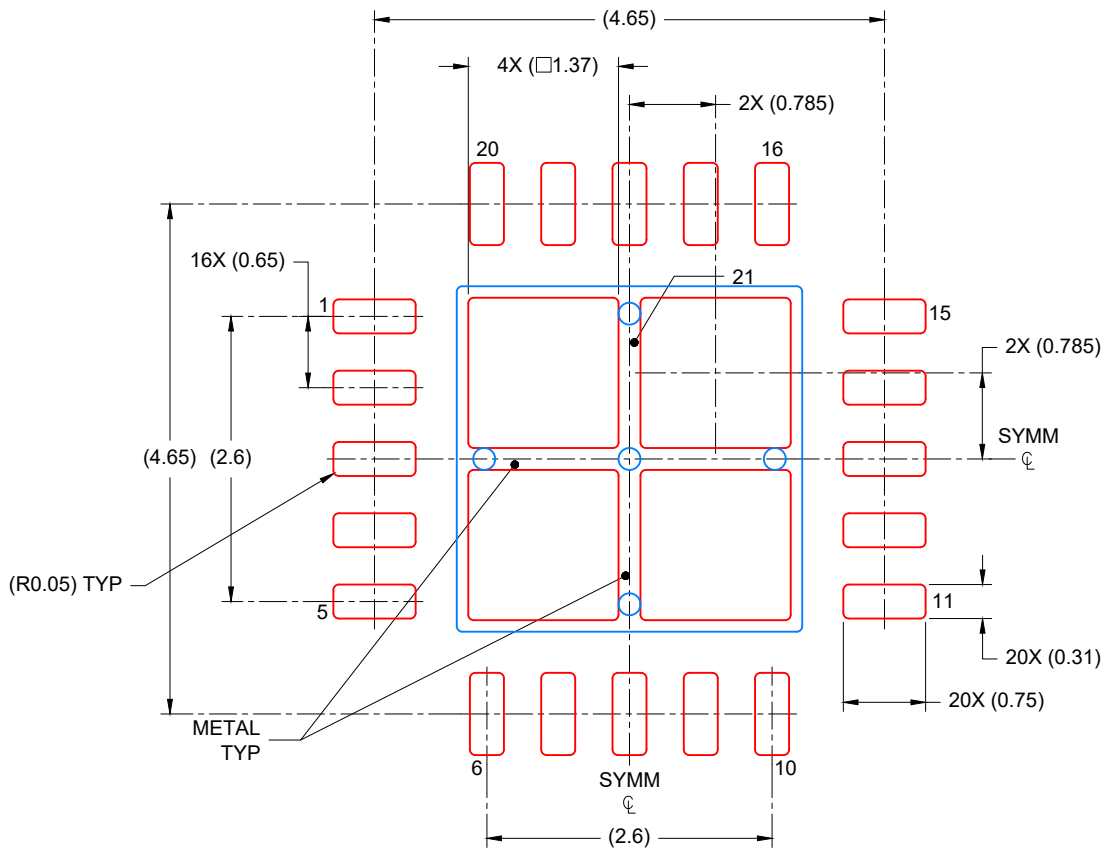


SOLDER MASK DETAILS

4219039/A 06/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



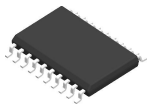
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
75% PRINTED COVERAGE BY AREA
SCALE: 15X

4219039/A 06/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

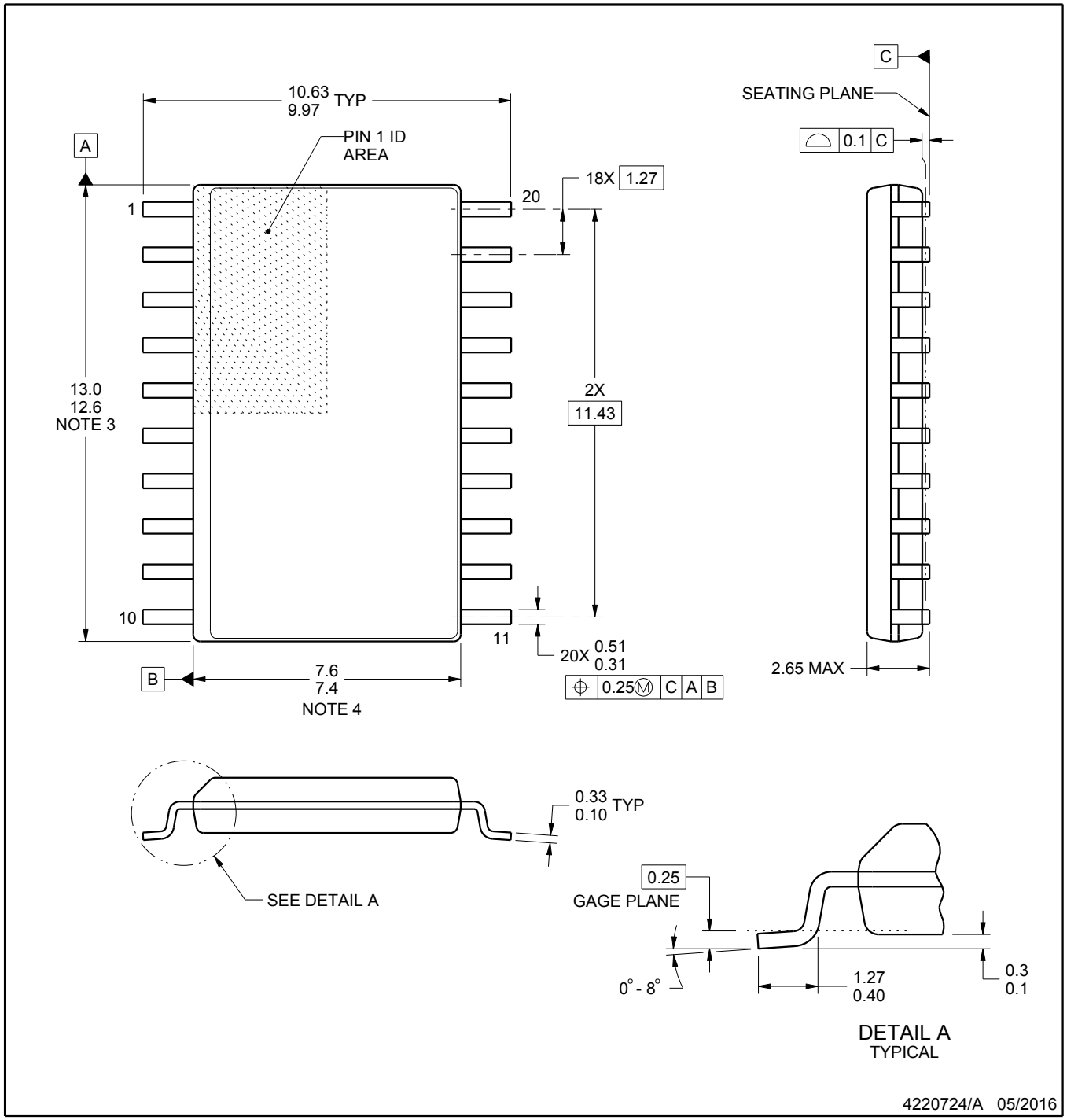


PACKAGE OUTLINE

DW0020A

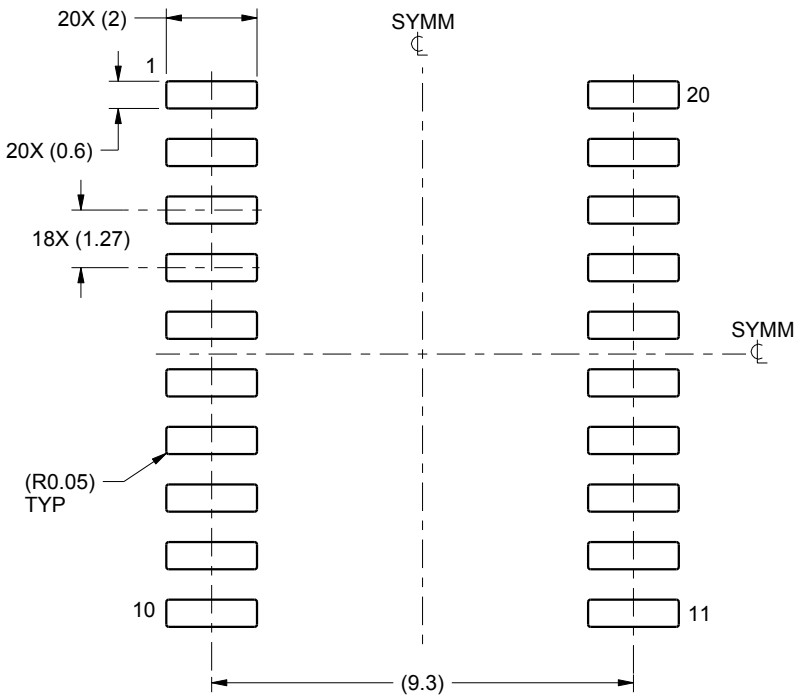
SOIC - 2.65 mm max height

SOIC

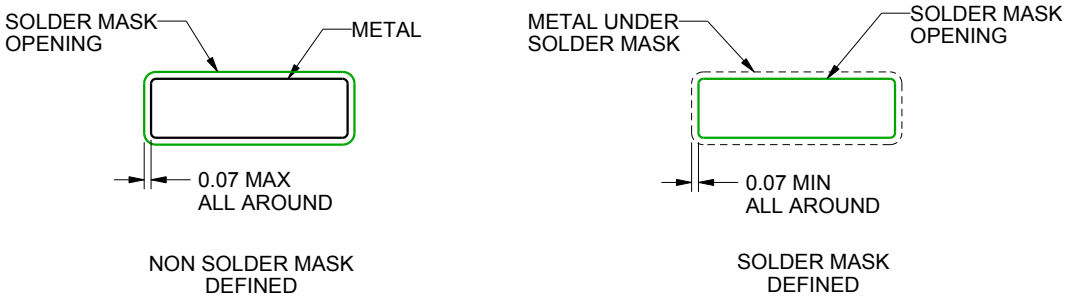


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

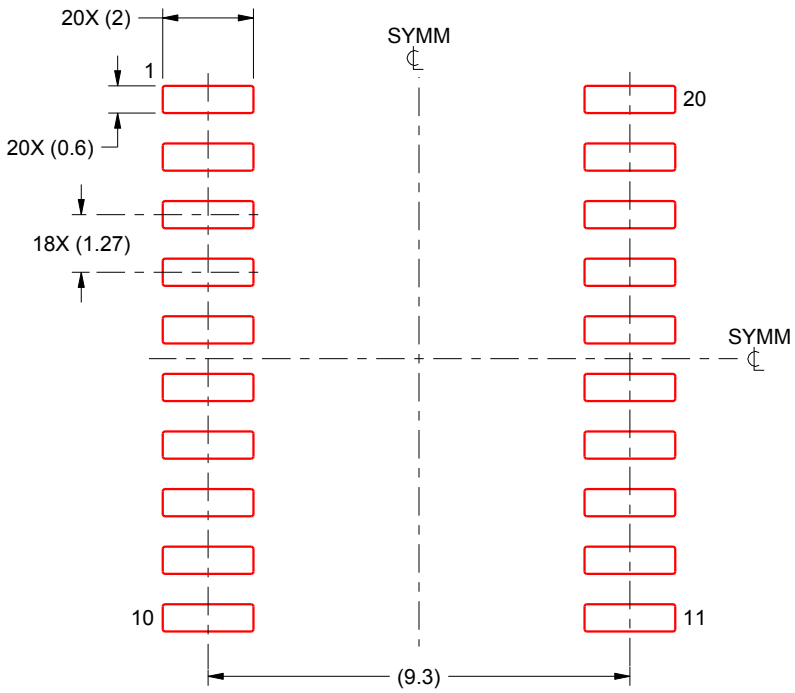


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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