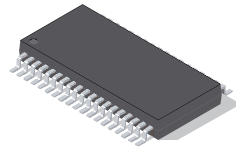


LVDS 4x4 CROSSPOINT SWITCH

Check for Samples: SN65LVDT125A, SN65LVDS125A

FEATURES

- **Signaling Rates >1.5 Gbps per Channel**
- **Supports Telecom/Datacom and HDTV Video Switching**
- **Non-Blocking Architecture Allows Each Output to be Connected to Any Input**
- **Compatible With ANSI TIA/EIA-644-A LVDS Standard**
- **25 mV of Input Voltage Threshold Hysteresis**
- **Propagation Delay Times, 900 ps Typical**
- **Inputs Electrically Compatible With LVPECL, CML and LVDS Signal Levels**
- **Operates From a Single 3.3-V Supply**
- **Integrated 110-Ω Line Termination Resistors Available With SN65LVDT125A**

APPLICATIONS

- **Clock Buffering/Clock Muxing**
- **Wireless Base Stations**
- **High-Speed Network Routing**
- **HDTV Video Switching**

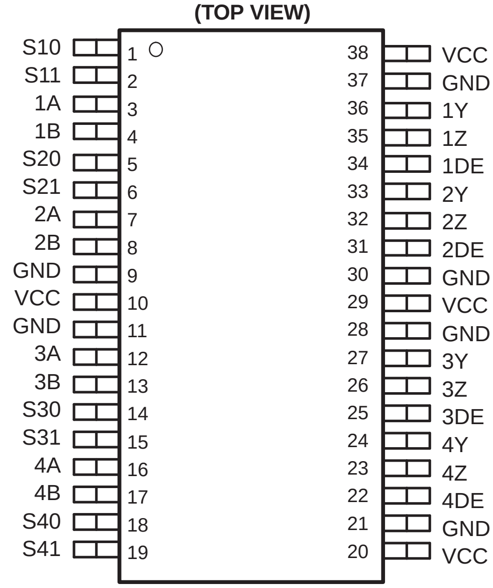
DESCRIPTION

The SN65LVDS125A and SN65LVDT125A are 4x4 nonblocking crosspoint switches. Low-voltage differential signaling (LVDS) is used to achieve signaling rates of 1.5 Gbps per channel. Each output driver includes a 4:1 multiplexer to allow any input to be routed to any output. Internal signal paths are fully differential to achieve the high signaling speeds while maintaining low signal skews. The SN65LVDT125A incorporates 110-Ω termination resistors for those applications where board space is a premium.

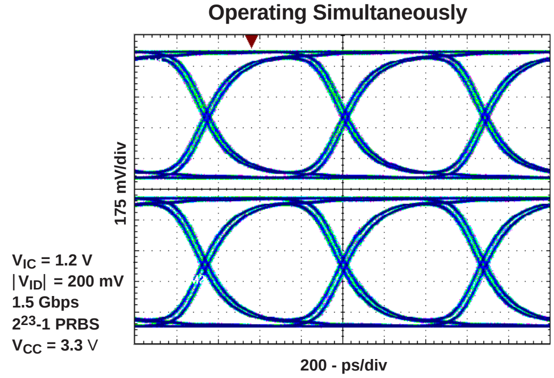
Designed to support signaling rates up to 1.5 Gbps for OC-12 clocks (622 MHz). The 1.5-Gbps signaling rate allows use in HDTV systems, including SMPTE 292 video applications requiring signaling rates of 1.485 Gbps.

The SN65LVDS125A and SN65LVDT125A are characterized for operation from -40°C to 85°C.

SN65LVDS125ADBT (Marked as LVDS125A)
SN65LVDT125ADBT (Marked as LVDT125A)
(TOP VIEW)



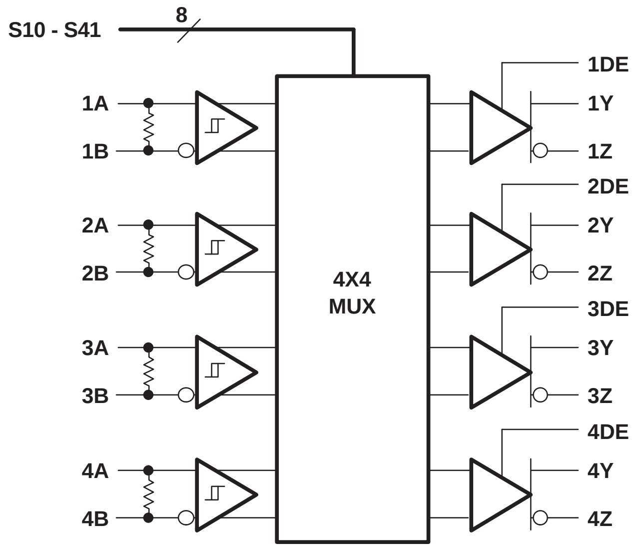
Eye Pattern of Two Outputs Operating Simultaneously



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

LOGIC DIAGRAM



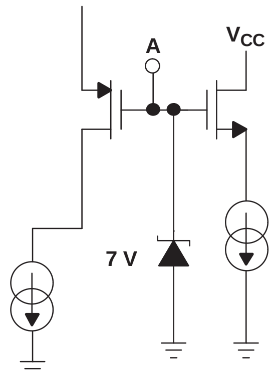
Integrated 110-Ω Termination on LVDT Only

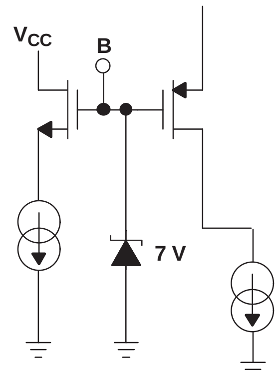
SN65LVDS125A Pin Description

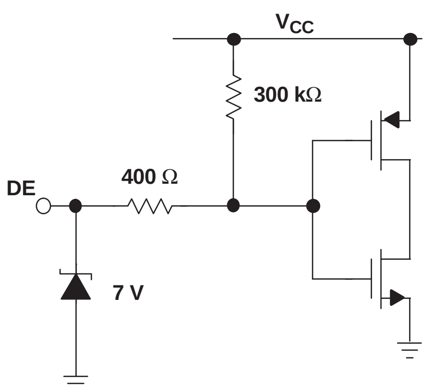
Pin Numbers	Pin Description
S10 - S41	Inputs; Input channel to out output channel selection control pins
1A, 2A, 3A, 4A	Inputs; Positive leg of LVDS data input
1B, 2B, 3B, 4B	Inputs; Negative leg of LVDS data input
1Y, 2Y, 3Y, 4Y	Outputs; Positive leg of LVDS data output
1Z, 2Z, 3Z, 4Z	Outputs; Negative leg of LVDS data output
1DE, 2DE, 3DE, 4DE	Inputs; Output port disable
V_{CC}	Input Voltage
GND	Ground

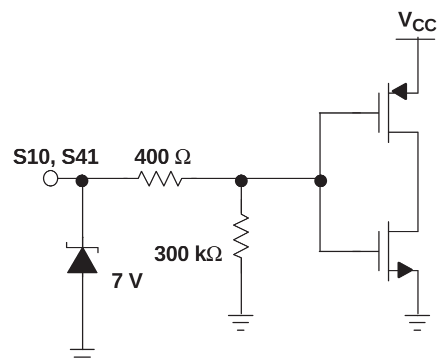
EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

INPUT LVDS125A









OUTPUT LVDS125A

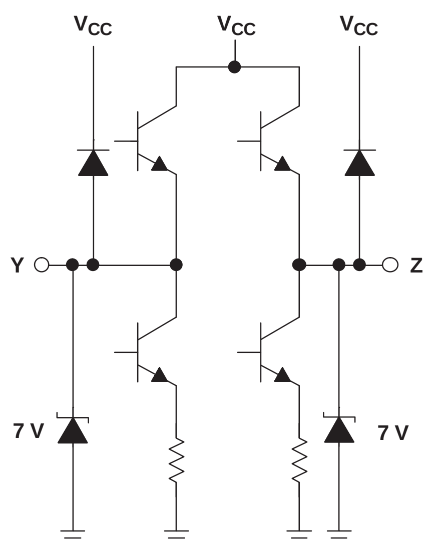


Table 1. CROSSPOINT LOGIC TABLES

OUTPUT CHANNEL 1			OUTPUT CHANNEL 2			OUTPUT CHANNEL 3			OUTPUT CHANNEL 4		
CONTROL PINS		INPUT SELECTED	CONTROL PINS		INPUT SELECTED	CONTROL PINS		INPUT SELECTED	CONTROL PINS		INPUT SELECTED
S10	S11	1Y/1Z	S20	S21	2Y/2Z	S30	S31	3Y/3Z	S40	S41	4Y/4Z
0	0	1A/1B	0	0	1A/1B	0	0	1A/1B	0	0	1A/1B
0	1	2A/2B	0	1	2A/2B	0	1	2A/2B	0	1	2A/2B
1	0	3A/3B	1	0	3A/3B	1	0	3A/3B	1	0	3A/3B
1	1	4A/4B	1	1	4A/4B	1	1	4A/4B	1	1	4A/4B

PACKAGE DISSIPATION RATINGS

PACKAGE	CIRCUIT BOARD MODEL	$T_A \le 25°C$ POWER RATING	DERATING FACTOR[(1)] ABOVE T_A = 25°C	T_A = 85°C POWER RATING
TSSOP (DBT)	High-K[(2)]	1772 mW	15.4 mW/°C	847 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounded and with no air flow.
(2) In accordance with the High-K thermal metric definitions of EIA/JESD51-6.

THERMAL CHARACTERISTICS

PARAMETER			TEST CONDITIONS	VALUE	UNITS
θ_{JB}	Junction-to-board thermal resistance			40.3	°C/W
θ_{JC}	Junction-to-case thermal resistance			8.5	
P_D	Device power dissipation	Typical	V_{CC} = 3.3 V, T_A = 25°C, 750 MHz	356	mW
		Maximum	V_{CC} = 3.6 V, T_A = 85°C, 750 MHz	522	mW

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted[(1)]

			UNITS
Supply voltage range, V_{cc}			-0.5 V to 4 V
Voltage range[(2)]	S, DE		-0.5 V to 4 V
	(A, B)		-0.5 V to 4 V
	$\lvert V_A - V_B \rvert$ (LVDT only)		1 V
	(Y, Z)		-0.5 V to 4 V
Electrostatic discharge	Human body model[(3)]	All pins	±3 kV
	Charged-device model[(4)]	All pins	±500 V
Continuous power dissipation			See Dissipation Rating Table
Storage temperature range			-65°C to 150°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-A.
(4) Tested in accordance with JEDEC Standard 22, Test Method C101.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		3	3.3	3.6	V
High-level input voltage, V_{IH}	S10-S41, 1DE-4DE	2			V
Low-level input voltage, V_{IL}	S10-S41, 1DE-4DE			0.8	V
Magnitude of differential input voltage $\|V_{ID}\|$	LVDS	0.1			V
	LVDT	0.1		0.8	V
Input voltage (any combination of common-mode or input signals)		0		3.3	V
Junction temperature, T_J				140	°C
Operating free-air temperature, T_A (1)		-40		85	°C

(1) Maximum free-air temperature operation is allowed as long as the device maximum junction temperature is not exceeded.

TIMING SPECIFICATIONS

PARAMETER			MIN	NOM	MAX	UNIT
t_{SET}	Input to select setup time	See Figure 7		0.6		ns
t_{HOLD}	Input to select hold time			0.2		ns
t_{SWITCH}	Select to switch output			1.2	1.6	ns

INPUT ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted(1)

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going differential input voltage threshold		See Figure 1			100	mV
V_{IT-}	Negative-going differential input voltage threshold		See Figure 1	-100			mV
$V_{ID(HYS)}$	Differential input voltage hysteresis				25		mV
I_{IH}	High-level input current	1DE-4DE	V_{IH} = 2 V			-10	µA
		S10-S41				20	µA
I_{IL}	Low-level input current	1DE-4DE	V_{IL} = 0.8 V			-10	µA
		S10-S41				20	µA
I_I	Input current		V_I = 0 V or 3.3 V, Second input at 1.2 V (other input open for LVDT)	-20		20	µA
$I_{I(OFF)}$	Input current		V_{CC} ≤ 1.5 V, V_I = 0 V or 3.3 V, Second input at 1.2 V (other input open for LVDT)	-20		20	µA
I_{IO}	Input offset current ($\|I_{IA}$ - $I_{IB}\|$) ('LVDS)		V_{IA} = $V_{IB,}$ 0 ≤ V_{IA}≤ 3.3 V	-6		6	µA
R_T	Termination resistance ('LVDT)		V_{ID} = 300 mV, V_{IC} = 0 V to 3.3 V	90	110	132	Ω
	Termination resistance('LVDT with power-off)		V_{ID} = 300 mV, V_{IC} = 0 V to 3.3 V, V_{CC}= 1.5 V	90	110	132	Ω
C_T	Differential input capacitance				0.6		pF

(1) All typical values are at 25°C and with a 3.3 V supply.

OUTPUT ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\|V_{OD}\|$	Differential output voltage magnitude	See Figure 2, V_{ID} = ±100 mV	247	350	454	mV
$\Delta\|V_{OD}\|$	Change in differential output voltage magnitude between logic states		-50		50	mV
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 3	1.125		1.375	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states		-50		50	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage			50	150	mV
I_{CC}	Supply current	R_L = 100 Ω, C_L = 1 pF		107	145	mA
I_{OS}	Short-circuit output current	V_{OY} or V_{OZ} = 0 V	-27		27	mA
I_{OSD}	Differential short circuit output current	V_{OD} = 0 V	-12		12	mA
I_{OZ}	High-impedance output current	V_O = 0 V or V_{CC}	-1		±1	μA
C_O	Differential output capacitance			1.2		pF

(1) All typical values are at 25°C and with a 3.3 V supply.

SWITCHING CHARACTERISTICS

over recommended operating conditions unless otherwise noted(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 4	700	900	1200	ps
t_{PHL}	Propagation delay time, high-to-low-level output		700	900	1200	
t_r	Differential output signal rise time (20%-80%)			210	270	
t_f	Differential output signal fall time (20%-80%)			210	270	
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)(1)			0	50	ps
$t_{sk(o)}$	Channel-to-channel output skew(2)				150	ps
$t_{sk(pp)}$	Part-to-part skew(3)				300	ps
$t_{jit(per)}$	Period jitter, rms (1 standard deviation)(4)	750 MHz clock input(5) (see Figure 6)		0.4	3	ps
$t_{jit(cc)}$	Cycle-to-cycle jitter (peak)(4)	750 MHz clock input(6) (see Figure 6)		4.7	13	ps
$t_{jit(pp)}$	Peak-to-peak jitter(4)	1.5 Gbps 2^{23}-1 PRBS input(7) (see Figure 6)		65	110	ps
$t_{jit(det)}$	Deterministic jitter, peak-to-peak(4)	1.5 Gbps 2^7-1 PRBS input(8) (see Figure 6)		56	90	ps
t_{PHZ}	Propagation delay, high-level-to-high-impedance output	See Figure 5			6	ns
t_{PLZ}	Propagation delay, low-level-to-high-impedance output				6	
t_{PZH}	Propagation delay, high-impedance -to-high-level output				300	
t_{PZL}	Propagation delay, high-impedance-to-low-level output				300	

(1) $t_{sk(p)}$ is the magnitude of the time difference between the t_{PLH} and t_{PHL} of any output of a single device.
(2) $t_{sk(o)}$ is the maximum delay time difference between drivers over temperature, V_{CC}, and process.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(4) Jitter specifications are based on design and characteriztion. Stimulus system jitter of 1.9 ps $t_{jit(per)}$, 16 ps $t_{jit(cc)}$. 17 ps $t_{jit(pp)}$, and 7.2 ps $t_{jit(det)}$ have been subtracted from the values.
(5) Input voltage = V_{ID} = 200 mV, 50% duty cycle at 750 MHz, t_r = t_f= 50 ps (20% to 80%), measured over 1000 samples.
(6) Input voltage = V_{ID} = 200 mV, 50% duty cycle at 750 MHz, t_r = t_f= 50 ps (20% to 80%).
(7) Input voltage = V_{ID} = 200 mV, 2^{23}-1 PRBS pattern at 1.5 Gbps, t_r = t_f = 50 ps (20% to 80%), measured over 200k samples.
(8) Input voltage = V_{ID} = 200 mV, 2^7-1 PRBS pattern at 1.5 Gbps, t_r= t_f = 50 ps (20% to 80%).

PARAMETER MEASUREMENT INFORMATION

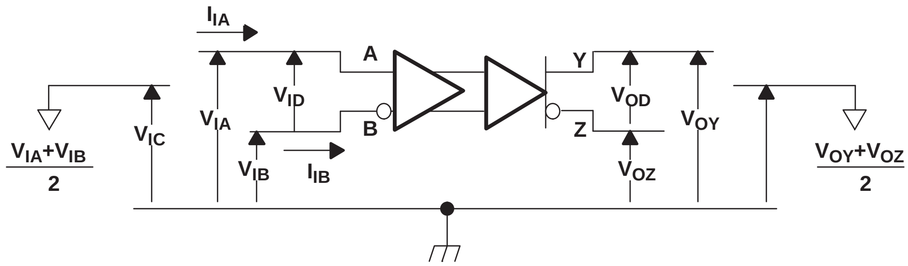


Figure 1. Voltage and Current Definitions

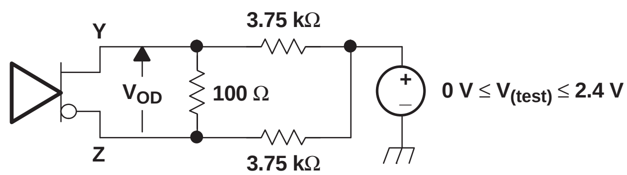
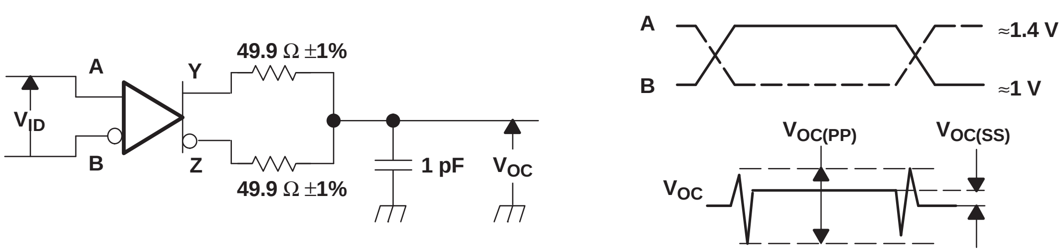
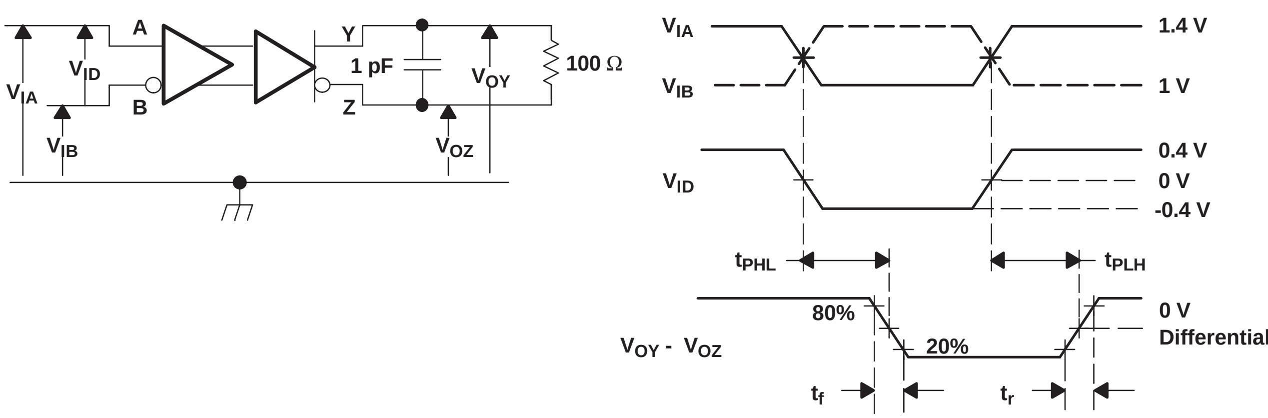


Figure 2. Differential Output Voltage (V_{OD}) Test Circuit



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 1 ns, pulse-repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ±10 ns; R_L = 100W; C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.; the measurement of $V_{OC(PP)}$ is made on test equipment with a -3 dB bandwidth of at least 300 MHz.

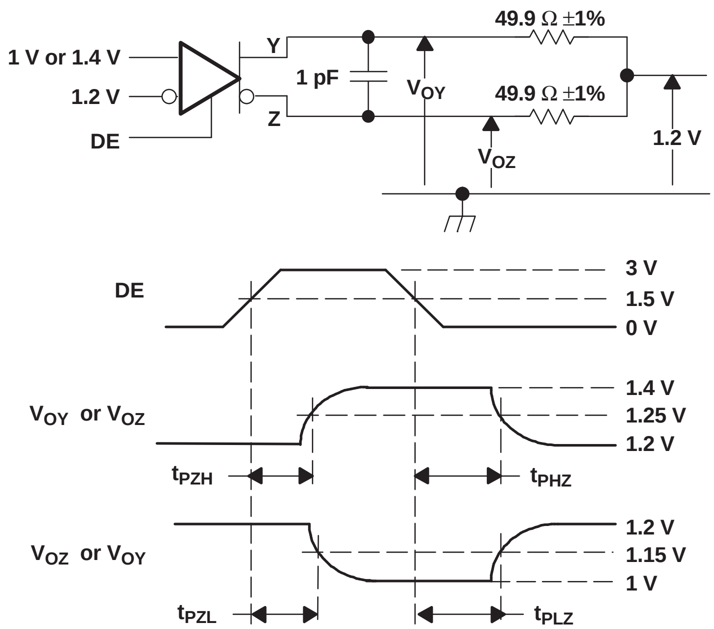
Figure 3. Test Circuit and Definitions fot the Driver Common-Mode Output Voltage



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or t_f≤ .25 ns, pulse-repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns . C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

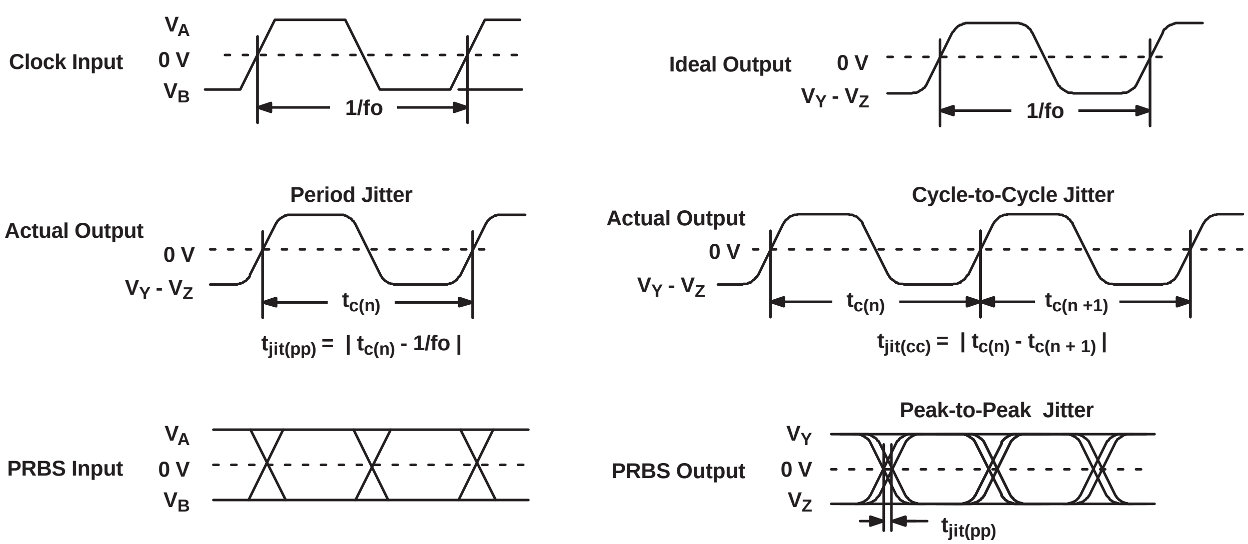
Figure 4. Timing Test Circuit and Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 1 ns, pulse-repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns . C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

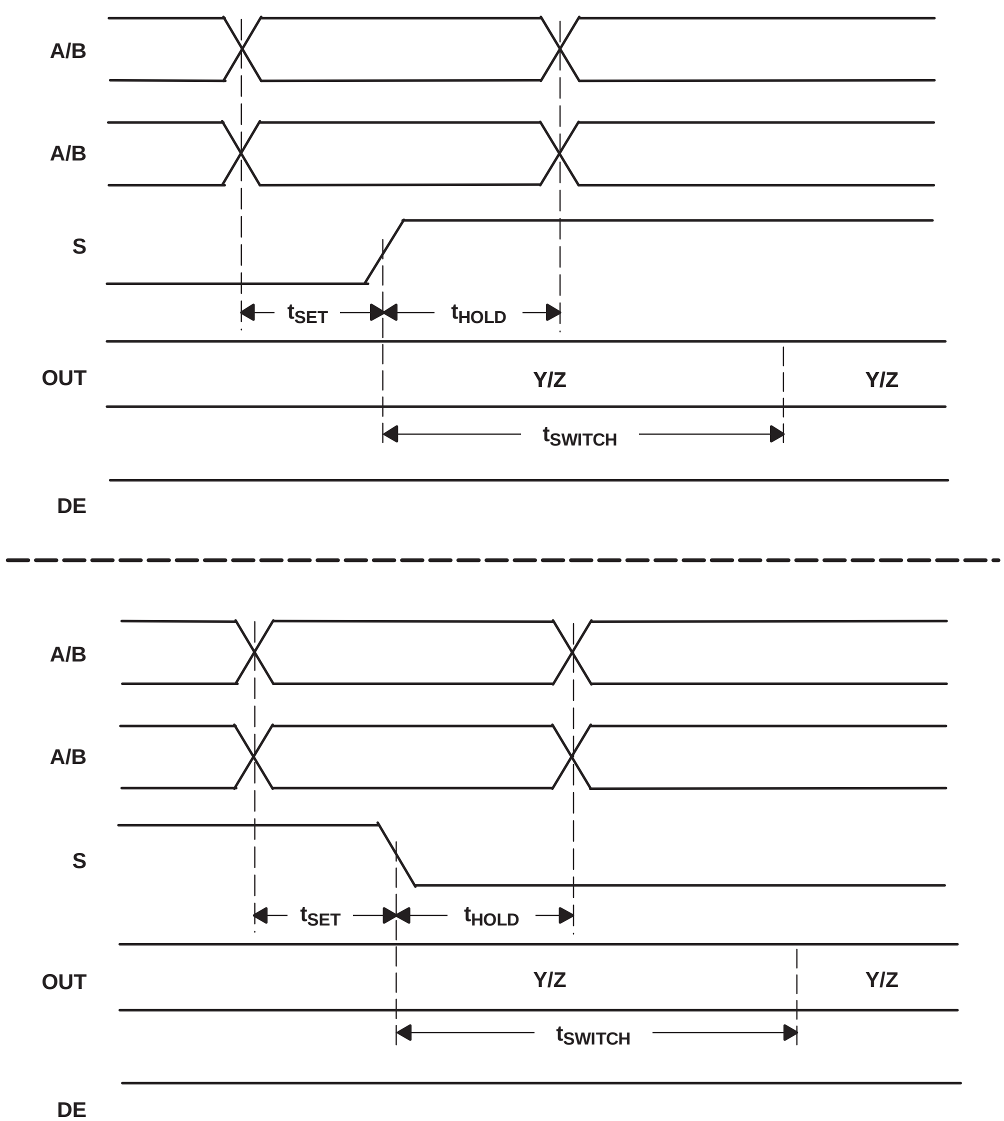
Figure 5. Enable and Disable Time Circuit and Definitions



NOTE: All input pulses are supplied by an Agilent 81250 Stimulus System. The measurement is made on a TEK TDS6604 running TDSJIT3 application software.

Figure 6. Driver Jitter Measurement Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)



NOTE: t_{SET} and t_{HOLD} times specify that data must be in a stable state before and after mux control switches.

Figure 7. Input to Select for Both Rising and Falling Edge Setup and Hold Times

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs FREQUENCY

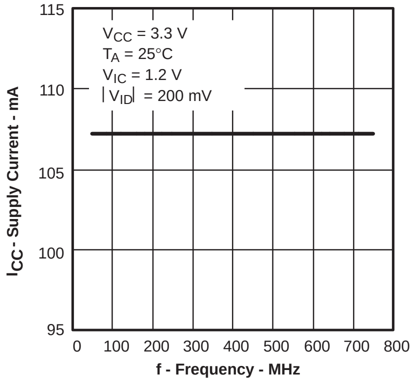


Figure 8.

PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE

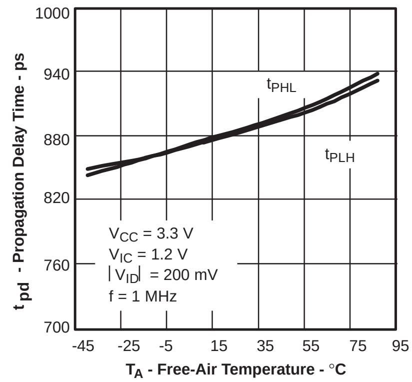


Figure 9.

PROPAGATION DELAY TIME vs COMMON-MODE INPUT VOLTAGE

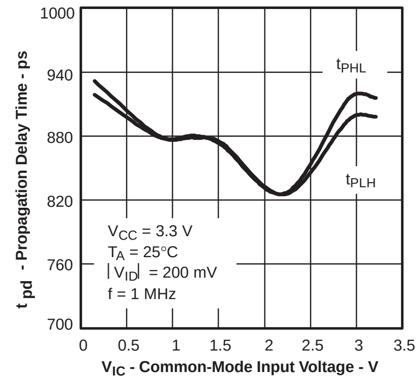


Figure 10.

PEAK-TO-PEAK JITTER vs FREQUENCY

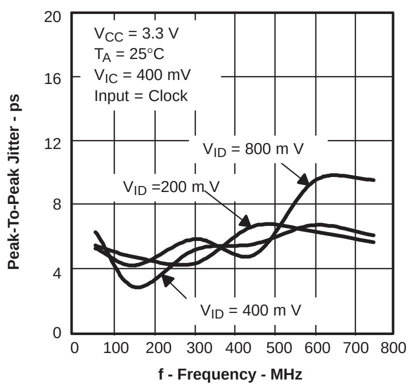


Figure 11.

PEAK-TO0PEAK JITTER vs DATA RATE

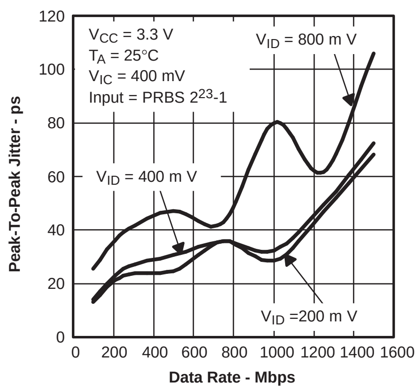


Figure 12.

PEAK-TO-PEAK JITTER vs FREQUENCY

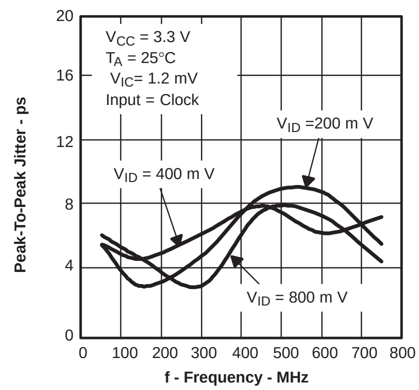


Figure 13.

PEAK-TO-PEAK JITTER vs DATA RATE

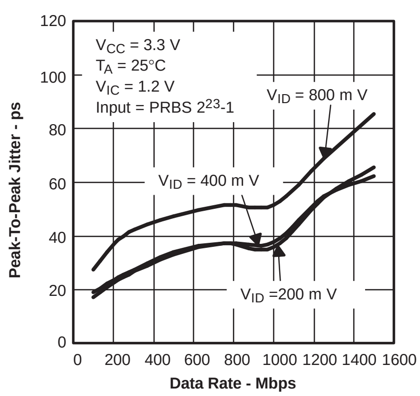


Figure 14.

PEAK-TO0PEAK JITTER vs FREQUENCY

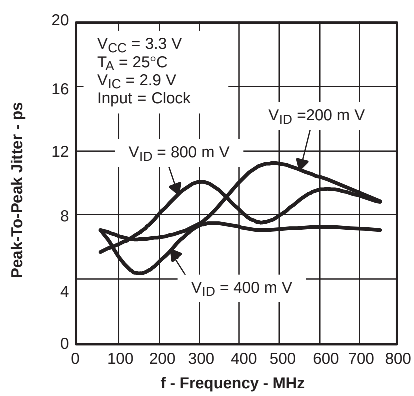


Figure 15.

PEAK-TO-PEAK JITTER vs DATA RATE

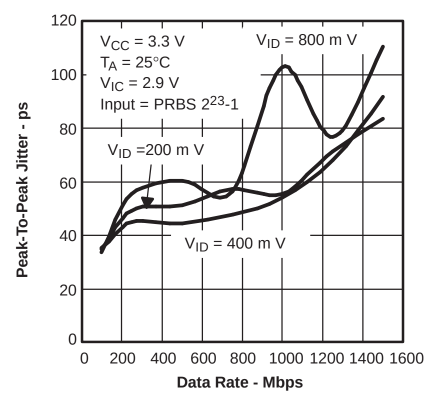


Figure 16.

TYPICAL CHARACTERISTICS (continued)

PEAK-TO-PEAK JITTER
vs
FREE-AIR TEMPERATURE

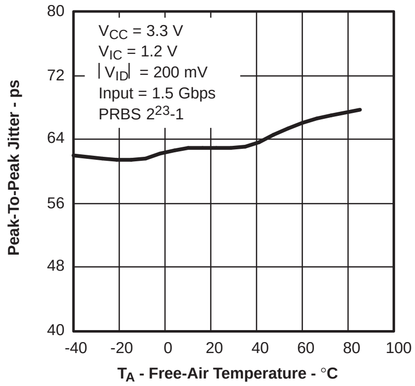


Figure 17.

PEAK-TO-PEAK JITTER
vs
DATA RATE

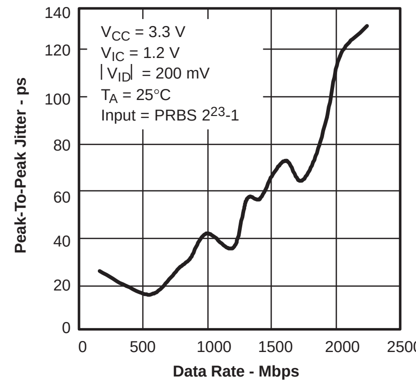
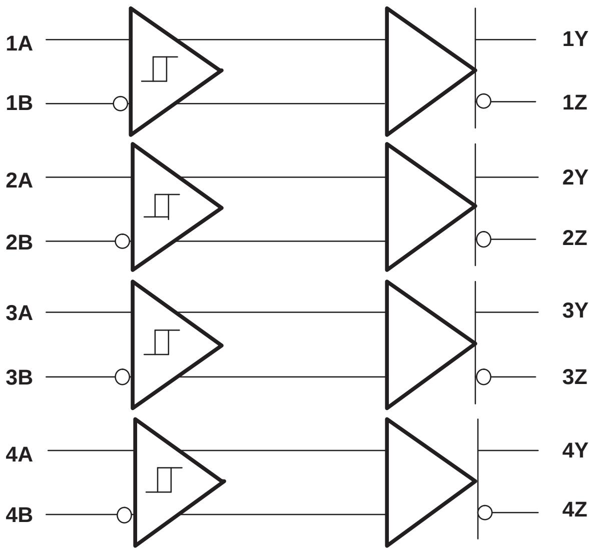


Figure 18.

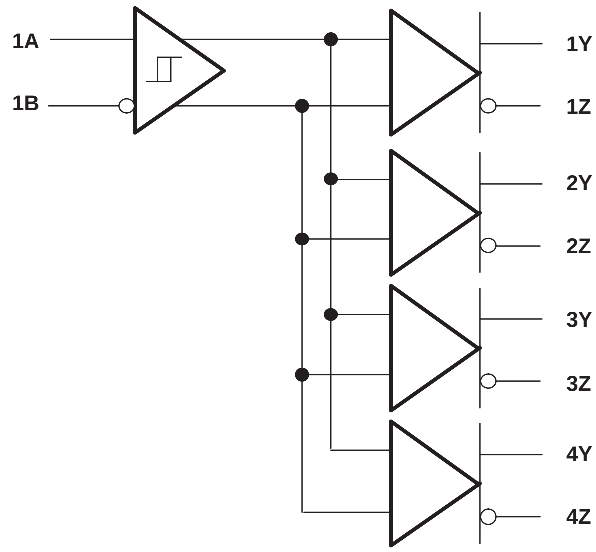
APPLICATION INFORMATION

CONFIGURATION EXAMPLES

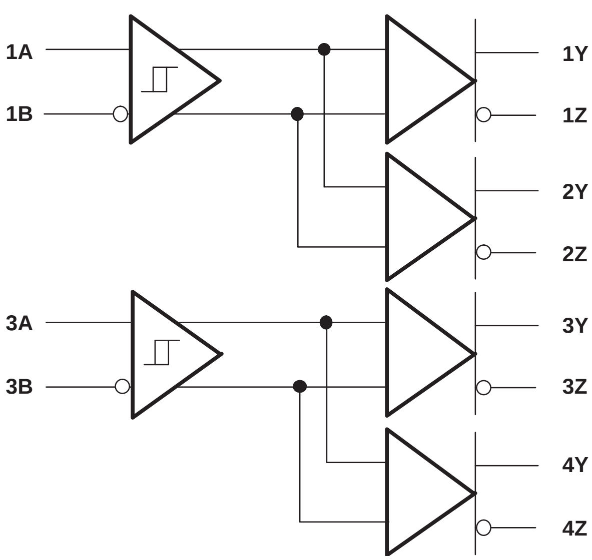
S10	S11	S20	S21
0	0	0	1
S30	S31	S40	S41
1	0	1	1



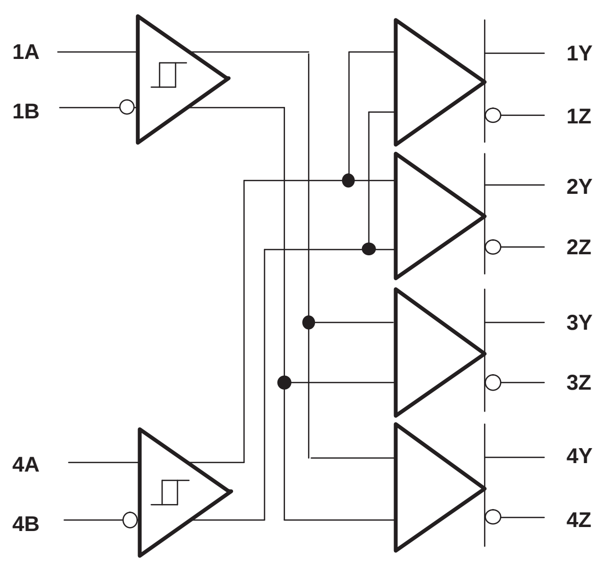
S10	S11	S20	S21
0	0	0	0
S30	S31	S40	S41
0	0	0	0



S10	S11	S20	S21
0	0	0	0
S30	S31	S40	S41
1	0	1	0



S10	S11	S20	S21
1	1	1	1
S30	S31	S40	S41
0	0	0	0



TYPICAL APPLICATION CIRCUITS (ECL, PECL, LVDS, etc.)

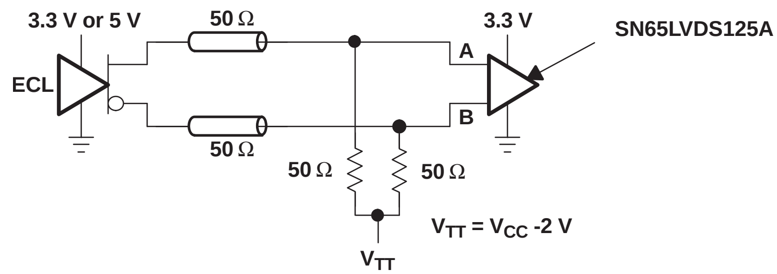


Figure 20. Low-Voltage Positive Emitter-Coupled Logic (LVPECL)

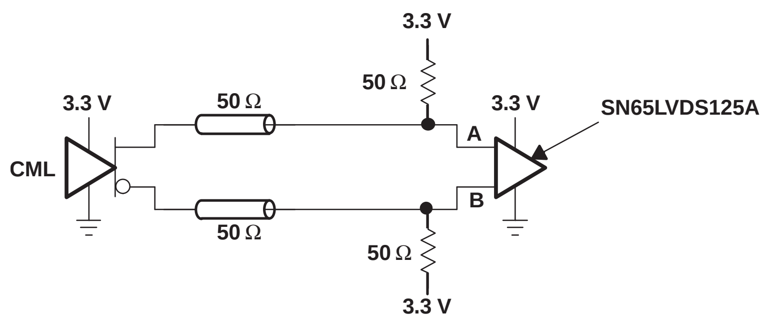


Figure 21. Current-Mode Logic (CML)

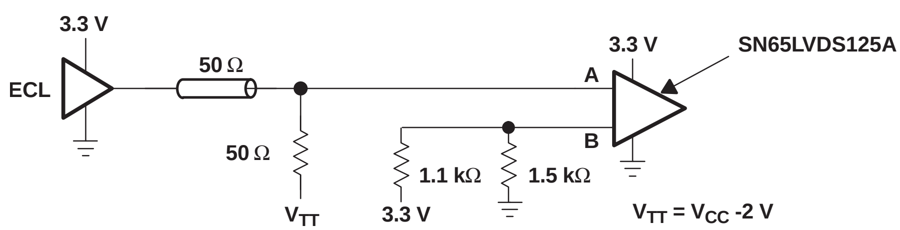


Figure 22. Single-Ended (LVPECL)

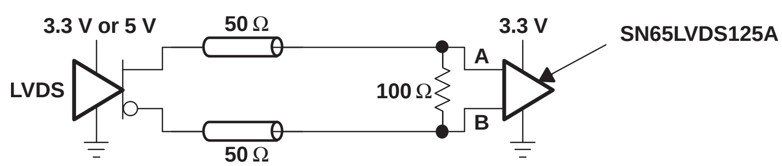


Figure 23. Low-Voltage Differential Signaling (LVDS)

See the EVM Users Guide (SLLU064) for example board layout and schematics examples.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LVDS125ADBT	ACTIVE	TSSOP	DBT	38	50	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDS125A	Samples
SN65LVDS125ADBTR	ACTIVE	TSSOP	DBT	38	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDS125A	Samples
SN65LVDT125ADBT	ACTIVE	TSSOP	DBT	38	50	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDT125A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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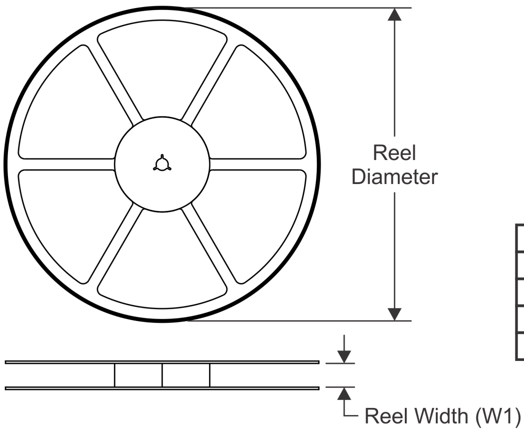
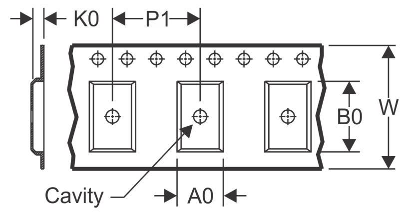
TAPE AND REEL INFORMATION

REEL DIMENSIONS

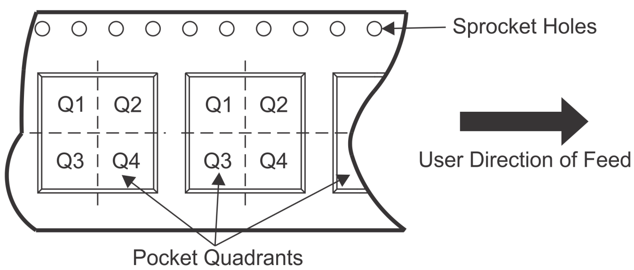


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

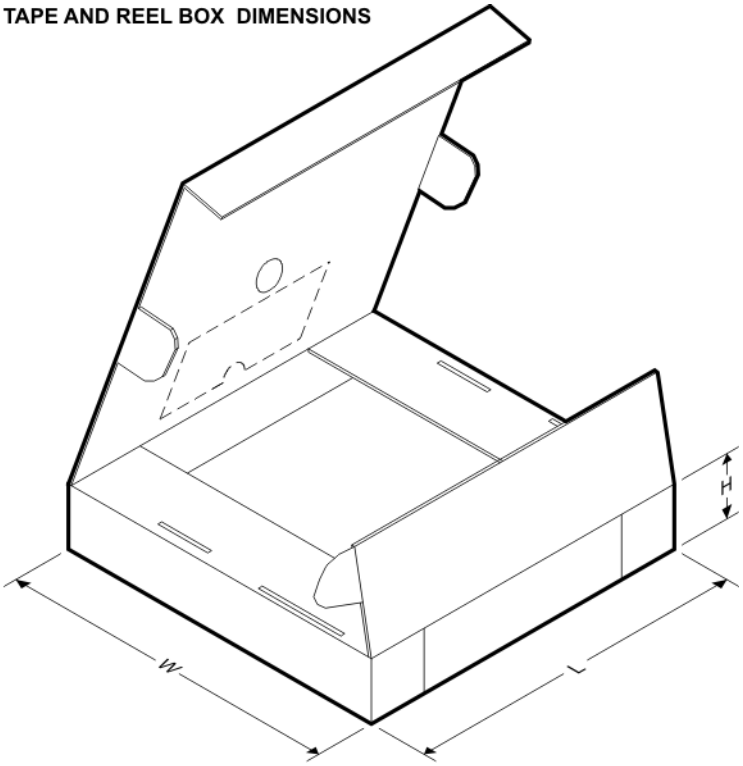
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVDS125ADBTR	TSSOP	DBT	38	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

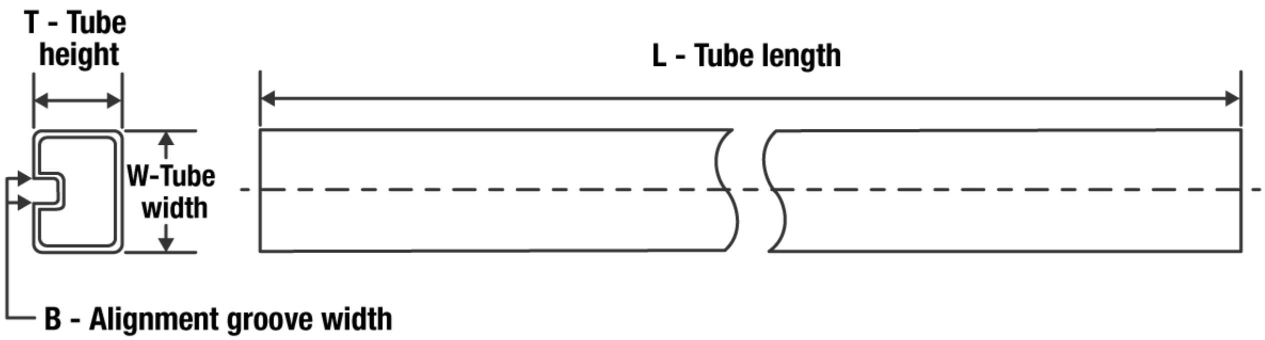
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVDS125ADBTR	TSSOP	DBT	38	2000	350.0	350.0	43.0

TUBE



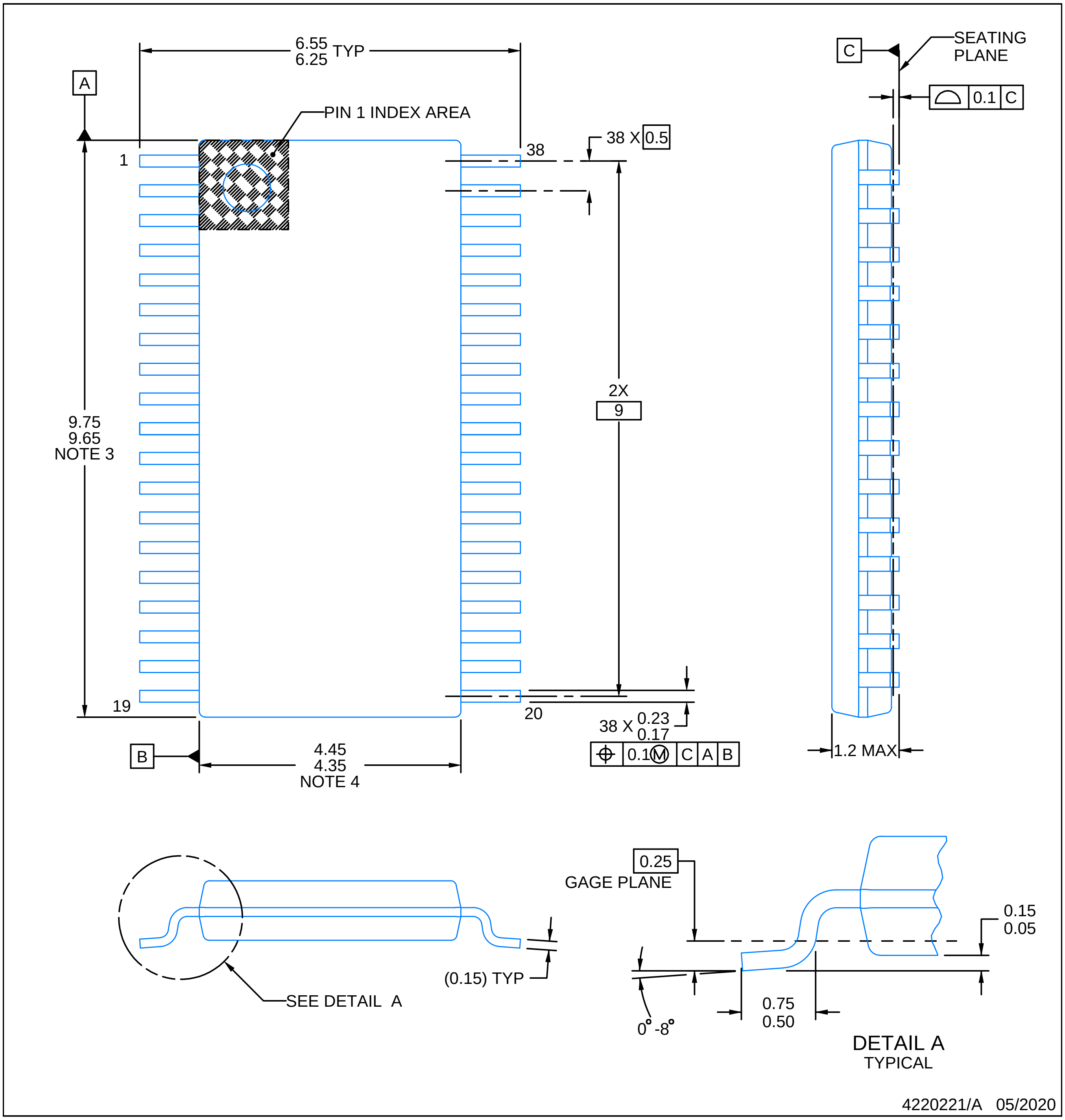
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65LVDS125ADBT	DBT	TSSOP	38	50	530	10.2	3600	3.5
SN65LVDT125ADBT	DBT	TSSOP	38	50	530	10.2	3600	3.5

DBT0038A

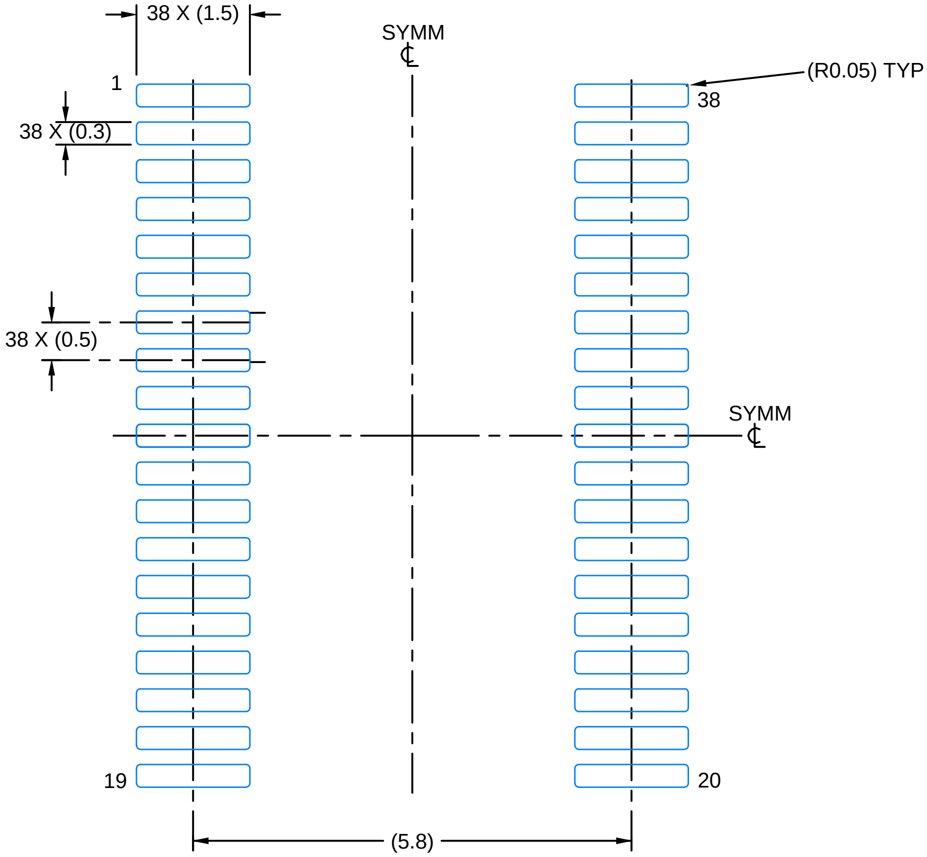
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

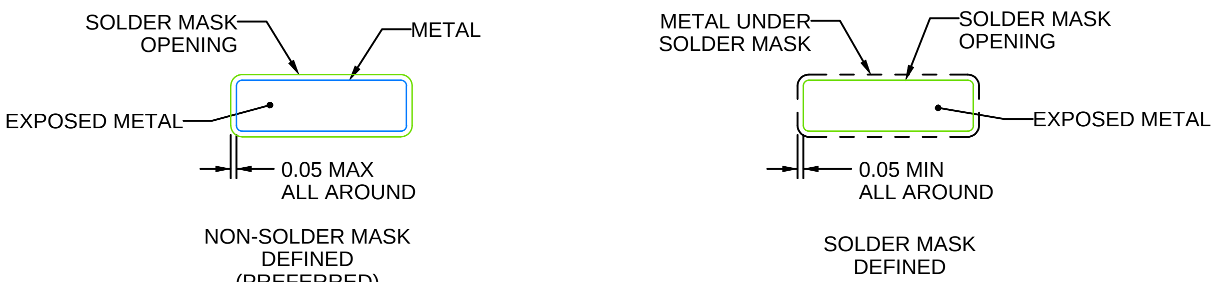


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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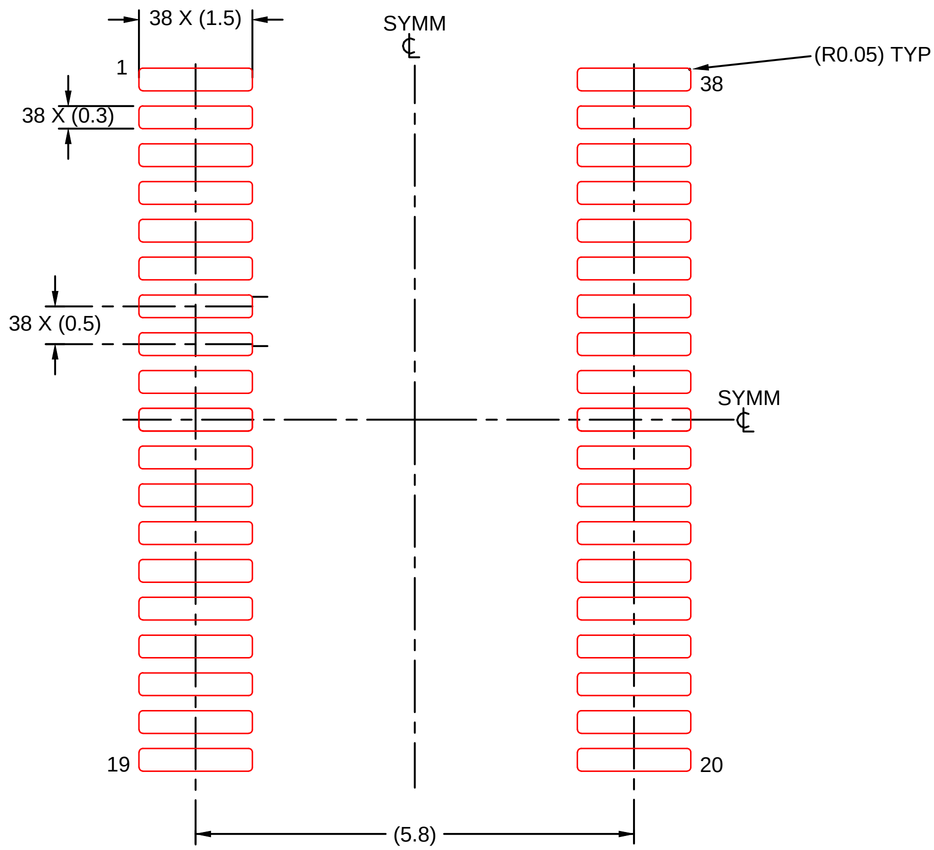
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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