

TUSB2E11 USB 2.0-eUSB2 Repeater

1 Features

- USB 2.0 and eUSB2 (rev 1.2) compliant
- Low-speed, full-speed, high-speed signaling
- Best-in-class high-speed total jitter of 20 ps
- Register access protocol receptor capable
- Host and device mode (dual-role device) support
- Auto detection for I²C or strap-pin options
 - Three strap-pins for USB 2.0 high-speed channel compensation settings
 - I²C device interface for more configurations
- Device variants
 - eUSB2 1.0-V or 1.2-V signaling interface
 - eUSB2 trace loss compensation levels for different product form-factors
 - 1.2-V or 1.8-V I²C interface
- Optional battery charging and detection support
 - BC 1.2 CDP or DCP divider mode advertising
 - Data-aware USB Type-C™ compatible BC 1.2 SDP, CDP, and DCP divider mode detection
 - Dual-role auto switching between charger advertising or detection
- CTA-936 USB CarKit UART support
- Supports auto-resume ECR as well as L2 interrupt resume mode
- Optional GPIOs: interrupt GPIO2, debug, I²C ↔ GPIO0/1
- I²C accessible debug capabilities for manufacturing tests

2 Applications

- [Notebooks and desktops](#)
- [Cell phones](#)
- [Tablets](#)
- [Wearables](#)
- [Portable electronics](#)

3 Description

TUSB2E11 is a USB compliant eUSB2 to USB 2.0 repeater supporting both device and host modes.

The device supports USB low-speed (LS), full-speed (FS) signals, and high-speed (HS) signals.

The device has multiple patented designs to provide robust interoperability, optimum performance, and power.

For systems without an I²C interface, the device offers eight individual settings with three strap-pins for USB 2.0 channel Equivalent Series Resistance (ESR) up to 20 Ω. Device variants are available for different levels of eUSB2 trace length compensation up to 10 inches.

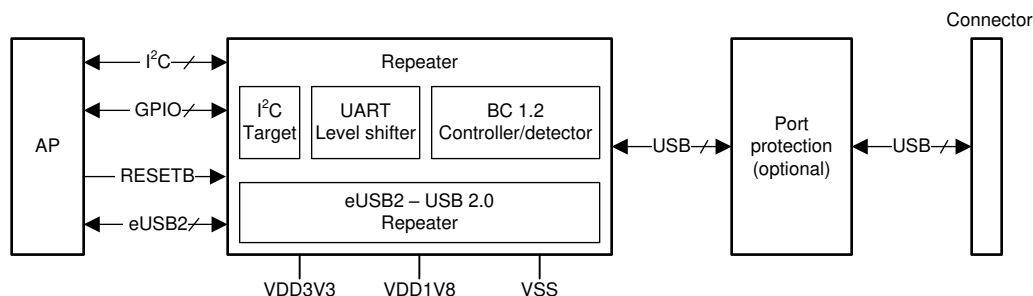
The I²C interface permits additional flexibility for fine tuning of device RX equalization and TX amplitude, slew rate and pre-emphasis to pass electrical compliance tests and compensate for channel loss.

Various debug options are available through the 3 GPIO pins that can be configured to monitor various USB bus states or interrupt as well as CTA-936 UART mode that can provide SoC debug capabilities. GPIO0 and GPIO1 can be used as general purpose I²C to GPIOs bridge.

Package Information

| PART NUMBER ⁽¹⁾ | PACKAGE ⁽²⁾ | PACKAGE SIZE ⁽³⁾ |
|----------------------------|------------------------|-----------------------------|
| TUSB2E11 | YCG (DSBGA, 15) | 1.75 mm × 1.05 mm |

- (1) See the [Device Comparison](#)
- (2) For all available packages, see the orderable addendum at the end of the data sheet.
- (3) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Application



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision A (June 2022) to Revision B (August 2023) | Page |
|--|------|
| • Updated the <i>Package Information</i> table to include package lead size..... | 1 |
| • Updated <i>Recommended Operating Conditions</i> to clarify the ROC for RESETB..... | 9 |
| • Updated register F5h to indicate OPN variants..... | 32 |

| Changes from Revision * (November 2021) to Revision A (June 2022) | Page |
|---|------|
| • First public release of the data sheet..... | 1 |

5 Device Version Comparison

Table 5-1. Device Register Comparison Table

| | Register Address | B0 default | B1 default |
|-----------------------------|------------------|------------|------------|
| Table 11-5 | 0x70h | 0x73h | 0x7Ch |
| Table 11-6 | 0x71h | 0x38h | 0x3Ch |
| Table 11-7 | 0x72h | 0x90h | 0x92h |
| Table 11-8 | 0x73h | 0x04h | 0x83h |
| Table 11-9 | 0x77h | 0x00h | 0x00h |
| Table 11-10 | 0x78h | 0x0Bh | 0x0Bh |
| Table 11-11 | 0x79h | 0x40h | 0x60h |
| Table 11-12 | 0x50h | 0x02h | 0x02h |
| Table 11-13 | 0xB0h | 0x02h | 0x03h |
| Table 11-14 | 0xB2h | 0x00h | 0x00h |
| Table 11-15 | 0xB3h | 0x00h | 0x00h |
| Table 11-16 | 0xB4h | 0x00h | 0x00h |
| Table 11-17 | 0xB6h | 0xC0h | 0xC0h |
| Table 11-21 | 0x60h | 0x00h | 0x00h |
| Table 11-22 | 0xF5h | 0x32h | 0x32h |

Table 5-2. Device Feature Comparison Table

| Features | B0 | B1 |
|---|---------------|--|
| Low Power Mode (RESETB = low) | not supported | supported (9 μ W) |
| Auto-resume ECR | not supported | supported (enabled by default) [see register 0x78h] |
| L2 State Interrupt Resume | supported | supported |

5.1 Device Variants

The following table describes the key differences between TUSB2E11x device variants.

Table 5-3. Device Variant Information

| Orderable Device | Package Type | Package Drawing | Pins | Version | I/O Voltage ⁽¹⁾ | Device Marking |
|------------------|--------------|-----------------|------|---------|----------------------------|----------------|
| TUSB2E111YCGR | WCSP | YCG | 15 | B1 | 1.8V | T2E111A |
| TUSB2E112YCGR | WCSP | YCG | 15 | B1 | 1.2V | T2E112 |

(1) **I/O Voltage:** I2C Bus voltage and GPIO voltage

For more information and availability of device variants such as eUSB2 1.0 signaling interface, 1.2 V I²C interface, and 1.2 V GPIO interface please contact [support](#).

6 Pin Configuration and Functions



Figure 6-1. TUSB2E11 YCG Package, 15-Pin DSBGA (Top View)

Table 6-1. Pin Functions

| PIN | | TYPE ⁽²⁾ | REST STATE | ASSOCIATED ESD SUPPLY | DESCRIPTION |
|--------|--------|---------------------|------------|-----------------------|--|
| NAME | NO. | | | | |
| VDD3V3 | B2 | PWR | N/A | N/A | 3.3 V Supply Voltage |
| VDD1V8 | D2, E3 | PWR | N/A | N/A | 1.8 V Supply Voltage |
| VSS | A3, D3 | GND | N/A | N/A | GND |
| RESETB | D1 | I | N/A | VDD1V8 | <ul style="list-style-type: none"> Active Low Reset Upon de-assertion of RESETB, repeater will be enabled and be in eUSB2 default mode awaiting configuration from eDSPr or eUSPr. If RESETB is not actively controlled, a pull-up resistor 100 kΩ to VDD1V8 is required. |

Table 6-1. Pin Functions (continued)

| PIN | | TYPE ⁽²⁾ | REST STATE | ASSOCIATED ESD SUPPLY | DESCRIPTION | | | | |
|-------|-----|---------------------|---|-----------------------|--|--------------------|---|--------------------------------|-----------------------------------|
| NAME | NO. | | | | SCL | SDA | Mode | | |
| SCL | C3 | I | Internal pull-down 1 MΩ typical (disabled after reset) ⁽¹⁾ | VDD1V8 | I ² C Clock | Device Mode Matrix | Low | See Table 6-4 for more details | Non-I ² C USB Repeater |
| SDA | B3 | I/O | Hi-Z ⁽¹⁾ | VDD1V8 | | | Bidirectional I ² C data Open drain I/O | High | Low |
| | | | | | | | High | High | I ² C Enabled |
| GPIO2 | C2 | I/O | Internal pull-down 1 MΩ typical (disabled after reset) | VDD1V8 | <ul style="list-style-type: none"> In I²C mode GPIO2 will be an open drain active low level interrupt output. Connect GPIO2 to input of APU and a pull-up resistor to use interrupt features In non I²C mode GPIO2 defaults to USB configuration input at power up reset. When a pull-up resistor is used to set high input, ensure VIH is met accounting for internal pull down as small as 500 kΩ GPIO2 is an open-drain output after reset and can be left floating when not used. | | | | |
| GPIO0 | B1 | I/O | Internal pull-down 1 MΩ typical (disabled after reset) ⁽¹⁾ | VDD1V8 | Defaults to an input mode at power up reset. RESETB assertion and de-assertion or soft reset will revert GPIO0 to input mode <ul style="list-style-type: none"> In I²C mode GPIO0 will default to control CarKit UART mode: active low to enable CarKit UART mode. Default CarKit UART direction is DP → eDP (RX) and eDN → DN (TX). GPIO0 must be pulled up to be in USB repeater mode. In non I²C mode GPIO0 defaults to USB configuration input at power up reset. When a pull-up resistor is used to set high input, ensure VIH is met accounting for internal pull down as small as 500 kΩ | | | | |
| GPIO1 | C1 | I/O | Internal pull-down 1 MΩ typical (disabled after reset) ⁽¹⁾ | VDD1V8 | Defaults to an input mode at power up reset. RESETB assertion and de-assertion or soft reset will revert GPIO1 to input mode <ul style="list-style-type: none"> In I²C mode GPIO1 defaults to debug input In non I²C mode GPIO1 defaults to USB Configuration input at power up reset. When a pull-up resistor is used to set high input, ensure VIH is met accounting for internal pull down as small as 500 kΩ | | | | |
| eDN | A2 | I/O | Hi-Z | VDD1V8 | eUSB2 port D- | | | | |
| eDP | A1 | I/O | Hi-Z | VDD1V8 | eUSB2 port D+ | | | | |
| DN | E2 | I/O | Hi-Z | VDD3V3 | USB port D- | | | | |
| DP | E1 | I/O | Hi-Z | VDD3V3 | USB port D+ | | | | |

(1) When configured as an input but not actively driven, use 1 MΩ external pull-down to strap low.
 (2) I = input, I/O = input or output, PWR= power, GND = ground

Table 6-2. Pin Configuration for Device Mode

| Device Mode | SCL (C3) | SDA (B3) | GPIO0 (B1) | GPIO1 (C1) | GPIO2 (C2) |
|--|---|--|--|---|--|
| I ² C Mode | Pull-up Input sampled at reset | Pull-up Input sampled at reset | Default to Input <ul style="list-style-type: none"> • Low = UART Mode • High = USB repeater mode Function can be reconfigured through register | Default to Input Function can be reconfigured through register | Default to Open drain output (can be left floating when not used) Function can be reconfigured through register |
| Non I ² C UART mode | Pull-up Input sampled at reset | Pull-down Input sampled at reset | Default to Input <ul style="list-style-type: none"> • Low = UART transfer enabled • High = UART transfer disabled | High-Z (can be left floating) | High-Z (can be left floating) |
| Non I ² C USB repeater mode | Pull-down Input sampled at reset See Table 6-4 | See Table 6-4 | Default input sampled at reset. See Table 6-3 | | |

Table 6-3. Pin Configuration for USB PHY Tuning without I²C

| GPIO2 | GPIO1 | GPIO0 | Equivalent series resistance (ESR) between repeater and USB connector | U_EQ_P1 setting | U_HS_TX_AMPLITUDE_P1 setting | U_HS_TX_PRE_EMPHASIS_P1 setting | U_SQUELCH_THRESHOLD_P1 setting | U_DISCONNECT_THRESHOLD_P1 setting | HS Term |
|---------|---------|---------|---|-----------------|------------------------------|---------------------------------|--------------------------------|-----------------------------------|---------|
| | | | Ω | dB | mV | dB | mV | mV | Ω |
| Float | Float | Float | 2.5 | 0.06 | 840 | 0.5 | 104 | 625 | 45 |
| | | | | (3'b000) | (4'b0101) | (3'b000) | (3'b100) | (4'b0101) | |
| Float | Float | Pull-Up | 5 | 0.06 | 880 | 0.9 | 98 | 645 | 45 |
| | | | | (3'b000) | (4'b0111) | (3'b001) | (3'b101) | (4'b0110) | |
| Float | Pull-Up | Float | 7.5 | 0.58 | 900 | 0.9 | 98 | 645 | 45 |
| | | | | (3'b001) | (4'b1000) | (3'b001) | (3'b101) | (4'b0110) | |
| Float | Pull-Up | Pull-Up | 10 | 1.09 | 920 | 0.9 | 98 | 685 | 45 |
| | | | | (3'b010) | (4'b1001) | (3'b001) | (3'b101) | (4'b1000) | |
| Pull-Up | Float | Float | 12.5 | 1.56 | 940 | 1.2 | 91 | 685 | 45 |
| | | | | (3'b011) | (4'b1010) | (3'b010) | (3'b110) | (4'b1000) | |
| Pull-Up | Float | Pull-Up | 15 | 2.26 | 980 | 1.2 | 91 | 685 | 45 |
| | | | | (3'b100) | (4'b1100) | (3'b010) | (3'b110) | (4'b1000) | |
| Pull-Up | Pull-Up | Float | 17.5 | 2.67 | 1000 | 1.7 | 91 | 685 | 45 |
| | | | | (3'b101) | (4'b1101) | (3'b011) | (3'b110) | (4'b1000) | |
| Pull-Up | Pull-Up | Pull-Up | 20 | 2.67 | 1020 | 1.7 | 85 | 705 | 42.75 |
| | | | | (3'b101) | (4'b1110) | (3'b011) | (3'b111) | (4'b1001) | |

Table 6-4. Pin Configuration for Battery Charging in non I²C Mode

| Device Mode | | | Repeater State | | | Charger Detection Status | VBUS Control Output |
|--|--|---|---|---------------|------------------------------|--|--|
| | SCL (C3) | SDA (B3) | Unconfigured | Host Repeater | Peripheral Repeater | {GPIO2, GPIO1} | GPIO0 |
| Non I ² C USB repeater mode | Pull-down resistor to ground 0 to 160 Ω | Input <ul style="list-style-type: none"> Low = BC 1.2 disabled High = BC 1.2 enabled | When BC 1.2 is enabled, charger detection | N/A | N/A | <ul style="list-style-type: none"> 2'b00: No charger detected 2'b01: CDP or DCP charger detected 2'b10: DCP (1.5A) or Divider Mode (2.1A) charger detected 2'b11: Divider Mode (2.4A) charger detected | N/A |
| Non I ² C USB repeater mode | Pull-down resistor to ground 1.5 kΩ to 2 kΩ | Input VBUS_Valid input: use a voltage divider to reduce VBUS voltage to appropriate VIH for 1.8 V or 1.2 V I/O mode. | When VBUS_valid is high enable charger detection | N/A | Charger detection is enabled | <ul style="list-style-type: none"> 2'b00: No charger detected 2'b01: CDP or DCP charger detected 2'b10: DCP (1.5A) or Divider Mode (2.1A) charger detected 2'b11: Divider Mode (2.4A) charger detected | N/A |
| Non I ² C USB repeater mode | Pull-down resistor to ground 3.4 kΩ to 3.96 kΩ | Input <ul style="list-style-type: none"> Low = BC 1.2 disabled High = BC 1.2 enabled | When BC 1.2 is enabled, advertise charging BC 1.2 DCP | Advertise CDP | N/A | N/A | Active High Push-Pull output for VBUS switch Control |
| Non I ² C USB repeater mode | Pull-down resistor to ground 7.5 kΩ to 11 kΩ | Input <ul style="list-style-type: none"> Low = BC 1.2 disabled High = BC 1.2 enabled | When BC 1.2 is enabled, advertise charging (auto cycle between BC 1.2 DCP and Divider mode) | Advertise CDP | N/A | N/A | <ul style="list-style-type: none"> High = VBUS ON Low = VBUS OFF |

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|-----------------------------|--|------|------|------|
| Supply voltage range | V _{DD3V3} | -0.3 | 4.32 | V |
| Analog Supply voltage range | V _{DD1V8} | -0.3 | 2.1 | V |
| Voltage range | DP, DN, (with OVP enabled), 1000 total number of short events and cumulative duration of 1000 hrs. | -0.3 | 6 | V |
| Voltage range | eDP, eDN | -0.3 | 1.6 | V |
| Voltage range | RESETB, GPIO0, GPIO1, GPIO2, SCL, SDA | -0.3 | 2.1 | V |
| Junction temperature | T _{J(max)} | | 125 | °C |
| Storage temperature | T _{stg} | -65 | 150 | °C |

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.

7.2 ESD Ratings

| | | | VALUE | UNIT |
|--------------------|-------------------------|---|-------|------|
| V _(ESD) | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾ | ±1500 | V |
| | | Charged device model (CDM), per JEDEC specification JS-002, all pins ⁽²⁾ | ±500 | |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|--------------------------|---|------|-----|------|------|
| V _{DD3V3} | Supply voltage (VDD3V3) | 3.0 | 3.3 | 3.6 | V |
| V _{DD1V8} | Analog Supply voltage (VDD1V8) | 1.62 | 1.8 | 1.98 | V |
| V _{_I2C_Pullup} | I2C and GPIO open drain Bus Voltage (1.2 V Variant) | 1.08 | 1.2 | 1.32 | V |
| V _{_I2C_Pullup} | I2C and GPIO open drain Bus Voltage (1.8 V Variant) | 1.62 | 1.8 | 1.98 | V |
| USB Voltage | DP, DN | 0 | | 3.6 | V |
| eUSB2 voltage | eDP, eDN | 0 | | 1.32 | V |
| Digital voltage | GPIO0, GPIO1, GPIO2, SCL, SDA (1.8 V Variant) | 0 | | 1.98 | V |
| Digital voltage | GPIO0, GPIO1, GPIO2, SCL, SDA (1.2 V Variant) | 0 | | 1.32 | V |
| RESETB | RESETB (1.2 V or 1.8 V Variant) | 0 | | 1.98 | V |
| T _A | Operating free-air temperature | -20 | | 85 | °C |
| T _J | Junction temperature | -20 | | 105 | °C |
| T _{CASE} | Case temperature | -20 | | 105 | °C |
| T _{PCB} | PCB temperature (1 mm away from the device) | -20 | | 92 | °C |

7.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | TUSB2E11 | UNIT |
|-------------------------------|--|-------------|------|
| | | YCG (DSBGA) | |
| | | 15 PINS | |
| R _{θJA} | Junction-to-ambient thermal resistance | 90.5 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 0.6 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 22.9 | °C/W |
| Ψ _{JT} | Junction-to-top characterization parameter | 0.4 | °C/W |
| Ψ _{JB} | Junction-to-board characterization parameter | 22.9 | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------|---|---|-----|-----|-----|------|
| POWER | | | | | | |
| P _{WC_1V8} | Absolute worst case peak power consumption (VDD1V8 only) for power supply budgeting | I2C interface active, GPIOs in output mode, repeater in HS mode with USB transmitting, maximum RX EQ, max TX VOD and PE settings, maximum transition density. T _A = -20°C to 85°C. | | | 280 | mW |
| P _{WC_3V3} | Absolute worst case peak power consumption (VDD3V3 only) for power supply budgeting | I2C interface active, GPIOs in output mode, repeater in HS mode with USB transmitting, maximum RX EQ, max TX VOD and PE settings, maximum transition density. T _A = -20°C to 85°C. | | | 30 | mW |
| P _{WCFS_3V3} | Absolute worst case peak power consumption (VDD3V3 only) for power supply budgeting | I2C interface active, GPIOs in output mode, repeater in FS mode with USB Asynchronous traffic. T _A = -20°C to 85°C. | | | 75 | mW |
| P _{HS_IOC} | USB Audio ISOC High-speed | Maximum TX Vod/Maximum TX PE for both USB and eUSB2. Averaged over 8 ms and only 1 uFrame with data packet. Toff threshold = 1/32. Host Peripheral Mode. | | 35 | | mW |
| P _{PD} | Powered down | Device powered, RESETB=Low, T _A =25°C, (DP/DN Voltage ≤ VDD3V3). | | | 9 | μW |
| P _{Disabled} | Disabled | Device powered, I2C/GPIO interfaces functional but idle, repeater is disabled and put into the lowest power state and non-functional. T _A =25°C, (DP/DN Voltage ≤ VDD3V3). | | 43 | 95 | μW |
| P _{Detach} | USB unconnected | I2C/GPIO interfaces idle, repeater is connected to a eUSB2 PHY and waiting for a USB attach event. T _A = 25°C, (DP/DN Voltage ≤ VDD3V3) | | 43 | 85 | μW |
| P _{Suspend} | L2 Suspend (host mode) | I2C/GPIO interfaces idle, USB link is in L2, repeater is monitoring for a resume/remote wake event. T _A = 25°C, (DP/DN Voltage ≤ VDD3V3). In peripheral mode additional current is present due the DP pull up. | | 45 | 85 | μW |

7.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------------|---|--|-------|-----|-------|------|
| P _{Sleep} | L1 Sleep | I2C/GPIO interfaces idle, repeater is supporting a USB connection, USB link is in L1 (host exists L1 every 1 ms) and repeater is monitoring for a L1 exit event. T _A = 25°C, (DP/DN Voltage ≤ VDD3V3) | | 2.3 | 5 | mW |
| P _{LS_Active} | Low Speed Active | I2C/GPIO interfaces idle, repeater in LS mode, maximum transition density. T _A = 85°C. | | 7.2 | 24 | mW |
| P _{FS1_Active} | Full Speed Active (ASYNCR Traffic) | I2C/GPIO interfaces idle, repeater in FS mode, maximum transition density. T _A = 85°C. | | 45 | 80 | mW |
| P _{FS2_Active} | Full Speed Active (ISO Traffic) | I2C/GPIO interfaces idle, repeater in FS mode, maximum transition density. T _A = 85°C. | | 9 | 24 | mW |
| P _{HS_Idle_Host} | High Speed Idle (Host mode) | L0.Idle. T _A = 85°C. (Typical at 25°C). | | 26 | 70 | mW |
| P _{HS_Idle_Peripheral} | High Speed Idle (Peripheral mode) | L0.Idle. T _A = 85°C. (Typical at 25°C). | | 108 | 200 | mW |
| DIGITAL INPUTS | | | | | | |
| V _{IH} | High level input voltage | GPIO0, GPIO1, GPIO2 (1.2 V Variant) | 0.702 | | | V |
| V _{IH} | High level input voltage | GPIO0, GPIO1, GPIO2 (1.8 V Variant) | 1.053 | | | V |
| V _{IL} | Low-level input voltage | GPIO0, GPIO1, GPIO2 (1.2 V Variant) | | | 0.462 | V |
| V _{IL} | Low-level input voltage | GPIO0, GPIO1, GPIO2 (1.8 V Variant) | | | 0.693 | V |
| V _{IL} | Low-level input voltage | RESETB | | | 0.35 | V |
| V _{IH} | High level input voltage | RESETB | 0.75 | | | V |
| I _{IH} | High level input current | V _{IH} = 1.98 V, VDD3V3=3.0 V or 0 V, VDD1V8=1.62 V or 0 V RESETB, GPIO0, GPIO1 | | | 0.5 | μA |
| I _{IL} | Low level input current | V _{IL} = 0 V, VDD3V3=3.0 V or 0 V, VDD1V8=1.62 V or 0 V RESETB, GPIO0, GPIO1 | | | 0.5 | μA |
| DIGITAL OUTPUTS | | | | | | |
| V _{OH} | High level output voltage | GPIO0, GPIO1, GPIO2, push-pull I/O mode (I _{OH} = 20 μA and maximum 3 pF C _{load}) (1.2 V Variant) | 0.81 | | | V |
| V _{OH} | High level output voltage | GPIO0, GPIO1, GPIO2, push-pull I/O mode (I _{OH} = 20 μA and maximum 3 pF C _{load}) (1.8 V Variant) | 1.21 | | | V |
| V _{OL} | Low level output voltage | GPIO0, GPIO1, GPIO2, push-pull I/O mode (I _{OL} = 1 mA) (1.2 V Variant) | | | 0.25 | V |
| V _{OL} | Low level output voltage | GPIO0, GPIO1, GPIO2, push-pull I/O mode (I _{OL} = 1 mA) (1.8 V Variant) | | | 0.35 | V |
| I _{OL_PP} | Low level output current in push-pull mode | GPIO0, GPIO1, GPIO2 (1.2 V Variant), VOL=0.4 V | 2.5 | 4 | 5.6 | mA |
| I _{OL_PP} | Low level output current in push-pull mode | GPIO0, GPIO1, GPIO2 (1.8 V Variant), VOL=0.4 V | 4 | 6 | 8 | mA |
| I _{OH_PP} | High level output current in push-pull mode | GPIO0, GPIO1, GPIO2, push-pull I/O mode, VOH=0.9 V (1.2 V Variant) | 22 | | | μA |
| I _{OH_PP} | High level output current in push-pull mode | GPIO0, GPIO1, GPIO2, push-pull I/O mode, VOH=0.9 V (1.8 V Variant) | 50 | | | μA |
| I2C (SDA, SCL) | | | | | | |
| V _{IL} | Low level input voltage, 1.2 V variant | SDA, SCL, V _{I2C_Pullup} = 1.08 V | | | 0.387 | V |

7.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------|--|---|-------|-----|-------|------|
| V _{IL} | Low level input voltage, 1.8 V variant | SDA, SCL, V _{I2C_Pullup} = 1.96 V | | | 0.588 | V |
| V _{IH} | High level input voltage, 1.2 V variant | SDA, SCL, V _{I2C_Pullup} = 1.08 V | 0.833 | | | V |
| V _{IH} | High level input voltage, 1.8 V variant | SDA, SCL, V _{I2C_Pullup} = 1.96 V | 1.372 | | | V |
| V _{HYS} | Input hysteresis, 1.2 V variant | V _{I2C_Pullup} = 1.08 V | 0.020 | | | V |
| V _{HYS} | Input hysteresis, 1.8 V variant | V _{I2C_Pullup} = 1.96 V | 0.098 | | | V |
| I _{IH} | High level input leakage current | V _{IH} = 1.98 V | | | 0.5 | μA |
| I _{IL} | Low level input leakage current | V _{IL} = 0 V | | | 0.5 | μA |
| V _{OL} | Low level output voltage (1 kΩ pull up), 1.2 V variant | I _{OL} = 2.5 mA, V _{I2C_Pullup} = 1.08 V | | | 0.2 | V |
| V _{OL} | Low level output voltage (1 kΩ pull up), 1.8V variant | I _{OL} = 2.5 mA, V _{I2C_Pullup} = 1.96 V | | | 0.3 | V |
| I _{OL} | Open drain drive strength, 1.2 V Variant | V _{OL} = 0.4 V | 1.6 | 2.4 | 3.0 | mA |
| I _{OL} | Open drain drive strength, 1.8 V Variant | V _{OL} = 0.4 V | 8 | 10 | 12.6 | mA |
| UART I/O | | | | | | |
| V _{OLI} | Internal output low | Internal UART output (eDP/eDN) 1.2 V signaling | | | 0.1 | V |
| V _{OHI} | Internal output high | Internal UART output (eDP/eDN) 1.2 V signaling | 0.918 | | 1.32 | V |
| V _{ILI} | Internal input low | Internal UART input (eDP/eDN) 1.2 V signaling | -0.1 | | 0.399 | V |
| V _{IHI} | Internal input high | Internal UART input (eDP/eDN) 1.2 V signaling | 0.819 | | 1.386 | V |
| V _{OLE} | External output low | External UART output (DP/DN) 3.3 V signaling | 0 | | 0.3 | V |
| V _{OHE} | External output high | External UART output (DP/DN) 3.3 V signaling | 2.8 | | 3.6 | V |
| V _{ILE} | External input low | External UART input (DP/DN) 3.3 V signaling | | | 0.8 | V |
| V _{IHE} | External input high | External UART input (DP/DN) 3.3 V signaling | 2 | | | V |
| USB (DP, DN) | | | | | | |
| Z _{inp_Dx} | Impedance to GND, no pull up or pull down | V _{in} =3.6 V, V _{DD3V3} =3.0 V, <i>Input Characteristics</i> ⁽¹⁾ | 390 | | | kΩ |
| C _{IO_Dx} | Capacitance to GND | Measured with VNA at 240 MHz, Driver Hi-Z | | | 10 | pF |
| R _{PUI} | Bus pull-up resistor on upstream facing port (idle) | <i>High-speed Device Speed Identification</i> ⁽¹⁾ | 0.92 | 1.1 | 1.475 | kΩ |
| R _{PUR} | Bus pull-up resistor on upstream facing port (receiving) | <i>High-speed Device Speed Identification</i> ⁽¹⁾ | 1.525 | 2.2 | 2.99 | kΩ |
| R _{PD} | Bus pull-down resistor on downstream facing port | <i>High-speed Device Speed Identification</i> ⁽¹⁾ | 14.35 | 19 | 24.6 | kΩ |
| V _{HSTERM} | Termination voltage in highspeed | The output voltage in the high-speed idle state, <i>High-speed Input Characteristics</i> ⁽¹⁾ | -10 | | 10 | mV |
| USB TERMINATION | | | | | | |
| Z _{HSTERM_P} | Driver Output Resistance (which also serves as high speed termination) | (V _{OH} = 0 to 600 mV) <i>Full-speed (12 Mb/s) Driver Characteristics</i> ⁽¹⁾ , Default, U _{HS_TERM_Px} setting 01 | 40.6 | 45 | 49.4 | Ω |
| Z _{HSTERM_N} | Driver Output Resistance (which also serves as high speed termination) | (V _{OH} = 0 to 600 mV) <i>Full-speed (12 Mb/s) Driver Characteristics</i> ⁽¹⁾ , Default, U _{HS_TERM_Px} setting 01 | 40.6 | 45 | 49.4 | Ω |

7.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------------------|---|--|-------|------|------|------|
| USB INPUT LEVELS LS/FS | | | | | | |
| V _{IH} | High (driven) | Receiver Characteristics ⁽¹⁾ (measured at the connector) | 2 | | | V |
| V _{IHZ} | High (floating) | Receiver Characteristics ⁽¹⁾ (HOST downstream port pull-down resistor enabled and external device pull up 1.5 kΩ ± 5% to 3.0-3.6 V) | 2.7 | | 3.6 | V |
| V _{IL} | Low | Receiver Characteristics ⁽¹⁾ | | | 0.8 | V |
| V _{DI} | Differential Input Sensitivity (hysteresis is off) | (D+)-(D-) ; Differential Input Sensitivity Range for Low-/full-speed ⁽¹⁾ ; (measured at connector) V _{CM} =0.8 V to 2.0 V | | | 0.2 | V |
| USB OUTPUT LEVELS LS/FS | | | | | | |
| V _{OL} | Low | USB Driver Characteristics ⁽¹⁾ , (measured at connector with RL of 1.425 kΩ to 3.6 V.) | 0 | | 0.3 | V |
| V _{OH} | High (Driven) | USB Driver Characteristics ⁽¹⁾ , (measured at the connector with RL of 14.25 kΩ to GND.) | 2.8 | | 3.6 | V |
| Z _{FSTERM} | Driver Series Output Resistance | USB Driver Characteristics ⁽¹⁾ , measured it during VOL or VOH | 28 | | 44 | Ω |
| V _{CRS2} | Output Signal Crossover Voltage | Measured as in Data Signal Rise and Fall Time ⁽¹⁾ , excluding the first transition from the Idle state. With external 1.5 kΩ pull up on DP to 3.0 V | 1.3 | | 2 | V |
| V _{CRS} | Output Signal Crossover Voltage | Measured as in Data Signal Rise and Fall Time ⁽¹⁾ , excluding the first transition from the Idle state | 1.3 | | 2 | V |
| USB INPUT LEVELS HS | | | | | | |
| V _{HSSQ} | High-speed squelch/no-squelch detection threshold | Full-/High-speed Signaling Level ⁽¹⁾ , specification refers to peak differential signal amplitude), measured at 240 MHz with increasing amplitude, U_SQUELCH_THRESHOLD_Px setting 011, V _{CM} = -50 mV to 500 mV | 111 | 128 | 161 | mV |
| V _{HSSQ} | High-speed squelch/no-squelch detection threshold | Full-/High-speed Signaling Levels ⁽¹⁾ , (specification refers to peak differential signal amplitude), measured at 240 MHz with increasing amplitude, U_SQUELCH_THRESHOLD_Px setting 100, V _{CM} = -50 mV to 500 mV | 104 | 125 | 150 | mV |
| V _{HSDSC} | High-speed disconnect detection threshold | Full-/High-speed Signaling Levels ⁽¹⁾ , (specification refers to differential signal amplitude). (HW Default), U_DISCONNECT_THRESHOLD_Px setting 0000, V _{CM} =200 mV to 600 mV | 525 | 575 | 625 | mV |
| V _{HSDSC} | High-speed disconnect detection threshold | Full-/High-speed Signaling Levels ⁽¹⁾ (specification refers to differential signal amplitude). (+25.6%), U_DISCONNECT_THRESHOLD_Px setting 1000, V _{CM} =280 mV to 680 mV | 685 | 757 | 846 | mV |
| EQ _{UHS} | USB high-speed data receiver equalization, (measured indirectly through jitter) | 240 MHz, U_EQ_Px setting 000 | -0.37 | 0.06 | 0.57 | dB |

7.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------------|--|---|------|------|------|------|
| EQ_UHS | USB High-speed data receiver equalization, (measured indirectly through jitter) | 240 MHz, U_EQ_Px setting 010 | 0.62 | 1.09 | 1.57 | dB |
| USB OUTPUT LEVELS HS | | | | | | |
| V_HSOH | High-speed data signaling high | <i>Full-/High-speed Signaling Levels⁽¹⁾</i> , measured single-ended peak voltage per USB 2.0 test measurement spec, U_HS_TX_AMPLITUDE_Px setting 0011, PE disabled, Test load is an ideal 45 Ω to GND on DP and DN | 360 | 400 | 440 | mV |
| V_HSOH | High-speed data signaling high | <i>Full-/High-speed Signaling Levels⁽¹⁾</i> , measured single ended peak voltage per USB 2.0 test measurement spec, U_HS_TX_AMPLITUDE_Px setting 1100, PE disabled, Test load is an ideal 45 Ω to GND on DP and DN | 441 | 490 | 539 | mV |
| V_HSOD | High-speed data signaling swing | Measured p-p, 0%, U_HS_TX_AMPLITUDE_Px setting 0011, PE disabled, Test load is an ideal 45 Ω to GND on DP and DN. | 720 | 800 | 880 | mV |
| V_HSOD | High-speed data signaling swing | Measured p-p, 22.5%, U_HS_TX_AMPLITUDE_Px setting 1100, PE disabled, Test load is an ideal 45 Ω to GND on DP and DN. | 882 | 980 | 1078 | mV |
| V_HSOL | High-speed data signaling low, driver is off termination is on (measured single ended) | <i>Full-/High-speed Signaling Levels⁽¹⁾</i> , PE disabled, test load is an ideal 45 Ω to GND on DP and DN. | -10 | | 10 | mV |
| V_CHIRPJ | Host or hub chirp J level (differential voltage) | <i>Full-/High-speed Signaling Levels⁽¹⁾</i> , (PE is disabled. swing setting has no impact but slew rate control has impact), Test load is an ideal 1.5 kΩ pull up on DP. | 700 | 900 | 1100 | mV |
| V_CHIRPK | Device chirp K level (differential voltage) | <i>Full-/High-speed Signaling Levels⁽¹⁾</i> , (PE is disabled. swing setting has no impact but slew rate control has impact), Test load is an ideal 45 Ω to GND on DP and DN. | -900 | -760 | -500 | mV |
| V_CHIRPK | Host or hub Chirp K level (differential voltage) | <i>Full-/High-speed Signaling Levels⁽¹⁾</i> , (PE is disabled. swing setting has no impact but slew rate control has impact), Test load is an ideal 1.5 kΩ pull up on DP. | -900 | -700 | -500 | mV |
| U2_TXPE | High-speed TX pre-emphasis | U_HS_TX_PRE_EMPHASIS_Px setting 000, test load is an ideal 45 Ω to GND on DP and DN. | 0.25 | 0.5 | 0.75 | dB |
| U2_TXPE | High-speed TX pre-emphasis | U_HS_TX_PRE_EMPHASIS_Px setting 100, test load is an ideal 45 Ω to GND on DP and DN. | 1.7 | 2.1 | 2.5 | dB |
| U2_TXPE_UI | High-speed TX pre-emphasis width | U_HS_TX_PE_WIDTH_Px setting 11 (measured with PE=2.5 dB setting of 101), Test load is an ideal 45 Ω to GND on DP and DN. | 0.54 | 0.65 | 0.77 | UI |
| eUSB2 TERMINATION | | | | | | |
| R_SRC_HS | High-speed transmit source termination impedance | <i>High-Speed Tx Electrical Specification⁽²⁾</i> | 33 | 40 | 47 | Ω |
| ΔR_SRC_HS | High-speed source impedance mismatch | <i>High-Speed Tx Electrical Specification⁽²⁾</i> | | | 4 | Ω |
| R_RCV_DIF | High-speed differential receiver termination (repeater) | <i>High-Speed Rx Electrical Specification⁽²⁾</i> | 74 | 80 | 86 | Ω |

7.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------------------|--|---|-------|-----|-------|------|
| R _{PD} | Pull-down resistors on eDP/eDN | <i>Pull-down</i> ⁽²⁾ , active during LS, FS and HS | 6 | 8 | 10 | kΩ |
| R _{SRC_LSFS} | Transmit output impedance | <i>Low-Speed /Full-Speed DC Specifications for 1.2 V ± 10%</i> ⁽²⁾ , TX output impedance | 28 | 44 | 59 | Ω |
| C _{IO_eDx} | Differential Capacitance | Measured with VNA at 240 MHz, Driver Hi-Z (V _{CM} = 120 mV to 450 mV), measured differentially. | | 3.9 | 5.2 | pF |
| eUSB2 FS/LS INPUT LEVELS | | | | | | |
| V _{IL} | Single-ended input low | <i>Low-Speed /Full-Speed DC Specifications for 1.2 V ± 10%</i> ⁽²⁾ | -0.1 | | 0.399 | V |
| V _{IL} | Single-ended input low | <i>Low-Speed /Full-Speed DC Specifications for 1.0 V ± 10%</i> ⁽²⁾ | -0.1 | | 0.332 | V |
| V _{IH} | Single-ended input high | <i>Low-Speed /Full-Speed DC Specifications for 1.2 V ± 10%</i> ⁽²⁾ | 0.819 | | 1.386 | V |
| V _{IH} | Single-ended input high | <i>Low-Speed /Full-Speed DC Specifications for 1.0 V ± 10%</i> ⁽²⁾ | 0.682 | | 1.1 | V |
| V _{HYS} | Receive single-ended hysteresis voltage | <i>Low-Speed /Full-Speed DC Specifications for 1.2 V ± 10%</i> ⁽²⁾ | 43.2 | | | mV |
| V _{HYS} | Receive single-ended hysteresis voltage | <i>Low-Speed /Full-Speed DC Specifications for 1.0 V ± 10%</i> ⁽²⁾ | 38 | | | mV |
| eUSB2 FS/LS OUTPUT LEVELS | | | | | | |
| V _{OL} | Single-ended output low | <i>Low-Speed /Full-Speed DC Specifications for 1.2 V ± 10%</i> ⁽²⁾ | | | 0.1 | V |
| V _{OL} | Single-ended output low | <i>Low-Speed /Full-Speed DC Specifications for 1.0 V ± 10%</i> ⁽²⁾ | | | 0.1 | V |
| V _{OH} | Single-ended output high | <i>Low-Speed /Full-Speed DC Specifications for 1.2 V ± 10%</i> ⁽²⁾ | 0.918 | | 1.32 | V |
| V _{OH} | Single-ended output high | <i>Low-Speed /Full-Speed DC Specifications for 1.0 V ± 10%</i> ⁽²⁾ | 0.765 | | 1.1 | V |
| eUSB2 HS INPUT LEVELS | | | | | | |
| V _{RX_CM} | Receive DC common mode range (low) | <i>High-Speed Rx Electrical Specification</i> ⁽²⁾ (normative), low DC common mode RX must tolerate | | | 120 | mV |
| V _{RX_CM} | Receive DC common mode range (high) | <i>High-Speed Rx Electrical Specification</i> ⁽²⁾ (normative), high DC common mode RX must tolerate | 280 | | | mV |
| V _{CM_RX_AC} | Receiver AC common mode (50 MHz–480 MHz) | <i>High-Speed Rx Electrical Specification</i> ⁽²⁾ (informative), across the DC common-mode range of 120 mV to 280 mV. (RX capability tested with intentional TX rise/fall time mismatch and prop delay mismatch) | -60 | | 60 | mV |
| C _{RX_CM} | Receive center-tapped capacitance | <i>High-Speed Rx Electrical Specification</i> ⁽²⁾ (informative) | 15 | | 50 | pF |
| V _{EHSSQ} | Squelch/No-squelch detect threshold | <i>High-Speed Rx Electrical Specification</i> ⁽²⁾ , (measured as differential peak voltage at 240 MHz with increasing amplitude) E_SQUELCH_THRESHOLD_Px setting 100, V _{CM} = 120 mV to 450 mV | 60 | 81 | 97 | mV |

7.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------------|---|--|------|------|------|------|
| V _{EHSQ} | Squelch/No-squelch detect threshold | <i>High-Speed Rx Electrical Specification</i> ⁽²⁾ , (measured as differential peak voltage at 240 MHz with increasing amplitude) E_SQUELCH_THRESHOLD_Px setting 110, V _{CM} = 120 mV to 450 mV | 47 | 67 | 83 | mV |
| EQ _{EHS} | eUSB2 high-speed data receiver equalization, (measured indirectly through jitter) | 240 MHz E_EQ_P1x setting 0000 | -0.2 | 0.34 | 0.73 | dB |
| eUSB2 HS OUTPUT LEVELS | | | | | | |
| V _{EHSOD} | Transmit differential (terminated) | Measured p2p, R _L = 80 Ω, E_HS_TX_AMPLITUDE_Px setting 011, ideal 80 Ω Rx differential termination load | 378 | 420 | 462 | mV |
| E_TXPE | High-speed TX Pre-emphasis | E_HS_TX_PRE_EMPHASIS_Px setting 000 | -0.2 | 0 | 0.2 | dB |
| E_TXPE_UI | High-speed TX Pre-emphasis width | E_HS_TX_PE_WIDTH_Px setting 00 | 0.29 | 0.40 | 0.59 | UI |
| V _{E_TX_CM} | Transmit DC common mode | <i>High-Speed Tx Electrical Specification</i> ⁽²⁾ | 170 | | 230 | mV |

(1) USB 2.0 Promoter Group 2000, USB 2.0 Specification USB 2.0 Promoter Group

(2) USB Implementers Forum (2018). Embedded USB2 (eUSB2) Physical Layer Supplement to the USB Revision 2.0 Specification, Rev. 1.2 USB Implementers Forum

7.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|-------------------------------------|---|-----|-----|-------|------|
| USB (DP, DN), HS Driver Switching Characteristics | | | | | | |
| T _{HRSR} | Rise time (10% – 90%) | <i>Data Signal Rise and Fall, Eye Patterns</i> ⁽¹⁾ , U_HS_TX_SLEW_RATE_Px setting 11, ideal 45 Ω to GND loads on DP and DN, pre-emphasis disabled. | 530 | 625 | 740 | ps |
| T _{HFSF} | Fall time (10% – 90%) | <i>Data Signal Rise and Fall, Eye Patterns</i> , U_HS_TX_SLEW_RATE_Px setting 11, ideal 45 Ω to GND loads on DP and DN, pre-emphasis disabled. | 530 | 625 | 740 | ps |
| USB (DP, DN), FS Driver Switching Characteristics | | | | | | |
| T _{FR} | Rise time (10% – 90%) | <i>Data Signal Rise and Fall Time and Full-speed Load</i> ⁽¹⁾ | 4 | | 20 | ns |
| T _{FF} | Fall time (10% – 90%) | <i>Data Signal Rise and Fall Time and Full-speed Load</i> ⁽¹⁾ | 4 | | 20 | ns |
| T _{FRFM} | (T _{FR} /T _{FM}) | <i>Data Signal Rise and Fall, Eye Patterns</i> ⁽¹⁾ , excluding the first transition from the Idle state | 90 | | 111.1 | % |
| USB (DP, DN), LS Driver Switching Characteristics | | | | | | |
| T _{LR} | Rise time (10% – 90%) | <i>Data Signal Rise and Fall Time and Full-speed Load</i> ⁽¹⁾ | 75 | | 300 | ns |
| T _{LF} | Fall time (10% – 90%) | <i>Data Signal Rise and Fall Time and Full-speed Load</i> ⁽¹⁾ | 75 | | 300 | ns |
| eUSB2 (eDP, eDN), HS Driver Switching Characteristics | | | | | | |
| T _{EHSRF} | Rise/fall time (20% – 80%) | <i>Full-Speed/Low-Speed Electrical Specification</i> ⁽²⁾ , ideal 80 Ω Rx differential termination E_HS_TX_SLEW_RATE_Px setting = 01 | 355 | 440 | 525 | ps |

7.6 Switching Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|-----------------------------|---|-----|-----|-------|------|
| T_{EHSRF_M} | Transmit rise/fall mismatch | Full-Speed/Low-Speed Electrical Specification ⁽²⁾ , rise/fall mismatch = absolute delta of (rise – fall time) / (average of rise and fall time). | | | 25 | % |
| eUSB2 (eDP, eDN), LS/FS Driver Switching Characteristics | | | | | | |
| T_{ERF} | Rise/fall time (10% – 90%) | Low-Speed /Full-Speed DC Specifications for 1.2 V ± 10% ⁽²⁾ | 2 | | 6 | ns |
| T_{ERF_MM} | Transmit rise/fall mismatch | Low-Speed /Full-Speed DC Specifications for 1.2 V ± 10% ⁽²⁾ | | | 25 | % |
| I2C (SDA) | | | | | | |
| T_r | Rise time (STD) | Bus Speed = 100 kHz, $C_L = 200$ pF, $R_{PU} = 4$ k Ω , $I_{OL} \cong 1$ mA | 600 | | | ns |
| T_r | Rise time (FM) | Bus Speed = 400 kHz, $C_L = 200$ pF, $R_{PU} = 2.2$ k Ω , $I_{OL} \cong 2$ mA | 180 | | | ns |
| T_r | Rise time (FM+) | Bus Speed = 1 MHz, $C_L = 10$ pF, $R_{PU} = 1$ k Ω , $I_{OL} \cong 4$ mA | 72 | | | ns |
| T_r | Rise time (STD) | Bus Speed = 100 kHz, $C_L = 200$ pF, $R_{PU} = 4$ k Ω , $I_{OL} \cong 2$ mA | | | 1000 | ns |
| T_r | Rise time (FM) | Bus Speed = 400 kHz, $C_L = 200$ pF, $R_{PU} = 1$ k Ω , $I_{OL} \cong 8$ mA | | | 300 | ns |
| T_r | Rise time (FM+) | Bus Speed = 1 MHz, $C_L = 50$ pF, $R_{PU} = 1$ k Ω , $I_{OL} \cong 4$ mA | | | 120 | ns |
| T_f | Fall time (STD) | Bus Speed = 100 kHz, $C_L = 200$ pF, $R_{PU} = 2.2$ k Ω , $I_{OL} \cong 4$ mA | | | 106.5 | ns |
| T_f | Fall time (FM) | Bus Speed = 400 kHz, $C_L = 200$ pF, $R_{PU} = 1$ k Ω , $I_{OL} \cong 8$ mA | | | 106.5 | ns |
| T_f | Fall time (FM+) | Bus Speed = 1 MHz, $C_L = 90$ pF, $R_{PU} = 1$ k Ω , $I_{OL} \cong 8$ mA | | | 81.5 | ns |
| T_f | Fall time (STD) | Bus Speed = 100 kHz, $C_L = 10$ pF, $R_{PU} = 4$ k Ω , $I_{OL} \cong 2$ mA | 6.5 | | | ns |
| T_f | Fall time (FM) | Bus Speed = 400 kHz, $C_L = 10$ pF, $R_{PU} = 2.2$ k Ω , $I_{OL} \cong 4$ mA | 6.5 | | | ns |
| T_f | Fall time (FM+) | Bus Speed = 1 MHz, $C_L = 10$ pF, $R_{PU} = 1$ k Ω , $I_{OL} \cong 8$ mA | 6.5 | | | ns |

(1) USB 2.0 Promoter Group 2000, USB 2.0 Specification USB 2.0 Promoter Group

(2) USB Implementers Forum (2018). Embedded USB2 (eUSB2) Physical Layer Supplement to the USB Revision 2.0 Specification, Rev. 1.2 USB Implementers Forum

7.7 Timing Requirements

| | | MIN | NOM | MAX | UNIT |
|---------------------|--|-----|-----|-----|---------|
| I/O TIMING | | | | | |
| t_{GPIO_PW} | Minimum GPIO pulse width for interrupt event | 8 | | | μ s |
| RESET TIMING | | | | | |
| $t_{VDD1V8_RAM P}$ | Ramp time for VDD1V8 to reach minimum 1.62 V | | | 2 | ms |
| $t_{VDD3V3_RAM P}$ | Ramp time for VDD3V3 to reach minimum 3.0 V | | | 2 | ms |
| $t_{aRESETB}$ | Duration for RESETB to be asserted low to complete reset while powered | 10 | | | us |

7.7 Timing Requirements (continued)

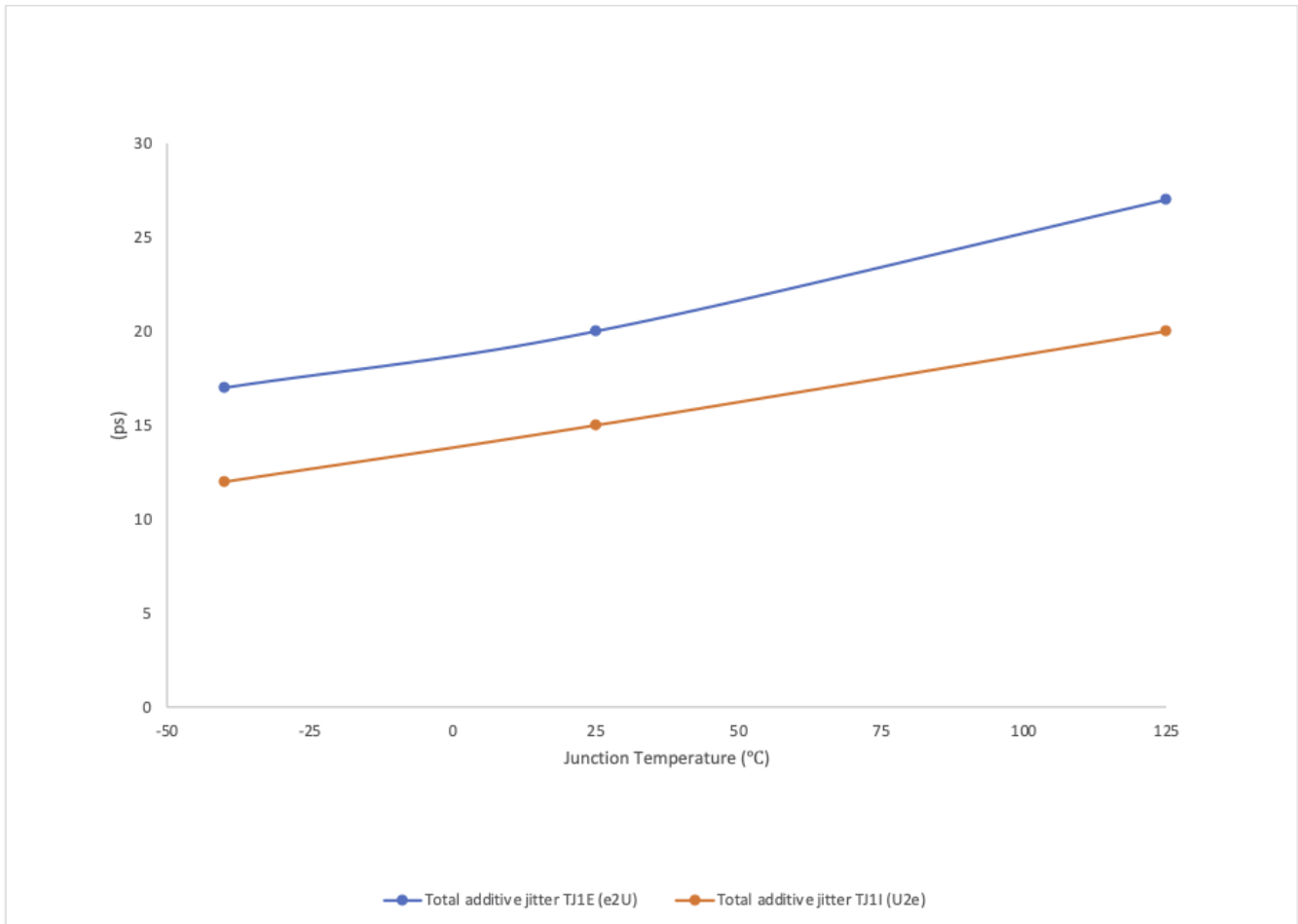
| | | MIN | NOM | MAX | UNIT |
|----------------------------|--|------|-----|------|------|
| t_{RH_READY} | Time for the device to be ready to accept RAP and I ² C requests and eUSB2 interface to be ready after RESETB is de-asserted or (VDD1V8 and VDD3V3) reach the minimum recommended voltages, whichever is later. | | | 3 | ms |
| t_{RS_READY} | Time for the device to be ready to accept RAP and I ² C requests and eUSB2 interface to be ready after a soft reset through I ² C. | | | 350 | μs |
| REPEATER TIMING | | | | | |
| T_{J1E} | Total additive jitter for eUSB2 to USB 2.0 (output jitter – input jitter) of the repeater. | | 20 | 42 | ps |
| T_{J1I} | Total additive jitter for USB 2.0 to eUSB2 (output jitter – input jitter) of the repeater. | | 17 | 42 | ps |
| $T_{e_to_U_DJ1}$ | eUSB2 to USB 2.0 repeater FS jitter to next transition (Per <i>Low-Speed / Full-Speed DC Specifications for 1.2 V ± 10%</i> ⁽¹⁾ condition for supply and GND delta). | -6.0 | | +6.0 | ns |
| $T_{U_to_e_DJ1}$ | USB 2.0 to eUSB2 repeater FS jitter to next transition (Per <i>Low-Speed / Full-Speed DC Specifications for 1.2 V ± 10%</i> ⁽¹⁾ condition for supply and GND delta). | -3.0 | | +3.0 | ns |
| T_{DJ2_e2U} | repeater FS paired transition jitter in eUSB2 to USB 2.0 direction (relaxed relative to THDJ2 defined by USB 2.0 ± 1 ns). eUSB2 in 1.2 V signaling mode. | -1.5 | | +1.5 | ns |
| T_{DJ2_U2e} | repeater FS paired transition jitter in USB 2.0 to eUSB2 direction (relaxed relative to THDJ2 defined by USB 2.0 ± 1 ns). eUSB2 in 1.2 V signaling mode. | -1.5 | | +1.5 | ns |
| MODE TIMING | | | | | |
| T_{MODE_SWITCH} | Time needed to change mode from UART bypass mode to and from USB mode | | | 1 | μs |
| T_{UART_START} | Time needed to start transmitting UART data, post toggling GPIO0 to '0' when in UART strap mode (SCL=1, SDA=0 at power-up) | | | 2 | ms |
| I2C (FM+) | | | | | |
| t_{SU_STA} | Start setup time, SCL ($T_r=72$ ns – 120 ns), SDA ($T_f=6.5$ ns – 81.5 ns), 1 MHz FM+ | 260 | | | ns |
| t_{SU_STO} | Stop setup time, SCL ($T_r=72$ ns – 120 ns), SDA ($T_f=6.5$ ns – 81.5 ns), 1 MHz FM+ | 260 | | | ns |
| t_{HD_STA} | Start hold time, SCL ($T_r=72$ ns – 120 ns), SDA ($T_f=6.5$ ns – 81.5 ns), 1 MHz FM+ | 260 | | | ns |
| t_{SU_DAT} | Data input or false start/stop, setup time, SCL ($T_r=72$ ns – 120 ns), SDA ($T_f=6.5$ ns – 81.5 ns), 1 MHz FM+ | 50 | | | ns |
| t_{HD_DAT} | Data input or False start/stop, hold time, SCL ($T_r=72$ ns – 120 ns), SDA ($T_f=6.5$ ns – 81.5 ns), 1 MHz FM+ | 0 | | | ns |
| t_{VD_DAT}, t_{VD_ACK} | SDA output delay, SCL ($T_r=72$ ns – 120 ns), SDA ($T_f=6.5$ ns – 81.5 ns), 1 MHz FM+ | 20 | | 450 | ns |
| $t_{HD_DAT_SL}$ | Data hold time when device is transmitting | 6.67 | | | ns |
| t_{SP} | Glitch width suppressed | 50 | | 91 | ns |
| t_{BUF} | Bus free time between a STOP and START condition (Controller minimum spec that device must tolerate) | 0.5 | | | μs |
| t_{LOW} | Low period for SCL clock (minimum spec that device must tolerate) | 0.5 | | | μs |
| t_{HIGH} | High period for SCL clock (minimum spec that device must tolerate) | 0.26 | | | μs |
| I2C (FM) | | | | | |
| t_{SU_STO} | Stop setup time, SCL ($T_r=180$ ns – 300 ns), SDA ($T_f=6.5$ ns – 106.5 ns), 400 kHz FM | 600 | | | ns |
| t_{HD_STA} | Start hold time, SCL ($T_r=180$ ns – 300 ns), SDA ($T_f=6.5$ ns – 106.5 ns), 400 kHz FM | 600 | | | ns |
| t_{SU_STA} | Start setup time, SCL ($T_r=180$ ns – 300 ns), SDA ($T_f=6.5$ ns – 106.5 ns), 400 kHz FM | 600 | | | ns |

7.7 Timing Requirements (continued)

| | | MIN | NOM | MAX | UNIT |
|--|--|------|-----|------|------|
| t _{SU_DAT} | Data input or false start/stop, setup time, SCL (T _r =180 ns – 300 ns), SDA (T _r =6.5 ns – 106.5 ns), 400 kHz FM | 100 | | | ns |
| t _{HD_DAT} | Data input or false start/stop, hold time, SCL (T _r =180 ns – 300 ns), SDA (T _r =6.5 ns – 106.5 ns), 400 kHz FM | 0 | | | ns |
| t _{VD_DAT} , t _{VD_ACK} | SDA output delay, SCL (T _r =180 ns – 300 ns), SDA (T _r =6.5 ns – 106.5 ns), 400 kHz FM | 20 | | 900 | ns |
| t _{HD_DAT_SL} | Data hold time when device is transmitting | 13.5 | | | ns |
| t _{SP} | Glitch width suppressed | 50 | | 91 | ns |
| t _{BUF} | Bus free time between a STOP and START condition (minimum spec that device must tolerate) | 1.3 | | | μs |
| t _{LOW} | Low period for SCL clock (minimum spec that device must tolerate) | 1.3 | | | μs |
| t _{HIGH} | High period for SCL clock (Master minimum spec that device must tolerate) | 0.6 | | | μs |
| I2C (STD) | | | | | |
| t _{SU_STO} | Stop setup time, SCL (T _r =600 ns – 1000 ns), SDA (T _r =6.5 ns – 106.5 ns), 100 kHz STD | 4 | | | μs |
| t _{HD_STA} | Start hold time, SCL (T _r =600 ns – 1000 ns), SDA (T _r =6.5 ns – 106.5 ns), 100 kHz STD | 4 | | | μs |
| t _{SU_STA} | Start setup time, SCL (T _r =600 ns – 1000 ns), SDA (T _r =6.5 ns – 106.5 ns), 100 kHz STD | 4.7 | | | μs |
| t _{SU_DAT} | Data input or false start/stop, setup time, SCL (T _r =600 ns – 1000 ns), SDA (T _r =6.5 ns – 106.5 ns), 100 kHz STD | 250 | | | ns |
| t _{HD_DAT} | Data input or false start/stop, hold time, SCL (T _r =600 ns – 1000 ns), SDA (T _r =6.5 ns – 106.5 ns), 100 kHz STD | 5 | | | μs |
| t _{VD_DAT} , t _{VD_ACK} | SDA output delay, SCL (T _r =600 ns – 1000 ns), SDA (T _r =6.5 ns – 106.5 ns), 100 kHz STD | | | 3.45 | μs |
| t _{HD_DAT_SL} | Data hold time when device is transmitting | 13.5 | | | ns |
| t _{SP} | Glitch width suppressed | 50 | | 91 | ns |
| t _{BUF} | Bus free time between a STOP and START condition (minimum spec that device must tolerate) | 4.7 | | | μs |
| t _{LOW} | Low period for SCL clock (minimum spec that device must tolerate) | 4.7 | | | μs |
| t _{HIGH} | High period for SCL clock (minimum spec that device must tolerate) | 4.0 | | | μs |

- (1) USB Implementers Forum (2018). Embedded USB2 (eUSB2) Physical Layer Supplement to the USB Revision 2.0 Specification, Rev. 1.2 USB Implementers Forum

7.8 Typical Characteristics



TJ1E is for egress direction from eUSB2 to USB and TJ1I is for ingress direction from USB to eUSB2

Figure 7-1. Total Additive Jitter (Typical)

8 Parameter Measurement Information

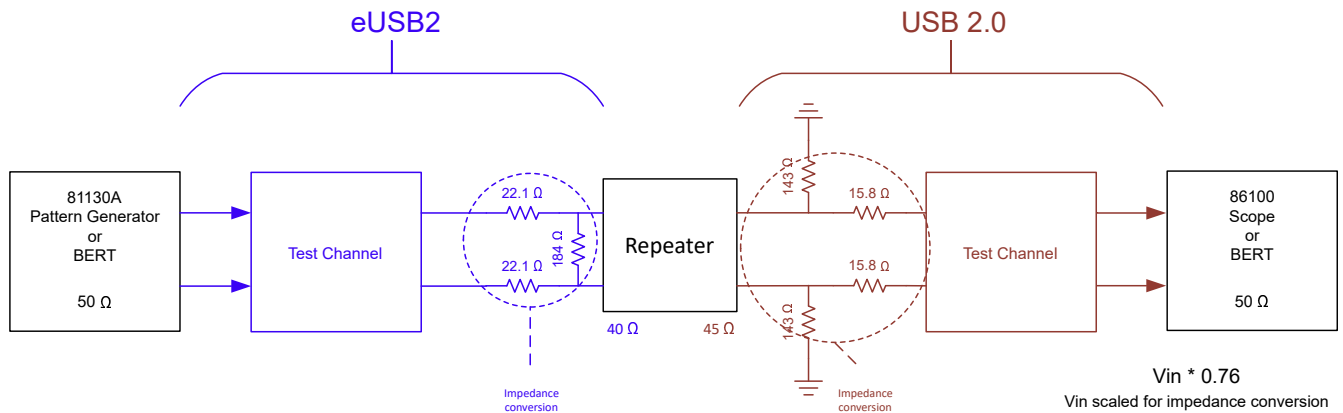


Figure 8-1. USB 2.0 TX Output (Egress) Jitter, Eye Mask Test Setup

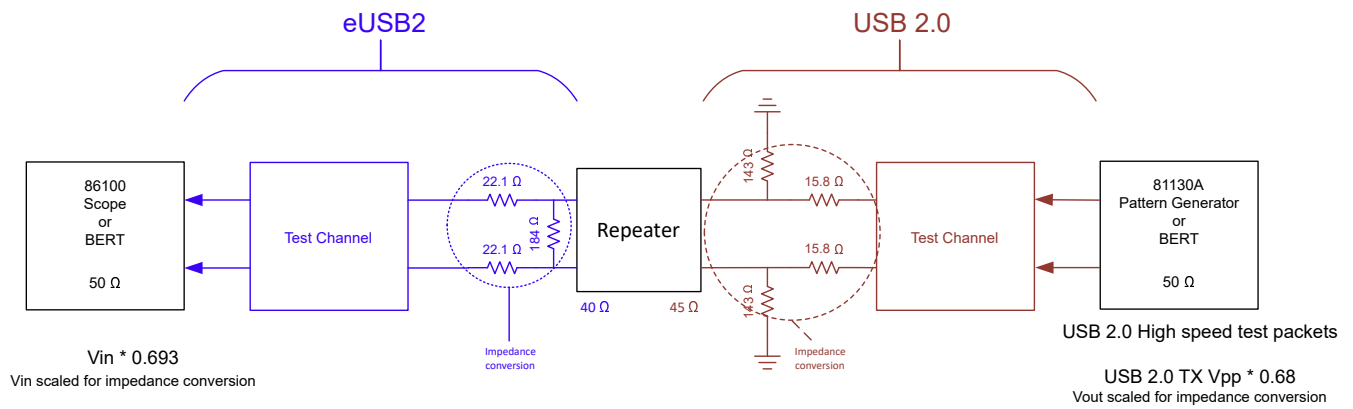


Figure 8-2. eUSB2 TX Output (Ingress) Jitter, Eye Mask Test Setup

9 Detailed Description

9.1 Overview

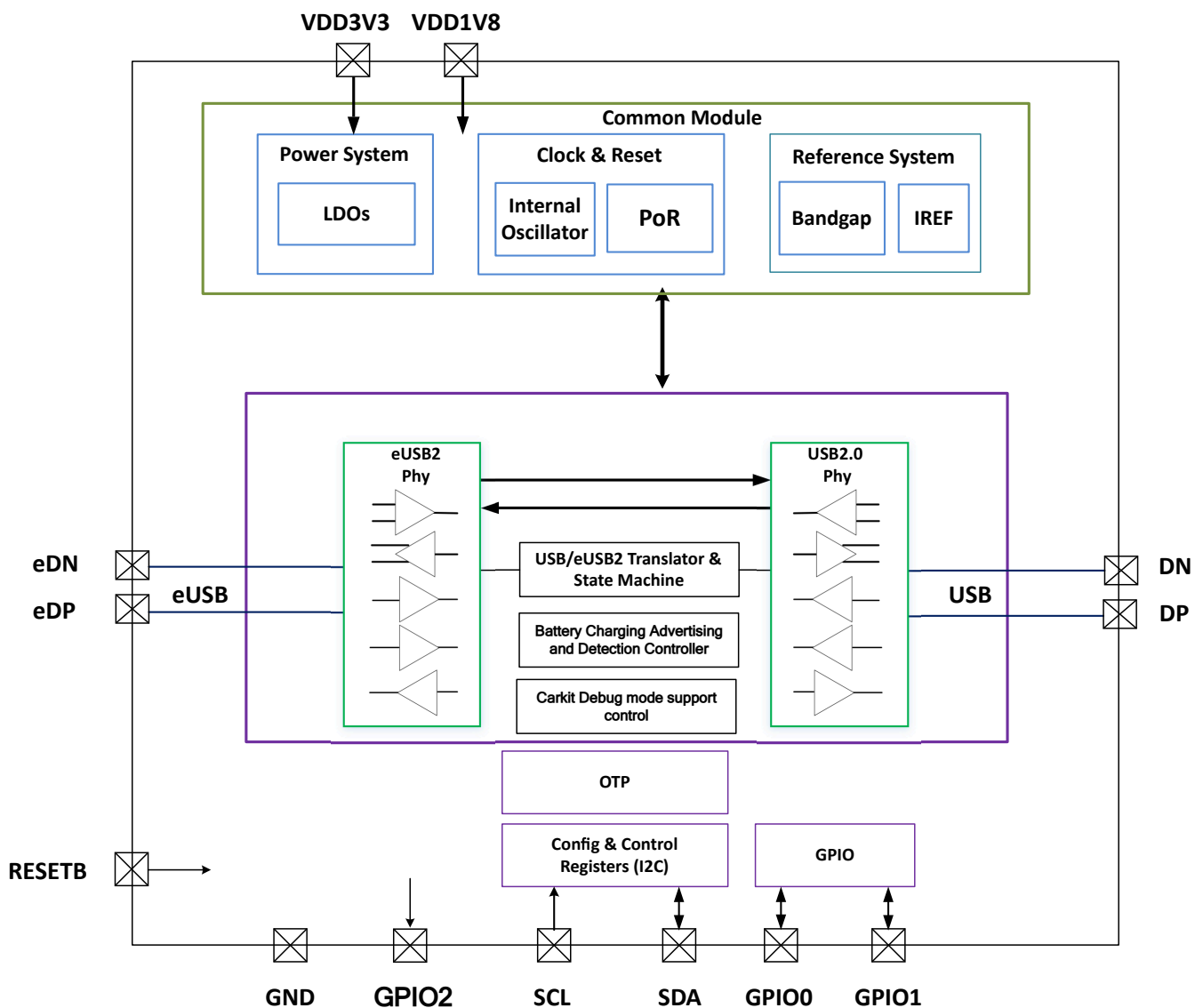
The TUSB2E11 is an eUSB2 to USB 2.0 repeater that resides between the SoC with an eUSB2 port and an external connector that supports USB 2.0. It can be configured by the register access protocol (RAP) or through the I²C. The repeater is configurable as either a host or device repeater (DRD repeater).

I²C port supports up to 1 MHz (fast mode plus) for internal register access. A subset of internal registers can be accessed through the register access protocol. Simultaneous register access using RAP and through the I²C is supported with RAP having priority over I²C.

To power up in I²C mode, both SDA and SCL should have pull-up resistors to appropriate I²C bus voltage.

GPIO2 output pin can be configured to provide an active low open drain or selectable active low or active high push-pull level sensitive interrupt output to the SoC.

9.2 Functional Block Diagram



9.3 Feature Description

TUSB2E11 is an USB compliant eUSB2 to USB 2.0 repeater supporting both device and host modes. Both USB and eUSB2 offer fully tunable TX and RX through I²C. Additionally, USB TX and RX can be tuned when I²C is not used.

9.4 Device Functional Modes

9.4.1 Repeater Mode

Upon de-assertion of RESETB or software reset and after t_{RH_READY} or t_{RS_READY} , TUSB2E11 will enable and enter the default state and be ready to accept eUSB2 packets, RAP, and I²C requests. The repeater will either be in host repeater mode or peripheral repeater mode depending on the receipt of either host mode enable or peripheral mode enable.

When TUSB2E11 is repeating high-speed packets, either from eUSB2 to USB 2.0 or from USB 2.0 to eUSB2, up to 4UI (may include partial UI) of HS SOP could be truncated. This is the same as a standard USB 2.0 HUB operating in high speed mode which could truncate up to 4UI.

When TUSB2E11 is repeating high-speed packets from eUSB2 to USB 2.0, up to 1.6UI of random dribble bits (may include partial UI) could be introduced after HS EOP. This is the less than a standard USB 2.0 HUB operating in high speed mode which could have up to 4UI of random dribble bits.

When TUSB2E11 is repeating high-speed packets from USB 2.0 to eUSB2, up to 5UI of random dribble bits (may include partial UI) could be introduced after HS EOP. This is more than a standard USB 2.0 HUB operating in high speed mode which could have up to 4UI of random dribble bits. eDSPr/eUSPr receiving eUSB2 high-speed packets should ignore 5UI of dribble bits after detecting no stuffed bit insertion indicating HS EOP.

Table 9-1. Number of Hubs Supported with Host and Peripheral Repeater

| Number of eUSB2 Repeaters | Number of Hubs Operating at HS | Number of Hubs Operating at FS | |
|---------------------------|--------------------------------|--------------------------------|--|
| 1 | 4 | 2 | Number of hubs operating at FS is reduced due to $T_{e_to_U_DJ1}$ and T_{RJR1} . Number of hubs operating at HS is reduced due to 2 3 1 SOP truncation and EOP dribble |
| 2 | 3 | 1 | |
| 0 | 5 | 5 | non-eUSB2 system for reference |

9.4.2 Power Down Mode

RESETB could be used as a power down pin when asserted low. Power down mode will put TUSB2E11 in lowest power mode.

9.4.3 Disabled Mode

The repeater could be disabled by setting DISABLE bit through the I²C.

9.4.4 UART Mode

In I²C mode GPIO0 will default to being an enable control for Carkit UART mode. GPIO0 is an active low signal to enable Carkit UART mode. GPIO0 is intended to be controlled through APU or SoC. When APU or SoC is not powered on or the firmware has not been loaded, the GPIO0 will be low, enabling the UART mode to allow APU or SoC debug interface to be accessed through the USB port.

Default Carkit UART direction is DP → eDP (RX) and eDN → DN (TX).

On the rising edge of GPIO0, followed by T_{MODE_SWITCH}, TUSB2E11 will enable and enter default state and be ready to accept eUSB2 port reset, configuration or RAP. The repeater mode will be configured as host or peripheral depending on the eUSB2-defined configuration received from eUSBr and acknowledged by the repeater.

UART mode enable is controlled through GPIO0 after power up. This can be changed through UART_use_bit1_P1 bit in UART-PORT1 register, so UART mode enable could be controlled through a register instead of GPIO0.

9.4.5 Auto-Resume ECR

Optional host repeater auto-resume is supported by TUSB2E11 in L1/L2 by driving Resume K at D+/D- until SOResume is received from eDSPr. In addition, TUSB2E11 eUSPh will hold Remote Wake line state until SOResume is received from eDSPr.

This auto-resume feature provides host controller extra time to exit low power state and issue SOResume while TUSB2E11 UDSP drives resume within 1 ms (TURSM) hub resume timing requirement. To take advantage of this low power feature, host controller shall implement low power mechanism to detect wake on eDSPr lines while host controller is in low power state.

This auto-resume is not needed if host controller is capable of initiating SOResume within 1 ms of detecting Remote Wake on eDSPr.

This auto-resume is enabled by default but can be disabled via bit 6 of register 0x78. This auto-resume ECR mode is disabled when L2 interrupt mode is enabled. When L2 interrupt mode is enabled, resume K at D+/D- is still driven when Remote wake is detected on UDSP but eUSPh will be held at SE0 instead of in Remote Wake state. See the *L2 State Interrupt Modes* section for more details.

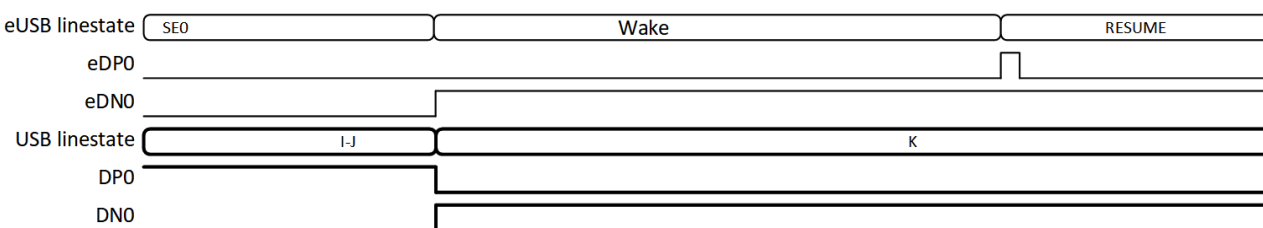


Figure 9-1. Timing Diagram for Auto-Resume for HS/FS

9.4.6 L2 State Interrupt Modes

To prevent signaling on eUSB2 while the eDSP is powered off, both L2 remote wake interrupt and disconnect event interrupt modes should be enabled. The special remote wake sequence when L2 remote wake interrupt mode is enabled.

- System enables interrupt USB_REMOTE_WAKE_P1.
- Repeater is in host mode and has received a CM.L2.
- Repeater detects wake on USB 2.0
- Repeater asserts interrupt.
- Repeater reflects *resume* on USB 2.0, but does not signal wake on eUSB2.
- Repeater waits for eDSPr to signal start of resume with no intervening configuration, connect, or reset sequence.
- Repeater and eDSP follow normal eUSB2 protocol to signal resume starting and ending in L0.

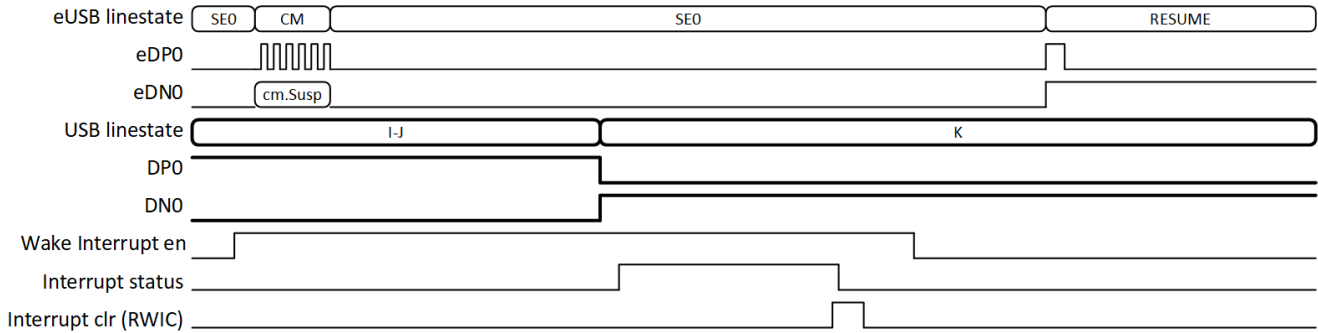


Figure 9-2. Timing Diagram for Wake Interrupt for HS/FS

The special wake on disconnect sequence when disconnect event interrupt mode is enabled

- System enables interrupt USB_DISCONNECT_P1.
- Repeater is in host mode and has received a CM.L2.
- Repeater detects SE0 for disconnect on USB 2.0.
- Repeater asserts interrupt.
- Interrupt must be cleared prior to eDSPr reinitializing TUSB2E11 as a host.
- Repeater does not signal or report USB 2.0 SE0 on eUSB2.
- Repeater waits for eDSPr to power up, which starts with port reset announcement.
- Repeater and eDSP follow normal eUSB2 protocol, ending in unconnected state of host mode.

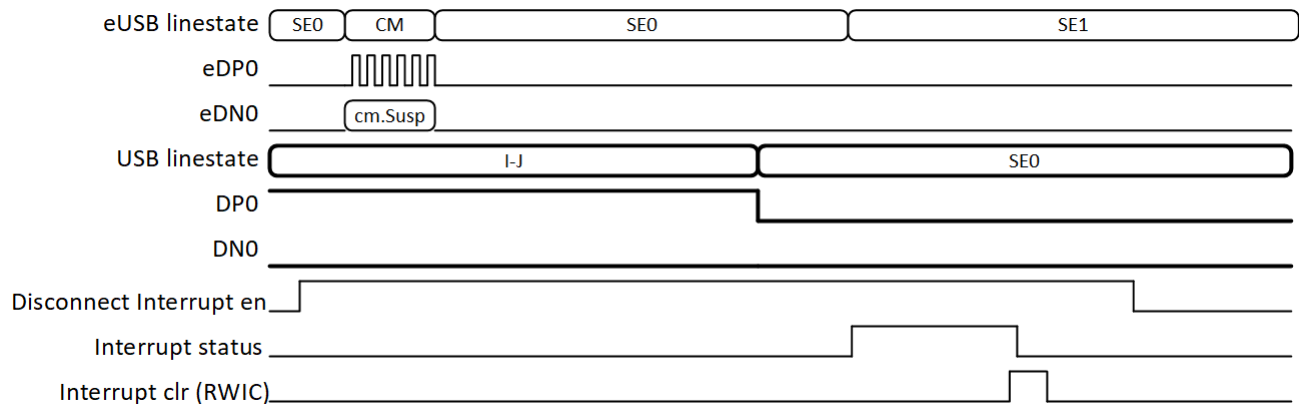


Figure 9-3. Timing Diagram for Disconnect Interrupt for HS/FS

9.4.7 Attach Detect Interrupt Mode

When attach event detect is enabled TUSB2E11 will issue an interrupt event instead of signaling attach on eUSB2.

- System enables interrupt USB_DETECT_ATTACH_P1. Interrupt has to be enabled prior to any connect event.
- Repeater is in host mode.
- Repeater detects attach on USB 2.0.
- Repeater debounces attach for 60 μ s and asserts interrupt instead of signaling attach on eUSB2.
- Interrupt must be disabled prior to eDSPr reinitializing as a host to process attach through normal mechanism.

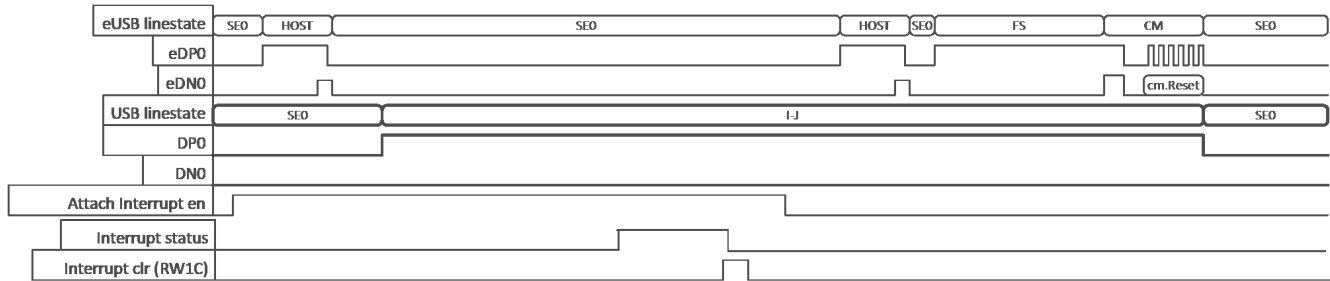


Figure 9-4. Timing Diagram for Attach Detect Interrupt for HS/FS

9.4.8 GPIO Mode

GPIO0

GPIO0 pin will be in input mode at power up, will be sampled during reset.

GPIO0 defaults to active low UART mode (bypass mode) enable control after power up. This can be changed through the `UART_use_bit1_P1` bit in `UART-PORT1` register, so GPIO0 can be repurposed. Refer to [UART Mode](#).

GPIO0 pin can be configured to be input or output mode through the I²C register write. Output event is selected through the I²C register. Refer to *GPIO0_CONFIG register* for more information.

GPIO0 input status change can be reported through the GPIO2 as an interrupt if enabled through the I²C. Status change trigger can be programmed to be edge trigger or level trigger through the I²C.

GPIO0 pin in output mode will default to open drain output but can be configured to be push-pull output. GPIO0 pin can drive up to 3 pF loads when in push-pull mode.

GPIO0 pin will revert back to input upon RESETB assert, de-assert, or soft reset.

In non I²C mode, GPIO0 is used for USB PHY tuning.

GPIO1

GPIO1 pin will be in input mode at power up, will be sampled during reset.

GPIO1 will be configured as an enable control for battery charger detection in repeater default state if `DEFAULT_STATE_BC_P1` is set to 0x01 through the `BC_CONTROL` register.

GPIO1 pin can be configured to be input or output mode through the I²C register write. Output event is selected through the I²C register. Refer to *GPIO1_CONFIG register*.

GPIO1 input status change can be reported through the GPIO2 as an interrupt if enabled through the I²C. Status change trigger can be programmed to be edge trigger or level trigger through the I²C.

GPIO1 pin in output mode will default to open drain output but can be configured to be push-pull output. GPIO1 pin can drive up to 3 pF loads when in push-pull mode.

GPIO1 pin will revert back to input upon RESETB assert, de-assert, or soft reset.

In non I²C mode, GPIO1 is used for USB PHY tuning.

GPIO2

GPIO2 pin will default to open drain interrupt (INT) active low output at power up but can be programmed through the I²C to be a push-pull output. In push-pull mode, it can be programmed to be either active high or active low. Interrupt output will be level sensitive interrupt. Trigger events can be selected through the I²C.

Connect GPIO2 to APU to use interrupt functions and a pull-up resistor (open drain mode).

GPIO2 interrupt output can be configured through the INT_ENABLE and INT_STATUS registers.

GPIO2 can be configured as battery charger detect indicator instead of the interrupt output through the BC_CONTROL register.

In non I²C mode, GPIO2 is used for USB PHY tuning.

9.4.9 USB 2.0 High-Speed HOST Disconnect Detection

USB 2.0 specification does not specify high-speed output differential swing V_{OD} during disconnect without external load. Only chirp level and HS host disconnect threshold are specified. Specification implicitly assumes high-speed output differential swing V_{OD} will double during disconnect. However, the high-speed output differential swing during disconnect depends on the USB 2.0 TX output swing and pre-emphasis setting as the common mode voltage increase will saturate the output swing level and might not double.

HS host disconnect threshold shall be adjusted to provide the most margin to avoid false disconnect as well as failure to detect a disconnect. See [Table 9-2](#).

Table 9-2. Recommended USB 2.0 High-speed HOST Disconnect Thresholds per USB HSTX Amplitude and Pre-Emphasis

| USB HS TX Amplitude (Vp-p) | USB HS TX Pre-Emphasis | | | | | |
|----------------------------|------------------------|-------------|-------------|-------------|-------------|-------------|
| | 0.5 dB (0h) | 0.9 dB (1h) | 1.2 dB (2h) | 1.7 dB (3h) | 2.1 dB (4h) | 2.5 dB (5h) |
| 740 mV (0h) | 545 mV (1h) | 545 mV (1h) | 545 mV (1h) | 545 mV (1h) | 545 mV (1h) | 545 mV (1h) |
| 760 mV (1h) | 565 mV (2h) | 565 mV (2h) | 565 mV (2h) | 565 mV (2h) | 565 mV (2h) | 565 mV (2h) |
| 780 mV (2h) | 585 mV (3h) | 585 mV (3h) | 585 mV (3h) | 585 mV (3h) | 585 mV (3h) | 585 mV (3h) |
| 800 mV (3h) | 585 mV (3h) | 585 mV (3h) | 585 mV (3h) | 585 mV (3h) | 585 mV (3h) | 585 mV (3h) |
| 820 mV (4h) | 605 mV (4h) | 605 mV (4h) | 605 mV (4h) | 605 mV (4h) | 605 mV (4h) | 605 mV (4h) |
| 840 mV (5h) | 625 mV (5h) | 625 mV (5h) | 625 mV (5h) | 625 mV (5h) | 625 mV (5h) | 625 mV (5h) |
| 860 mV (6h) | 645 mV (6h) | 645 mV (6h) | 645 mV (6h) | 645 mV (6h) | 625 mV (5h) | 625 mV (5h) |
| 880 mV (7h) | 645 mV (6h) | 645 mV (6h) | 645 mV (6h) | 645 mV (6h) | 645 mV (6h) | 645 mV (6h) |
| 900 mV (8h) | 665 mV (7h) | 665 mV (7h) | 665 mV (7h) | 665 mV (7h) | 665 mV (7h) | 645 mV (6h) |
| 920 mV (9h) | 685 mV (8h) | 685 mV (8h) | 685 mV (8h) | 665 mV (7h) | 665 mV (7h) | 665 mV (7h) |
| 940 mV (Ah) | 685 mV (8h) | 685 mV (8h) | 685 mV (8h) | 685 mV (8h) | 665 mV (7h) | 665 mV (7h) |
| 960 mV (Bh) | 705 mV (9h) | 705 mV (9h) | 705 mV (9h) | 685 mV (8h) | 685 mV (8h) | 665 mV (7h) |
| 980 mV (Ch) | 725 mV (Ah) | 705 mV (9h) | 705 mV (9h) | 705 mV (9h) | 685 mV (8h) | 685 mV (8h) |
| 1000 mV (Dh) | 725 mV (Ah) | 725 mV (Ah) | 705 mV (9h) | 705 mV (9h) | 685 mV (8h) | 685 mV (8h) |
| 1020 mV (Eh) | 725 mV (Ah) | 725 mV (Ah) | 725 mV (Ah) | 705 mV (9h) | 705 mV (9h) | 685 mV (8h) |
| 1040 mV (Fh) | 745 mV (Bh) | 725 mV (Ah) | 725 mV (Ah) | 705 mV (9h) | 705 mV (9h) | 685 mV (8h) |

9.5 Manufacturing Test Modes

Below test procedures show how to use I²C to enter test modes to perform continuity test of DP/DM during manufacturing or debug. During this mode the TUSB2E11 will not operate as a repeater.

9.5.1 USB DP Test Procedure

I²C Commands to use DP pull-up to test DP/DM continuity:

Enable GPIOs and DP Pull-up:

h00, hA0 <-set gpio0 to push-pull output mode

h40, hA0 <-set gpio1 to push-pull output mode

hD5, h28

hD6, h04

hD7, h10 <-DP pull-up is now on

hCE, h18

hDC, h15 <-muxes DP / DM status onto GPIO lines

Status Readback Check:

h00 = hA0 <-DM status on bit 4 (normal, DM low)

h40 = hB0 <-DP status on bit 4 (normal, DP high)

h00 = hB0 <-DM status on bit 4 (DP + DM shorted together)

h40 = hA0 <-DP status on bit 4 (DP shorted to ground)

Exit Test Mode:

hB2, h80 <-soft reset (end test)

9.5.2 USB DM Test Procedure

I²C Commands to use DM pull-up to test DP/DM continuity:

Enable GPIOs and DM Pull-up:

h00, hA0 <-set gpio0 to push-pull output mode

h40, hA0 <-set gpio1 to push-pull output mode

hD5, h28

hD6, h04

hD7, h08 <-DM pull-up is now on

hCE, h18

hDC, h15 <-mux DP / DM status onto GPIO lines

Status Readback Check:

h00 = hB0 <-DM status on bit 4 (normal, DM high)

h40 = hA0 <-DP status on bit 4 (normal, DP low)

h40 = hB0 <-DP status on bit 4 (DP + DM shorted together)

h00 = hA0 <-DM status on bit 4 (DM shorted to ground)

Exit Test Mode:

hB2, h80 <-soft reset (end test)

9.6 I²C Target Interface

I²C target interface enables access to internal registers by the system application processor. The primary function of the interface is to enable configuring various PHY parameters, controlling the GPIO pins, and enabling USB-BC functions. TUSB2E11 repeater functions will operate upon power up without requiring I²C configuration.

TUSB2E11 has I²C 7-bit target address of 0x5E. 8-bit address of Write: 0x7C and Read: 0x7D.

I²C default target address could be changed at the factory through one time programming.

I²C drive strength could be changed through the I²C.

Table 9-3. Recommended I²C Drive Strength for I²C Bus Speed, Bus Pull Up and Bus Capacitance

| I ² C FM+ (1 MHz Max) | I ² C drive strength (I _{OL}) selection | | | |
|----------------------------------|--|--------|------|------|
| | I ² C bus pull up R _{PU} | | | |
| C(bus) pF | 1 kΩ | 2.2 kΩ | 4 kΩ | 7 kΩ |
| 10-50 | ≅8 mA | ≅4 mA | N/A | N/A |
| 10-90 | ≅8 mA | N/A | N/A | N/A |
| 10-150 | N/A | N/A | N/A | N/A |
| 10-200 | N/A | N/A | N/A | N/A |

| I ² C FM (400kHz Max) | I ² C drive strength (I _{OL}) selection | | | |
|----------------------------------|--|--------|-------|------|
| | I ² C bus pull up R _{PU} | | | |
| C(bus) pF | 1 kΩ | 2.2 kΩ | 4 kΩ | 7 kΩ |
| 10-50 | ≅8 mA | ≅4 mA | ≅2 mA | N/A |
| 10-90 | ≅8 mA | ≅4 mA | N/A | N/A |
| 10-150 | ≅8 mA | ≅8 mA | N/A | N/A |
| 10-200 | ≅8 mA | N/A | N/A | N/A |

| I ² C STD (100 kHz Max) | I ² C drive strength (I _{OL}) selection | | | |
|------------------------------------|--|--------|-------|-------|
| | I ² C bus pull up R _{PU} | | | |
| C(bus) pF | 1 kΩ | 2.2 kΩ | 4 kΩ | 7 kΩ |
| 10-50 | ≅8 mA | ≅4 mA | ≅2 mA | ≅1 mA |
| 10-90 | ≅8 mA | ≅4 mA | ≅2 mA | ≅1 mA |
| 10-150 | ≅8 mA | ≅4 mA | ≅2 mA | ≅2 mA |
| 10-200 | ≅8 mA | ≅4 mA | ≅2 mA | ≅2 mA |

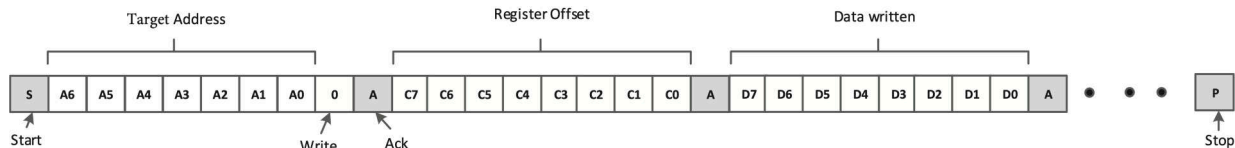


Figure 9-5. I²C Write with Data

The following procedure should be followed to write data to TUSB2E11 I²C registers (refer to [Figure 9-5](#)):

1. The host initiates a write operation by generating a start condition (S), followed by the TUSB2E11 7-bit address and a zero-value “W/R” bit to indicate a write cycle.
2. The TUSB2E11 acknowledges the address cycle.
3. The host presents the register offset within TUSB2E11 to be written, consisting of one byte of data, MSB-first.
4. The TUSB2E11 acknowledges the sub-address cycle.
5. The host presents the first byte of data to be written to the I²C register.
6. The TUSB2E11 acknowledges the byte transfer.

7. The host may continue presenting additional bytes of data to be written, with each byte transfer completing with an acknowledge from the TUSB2E11.
8. The host terminates the write operation by generating a stop condition (P).

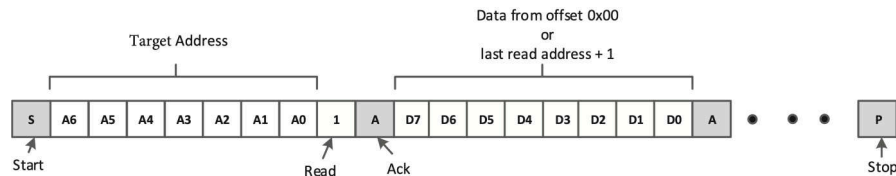


Figure 9-6. I²C Read Without Repeated Start

The following procedure should be followed to read the TUSB2E11 I²C registers without a repeated Start (refer Figure 9-6).

1. The host initiates a read operation by generating a start condition (S), followed by the TUSB2E11 7-bit address and a zero-value “W/R” bit to indicate a read cycle.
2. The TUSB2E11 acknowledges the 7-bit address cycle.
3. Following the acknowledge the host continues sending clock.
4. The TUSB2E11 transmit the contents of the memory registers MSB-first starting at register 00h or last read register offset+1. If a write to the I²C register occurred prior to the read, then the TUSB2E11 shall start at the register offset specified in the write.
5. The TUSB2E11 waits for either an acknowledge (ACK) or a not-acknowledge (NACK) from the host after each byte transfer; the I²C host acknowledges reception of each data byte transfer.
6. If an ACK is received, the TUSB2E11 transmits the next byte of data as long as host provides the clock. If a NAK is received, the TUSB2E11 stops providing data and waits for a stop condition (P).
7. The host terminates the write operation by generating a stop condition (P).

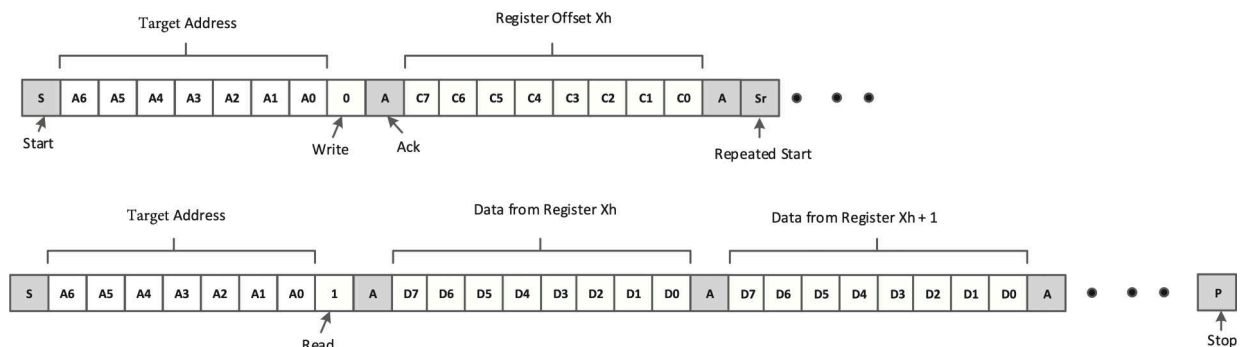


Figure 9-7. I²C Read with Repeated Start

The following procedure should be followed to read the TUSB2E11 I²C registers with a repeated Start (refer Figure 9-7).

1. The host initiates a read operation by generating a start condition (S), followed by the TUSB2E11 7-bit address and a zero-value “W/R” bit to indicate a write cycle.
2. The TUSB2E11 acknowledges the 7-bit address cycle.
3. The host presents the register offset within TUSB2E11 to be written, consisting of one byte of data, MSB-first.
4. The TUSB2E11 acknowledges the register offset cycle.
5. The host presents a repeated start condition (Sr).
6. The host initiates a read operation by generating a start condition (S), followed by the TUSB2E11 7-bit address and a one-value “W/R” bit to indicate a read cycle.
7. The TUSB2E11 acknowledges the 7-bit address cycle.
8. The TUSB2E11 transmit the contents of the memory registers MSB-first starting at the register offset.
9. The TUSB2E11 shall wait for either an acknowledge (ACK) or a not-acknowledge (NACK) from the host after each byte transfer; the I²C host acknowledges reception of each data byte transfer.

10. If an ACK is received, the TUSB2E11 transmits the next byte of data as long as host provides the clock. If a NAK is received, the TUSB2E11 stops providing data and waits for a stop condition (P).
11. The host terminates the read operation by generating a stop condition (P).

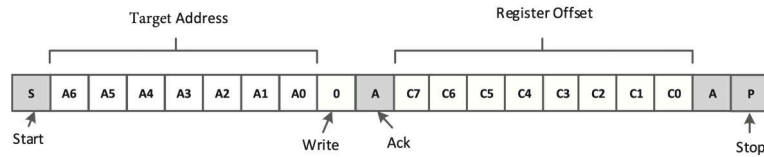


Figure 9-8. I²C Write Without Data

The following procedure should be followed for setting a starting sub-address for I²C reads (refer to [Figure 9-8](#)).

1. The host initiates a write operation by generating a start condition (S), followed by the TUSB2E11 7-bit address and a zero-value “W/R” bit to indicate a write cycle.
2. The TUSB2E11 acknowledges the address cycle.
3. The host presents the register offset within TUSB2E11 to be written, consisting of one byte of data, MSB-first.
4. The TUSB2E11 acknowledges the register offset cycle.
5. The host terminates the write operation by generating a stop condition (P).

Note

After initial power-up, if no register offset is included for the read procedure (refer to [Figure 9-6](#)), then reads start at register offset 00h and continue byte by byte through the registers until the I²C host terminates the read operation. During a read operation, the TUSB2E11 auto-increments the I²C internal register address of the last byte transferred independent of whether or not an ACK was received from the I²C host.

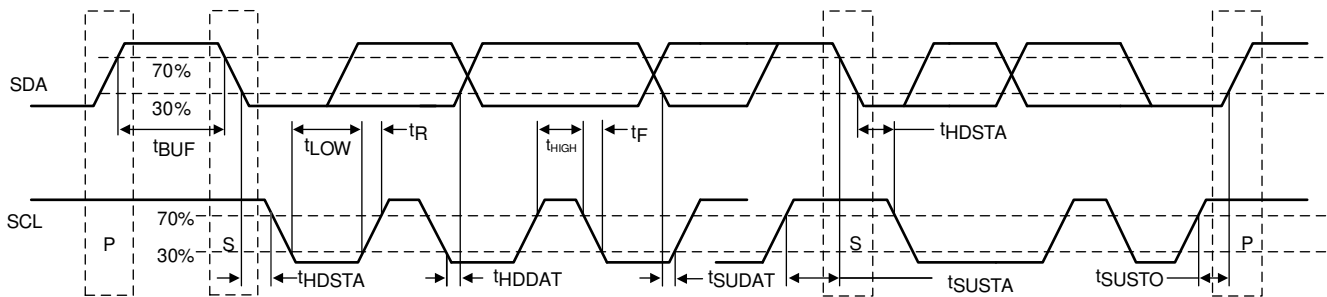


Figure 9-9. I²C Timing Diagram

10 Register Access Protocol (RAP)

The repeater in TUSB2E11 supports the register access protocol (RAP) over eUSB2 to allow access to its related registers.

RAP accessible registers are indicated with corresponding RAP addresses in the register map. Default value of a subset of the registers are factory programmable and are indicated in register map.

11 Register Map

11.1 TUSB2E11 Registers

Table 11-1 lists the TUSB2E11 registers. All register offset addresses not listed in Table 11-1 should be considered as reserved locations and the register contents should not be modified.

Table 11-1. TUSB2E11 Registers

| Offset | Acronym | Register Name | Section |
|--------|----------------------------|---|--------------------|
| 70h | U_TX_ADJUST_PORT1 | RAP Register for Port 1 (0h), Default through OTP | Go |
| 71h | U_HS_TX_PRE_EMPHASIS_P1 | RAP Register for Port 1 (1h), Default through OTP | Go |
| 72h | U_RX_ADJUST_PORT1 | RAP Register for Port 1 (2h), Default through OTP | Go |
| 73h | U_DISCONNECT_SQUELCH_PORT1 | RAP Register for Port 1 (3h), Default through OTP | Go |
| 77h | E_HS_TX_PRE_EMPHASIS_P1 | RAP Register for Port 1 (7h), Default through OTP | Go |
| 78h | E_TX_ADJUST_PORT1 | RAP Register for Port 1 (8h), Default through OTP | Go |
| 79h | E_RX_ADJUST_PORT1 | RAP Register for Port 1 (9h), Default through OTP | Go |
| 0h | GPIO0_CONFIG | | Go |
| 40h | GPIO1_CONFIG | | Go |
| 50h | UART_PORT1 | RAP Register for Port 1 (20h) | Go |
| B0h | REV_ID | | Go |
| B2h | GLOBAL_CONFIG | | Go |
| B3h | INT_ENABLE_1 | | Go |
| B4h | INT_ENABLE_2 | | Go |
| B6h | BC_CONTROL | | Go |
| B7h | BC_STATUS_1 | | Go |
| A3h | INT_STATUS_1 | | Go |
| A4h | INT_STATUS_2 | | Go |
| 60h | CONFIG_PORT1 | | Go |
| F5h | TEST_MODE1 | | Go |

Complex bit access types are encoded to fit into small table cells. Table 11-2 shows the codes that are used for access types in this section.

Table 11-2. TUSB2E11 Access Type Codes

| Access Type | Code | Description |
|------------------------|---------|--|
| Read Type | | |
| H | H | Set or cleared by hardware |
| R | R | Read |
| RH | R H | Read Set or cleared by hardware |
| Write Type | | |
| W | W | Write |
| W1C | W 1C | Write 1 to clear |
| WtoP | W | Write |
| Reset or Default Value | | |
| - n | | Value after reset or the default value |

11.1.1 GPIO0_CONFIG Register (Offset = 00h) [Reset = 00h]

GPIO0_CONFIG is shown in [GPIO0_CONFIG Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 11-3. GPIO0_CONFIG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------------|------|-------|--|
| 7 | GPIO0_OD_PP | R/W | 0h | GPIO0 output type 0h = open drain output 1h = push pull output |
| 6 | Reserved | R | 0h | Reserved |
| 5 | GPIO0_DIRECTION | R/W | 0h | GPIO0 direction 0h = input 1h = output |
| 4 | GPIO0_INPUT_STATUS | RH | 0h | Logical value of GPIO0 pin input (0=Low, 1=High) 0h = input is low 1h = input is high |
| 3-0 | GPIO0_OUTPUT_SELECT | R/W | 0h | Dh = HIGH_OUTPUT – output is forced static high Eh = LOW_OUTPUT – output is forced static low |

11.1.2 GPIO1_CONFIG Register (Offset = 40h) [Reset = 00h]

GPIO1_CONFIG is shown in [GPIO1_CONFIG Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 11-4. GPIO1_CONFIG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------------------|------|-------|---|
| 7 | GPIO1_OD_PP | R/W | 0h | GPIO1 output type selection 0h = open drain output 1h = push pull output |
| 6 | GPIO1_IN_TRIGGER_TYPE | R/W | 0h | GPIO1 input trigger type selection for interrupt 0h = edge trigger input 1h = level trigger input (GPIO2 output will reflect the input level state) |
| 5 | GPIO1_DIRECTION | R/W | 0h | GPIO1 direction selection 0h = input 1h = output |
| 4 | GPIO1_INPUT_STATUS | RH | 0h | Logical value of GPIO1 pin input status (0=Low, 1=High) 0h = input is low 1h = input is high |

Table 11-4. GPIO1_CONFIG Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|---------------------|------|-------|--|
| 3-0 | GPIO1_OUTPUT_SELECT | R/W | 0h | <p>GPIO1 output selection</p> <p>0h = Remote wakeup – host repeater is receiving remote wake but has not seen start of resume</p> <p>1h = USB disconnect – host repeater is actively forwarding LS/FS disconnect.</p> <p>2h = USB_HS_Unsquelched – host repeater in L0 seeing USB HS or in reset seeing Chirp</p> <p>3h = PVTB – HOST repeater is actively transmitting ESE1 due to HS disconnect.</p> <p>4h = DEFAULT – waiting to be configured host/peripheral</p> <p>5h = HOST – in host repeater mode</p> <p>6h = PERIPHERAL – in peripheral repeater mode</p> <p>7h = CONNECTED – repeater is connected, connection seen acknowledged by start of reset</p> <p>8h = RESET – reset in progress, reset is detected is high, L0 is low</p> <p>9h = L0 – fully configured and repeating data, keep-alive and reset/disconnect</p> <p>Ah = L1 – device has received CM.FS/CM.L1, has stopped repeating and is waiting for wake or resume</p> <p>Bh = L2 – device has received CM.L2, has stopped repeating and is waiting for wake or resume.</p> <p>Ch = GPIO1_HS_TEST – in host repeater in L0 mode, received CM.TEST</p> <p>Dh = HIGH_OUTPUT – output is forced static high</p> <p>Eh = LOW_OUTPUT – output is forced static low</p> <p>Fh = OVP – over voltage (DP/DN voltage > VOVP_TH) detected on the USB DP/DN</p> |

11.1.3 U_TX_ADJUST_PORT1 Register (Offset = 70h) [Reset = 7Ch]

U_TX_ADJUST_PORT1 is shown in [Table 11-5](#).

Return to the [Summary Table](#).

Hardware default value can be overridden through factory programmable OTP for this register.

Table 11-5. U_TX_ADJUST_PORT1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------------|------|-------|---|
| 7-6 | U_HS_TERM_P1 | RH/W | 1h | <p>0h = 42.75 Ω (typical)</p> <p>1h = 45 Ω (typical) (default)</p> <p>2h = 47.25 Ω (typical)</p> <p>3h = 49.5 Ω (typical)</p> |
| 5-4 | U_HS_TX_SLEW_RATE_P1 | RH/W | 3h | <p>0h = 425 ps (typical)</p> <p>1h = 465 ps (typical)</p> <p>2h = 510 ps (typical)</p> <p>3h = 625 ps (typical) (OTP default)</p> |

Table 11-5. U_TX_ADJUST_PORT1 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|----------------------|------|-------|--|
| 3-0 | U_HS_TX_AMPLITUDE_P1 | RH/W | Ch | 0h = 800 mV – 7.5%, 740 mV (typical) 1h = 800 mV – 5.0%, 760 mV (typical) 2h = 800 mV – 2.5%, 780 mV (typical) 3h = 800 mV (USB 2.0 spec nominal), 800 mV (typical) (B0 OTP default) 4h = 800 mV + 2.5%, 820 mV (typical) 5h = 800 mV + 5.0%, 840 mV (typical) 6h = 800 mV + 7.5%, 860 mV (typical) 7h = 800 mV + 10%, 880 mV (typical) 8h = 800 mV + 12.5%, 900 mV (typical) 9h = 800 mV + 15%, 920 mV (typical) Ah = 800 mV + 17.5%, 940 mV (typical) Bh = 800 mV + 20%, 960 mV (typical) Ch = 800 mV + 22.5%, 980 mV (typical) (B1 OTP default) Dh = 800 mV + 25%, 1000 mV (typical) Eh = 800 mV + 27.5%, 1020 mV (typical) Fh = 800 mV + 30%, 1040 mV (typical) |

11.1.4 U_HS_TX_PRE_EMPHASIS_P1 Register (Offset = 71h) [Reset = 3Ch]

U_HS_TX_PRE_EMPHASIS_P1 is shown in [Table 11-6](#).

Return to the [Summary Table](#).

Hardware default value can be overridden through factory programmable OTP for this register.

Table 11-6. U_HS_TX_PRE_EMPHASIS_P1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------------|------|-------|--|
| 7 | CDP_2_EN_P1 | RH/W | 0h | 0h = CDP advertising disabled 1h = CDP advertising enabled |
| 6 | Reserved | RH/W | 0h | Reserved |
| 5-4 | U_HS_TX_PE_WIDTH_P1 | RH/W | 3h | 0h = 0.35 UI (typical) 1h = 0.45 UI (typical) 2h = 0.55 UI (typical) 3h = 0.65 UI (typical) (OTP default) |
| 3 | U_HS_TX_PE_ENABLE_P1 | RH/W | 1h | USB HS TX pre-emphasis enable Default through OTP PE is disabled during chirp J (VCHIRPJ) or chirp K (VCHIRPK) 0h = Disabled 1h = Enabled (OTP default) |
| 2-0 | U_HS_TX_PRE_EMPHASIS_P1 | RH/W | 4h | 0h = 0.5 dB (typical) (B0 OTP default) 1h = 0.9 dB (typical) 2h = 1.2 dB (typical) 3h = 1.7 dB (typical) 4h = 2.1 dB (typical) (B1 OTP default) 5h = 2.5 dB (typical) 6h = not recommended 7h = not recommended |

11.1.5 U_RX_ADJUST_PORT1 Register (Offset = 72h) [Reset = 92h]

U_RX_ADJUST_PORT1 is shown in [Table 11-7](#).

Return to the [Summary Table](#).

Hardware default value can be overridden through factory programmable OTP for this register.

Table 11-7. U_RX_ADJUST_PORT1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|--|
| 7-4 | Reserved | RH/W | 9h | Reserved |
| 3 | Reserved | RH/W | 0h | Reserved |
| 2-0 | U_EQ_P1 | RH/W | 2h | 0h = 0.06 dB (typical) (B0 OTP default) 1h = 0.58 dB (typical) 2h = 1.09 dB (typical) (B1 OTP default) 3h = 1.56 dB (typical) 4h = 2.26 dB (typical) 5h = 2.67 dB (typical) 6h = 3.03 dB (typical) 7h = 3.35 dB (typical) |

11.1.6 U_DISCONNECT_SQUELCH_PORT1 Register (Offset = 73h) [Reset = 83h]

U_DISCONNECT_SQUELCH_PORT1 is shown in [Table 11-8](#).

Return to the [Summary Table](#).

Hardware default value can be overridden through factory programmable OTP for this register.

Table 11-8. U_DISCONNECT_SQUELCH_PORT1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------------------|------|-------|--|
| 7-4 | U_DISCONNECT_THRES HOLD_P1 | RH/W | 8h | 0h = 525 mV (minimum), 0% (B0 OTP default) 1h = 545 mV (minimum), +4% 2h = 565 mV (minimum), +8% 3h = 585 mV (minimum), +11% 4h = 605 mV (minimum), +15% 5h = 625 mV (minimum), +19% 6h = 645 mV (minimum), +23% 7h = 665 mV (minimum), +27% 8h = 685 mV (minimum) (B1 OTP default), +31% 9h = 705 mV (minimum), +34% Ah = 725 mV (minimum), +38% Bh = 745 mV (minimum), +42% Ch = 765 mV (minimum), +46% Dh = 785 mV (minimum), +50% Eh = 805 mV (minimum), +53% Fh = 825 mV (minimum), +57% |
| 3 | Reserved | RH/W | 0h | Reserved |
| 2-0 | U_SQUELCH_THRESHO LD_P1 | RH/W | 3h | 0h = 130 mV (minimum), +30% 1h = 124 mV (minimum), +24% 2h = 117 mV (minimum), +17% 3h = 111 mV (minimum), +11% (B1 OTP default) 4h = 104 mV (minimum), +4% (B0 OTP default) 5h = 98 mV (minimum), -2% 6h = 91 mV (minimum), -9% 7h = 85 mV (minimum), -15% |

11.1.7 E_HS_TX_PRE_EMPHASIS_P1 Register (Offset = 77h) [Reset = 0h]

E_HS_TX_PRE_EMPHASIS_P1 is shown in [Table 11-9](#).

Return to the [Summary Table](#).

Hardware default value can be overridden through factory programmable OTP for this register.

Table 11-9. E_HS_TX_PRE_EMPHASIS_P1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------------|------|-------|--|
| 7-5 | E_HS_TX_PRE_EMPHASIS_P1 | RH/W | 0h | 0h = 0 dB (typical) (default) 1h = 0.67 dB (typical) 2h = 1.29 dB (typical) 3h = 1.87 dB (typical) 4h = 2.41 dB (typical) 5h = 2.92 dB (typical) 6h = 3.41 dB (typical) 7h = 3.86 dB (typical) |
| 4-3 | E_HS_TX_PE_WIDTH_P1 | RH/W | 0h | 0h = 0.40 UI (typical) (default) 1h = 0.5 UI (typical) 2h = 0.55 UI (typical) 3h = 0.65 UI (typical) |
| 2-1 | Reserved | RH/W | 0h | Reserved |
| 0 | BC_DETECTION_ENABLE_P1 | RH/W | 0h | Enables battery charger (BC) detection during peripheral repeater mode. BC detection is disabled if the corresponding register is written low. Detection enable is further gated with connect announcement by SoC. After detection attempt completes, repeater will enable the pull up. 0h = detection disabled. 1h = detection enabled |

11.1.8 E_TX_ADJUST_PORT1 Register (Offset = 78h) [Reset = 0Bh]

E_TX_ADJUST_PORT1 is shown in [Table 11-10](#).

Return to the [Summary Table](#).

Hardware default value can be overridden through factory programmable OTP for this register.

Table 11-10. E_TX_ADJUST_PORT1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------------|------|-------|--|
| 7 | Reserved | RH/W | 0h | Reserved |
| 6 | Autoresume Disable | RH/W | 0h | Added in B1 0h = autoresume enabled 1h = autoresume disabled |
| 5 | Reserved | RH/W | 0h | Reserved |
| 4-3 | E_HS_TX_SLEW_RATE_P1 | RH/W | 1h | 0h = 390 ps (typical) 1h = 440 ps (typical) (default) 2h = 460 ps (typical) 3h = 490 ps (typical) |
| 2-0 | E_HS_TX_AMPLITUDE_P1 | RH/W | 3h | 0h = 360 mV (typical) 1h = 380 mV (typical) 2h = 400 mV (typical) 3h = 420 mV (typical) (default) 4h = 440 mV (typical) 5h = 460 mV (typical) 6h = 480 mV (typical) 7h = 500 mV (typical) |

11.1.9 E_RX_ADJUST_PORT1 Register (Offset = 79h) [Reset = 60h]

E_RX_ADJUST_PORT1 is shown in [Table 11-11](#).

Return to the [Summary Table](#).

Hardware default value can be overridden through factory programmable OTP for this register.

Table 11-11. E_RX_ADJUST_PORT1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------------------|------|-------|--|
| 7 | Reserved | RH/W | 0h | Reserved |
| 6-4 | E_SQUELCH_THRESHO LD_P1 | RH/W | 6h | 0h = 104 mV (typical) 1h = 101 mV (typical) 2h = 98 mV (typical) 3h = 90 mV (typical) 4h = 81 mV (typical) (B0 OTP default) 5h = 73 mV (typical) 6h = 67 mV (typical) (B1 OTP default) 7h = 60 mV (typical) |
| 3-0 | E_EQ_P1 | RH/W | 0h | 0h = 0.34 dB (typical) (default) 1h = 0.71 dB (typical) 2h = 1.02 dB (typical) 3h = 1.36 dB (typical) 4h = 1.64 dB (typical) 5h = 1.94 dB (typical) 6h = 2.19 dB (typical) 7h = 2.45 dB (typical) 8h = 2.69 dB (typical) 9h = 2.93 dB (typical) Ah = 3.13 dB (typical) Bh = 3.35 dB (typical) Ch = 3.53 dB (typical) Dh = 3.72 dB (typical) Eh = 3.89 dB (typical) Fh = 4.07 dB (typical) |

11.1.10 UART_PORT1 Register (Offset = 50h) [Reset = 02h]

UART_PORT1 is shown in [Table 11-12](#).

Return to the [Summary Table](#).

Table 11-12. UART_PORT1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------------------|------|-------|---|
| 7-6 | Reserved | R/W | 0h | Reserved |
| 4 | uart_cross_P1 | R/W | 0h | Select whether plus and minus pins are crossed between USB 2.0 and eUSB2 during UART mode 0h = if UART mode is enabled, pair eD+ with D+ and eD- with D- 1h = if UART mode is enabled, pair eD+ with D- and eD- with D+ |
| 3 | UART_use_bit1_P1 | R/W | 0h | Select whether UART enable select is set by register bit 1 or not 0h = bit 1 ignored. UART mode enabled by GPIO0 1h = bit 1 (UART_en_by_reg_not_pin_P1) enabled |
| 2 | UART_dir_not_Carkit_P1 | R/W | 0h | Set UART mode, direction, low for Carkit and high for opposite 0h = UART mode uses Carkit directions, D+ to eUSB2 and eD- to USB 2.0 1h = UART mode directions are opposite of Carkit, D- to eUSB2 and eD+ to USB 2.0 |
| 1 | UART_en_by_reg_not_pin_P1 | R/W | 1h | Select whether Carkit UART mode is enabled by register or by GPIO0 pin 0h = select GPIO0 pin to enable UART mode 1h = select UART_mode_en_P1 register to enable UART mode |
| 0 | UART_mode_en_P1 | R/W | 0h | If GPIO0 is not selected to enable Carkit UART mode, this register will enable it. 0h = disable UART mode between eUSB2 and USB 2.0 pins 1h = enable UART mode between eUSB2 and USB 2.0 pins |

11.1.11 REV_ID Register (Offset = B0h) [Reset = 02h]

REV_ID is shown in [Table 11-13](#).

Return to the [Summary Table](#).

Table 11-13. REV_ID Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------|------|-------|--|
| 7-0 | REV_ID | RH | 02h | Device revision. 01h = A0 02h = B0 03h = B1 |

11.1.12 GLOBAL_CONFIG Register (Offset = B2h) [Reset = 0h]

GLOBAL_CONFIG is shown in [Table 11-14](#).

Return to the [Summary Table](#).

Table 11-14. GLOBAL_CONFIG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------|-------|-------|--|
| 7 | SOFT_RST | HWtoP | 0h | Writing a 1 to this field is equivalent to pulsing RESETB low |
| 6 | DISABLE_P1 | R/W | 0h | Disabled Mode Repeater 1 (I2C will remain Active) (If port is not disconnected, wait until disconnect event to disable the repeater) 0h = repeater enabled 1h = repeater disabled |
| 5 | Reserved | R | 0h | Reserved |
| 4 | GPIO2_OUT_TYPE | R/W | 0h | GPIO2 output type 0h = open drain 1h = push-pull |
| 3 | GPIO2_POLARITY | R/W | 0h | GPIO2 pin polarity in push-pull mode only (open drain mode will always be active low) 0h = active high 1h = active low |
| 2-0 | Reserved | R | 0h | Reserved |

11.1.13 INT_ENABLE_1 Register (Offset = B3h) [Reset = 00h]

INT_ENABLE_1 is shown in [INT_ENABLE_1 Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 11-15. INT_ENABLE_1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------------|------|-------|---|
| 7 | GPIO1_RISING_EDGE | R/W | 0h | INT_GPIO1_RISING_EDGE enable. When GPIO1_IN_TRIGGER_TYPE = 0 (Edge), this enables interrupt on Rising Edge of GPIO1. When GPIO1_IN_TRIGGER_TYPE = 1 (Level), this enables interrupt when GPIO1 = High. 0h = not enabled 1h = enabled |
| 6 | GPIO1_FALLING_EDGE | R/W | 0h | INT_GPIO1_FALLING_EDGE enable. When GPIO1_IN_TRIGGER_TYPE = 0 (Edge), this enables interrupt on Falling Edge of GPIO1. When GPIO1_IN_TRIGGER_TYPE = 1 (Level), this enables interrupt when GPIO1 = Low. 0h = not enabled 1h = enabled |
| 5 | Reserved | R | 0h | Reserved |
| 4 | Reserved | R | 0h | Reserved |

Table 11-15. INT_ENABLE_1 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--------------------|------|-------|---|
| 3 | USB_REMOTE_WAKE_P1 | R/W | 0h | INT_USB_REMOTE_WAKE_P1 enable. See Section 9.4.6 0h = not enabled 1h = enabled |
| 2 | USB_DISCONNECT_P1 | R/W | 0h | INT_USB_DISCONNECT_P1 enable. See Section 9.4.6 0h = not enabled 1h = enabled |
| 1 | Reserved | R | 0h | Reserved |
| 0 | Reserved | R | 0h | Reserved |

11.1.14 INT_ENABLE_2 Register (Offset = B4h) [Reset = 00h]

INT_ENABLE_2 is shown in [INT_ENABLE_2 Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 11-16. INT_ENABLE_2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------------|------|-------|---|
| 7 | INT_OVERRIDE_EN | R/W | 0h | Override GPIO2 INT output 0h = not enabled 1h = enabled See INT_VALUE |
| 6 | INT_VALUE | R/W | 0h | Value to drive on GPIO2 when INT_OVERRIDE_EN=1 GPIO2 output pin will indicate the interrupt assertion. It will follow the GPIO2 pin configuration. In open drain mode it will be active low to indicate interrupt assertion and in push-pull mode it will follow active low/high configuration to indicate GPIO2 assertion. 0h = output: interrupt not asserted 1h = output: interrupt asserted |
| 5 | BC_CHG_DET_P1 | R/W | 0h | INT_BC_CHG_DET_P1 enable. 0h = not enabled 1h = enabled |
| 4 | Reserved | R | 0h | Reserved |
| 3 | USB_DETECT_ATTACH_P1 | R/W | 0h | INT_USB_DET_ATTACH_P1 enable. Enable device attach detection while eDSP is powered down See Section 9.4.7 0h = not enabled 1h = enabled |
| 2 | Reserved | R | 0h | Reserved |
| 1 | USB_OVP_P1 | R/W | 0h | Over Voltage Port 1 interrupt enable 0h = not enabled 1h = enabled |
| 0 | Reserved | R | 0h | Reserved |

11.1.15 BC_CONTROL Register (Offset = B6h) [Reset = C0]

BC_CONTROL is shown in [BC_CONTROL Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 11-17. BC_CONTROL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------------------|------|-------|---|
| 7-6 | i2c_ds_config | RH/W | 3h | I2C open drain output drive strength selection This is intended to be set through I2C. 0h \approx 1 mA (typical) 1h \approx 2 mA (typical) 2h \approx 4 mA (typical) 3h \approx 8 mA (typical) (default) |
| 5-4 | DEFAULT_STATE_BC_P1 | RH/W | 0h | Battery charger advertisement or detection selected for default state of eUSB2 repeater 0h = neither detect nor advertise charger 1h = detect charger starting when GPIO1 goes high. 2h = advertise short mode DCP. DCP is 1.2 V if 1P2V_MODE is '1' else pure BC 1.2 DCP 3h = auto-cycle ACP3 to short mode DCP. Short mode will pass through 1.2V DCP for 12 seconds prior to pure BC 1.2 DCP if 1P2V_MODE is '1' |
| 3 | VBUS_CONTROL_POLARITY | RH/W | 0h | Select polarity of VBUS control output pin 0h = active high 1h = active low |
| 2 | 1P2V_MODE_DIS | RH/W | 0h | Disable advertising 1.2 V mode in default state whether enabled to auto-cycle or not 0h = 1.2 V mode enabled 1h = 1.2 V mode disabled |
| 1 | INT_PIN_FUNCTION | RH/W | 0h | Select function of GPIO2 pin in I2C mode 0h = INT (interrupt) 1h = CHG_DET (Charger Detected) |
| 0 | CHG_DET_POLARITY | RH/W | 0h | Select polarity of CHG_DET I2C mode status output pin 0h = active low 1h = active high |

11.1.16 BC_STATUS_1 Register (Offset = B7h) [Reset = 00h]

BC_STATUS_1 is shown in [BC_STATUS_1 Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 11-18. BC_STATUS_1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------------|------|-------|--|
| 7 | Reserved | RH | 0h | Reserved |
| 6-4 | CHARGER_TYPE_DET_P1 | RH | 0h | Type of battery charger detected on Port 1 0h = SDP – 500 mA 1h = divider 0 – 500 mA 2h = divider 1 – 1 A 3h = CDP – 1.5 A 4h = BC 1.2 DCP – 1.5 A 5h = 1.2 V pullup and short – 2 A 6h = divider 2 – 2.1 A 7h = divider 3 – 2.4 A |
| 3 | Reserved | RH | 0h | Reserved |

Table 11-18. BC_STATUS_1 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------------|------|-------|---|
| 2-0 | Auto_DCP_STATE_P1 | RH | 0h | State of auto-DCP sequence on Port 1 0h = no advertisement 5h = divider 3 (2.4 A) 6h = 1.2 V pullup and short 7h = BC 1.2 DCP |

11.1.17 INT_STATUS_1 Register (Offset = A3h) [Reset = 00h]

INT_STATUS_1 is shown in [INT_STATUS_1 Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 11-19. INT_STATUS_1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------------------|-------|-------|---|
| 7 | INT_GPIO1_RISING_EDGE | R/W1C | 0h | GPIO1 Rising Edge enable 0h = no interrupt 1h = interrupt |
| 6 | INT_GPIO1_FALLING_EDGE | R/W1C | 0h | GPIO1 Falling Edge enable 0h = no interrupt 1h = interrupt |
| 5 | Reserved | R | 0h | Reserved |
| 4 | Reserved | R | 0h | Reserved |
| 3 | INT_USB_REMOTE_WAKEUP_P1 | R/W1C | 0h | Remote Wake Event Detect on USB Port 1 See Section 9.4.6 0h = no interrupt 1h = interrupt |
| 2 | INT_USB_DISCONNECT_P1 | R/W1C | 0h | Disconnect event has occurred on Port 1 See Section 9.4.6 0h = no interrupt 1h = interrupt |
| 1-0 | Reserved | R | 0h | Reserved |

11.1.18 INT_STATUS_2 Register (Offset = A4h) [Reset = 00h]

INT_STATUS_2 is shown in [INT_STATUS_2 Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 11-20. INT_STATUS_2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------------------|-------|-------|---|
| 7-6 | Reserved | R | 0h | Reserved |
| 5 | INT_BC_CHG_DET_P1 | R/W1C | 0h | Detected battery charger on Port 1 0h = no interrupt 1h = interrupt |
| 4 | Reserved | R | 0h | Reserved |
| 3 | INT_USB_DET_ATTACH_P1 | R/W1C | 0h | Device Attach event has occurred on Port 1 See Section 9.4.7 0h = no interrupt 1h = interrupt |
| 2 | Reserved | R | 0h | Reserved |
| 1 | INT_USB_OVP_P1 | R/W1C | 0h | Over voltage condition has occurred (DP/DN) 0h = no interrupt 1h = interrupt |

Table 11-20. INT_STATUS_2 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|-------------|
| 0 | Reserved | R | 0h | Reserved |

11.1.19 CONFIG_PORT1 Register (Offset = 60h) [Reset = 00h]

CONFIG_PORT1 is shown in [CONFIG_PORT1 Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 11-21. CONFIG_PORT1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------------|------|-------|---|
| 7-5 | Reserved | R | 0h | Reserved |
| 4-3 | HOST_DEVICE_P1 | RH | 0h | Port1 is configured as a Host repeater or a Device repeater 0h = not configured 1h = host repeater 2h = device repeater 3h = reserved |
| 2-1 | Reserved | R | 0h | Reserved |
| 0 | CDP_2_STATUS_P1 | RH | 0h | Primary detection detected on port1 if CDP_2_EN_P1=1 0h = CDP primary detection detected 1h = CDP primary detection not detected |

11.1.20 TEST_MODE1 Register (Offset = F5h) [Reset = 3Xh]

TEST_MODE1 is shown in [TEST_MODE1 Register Field Descriptions](#).

Return to the [Summary Table](#).

Table 11-22. TEST_MODE1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------|------|-------|--|
| 7-4 | Reserved | R/W | 0h | Reserved, make sure to rewrite what was read |
| 3 | FORCE_HS_L0 | R/W | 0h | Force repeater into high-speed L0 state for test purposes only. 0h = normal repeater mode (setting this bit to 0 will not return the device to normal repeater mode, the device needs to be hard reset, soft reset or power cycled) 1h = forced high-speed L0 mode |
| 2-0 | Reserved | R/W | Xh | Variant ID. 00h = 1.2V I/O 02h = 1.8V I/O Must not change the value, rewrite the value that is read. |

12 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

12.1 Application Information

TUSB2E11 can be used in either HOST or Peripheral implementation. The mode is configured by the eUSB2 SoC.

12.2 Typical Application

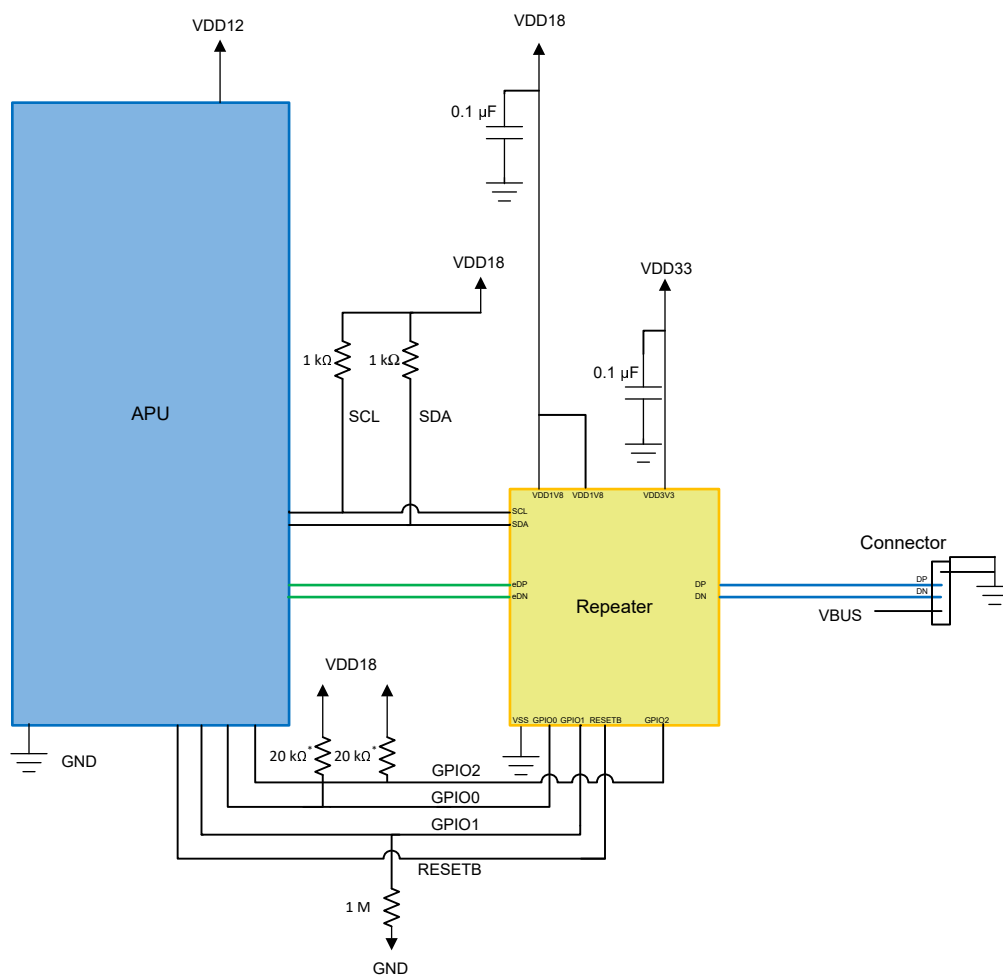


Figure 12-1. Typical System Implementation Using 1.8 V I²C Variant

The 0.1 µF recommendation per supply pin is based on capacitor placement of 2 mm or less trace length away. If the placement of capacitor is further away, the value of the capacitor needs to be redetermined to account for the additional trace inductance and maintain resonance around 12 MHz. Additionally, system power design should have adequate bulk capacitance to account for maximum transient current expected by the device when transitioning from low power mode to active mode. GPIO2 can be optionally used as interrupt output. Note that the pull-up resistor on GPIO[0:2] should be adjusted based on leakage of the APU I/O so that VIH and VIL of GPIO0 are met.

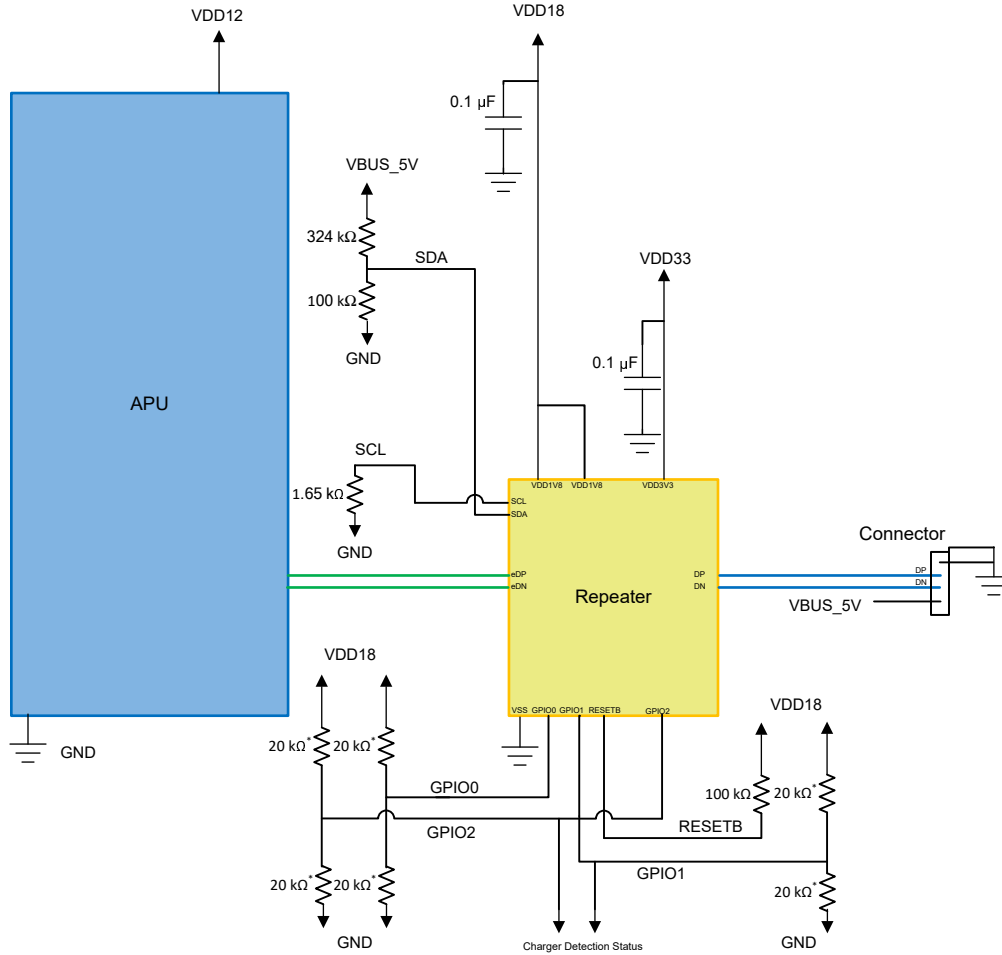


Figure 12-2. Typical System Implementation Using 1.8 V Variant without I²C (Configured for Charger Detection)

The 0.1 μF recommendation per supply pin is based on capacitor placement of 2 mm or less trace length away. If the placement of the capacitor is further away, then the value of the capacitor needs to be redetermined to account for the additional trace inductance and maintain resonance around 12 MHz. Additionally, system power design should have adequate bulk capacitance to account for maximum transient current expected by the device when transitioning from low power mode to active mode. GPIO2 can be optionally used as interrupt output. Note that the pull-up and pull-down resistors on GPIO[0:2] should be selected based on USB PHY tuning needs. SDA should be used for Vbus_valid detection with a voltage divider. GPIO1 and GPIO2 can be routed as needed for charger detection status. Pull-down resistor value on SCL determines the battery charging mode.

12.2.1 Design Requirements

TUSB2E11 requires a valid reset signal as described in the [Power Supply Recommendations](#) section.

For design examples, use the parameters shown in [Table 12-1](#), [Table 12-2](#), and [Table 12-3](#).

Table 12-1. Design Parameters for High Loss USB 2.0 System Using I²C

| PARAMETER | | | VALUE ⁽¹⁾ |
|---|-------------------------------------|---------|----------------------|
| V _{DD3V3} | | | 3.3 V ±10% |
| V _{DD1V8} | | | 1.8 V ±5% |
| I ² C support required in system (Yes or No) | | | Yes |
| Parameter | Register | Setting | Value |
| USB 2.0 TX Swing (peak to peak) | U_TX_ADJUST_PORT1 (Offset = 70h) | 7Ch | 980 mVp-p |

Table 12-1. Design Parameters for High Loss USB 2.0 System Using I²C (continued)

| PARAMETER | | | VALUE ⁽¹⁾ |
|---|--|-----|----------------------|
| USB 2.0 TX Pre-emphasis | U_HS_TX_PRE_EMPHASIS_P1 (Offset = 71h) | 3Ch | 2.1 dB |
| USB 2.0 RX Equalization | U_RX_ADJUST_PORT1 (Offset = 72h) | 92h | 1.09 dB |
| USB 2.0 HS host disconnect threshold (peak differential) | U_DISCONNECT_SQUELCH_PORT1 (Offset = 73h) | 83h | 685 mV |
| USB 2.0 HS squelch/RX sensitivity threshold (peak differential) | U_DISCONNECT_SQUELCH_PORT1 (Offset = 73h) | 83h | 111 mV |

Table 12-2. Design Parameters for Medium Loss USB 2.0 System Using I²C

| PARAMETER | | | VALUE ⁽¹⁾ |
|---|--|---------|----------------------|
| V _{DD3V3} | | | 3.3 V ±10% |
| V _{DD1V8} | | | 1.8 V ±5% |
| I ² C support required in system (Yes or No) | | | Yes |
| Parameter | Register | Setting | Value |
| USB 2.0 TX Swing (peak to peak) | U_TX_ADJUST_PORT1 (Offset = 70h) | 79h | 920 mVp-p |
| USB 2.0 TX Pre-emphasis | U_HS_TX_PRE_EMPHASIS_P1 (Offset = 71h) | 39h | 0.9 dB |
| USB 2.0 RX Equalization | U_RX_ADJUST_PORT1 (Offset = 72h) | 92h | 1.09 dB |
| USB 2.0 HS host disconnect threshold (peak differential) | U_DISCONNECT_SQUELCH_PORT1 (Offset = 73h) | 83h | 685 mV |
| USB 2.0 HS squelch/RX sensitivity threshold (peak differential) | U_DISCONNECT_SQUELCH_PORT1 (Offset = 73h) | 83h | 111 mV |

(1) These parameters are starting values for a high loss system. Further tuning might be required based on specific loss profile and measurements.

Table 12-3. Design Parameters for Medium Loss USB 2.0 System without I²C and Configured for Charger Detection

| PARAMETER | | | | VALUE ⁽¹⁾ |
|---|-------|---------|---------|----------------------|
| V _{DD3V3} | | | | 3.3 V ±10% |
| V _{DD1V8} | | | | 1.8 V ±5% |
| I ² C support required in system (Yes or No) | | | | No |
| SCL (pull-down resistor to ground) | | | | 1.65 kΩ |
| SDA (pull-down resistor to ground) | | | | 100 kΩ |
| SDA (pull-up resistor to VBUS5V) | | | | 324 kΩ |
| Parameter | GPIO0 | GPIO1 | GPIO2 | Value |
| USB 2.0 TX Swing (peak to peak) | Float | Pull-up | Pull-up | 920 mVp-p |
| USB 2.0 TX Pre-emphasis | Float | Pull-up | Pull-up | 0.9 dB |
| USB 2.0 RX Equalization | Float | Pull-up | Pull-up | 1.09 dB |
| USB 2.0 HS host disconnect threshold (peak differential) | Float | Pull-up | Pull-up | 685 mV |
| USB 2.0 HS squelch/RX sensitivity threshold (peak differential) | Float | Pull-up | Pull-up | 98 mV |

(1) These parameters are starting values for a medium loss system. Further tuning might be required based on specific loss profile and measurements.

12.2.2 Detailed Design Procedure

The best PHY setting is dependent upon the signal chain loss characteristics of the target platform. The recommendation is to start with lowest level of compensation for TX swing and pre-emphasis, and then increment until the optimal eye diagram margin is achieved. Same applies to the RX sensitivity or squelch threshold setting where it is recommended to adjust from low threshold until optimum RX sensitivity and squelch margins are achieved.

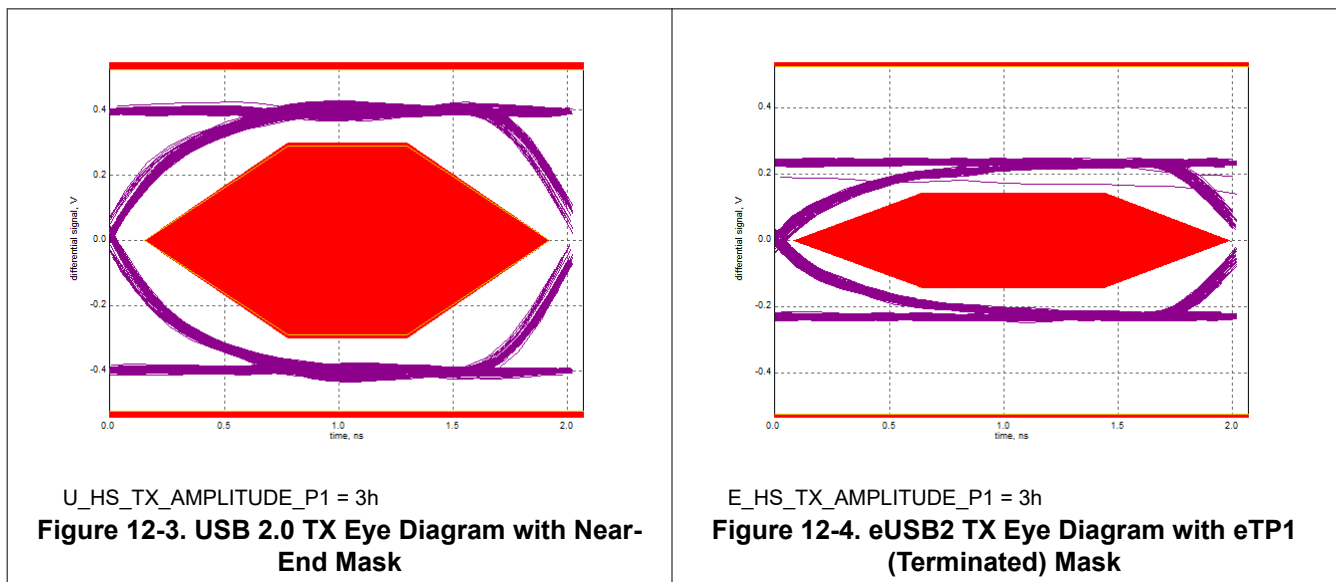
To optimize the TUSB2E11 RX equalization, monitor the corresponding TX eye diagram to achieve best RX EQ setting. In other words, to optimize eUSB2 RX equalization, monitor USB 2.0 TX eye and monitor eUSB2.0 TX eye to optimize USB RX equalization.

HS host disconnect threshold shall be adjusted to provide the most margin to avoid false disconnect as well as failure to detect a disconnect. See [Table 9-2](#).

Note

The TUSB2E11 compensates for extra attenuation in the signal path according to the configuration of the TX and RX settings. General recommendation is to use just enough pre-emphasis and equalization to achieve eye margin and not over-equalize to avoid excessive jitter. Maximum PE width and slew rates are recommended.

12.2.3 Application Curves



12.3 Power Supply Recommendations

12.3.1 Power Up Reset

RESETB pin is active low reset pin and can also be used as a power down pin.

TUSB2E11 does not have power supply sequence requirements between VDD3V3 and VDD1V8.

Maximum VDD3V3 and VDD1V8 ramp time to reach minimum supply voltages should be 2 ms.

Digital and analog inputs may be applied when VDD3V3 and VDD1V8 are in unpowered state.

Internal power on reset circuit along with the external RESETB input pin allows for proper initialization when RESETB is de-asserted high prior to the power rails being valid. If RESETB de-assert high before the power supplies are stable, internal power on reset circuit will hold off internal reset until the supplies are stable.

I²C/RAP and eUSB2 interfaces will be ready after t_{RH_READY} upon de-assertion of RESETB or power up.

I²C/RAP and eUSB2 interfaces will be ready after t_{RH_READY} upon soft reset through the I²C.

Upon de-assertion of RESETB (after t_{RH_READY}) or software reset (after t_{RH_READY}), TUSB2E11 will enable and enter default state and be ready to accept eUSB2 packets, RAP and I²C requests. The repeater will either be in host repeater mode or device repeater mode depending on the receipt of either host mode enable or peripheral mode enable.

12.4 Layout

12.4.1 Layout Guidelines

1. Place supply bypass capacitors as close to VDD1V8 and VDD3V3 pins as possible and avoid placing the bypass caps near the eDP/eDN and DP/DN traces.
2. Route the high-speed USB signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points on twisted pair lines; through-hole pins are not recommended.
3. When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal traces by minimizing impedance discontinuities.
4. Do not route USB traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or ICs that use or duplicate clock signals.
5. Avoid stubs on the high-speed USB signals due to signal reflections. If a stub is unavoidable, then the stub must be less than 200 mil.
6. Route all high-speed USB signal traces over continuous GND planes, with no interruptions.
7. Avoid crossing over anti-etch, commonly found with plane splits.
8. Due to high frequencies associated with the USB, a printed circuit board with at least four layers is recommended; two signal layers separated by a ground and power layer as shown in [Figure 12-5](#).

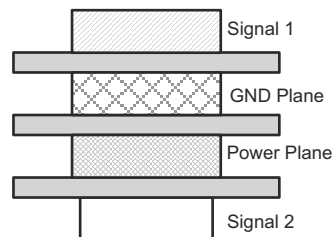


Figure 12-5. Four-Layer Board Stack-Up

12.4.2 Example Layout for Application with 1.8 V I²C Variant

Figure 12-6 shows how GPIO2 can be optionally used as an open drain interrupt output with a pull-up resistor to VDD18.

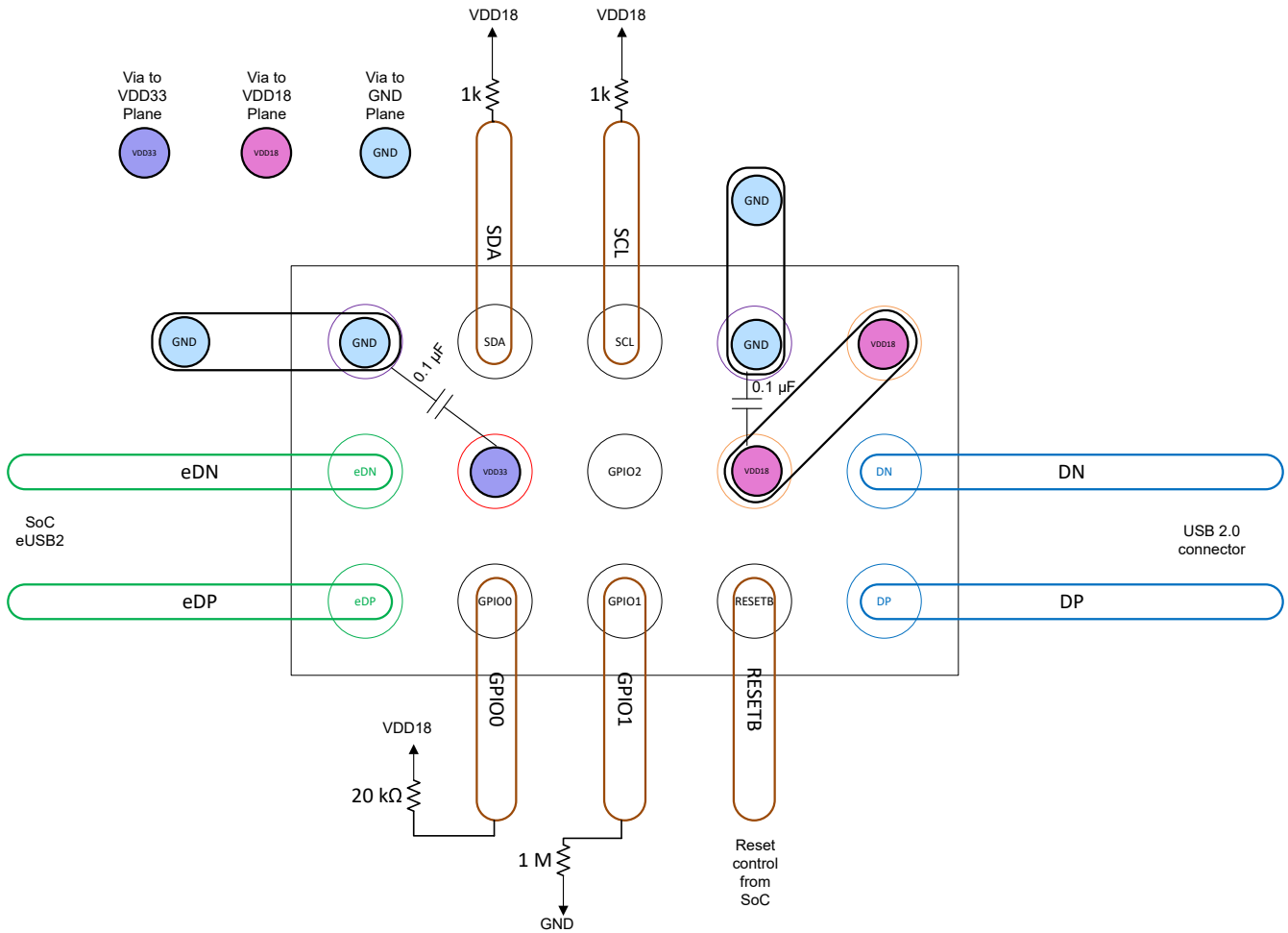


Figure 12-6. Example Layout for Application with 1.8 V I²C Variant

13 Device and Documentation Support

13.1 Device Support

13.1.1 Third-Party Products Disclaimer

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13.2 Documentation Support

13.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [High-Speed Interface Layout Guidelines application note](#)
- USB 2.0 Promoter Group (2000). [USB 2.0 Specification](#) USB 2.0 Promoter Group
- USB Implementers Forum (2018). [Embedded USB2 \(eUSB2\) Physical Layer Supplement to the USB Revision 2.0 Specification, Rev. 1.2](#) USB Implementers Forum

13.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on [Subscribe to updates](#) to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.4 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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13.5 Trademarks

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13.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.7 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| TUSB2E111YCGR | ACTIVE | DSBGA | YCG | 15 | 3000 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -20 to 85 | T2E111A | Samples |
| TUSB2E112YCGR | ACTIVE | DSBGA | YCG | 15 | 3000 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -20 to 85 | T2E112 | Samples |
| TUSB2E112YCGT | ACTIVE | DSBGA | YCG | 15 | 250 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -20 to 85 | T2E112 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

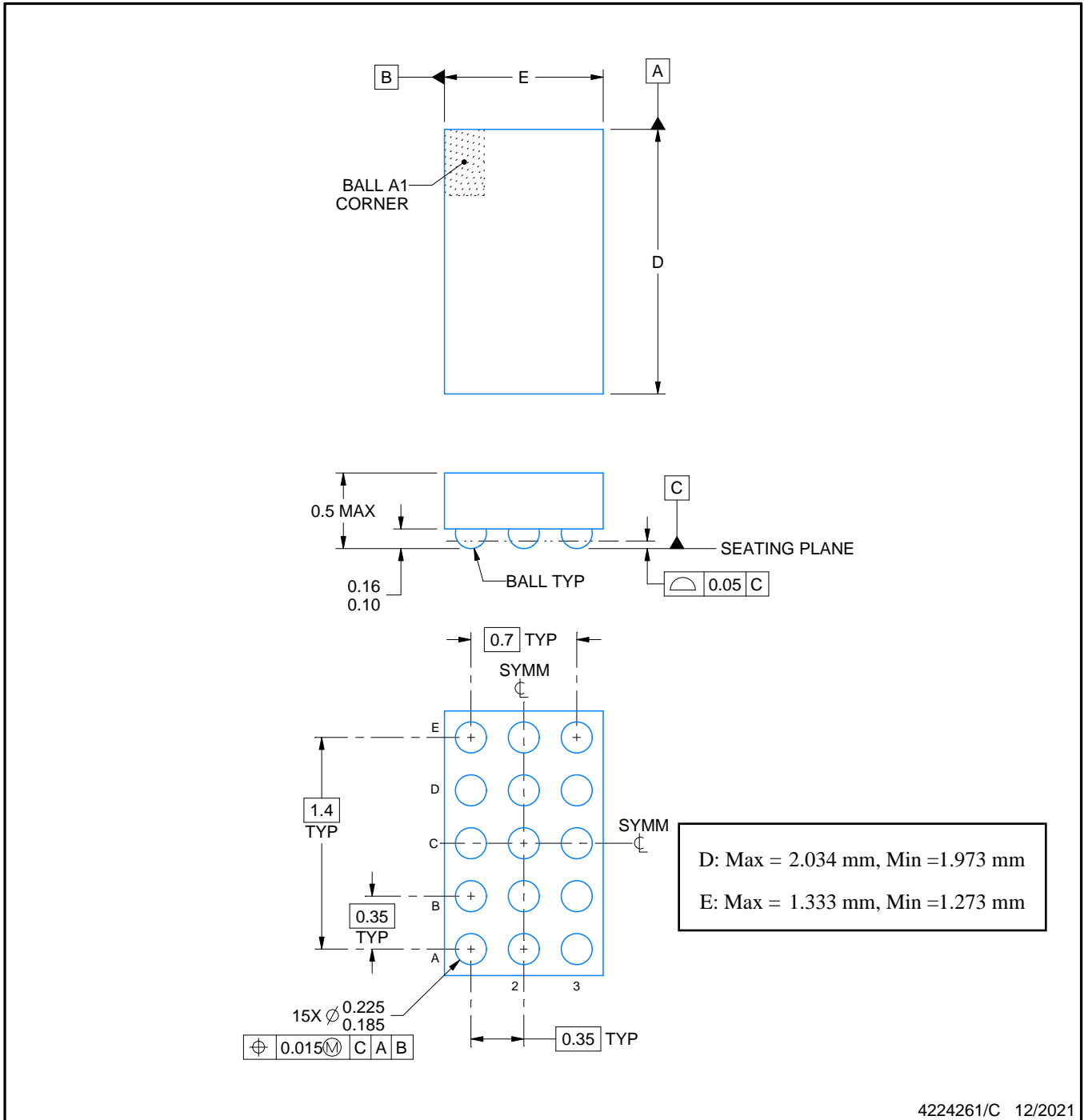
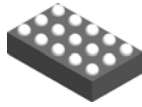

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TUSB2E111YCGR | DSBGA | YCG | 15 | 3000 | 180.0 | 8.4 | 1.42 | 2.16 | 0.65 | 4.0 | 8.0 | Q1 |
| TUSB2E111YCGR | DSBGA | YCG | 15 | 3000 | 180.0 | 8.4 | 1.42 | 2.16 | 0.65 | 4.0 | 8.0 | Q1 |
| TUSB2E112YCGR | DSBGA | YCG | 15 | 3000 | 180.0 | 8.4 | 1.42 | 2.16 | 0.65 | 4.0 | 8.0 | Q1 |
| TUSB2E112YCGR | DSBGA | YCG | 15 | 3000 | 180.0 | 8.4 | 1.42 | 2.16 | 0.65 | 4.0 | 8.0 | Q1 |
| TUSB2E112YCGT | DSBGA | YCG | 15 | 250 | 180.0 | 8.4 | 1.42 | 2.16 | 0.65 | 4.0 | 8.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TUSB2E111YCGR | DSBGA | YCG | 15 | 3000 | 182.0 | 182.0 | 20.0 |
| TUSB2E111YCGR | DSBGA | YCG | 15 | 3000 | 182.0 | 182.0 | 20.0 |
| TUSB2E112YCGR | DSBGA | YCG | 15 | 3000 | 182.0 | 182.0 | 20.0 |
| TUSB2E112YCGR | DSBGA | YCG | 15 | 3000 | 182.0 | 182.0 | 20.0 |
| TUSB2E112YCGT | DSBGA | YCG | 15 | 250 | 182.0 | 182.0 | 20.0 |



NOTES:

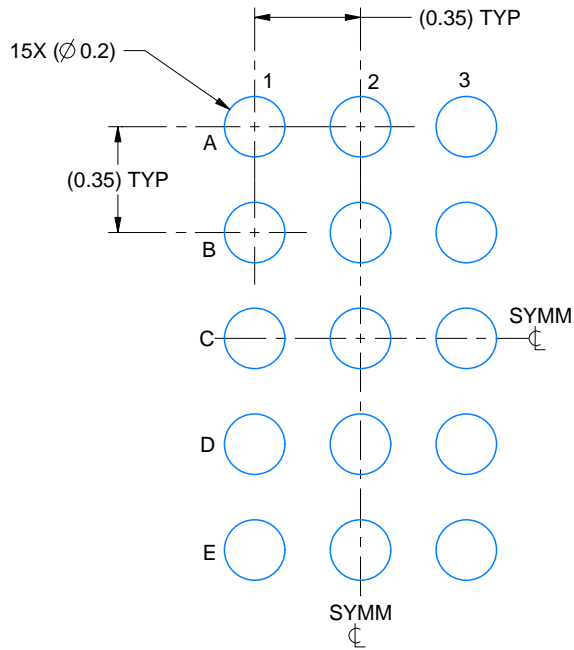
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

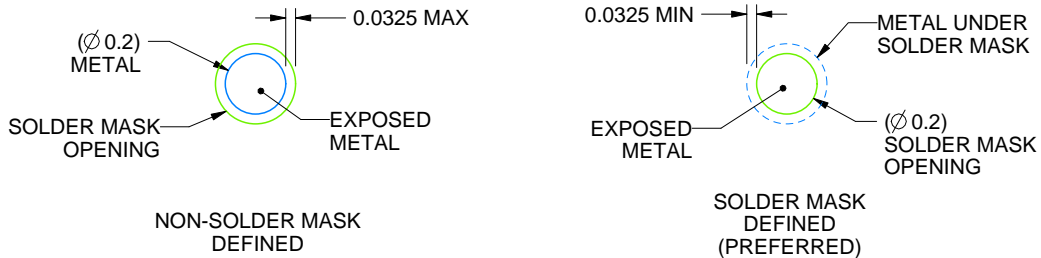
YCG0015

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 40X



SOLDER MASK DETAILS
NOT TO SCALE

4224261/C 12/2021

NOTES: (continued)

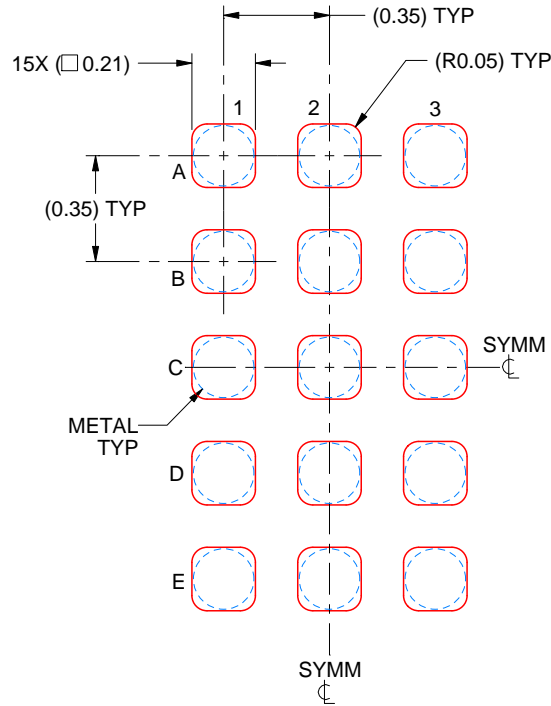
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YCG0015

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.075 mm THICK STENCIL
SCALE: 40X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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