# SNx5LBC176A, Differential Bus Transceivers

## 1 Features

- Designed for signaling rates[1] up to 30 Mbps
- Bus-Pin ESD protection exceeds 12 kV HBM
- Compatible with ANSI standard TIA/EIA-485-A and ISO 8482:1987(E)
- Low Skew
- Designed for multipoint transmission on long bus lines in noisy environments
- Very low disabled supply-current requirements: 700 mA maximum
- Common mode voltage range of –7 V to 12 V
- Thermal-shutdown protection
- Driver positive and negative current limiting
- Open-circuit failsafe receiver design
- Receiver input sensitivity: ±200 mV Maximum
- Receiver input hysteresis: 50 mV typical
- Glitch-free power-up and power-down protection
- Available in Q-temp automotive
  - High reliability automotive applications
  - Configuration control / print support
  - Qualification to automotive standards

## 2 Description

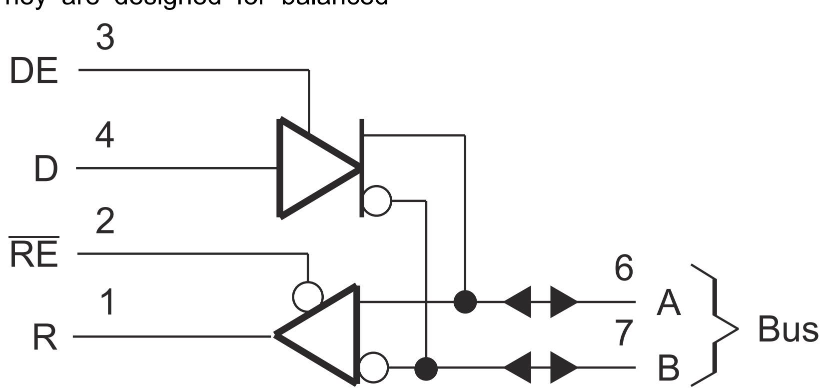
The SN65LBC176A, SN65LBC176AQ, and SN75LBC176A differential bus transceivers are monolithic, integrated circuits designed for bidirectional data communication on multipoint bus-transmission lines. They are designed for balanced transmission lines and are compatible with ANSI standard TIA/EIA-485-A and ISO 8482. The A version offers improved switching performance over its predecessors without sacrificing significantly more power.

The SN65LBC176A, SN65LBC176AQ, and SN75LBC176A combine a 3-state, differential line driver and a differential input line receiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, which can externally connect together to function as a direction control. The driver differential outputs and the receiver differential inputs connect internally to form a differential input /output (I/O) bus port that is designed to offer minimum loading to the bus whenever the driver is disabled or $V_{CC}$ = 0. This port features wide positive and negative common-mode voltage ranges, making the device suitable for party-line applications. Very low device supply current can be achieved by disabling the driver and the receiver.

**Package Information**

| PART NUMBER | PACKAGE(1) | BODY SIZE (NOM) |
|---|---|---|
| SN65LBC176A<br>SN75LBC176A | D (SOIC) | 4.9 mm x 3.91 mm |
| | P (PDIP) | 9.81 mm x 6.35 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.




[1] Signaling rate by TIA/EIA-485-A definition restrict transition times to 30% of the bit duration, and much higher signaling rates may be achieved using a different criteria (see the Typical Characteristics section).

## Table of Contents



## 3 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision F (January 2023) to Revision G (February 2023)** **Page**

- Changed the *Thermal Information* table........ 5

**Changes from Revision E (January 2023) to Revision F (January 2023)** **Page**

- Changed the SN65LBC176AQ values in the *Thermal Information* table........ 5

**Changes from Revision D (August 200/8) to Revision E (January 2023)** **Page**

- Changed the document to the latest TI format........ 1
- Added the *Thermal Information* table........ 5

# 4 Pin Configuration and Functions

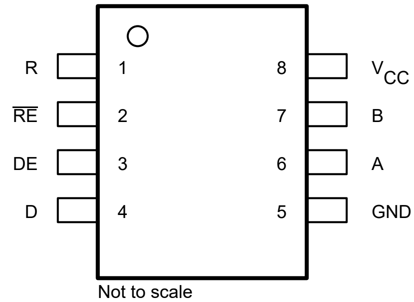



**Figure 4-1. SN65LBC176AQD (Marked as B176AQ)
SN65LBC176AD (Marked as BL176A)
SN65LBC176AP (Marked as 65LBC176A)
SN75LBC176AD (Marked as LB176A)
SN75LBC176AP (Marked as 75LBC176A)
(Top View)**

**Table 4-1. Pin Functions**

| NO | NAME | TYPE | DESCRIPTION |
|---|---|---|---|
| 1 | R | O | Receive data output |
| 2 | $\overline{RE}$ | I | Receiver enable, active low |
| 3 | DE | I | Driver enable, active high |
| 4 | D | I | Driver data input |
| 5 | GND | GND | Device ground |
| 6 | A | I/O | Bus I/O port, A (complementary to B) |
| 7 | B | I/O | Bus I/O port, B(complementary to A) |
| 8 | $V_{CC}$ | P | 5 V Supply Pin |

# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

| | | VALUE | UNIT |
|---|---|---|---|
| Supply voltage, $V_{CC}$ [(2)] | | –0.3 to 6 | V |
| Voltage range at any bus terminal (A or B) | | –10 to 15 | V |
| Input voltage, $V_I$ (D, DE, R, or $\overline{RE}$) | | –0.3 to $V_{CC}$ + 0.5 | V |
| Electrostatic discharge: | Bus terminals and GND, Class 3, A: [(3)] | 12 | kV |
| | Bus terminals and GND, Class 3, B: [(3)] | 400 | V |
| | All terminals, Class 3, A | 3 | kV |
| | All terminals, Class 3, B | 400 | V |
| Continuous total power dissipation[(4)] | | See Dissipation Rating Table | |
| Storage temperature range, $T_{stg}$ | | –65 to 150 | °C |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.
(3) The maximum operating junction temperature is internally limited. Use the dissipation rating table to operate below this temperature.
(4) Tested in accordance with MIL-STD-883C, Method 3015.7

## 5.2 Dissipation Ratings

| PACKAGE | $T_A \le 25°C$ POWER RATING | DERATING FACTOR[(1)] ABOVE $T_A$ = 25°C | $T_A$ = 70°C POWER RATING | $T_A$ = 85°C POWER RATING | $T_A$ = 125°C POWER RATING |
|---|---|---|---|---|---|
| D | 725 mW | 5.5 mW/°C | 464 mW | 377 mW | 145 mW |
| P | 1000 mW | 8.0 mW/°C | 640 mW | 520 mW | — |

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

## 5.3 Recommended Operating Conditions

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 4.75 | 5 | 5.25 | V |
| $V_I$ or $V_{IC}$ | Voltage at any bus terminal (separately or common mode) | | –7 | | 12 | V |
| $V_{IH}$ | High-level input voltage | D, DE, and $\overline{RE}$ | 2 | | $V_{CC}$ | V |
| $V_{IL}$ | Low-level input voltage | D, DE, and $\overline{RE}$ | 0 | | 0.8 | V |
| $V_{ID}$ | Differential input voltage[(2)] | | –12[(1)] | | 12 | V |
| $I_{OH}$ | High-level output current | Driver | –60 | | | mA |
| | | Receiver | –8 | | | |
| $I_{OL}$ | Low-level output current | Driver | | | 60 | mA |
| | | Reciever | | | 8 | |
| $T_A$ | Operating free-air temperature | SN65LBC176AQ | –40 | | 125 | °C |
| | | SN65LBC176A | –40 | | 85 | |
| | | SN75LBC176A | 0 | | 70 | |

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum, is used in this data sheet.
(2) Differential input /output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

## 5.4 Thermal Information

| THERMAL METRIC[1] | | All Devices in 'P' Package | SN65LBC176ADR SN65LBC176AQDR | OPNs Not Listed in Previous Column | UNIT |
|---|---|---|---|---|---|
| | | P (PDIP) | D (SOIC) | D (SOIC) | |
| | | 8-Pins | 8-Pins | 8-Pins | |
| $R_{θJA}$ | Junction-to-ambient thermal resistance | 65.7 | 116.7 | 110 | °C/W |
| $R_{θJC}$ | Junction-to-case thermal resistance | 54.7 | 56.3 | 44.1 | °C/W |
| $R_{θJB}$ | Junction-to-board thermal resistance | 42.1 | 63.4 | 53.5 | °C/W |
| $Ψ_{JT}$ | Junction-to-top characterization parameter | 23 | 8.8 | 4.8 | °C/W |
| $Ψ_{JB}$ | Junction-to-board characterization parameter | 41.7 | 62.9 | 52.7 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

## 5.5 Driver Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | | MIN | TYP[1] | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{IK}$ | Input clamp voltage | $I_I$ = –18 mA | | | –1.5 | –0.8 | | V |
| $\|V_{OD}\|$ | Differential output voltage | $I_O$ = 0 | | SN65LBC176AQ | 1.5 | 4 | 6 | V |
| | | | | SN65LBC176A, SN75LBC176A | | 4 | | |
| | | $R_L$ = 54 Ω, | See Figure 6-1 | SN65LBC176AQ | 0.9 | 1.5 | 6 | V |
| | | | | SN65LBC176A | 1 | 1.5 | 3 | |
| | | | | SN75LBC176A | 1.1 | 1.5 | 3 | |
| | | $V_{test}$ = –7 to 12 V, | See Figure 6-2 | SN65LBC176AQ | 0.9 | 1.5 | 6 | V |
| | | | | SN65LBC176A | 1 | 1.5 | 3 | |
| | | | | SN75LBC176A | 1.1 | 1.5 | 3 | |
| $Δ\|V_{OD}\|$ | Change in magnitude of differential output voltage | See Figure 6-1 and Figure 6-2 | | | –0.2 | | 0.2 | V |
| $V_{OC(SS)}$ | Steady-state common-mode output voltage | See Figure 6-1 | | SN65LBC176AQ | 1.8 | 2.4 | 3 | V |
| | | | | SN65LBC176A, SN75LBC176A | 1.8 | 2.4 | 2.8 | |
| $ΔV_{OC(SS)}$ | Change in steady-state common-mode output voltage | | | SN65LBC176AQ | –0.2 | | 0.2 | V |
| | | | | SN65LBC176A, SN75LBC176A | –0.1 | | 0.1 | |
| $I_{OZ}$ | High-impedance output current | See receiver input currents | | | | | | |
| $I_{IH}$ | High-level enable input current | $V_I$ = 2 V | | | –100 | | | µA |
| $I_{IL}$ | Low-level enable input current | $V_I$ = 0.8 V | | | –100 | | | µA |
| $I_{OS}$ | Short-circuit output current | –7 V ≤ $V_O$ ≤ 12 V | | | –250 | | 250 | mA |
| $I_{CC}$ | Supply current | $V_I$ = 0 or $V_{CC}$, No load | Receiver disabled and driver enabled | | | 5 | 9 | mA |
| | | | Receiver disabled and driver disabled | | | 0.4 | 0.7 | |
| | | | Receiver enabled and driver enabled | | | 8.5 | 15 | |

(1) All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

## 5.6 Driver Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | SN65LBC176AQ | | | SN65LBC176A SN75LBC176A | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP(1) | MAX | MIN | TYP(1) | MAX | |
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | $R_L$ = 54 Ω, $C_L$ = 50 pF, See Figure 6-3 | 2 | | 12 | 2 | 6 | 12 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | | 2 | | 12 | 2 | 6 | 12 | ns |
| $t_{sk(p)}$ | Pulse skew ( \| $t_{PLH}$ – $t_{PHL}$ \| ) | | | | 2 | | 0.3 | 1 | ns |
| $t_r$ | Differential output signal rise time | | 1.2 | | 11 | 4 | 7.5 | 11 | ns |
| $t_f$ | Differential output signal fall time | | 1.2 | | 11 | 4 | 7.5 | 11 | ns |
| $t_{PZH}$ | Propagation delay time, high-impedance-to-high-level output | $R_L$ = 110 Ω, See Figure 6-4 | | | 22 | | 12 | 22 | ns |
| $t_{PZL}$ | Propagation delay time, high-impedance-to-low- level output | $R_L$ = 110 Ω, See Figure 6-5 | | | 25 | | 12 | 22 | ns |
| $t_{PHZ}$ | Propagation delay time, high-level-to-high- impedance output | $R_L$ = 110 Ω, See Figure 6-4 | | | 22 | | 12 | 22 | ns |
| $t_{PLZ}$ | Propagation delay time, low-level-to-high- impedance output | $R_L$ = 110 Ω, See Figure 6-5 | | | 22 | | 12 | 22 | ns |

(1) All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

## 5.7 Receiver Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{IT+}$ | Positive-going input threshold voltage | $I_O$ = –8 mA | | | | | 0.2 | V |
| $V_{IT–}$ | Negative-going input threshold voltage | $I_O$ = 8 mA | | | –0.2 | | | V |
| $V_{hys}$ | Hysteresis voltage (VIT + - VIT -) | | | | | 50 | | mV |
| $V_{IK}$ | Enable-input clamp voltage | II = - 18 mA | | | –1.5 | –0.8 | | V |
| $V_{OH}$ | High-level output voltage | $V_{ID}$ = 200 mV, | $I_{OH}$ = –8 mA, | See Figure 6-6 | 4 | 4.9 | | V |
| $V_{OL}$ | Low-level output voltage | $V_{ID}$ = –200 mV, | $I_{OH}$ = 8 mA, | See Figure 6-6 | | 0.1 | 0.8 | V |
| $I_{OZ}$ | High-impedance-state output current | $V_O$ = 0 to $V_{CC}$ | | SN65LBC176AQ | –10 | | 10 | μA |
| | | | | SN65LBC176A, SN75LBC176A | –1 | | 1 | |
| $I_I$ | Bus input current | $V_{IH}$ = 12 V, | $V_{CC}$ = 5 V | Other input at 0 V | | 0.4 | 1 | mA |
| | | $V_{IH}$ = 12 V, | $V_{CC}$ = 0 | | | 0.5 | 1 | |
| | | $V_{IH}$ = –7 V, | $V_{CC}$ = 5 V | | –0.8 | –0.4 | | |
| | | $V_{IH}$ = –7 V, | $V_{CC}$ = 0 | | –0.8 | –0.3 | | |
| $I_{IH}$ | High-level enable-input current | $V_{IH}$ = 2 V | | | –100 | | | μA |
| $I_{IL}$ | Low-level enable-input current | $V_{IL}$ = 0.8 V | | | –100 | | | μA |
| $I_{CC}$ | Supply current | $V_I$ = 0 or $V_{CC}$, No load | Receiver enabled and driver disabled | | | 4 | 7 | mA |
| | | | Receiver disabled and driver disabled | | | 0.4 | 0.7 | |
| | | | Receiver enabled and driver enabled | | | 8.5 | 15 | |

(1) All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

## 5.8 Receiver Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | SN65LBC176AQ | | | SN65LBC176A SN75LBC176A | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP(1) | MAX | MIN | TYP(1) | MAX | |
| $t_{PLH}$ | Propagation delay time output↑ | $V_{ID}$ = –1.5 V to 1.5 V, See Figure 6-7 | 7 | | 30 | 7 | 13 | 20 | ns |
| $t_{PHL}$ | Propagation delay time output↓ | | 7 | | 30 | 7 | 13 | 20 | ns |
| $t_{sk(p)}$ | Pulse skew ( \| $t_{PLH}$ – $t_{PHL}$ \| ) | | | | 6 | | 0.5 | 1.5 | ns |
| $t_r$ | Rise time, output | See Figure 6-7 | | | 5 | | 2.1 | 3.3 | ns |
| $t_f$ | Fall time, output | | | | 5 | | 2.1 | 3.3 | ns |
| $t_{PZH}$ | Output enable time to high level | $C_L$ = 10 pF, See Figure 6-8 | | | 50 | | 30 | 45 | ns |
| $t_{PZL}$ | Output enable time to low level | | | | 50 | | 30 | 45 | ns |
| $t_{PHZ}$ | Output disable time to high level | | | | 60 | | 20 | 40 | ns |
| $t_{PLZ}$ | Output disable time to low level | | | | 60 | | 20 | 40 | ns |

(1) All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

## Typical Characteristics

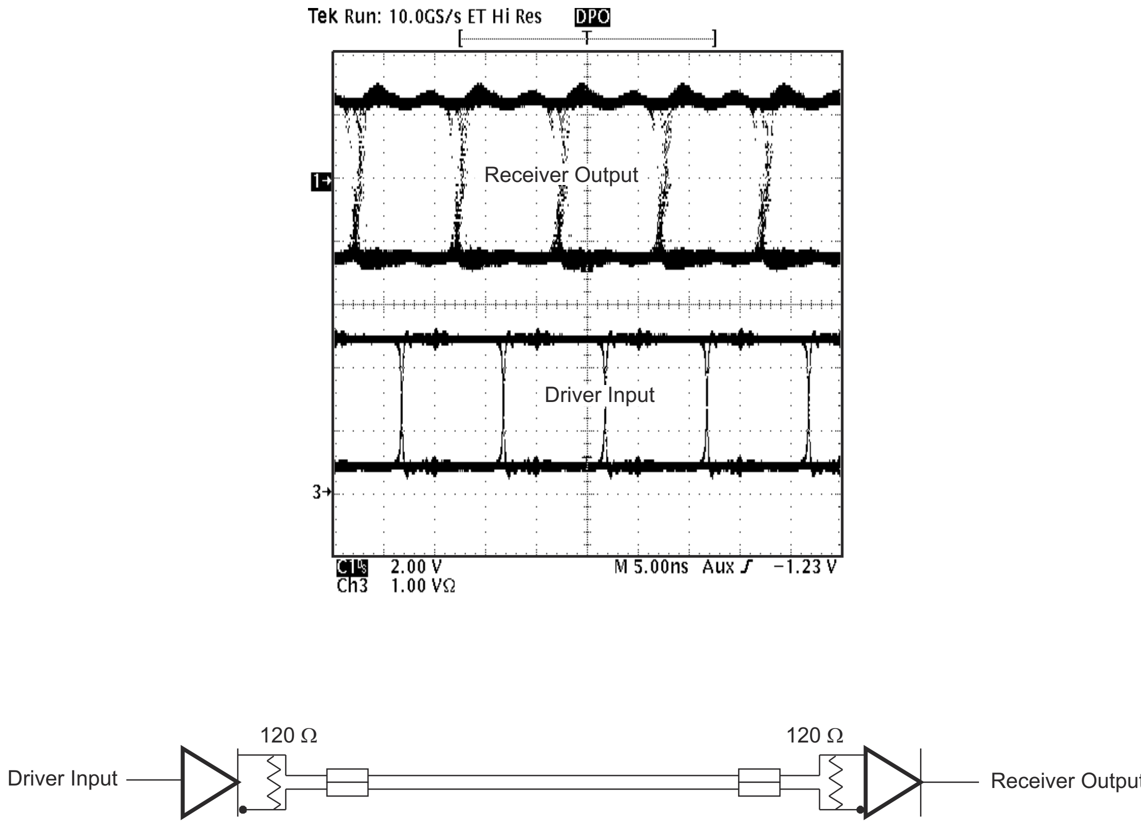



**Figure 5-1. Typical Waveform of Non-Return-To-Zero (NRZ), Pseudorandom Binary Sequence (PRBS) Data at 100 Mbps Through 15m, of CAT 5 Unshielded Twisted Pair (UTP) Cable**

TIA/EIA-485-A defines a maximum signaling rate as that in which the transition time of the voltage transition of a logic-state change remains less than or equal to 30% of the bit length. Transition times of greater length perform quite well even though they do not meet the standard definition.

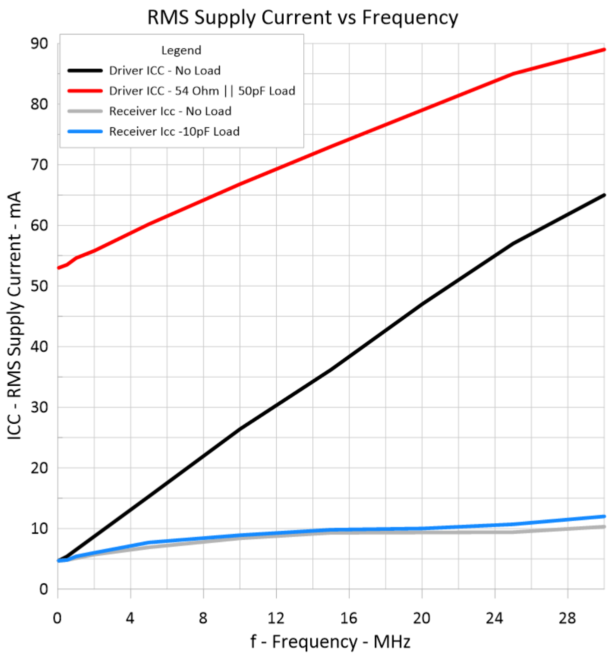



**Figure 5-2. RMS Supply Current vs Frequency**

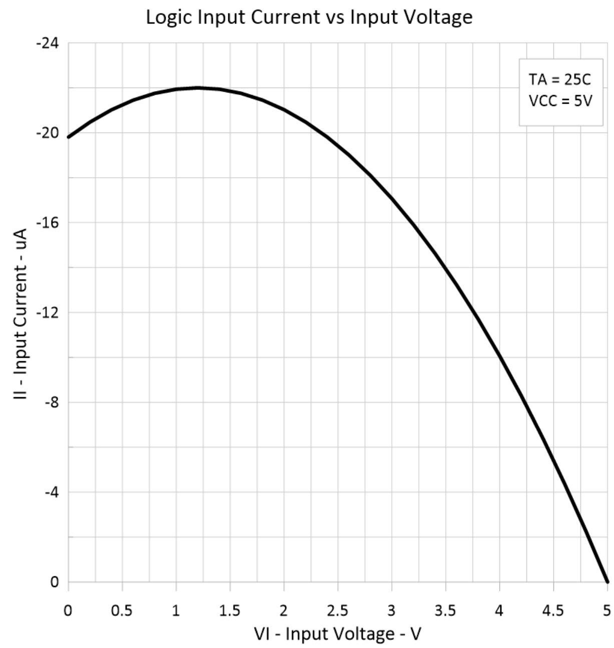



**Figure 5-3. Logic Input Current vs Input Voltage**

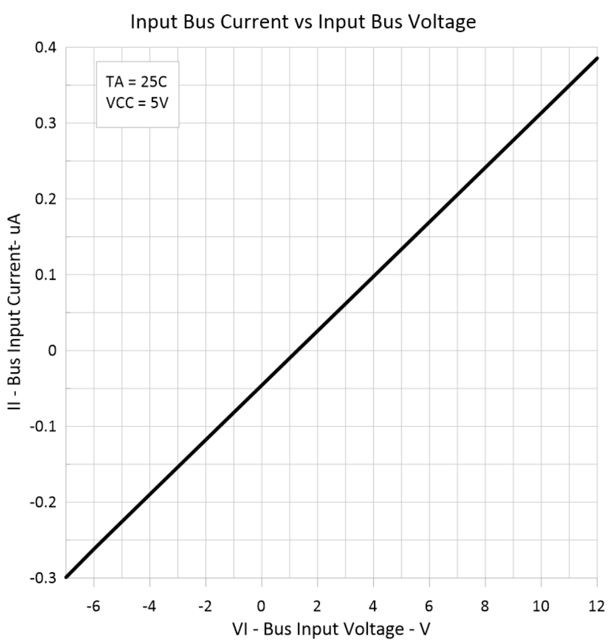



**Figure 5-4. Input Current vs Input Voltage**

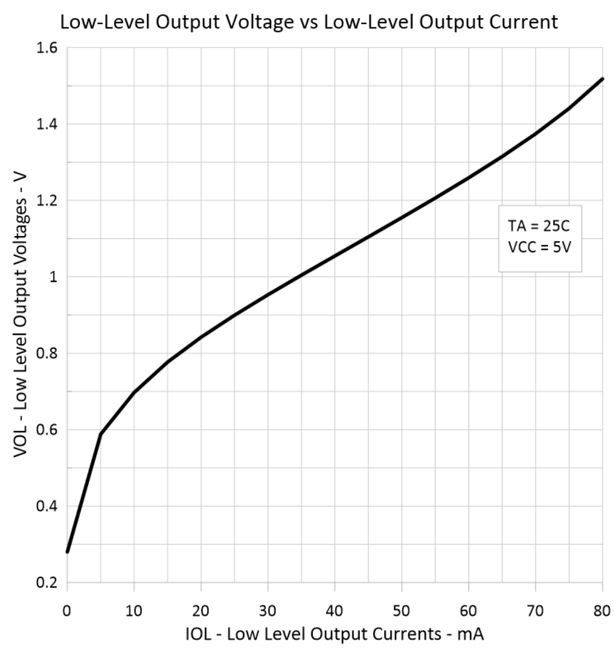



**Figure 5-5. Low-Level Output Voltage vs Low-Level Output Current**

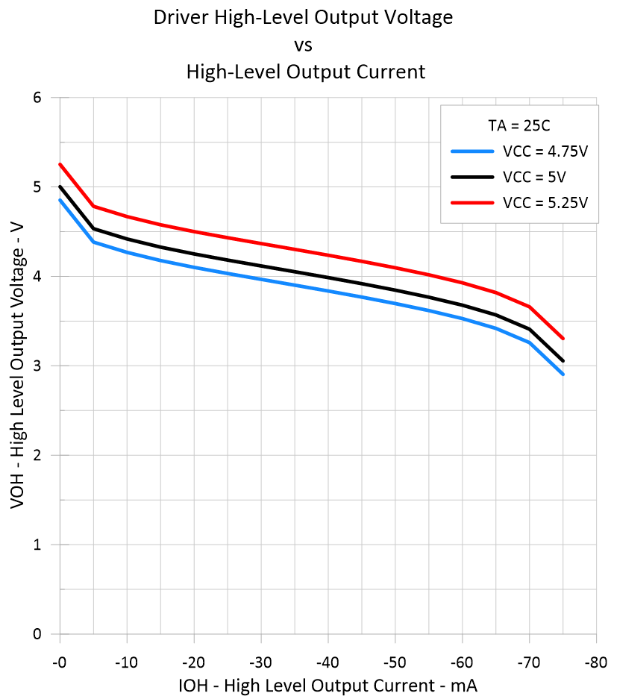



**Figure 5-6. Driver High-Level Output Voltage vs High-Level Output Current**

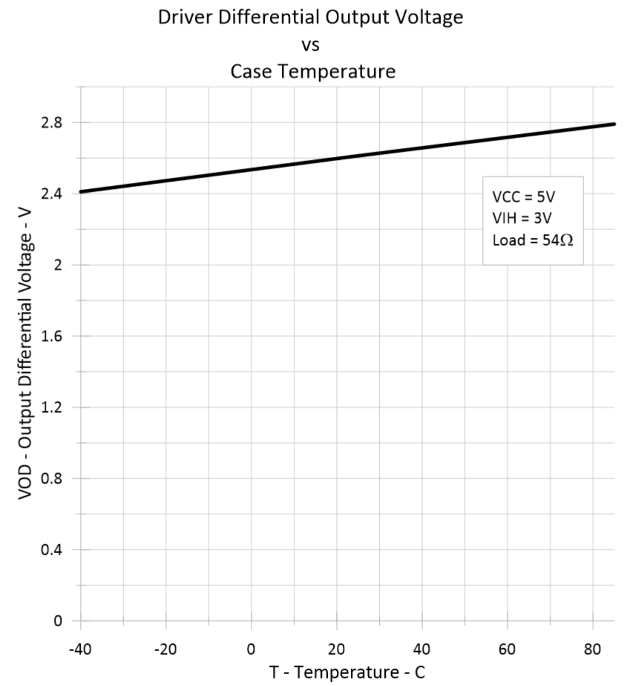



**Figure 5-7. Driver Differential Output Voltage vs Case Temperature**

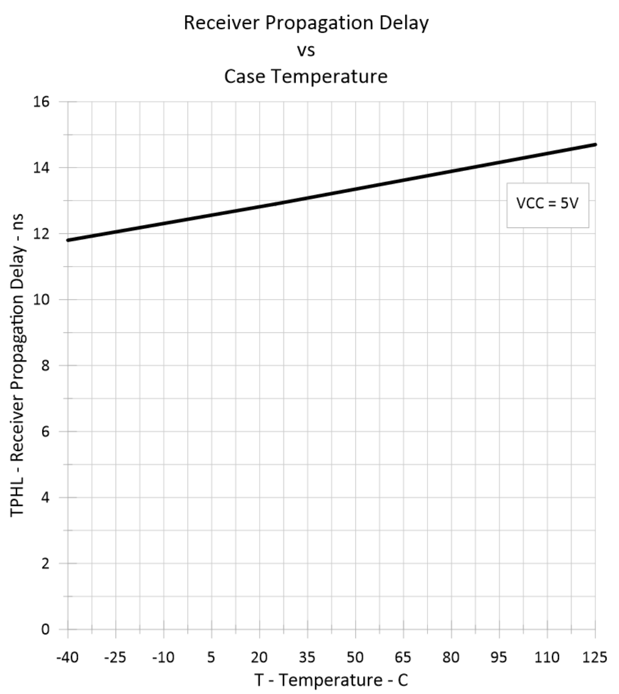



**Figure 5-8. Receiver Propagation Time vs Case Temperature**

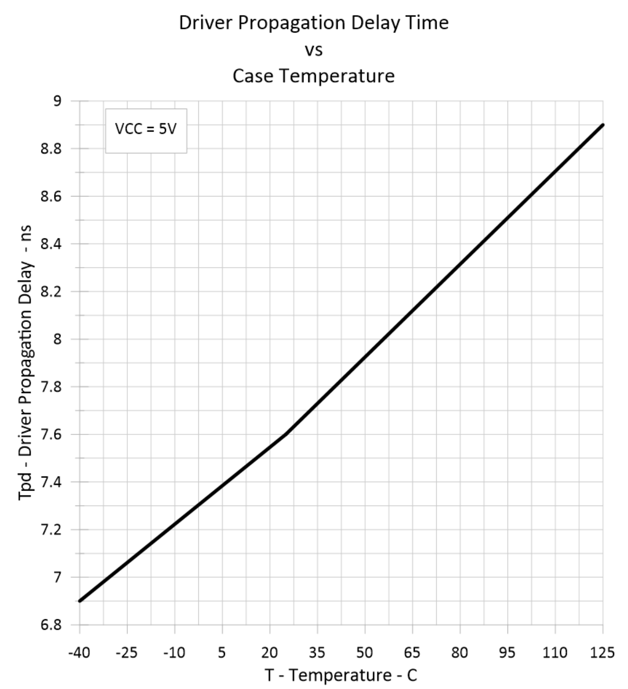



**Figure 5-9. Driver Propagation Delay Time vs Case Temperature**

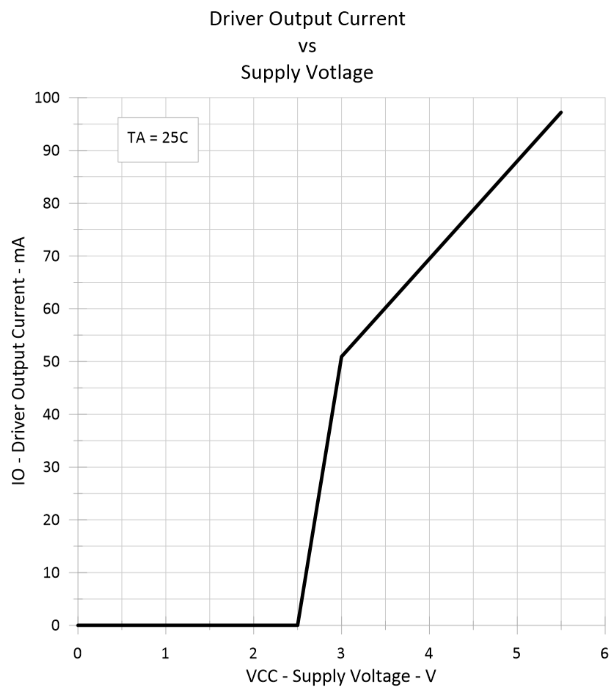



**Figure 5-10. Driver Output Current vs Supply Voltage**

## Parameter Measurement Information

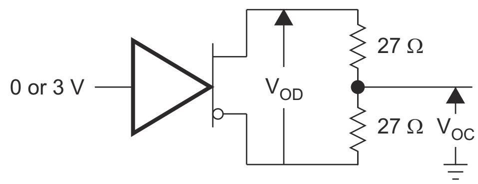



**Figure 6-1. Driver $V_{OD}$ and $V_{OC}$**

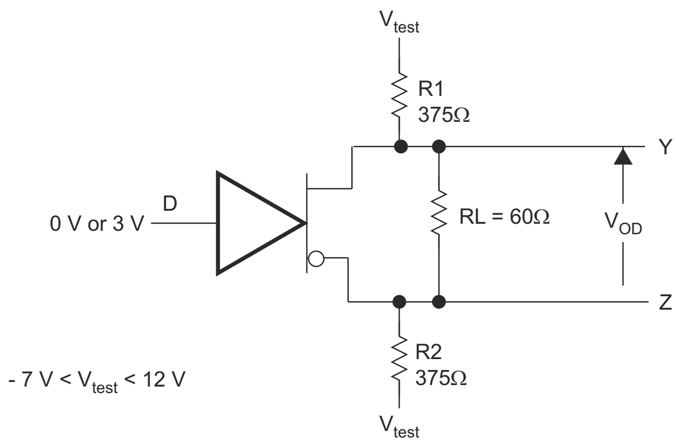
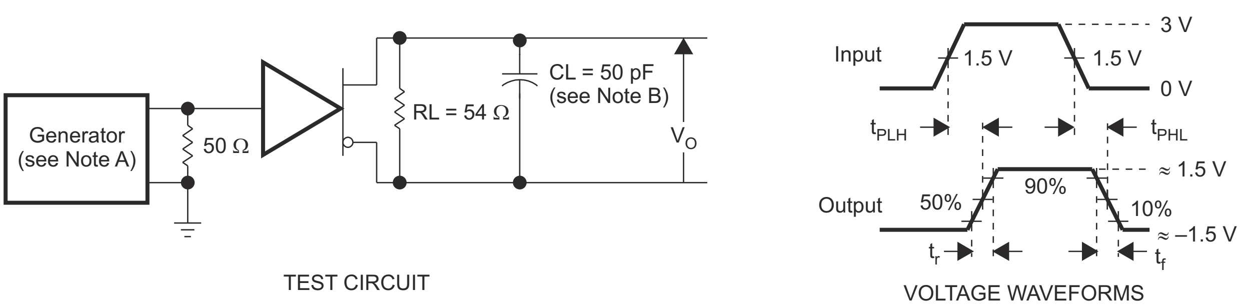


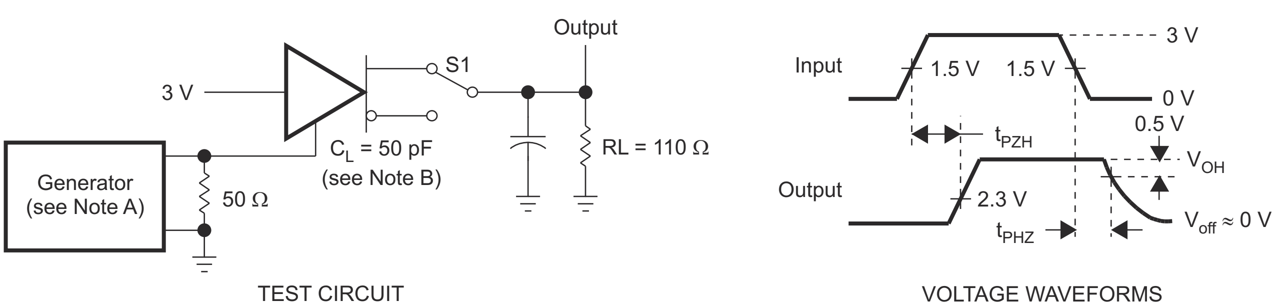

**Figure 6-2. Driver $V_{OD3}$**




A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, $t_r$ ≤ 6 ns, $t_f$ ≤ 6 ns, $Z_O$ = 50Ω.

B. $C_L$ includes probe and jig capacitance.

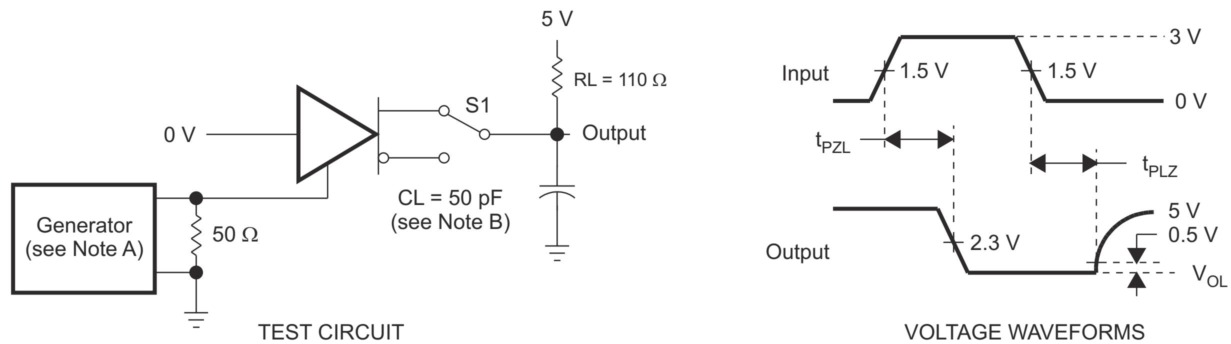
**Figure 6-3. Driver Test Circuit and Voltage Waveforms**




A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, $t_r$ ≤ 6 ns, $t_f$ ≤ 6 ns, $Z_O$ = 50Ω.

B. $C_L$ includes probe and jig capacitance.

**Figure 6-4. Driver Test Circuit and Voltage Waveforms**




A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, $t_r$ ≤ 6 ns, $t_f$ ≤ 6 ns, $Z_O$ = 50Ω.

B. $C_L$ includes probe and jig capacitance.

**Figure 6-5. Driver Test Circuit and Voltage Waveforms**

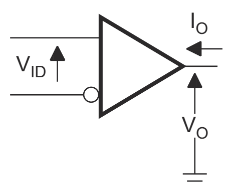
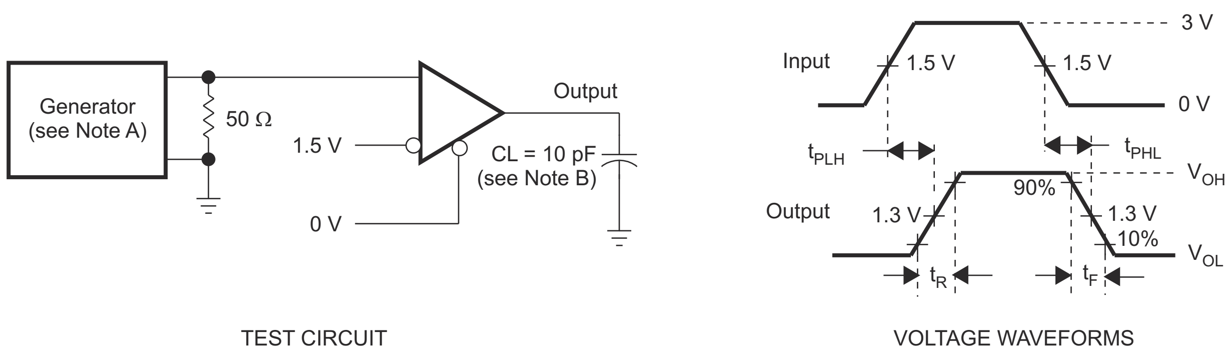


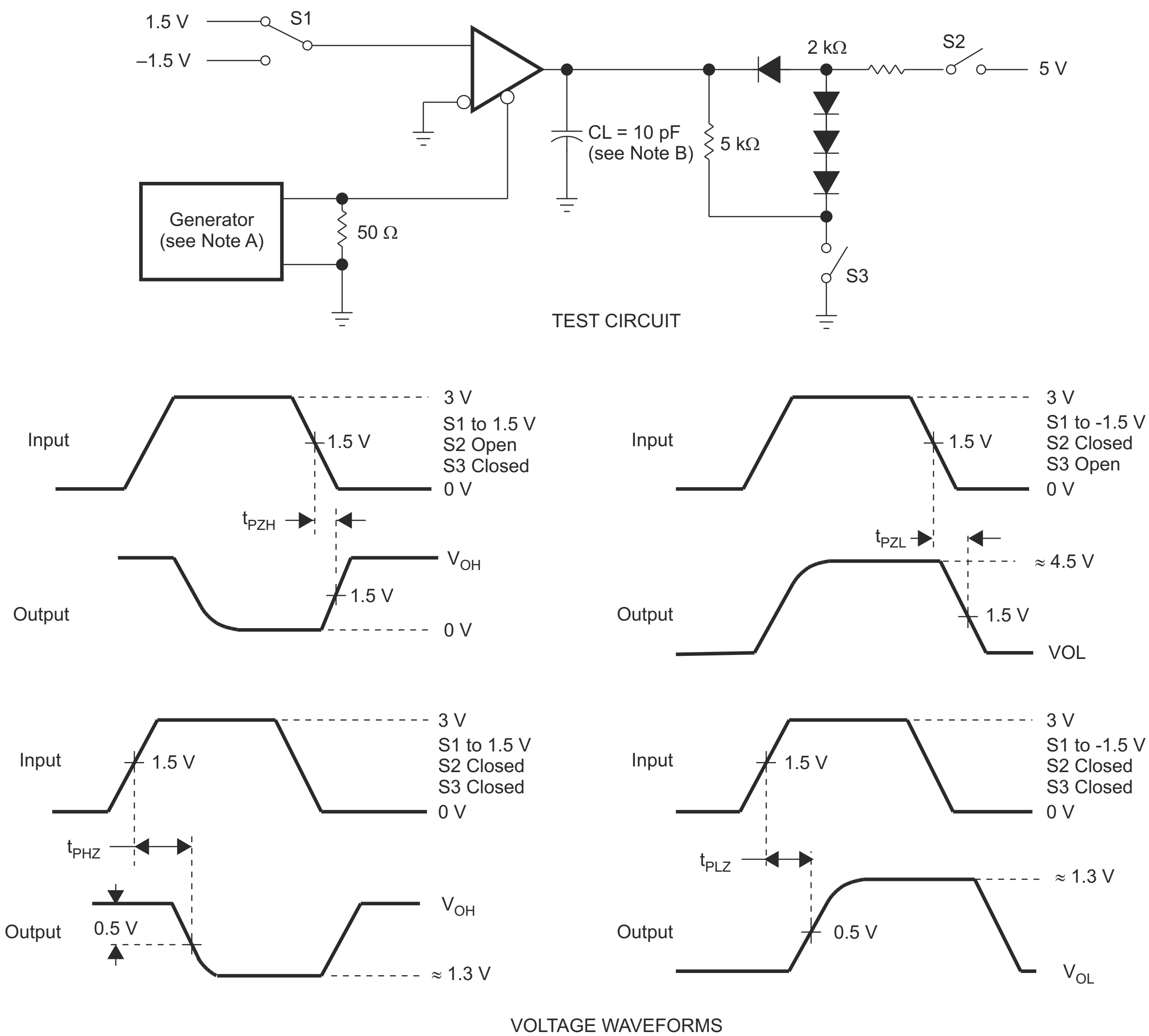

**Figure 6-6. Receiver $V_{OH}$ and $V_{OL}$**




A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, $t_r$ ≤ 6 ns, $t_f$ ≤ 6 ns, $Z_O$ = 50Ω.

B. $C_L$ includes probe and jig capacitance.

**Figure 6-7. Receiver Test Circuit and Voltage Waveforms**




A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, $t_r$ ≤ 6 ns, $t_f$ ≤ 6 ns, $Z_O$ = 50Ω.

B. $C_L$ includes probe and jig capacitance.

**Figure 6-8. Receiver Test Circuit and Voltage Waveforms**

# 6 Detailed Description

## 6.1 Device Functional Modes

### 6.1.1 Function Tables

| DRIVER | | | |
|---|---|---|---|
| INPUT D | ENABLE DE | OUTPUTS A | OUTPUTS B |
| H | H | H | L |
| L | H | L | H |
| X | L | Z | Z |
| Open | H | H | L |

| RECEIVER | | |
|---|---|---|
| DIFFERENTIAL INPUTS $V_A – V_B$ | ENABLE(1) $\overline{RE}$ | OUTPUT(1) R |
| $V_{ID} \geq 0.2$ V | L | H |
| $–0.2$ V < $V_{ID}$ < 0.2 V | L | ? |
| $V_{ID} \leq –0.2$ V | L | L |
| X | H | Z |
| Open | L | H |

(1) H = high level, L - low level, ? = indeterminate, X = Irrelevant, Z = high impedance (off)

### 6.1.2 Schematics

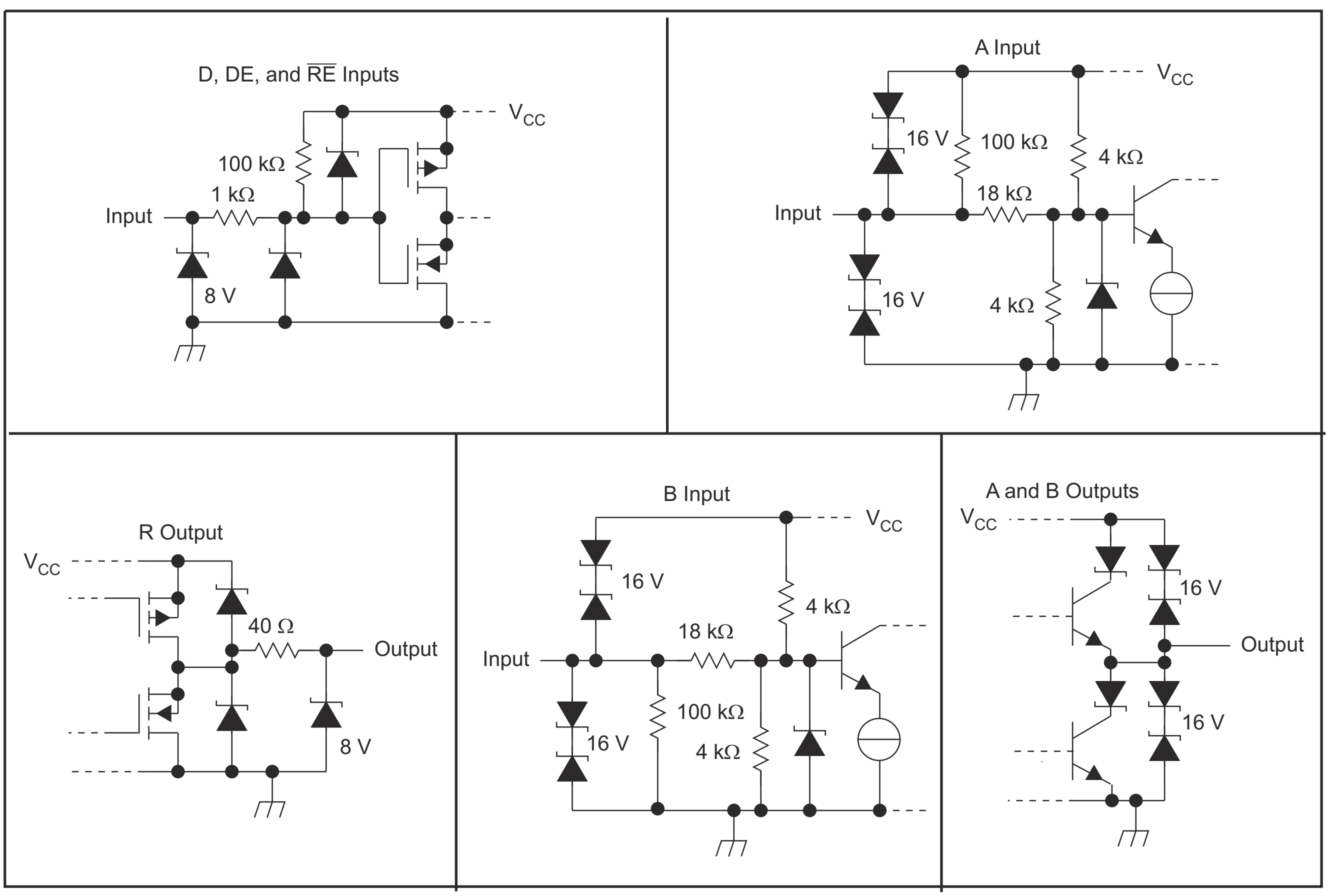



**Figure 6-1. Schematics of Inputs and Outputs**

# 7 Device and Documentation Support

## 7.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 7.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 7.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

## 7.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 7.5 Glossary

TI Glossary    This glossary lists and explains terms, acronyms, and definitions.

# 8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN65LBC176ADR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | BL176A | Samples |
| SN65LBC176AQD | NRND | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | B176AQ | |
| SN65LBC176AQDG4 | NRND | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | | B176AQ | |
| SN65LBC176AQDR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | B176AQ | Samples |
| SN65LBC176AQDRG4 | NRND | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | | B176AQ | |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN65LBC176A :**

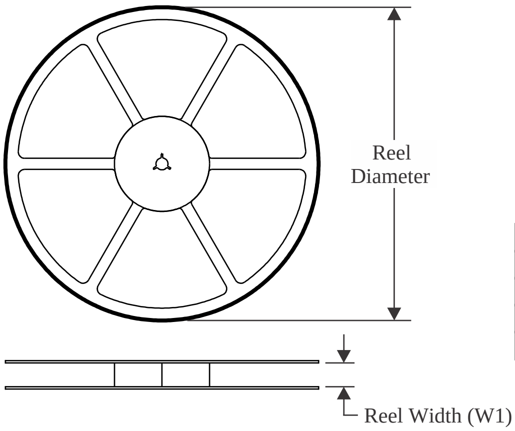
- Enhanced Product : SN65LBC176A-EP

NOTE: Qualified Version Definitions:

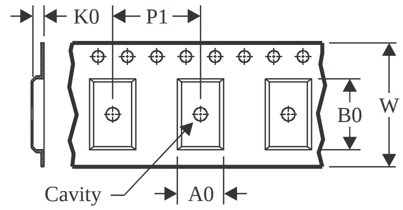
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

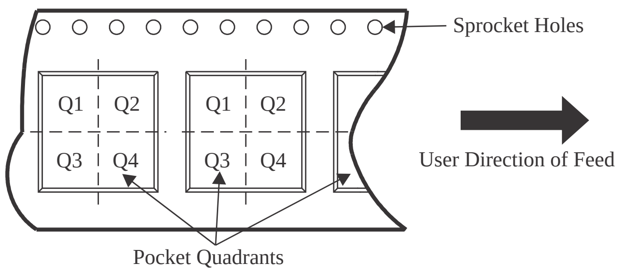



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

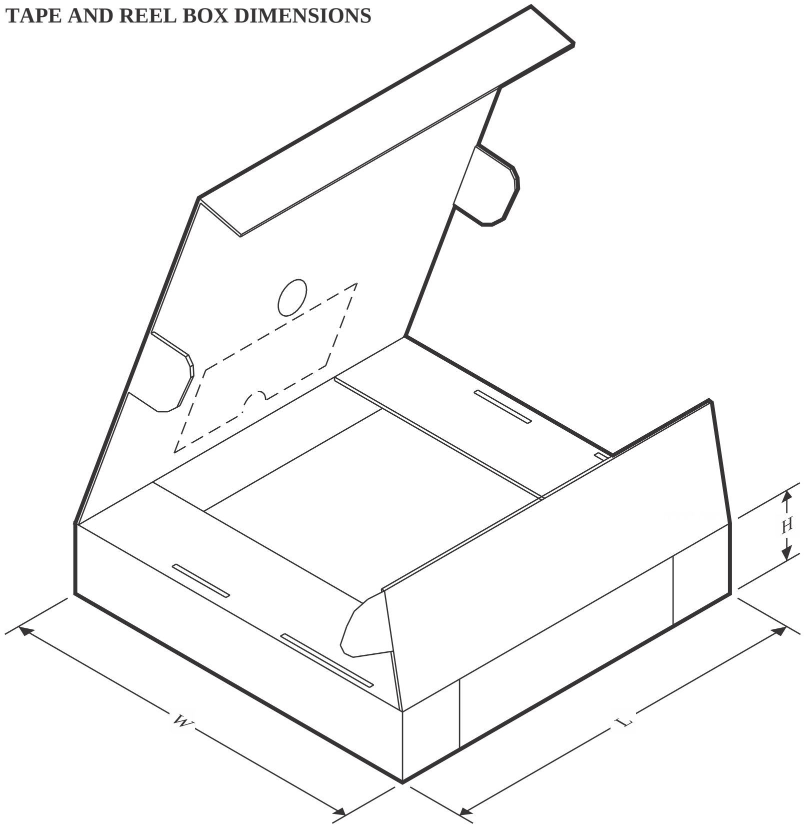
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN65LBC176ADR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

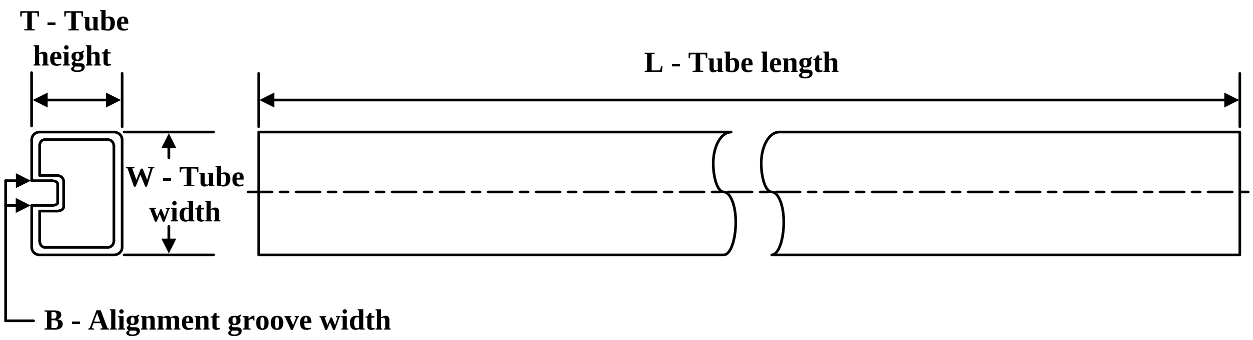
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

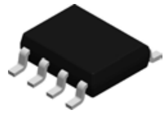
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN65LBC176ADR | SOIC | D | 8 | 2500 | 356.0 | 356.0 | 35.0 |

## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| SN65LBC176AQD | D | SOIC | 8 | 75 | 505.46 | 6.76 | 3810 | 4 |
| SN65LBC176AQDG4 | D | SOIC | 8 | 75 | 505.46 | 6.76 | 3810 | 4 |

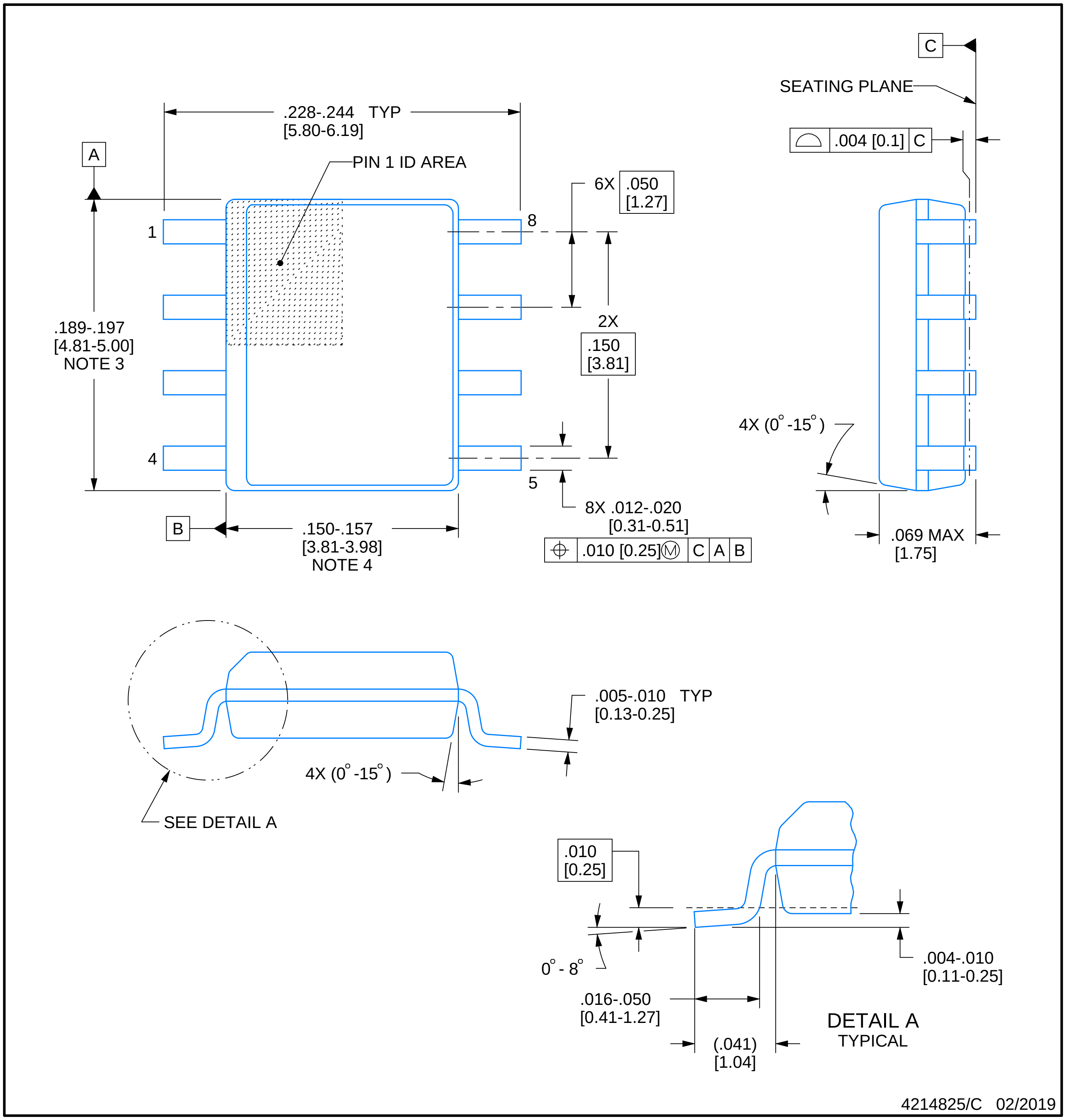


# PACKAGE OUTLINE

## D0008A

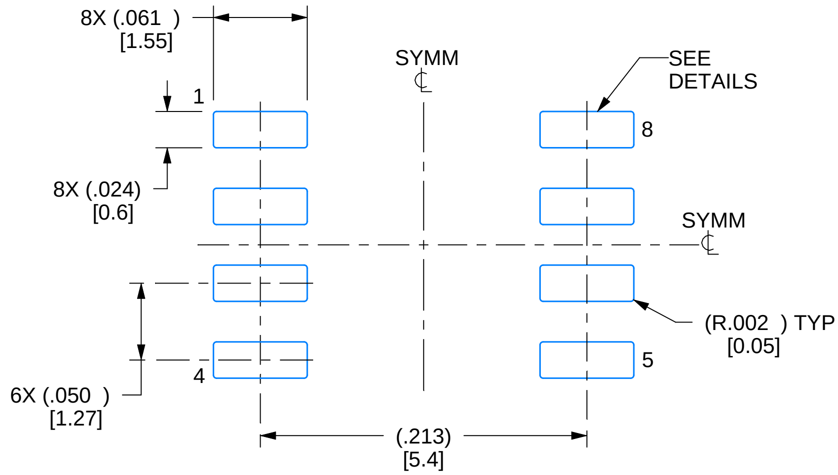
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

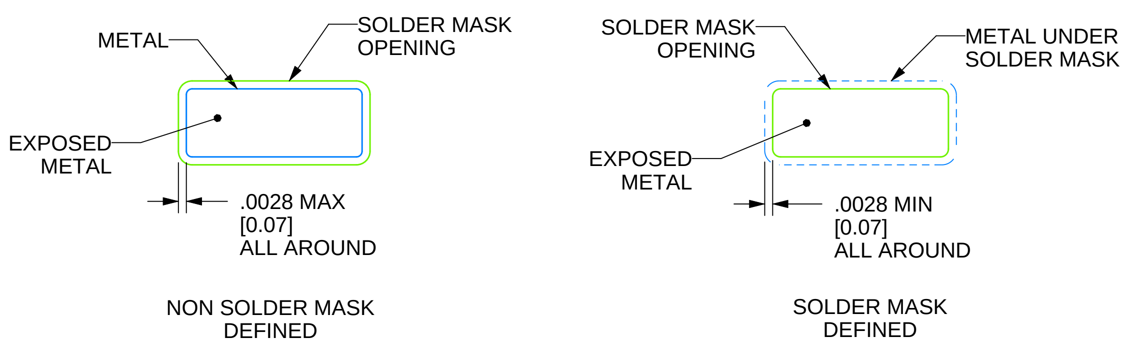



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

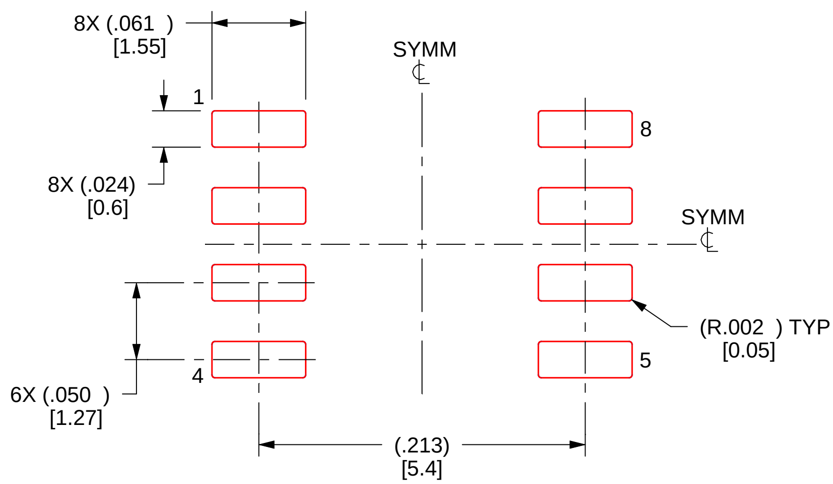



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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