ISO723xx High-Speed, Triple-Channel Digital Isolators

1 Features

- 25 and 150-Mbps Signaling Rate Options
  - Low Channel-to-Channel Output Skew; 1 ns Maximum
  - Low Pulse-Width Distortion (PWD); 2 ns Maximum
  - Low Jitter Content; 1 ns Typical at 150 Mbps
- Typical 25-Year Life at Rated Working Voltage (See Application Note SLLA197 and Figure 19)
- 4-kV ESD Protection
- Operate With 3.3-V or 5-V Supplies
- 3.3-V and 5-V Level Translation
- High Electromagnetic Immunity (See Application Note SLLA181)
- –40°C to 125°C Operating Range
- Safety and Regulatory Approvals
  - 4000-V_{PK} Isolation per DIN V VDE V 0884-10 and DIN EN 61010-1
  - 2500 V_{RMS} Isolation for 1 minute per UL 1577
  - CSA Component Acceptance Notice 5A and IEC 60950-1 End Equipment Standard

2 Applications

- Industrial Fieldbus
- Computer Peripheral Interface
- Servo Control Interface
- Data Acquisition

3 Description

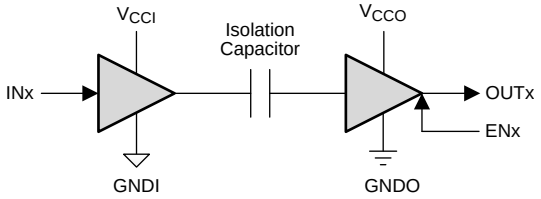
The ISO7230 and ISO7231 are triple-channel digital isolators each with multiple channel configurations and output enable functions. These devices have logic input and output buffers separated by TI's silicon dioxide (SiO_2) isolation barrier. Used in conjunction with isolated power supplies, these devices block high voltage, isolate grounds, and prevent noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ISO7230C ISO7230M ISO7231C ISO7231M	SOIC (16)	10.30 mm × 7.50 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



(1) V_{CCI} and GNDI are supply and ground connections respectively for the input channels.

(2) V_{CCO} and GNDO are supply and ground connections respectively for the output channels.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision J (May 2015) to Revision K — **Page**

- Added Note 1 to L(I01) and changed the MIN value From: 8.34 To 8 mm in the *Package Insulation and Safety-Related Specifications* table ... 18
- Added Note 1 to LI02) and changed the MIN value From: 8.1 To 8 mm in the *Package Insulation and Safety-Related Specifications* table ... 18
- Deleted Note 1 From the *Regulatory Information* table ... 18
- Changed The ground symbols on the Enable circuit in Figure 15 ... 20

Changes from Revision I (January 2011) to Revision J — **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Updated Thermal Information ... 6
- Updated Regulatory Information ... 18

Changes from Revision H (December 2009) to Revision I — **Page**

- Changed I_{OH} Min value to -4 and deleted the Max value, in the *Recommended Operating Conditions* Table ... 5
- Changed I_{OL} Max value to 4 and deleted the Min value, in the *Recommended Operating Conditions* Table ... 5
- Changed Figure 8, Figure 10, Figure 11, and Figure 12 ... 15
- Changed File Number: 1698195 To: 220991 ... 18

Changes from Revision G (September 2009) to Revision H **Page**

- Changed The Input circuit in Figure 15 20

Changes from Revision F (December 2008) to Revision G **Page**

- Added IEC 60950-1 and CSA Approved to the *Features* list 1

Changes from Revision E (June 2008) to Revision F **Page**

- Deleted device numbers ISO7230A and ISO7231A from the data sheet. 1
- Added $t_{sk(pp)}$ footnote 10
- Added $t_{sk(o)}$ footnote. 10
- Added $t_{sk(pp)}$ footnote 12
- Added $t_{sk(o)}$ footnote. 12
- Changed the *Package Insulation and Safety-Related Specifications* table, line 1, $L_{(IO1)}$ MIN from 7.7 to 8.34 18

Changes from Revision D (May 2008) to Revision E **Page**

- Added Note: For the 5-V operation, VCC1 or VCC2 is specified from 4.5 V to 5.5 V. For the 3-V operation, VCC1 or VCC2 is specified from 3.15 V to 3.6 V. 6
- Added Note: For the 5-V operation, VCC1 or VCC2 is specified from 4.5 V to 5.5 V. For the 3-V operation, VCC1 or VCC2 is specified from 3.15 V to 3.6 V. 7
- Added Note: For the 5-V operation, VCC1 or VCC2 is specified from 4.5 V to 5.5 V. For the 3-V operation, VCC1 or VCC2 is specified from 3.15 V to 3.6 V. 8
- Added Note: For the 5-V operation, VCC1 or VCC2 is specified from 4.5 V to 5.5 V. For the 3-V operation, VCC1 or VCC2 is specified from 3.15 V to 3.6 V. 9

Changes from Revision C (April 2008) to Revision D **Page**

- Changed Features bullet 4000-V_{peak} Isolation to the *Features* list 1
- Added $t_{sk(pp)}$ Part-to-part skew 10
- Added $t_{sk(pp)}$ Part-to-part skew 11
- Added $t_{sk(pp)}$ Part-to-part skew 12
- Added $t_{sk(pp)}$ Part-to-part skew 12

Changes from Revision B (April 2008) to Revision C **Page**

- Deleted Min = 4.5 V and max = 5.5 V for Supply Voltage of the *Recommended Operating Conditions* Table 5
- Changed Supply Voltage of the *Recommended Operating Conditions* Table From: 3.6 To: 5.5 5

Changes from Revision A (December 2007) to Revision B **Page**

- Changed Supply Voltage of the ROC Table From: 3.45 To: 3.6 5

Changes from Original (September 2007) to Revision A **Page**

- Deleted Product Preview note 4
- Changed TBD to actual values 6
- Changed V_{CC} – 0.4 To: V_{CC} – 0.8 6

- Changed C_I - Typical value from 1 To: 2 6
- Changed C_I - Typical value from 1 To: 2 7
- Changed C_I - Typical value from 1 To: 2 8
- Changed C_I - Typical value from 1 To: 2 9
- Changed Propagation delay max From: 22 To: 23 10
- Changed Propagation delay max From: 46 To: 50 11
- Changed Propagation delay max From: 28 To: 29 11
- Changed Propagation delay max From: 26 To: 30 12
- Changed Propagation delay max From: 32 To: 34 12
- Changed C_{IO} - Typical value from 1 To: 2 18

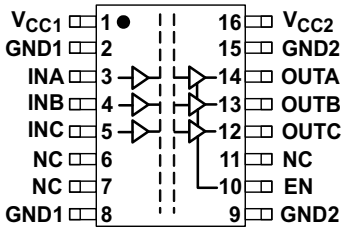
5 Device Comparison Table

PRODUCT	SIGNALING RATE	INPUT THRESHOLD	CHANNEL CONFIGURATION	ISOLATION RATING
ISO7230C	25 Mbps	~1.5 V (TTL) (CMOS compatible)	3/0	4000 V_{PK}, 2500 V_{RMS}
ISO7230M	150 Mbps	V_{CC}/2 (CMOS)		
ISO7231C	25 Mbps	~1.5 V (TTL) (CMOS compatible)	2/1	
ISO7231M	150 Mbps	V_{CC}/2 (CMOS)		

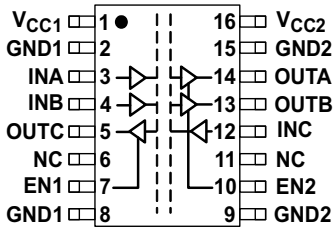
6 Pin Configuration and Functions

DW Package
16-Pin SOIC
Top View

ISO7230



ISO7231



Pin Functions

PIN			TYPE	DESCRIPTION
NAME	ISO7230	ISO7231		
EN	10	–	I	Enable, channel A, B, and C
EN1	–	7	I	Enable, channel C
EN2	–	10	I	Enable, channel A and B
GND1	2, 8	2, 8	–	Ground connection for V_{CC1}
GND2	9, 15	9. 15	–	Ground connection for V_{CC2}
INA	3	3	I	Input, channel A
INB	4	4	I	Input, channel B
INC	5	12	I	Input, channel C
NC	6, 7, 11	6, 11	–	Not connected
OUTA	14	14	O	Output, channel A
OUTB	13	13	O	Output, channel B
OUTC	12	5	O	Output, channel C
V_{CC1}	1	1	–	Power supply, V_{CC1}
V_{CC2}	16	16	–	Power supply, V_{CC2}

7 Specifications

7.1 Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage(2), V_{CC1}, V_{CC2}	–0.5	6	V
V_I	Voltage at INx, OUTx, ENx	–0.5	V_{CC} + 0.5(3)	V
I_O	Output current	–15	15	mA
T_J	Maximum junction temperature		170	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal and are peak voltage values.
(3) Maximum voltage must not exceed 6 V.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	
		Machine model (MM), ANSI/ESDS5.2-1996	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage - 3.3-V Operation		3.15		5.5	V
	Supply voltage - 5-V Operation					
I_{OH}	High-level output current		–4			mA
I_{OL}	Low-level output current				4	mA
t_{ui}	Input pulse width	ISO723xC	40			ns
		ISO723xM	6.67	5		
$1/t_{ui}$	Signaling rate	ISO723xC	0	30(1)	25	Mbps
		ISO723xM	0	200(1)	150	
V_{IH}	High-level input voltage (IN)	ISO723xM	0.7 V_{CC}		V_{CC}	V
V_{IL}	Low-level input voltage (IN)		0		0.3 V_{CC}	
V_{IH}	High-level input voltage (IN) (EN on all devices)	ISO723xC	2		5.5	V
V_{IL}	Low-level input voltage (IN) (EN on all devices)		0		0.8	
T_A	Ambient temperature		-40	25	125	°C
T_J	Junction temperature				150	°C
H	External magnetic field-strength immunity per IEC 61000-4-8 and IEC 61000-4-9				1000	A/m

(1) Typical sigalling rate under ideal conditions at 25°C.

7.4 Thermal Information

THERMAL METRIC[1]		ISO7230C, ISO7230M ISO7231C, ISO7231M DW (SOIC) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	168	°C/W
		77.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	39.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	41.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	13.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	41.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics: V_{CC1} and V_{CC2} at 5-V[1]

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I_{CC1}	ISO7230C/M	Quiescent	V_I = V_{CCI} or 0 V, all channels, no load, EN at 3 V		1	3	mA
		25 Mbps			7	9.5	
	ISO7231C/M	Quiescent	V_I = V_{CCI} or 0 V, all channels, no load, EN1 at 3 V, EN2 at 3 V		6.5	11	mA
		25 Mbps			11	17	
I_{CC2}	ISO7230C/M	Quiescent	V_I = V_{CCI} or 0 V, all channels, no load, EN at 3 V		15	22	mA
		25 Mbps			17	24	
	ISO7231C/M	Quiescent	V_I = V_{CCI} or 0 V, all channels, no load, EN1 at 3 V, EN2 at 3 V		13	20	mA
		25 Mbps			17.5	27	
ELECTRICAL CHARACTERISTICS							
I_{OFF}	Sleep mode output current		ENx at 0 V, single channel		0		µA
V_{OH}	High-level output voltage		I_{OH} = –4 mA, See Figure 8	V_{CCO} – 0.8			V
			I_{OH} = –20 µA, See Figure 8	V_{CCO} – 0.1			
V_{OL}	Low-level output voltage		I_{OL} = 4 mA, See Figure 8			0.4	V
			I_{OL} = 20 µA, See Figure 8			0.1	
$V_{I(HYS)}$	Input voltage hysteresis				150		mV
I_{IH}	High-level input current		INx at V_{CCI}			10	µA
I_{IL}	Low-level input current		INx at 0 V	–10			
C_I	Input capacitance to ground		INx at V_{CCI}, V_I = 0.4 sin (4E6πt)		2		pF
CMTI	Common-mode transient immunity		V_I = V_{CCI} or 0 V, See Figure 11	25	50		kV/µs

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3.3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V.

7.6 Electrical Characteristics: V_{CC1} at 5-V, V_{CC2} at 3.3-V[1]

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENT								
I_{CC1}	ISO7230C/M	Quiescent	V_I = V_{CCI} or 0 V, all channels, no load, EN at 3 V			1	3	mA
		25 Mbps				7	9.5	
	ISO7231C/M	Quiescent	V_I = V_{CCI} or 0 V, all channels, no load, EN1 at 3 V, EN2 at 3 V			6.5	11	mA
		25 Mbps				11	17	
I_{CC2}	ISO7230C/M	Quiescent	V_I = V_{CCI} or 0 V, all channels, no load, EN at 3 V			9	15	mA
		25 Mbps				10	17	
	ISO7231C/M	Quiescent	V_I = V_{CCI} or 0 V, all channels, no load, EN1 at 3 V, EN2 at 3 V			8	12	mA
		25 Mbps				10.5	16	
ELECTRICAL CHARACTERISTICS								
I_{OFF}	Sleep mode output current		ENx at 0 V, Single channel			0		µA
V_{OH}	High-level output voltage		I_{OH} = –4 mA, See Figure 8	ISO7230	V_{CCO} – 0.4			V
				ISO7231 (5-V side)	V_{CCO} – 0.8			
			I_{OH} = –20 µA, See Figure 8		V_{CCO} – 0.1			
V_{OL}	Low-level output voltage		I_{OL} = 4 mA, See Figure 8				0.4	V
			I_{OL} = 20 µA, See Figure 8				0.1	
$V_{I(HYS)}$	Input voltage hysteresis					150		mV
I_{IH}	High-level input current		INx at V_{CCI}				10	µA
I_{IL}	Low-level input current		INx at 0 V		–10			
C_I	Input capacitance to ground		INx at V_{CCI}, V_I = 0.4 sin (4E6πt)			2		pF
CMTI	Common-mode transient immunity		V_I = V_{CCI} or 0 V, See Figure 11		25	50		kV/µs

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3.3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V.

7.7 Electrical Characteristics: V_{CC1} at 3.3-V, V_{CC2} at 5-V(1)

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENT								
I_{CC1}	ISO7230C/M	Quiescent	V_I = V_{CCI} or 0 V, all channels, no load, EN at 3 V			0.5	1	mA
		25 Mbps				3	5	
	ISO7231C/M	Quiescent	V_I = V_{CCI} or 0 V, all channels, no load, EN1 at 3 V, EN2 at 3 V			4.5	7	mA
		25 Mbps				6.5	11	
I_{CC2}	ISO7230C/M	Quiescent	V_I = V_{CCI} or 0 V, all channels, no load, EN at 3 V			15	22	mA
		25 Mbps				17	24	
	ISO7231C/M	Quiescent	V_I = V_{CCI} or 0 V, all channels, no load, EN1 at 3 V, EN2 at 3 V			13	20	mA
		25 Mbps				17.5	27	
ELECTRICAL CHARACTERISTICS								
I_{OFF}	Sleep mode output current		ENx at 0 V, Single channel			0		µA
V_{OH}	High-level output voltage		I_{OH} = –4 mA, See Figure 8	ISO7230	V_{CCO} – 0.4			V
				ISO7231 (5-V side)	V_{CCO} – 0.8			
			I_{OH} = –20 µA, See Figure 8		V_{CCO} – 0.1			
V_{OL}	Low-level output voltage		I_{OL} = 4 mA, See Figure 8				0.4	V
			I_{OL} = 20 µA, See Figure 8				0.1	
$V_{I(HYS)}$	Input voltage hysteresis					150		mV
I_{IH}	High-level input current		INx at V_{CCI}				10	µA
I_{IL}	Low-level input current		INx at 0 V		–10			
C_I	Input capacitance to ground		INx at V_{CCI}, V_I = 0.4 sin (4E6πt)			2		pF
CMTI	Common-mode transient immunity		V_I = V_{CCI} or 0 V, See Figure 11		25	50		kV/µs

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3.3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V.

7.8 Electrical Characteristics: V_{CC1} and V_{CC2} at 3.3 V(1)

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I_{CC1}	ISO7230C/M	Quiescent	V_I = V_{CCI} or 0 V, all channels, no load, EN at 3 V		0.5	1	mA
		25 Mbps			3	5	
	ISO7231C/M	Quiescent	V_I = V_{CCI} or 0 V, all channels, no load, EN1 at 3 V, EN2 at 3 V		4.5	7	mA
		25 Mbps			6.5	11	
I_{CC2}	ISO7230C/M	Quiescent	V_I = V_{CCI} or 0 V, all channels, no load, EN at 3 V		9	15	mA
		25 Mbps			10	17	
	ISO7231C/M	Quiescent	V_I = V_{CCI} or 0 V, all channels, no load, EN1 at 3 V, EN2 at 3 V		8	12	mA
		25 Mbps			10.5	16	
ELECTRICAL CHARACTERISTICS							
I_{OFF}	Sleep mode output current		ENx at 0 V, single channel		0		µA
V_{OH}	High-level output voltage		I_{OH} = –4 mA, See Figure 8	V_{CCO} – 0.4			V
			I_{OH} = –20 µA, See Figure 8	V_{CCO} – 0.1			
V_{OL}	Low-level output voltage		I_{OL} = 4 mA, See Figure 8			0.4	V
			I_{OL} = 20 µA, See Figure 8			0.1	
$V_{I(HYS)}$	Input voltage hysteresis				150		mV
I_{IH}	High-level input current		INx at V_{CCI}			10	µA
I_{IL}	Low-level input current		INx at 0 V	–10			
C_I	Input capacitance to ground		INx at V_{CCI}, V_I = 0.4 sin (4E6πt)		2		pF
CMTI	Common-mode transient immunity		V_I = V_{CCI} or 0 V, See Figure 11	25	50		kV/µs

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3.3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V.

7.9 Power Dissipation Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		ISO7230C, ISO7230M, ISO7231C, ISO7231M	UNIT
		DW (SOIC)	
		16 PINS	
P_D	Device power dissipation, V_{CC1} = V_{CC2} = 5.5 V, TJ = 150°C, C_L = 15 pF, D Input a 50% duty cycle square wave	220	mW

7.10 Switching Characteristics: V_{CC1} and V_{CC2} at 5-V

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay	ISO723xC	See Figure 8	18		42	ns
PWD	Pulse-width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$	ISO723xC	See Figure 8			2.5	ns
t_{PLH}, t_{PHL}	Propagation delay	ISO723xM	See Figure 8	10		23	ns
PWD	Pulse-width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$	ISO723xM	See Figure 8		1	2	ns
$t_{sk(pp)}$	Part-to-part skew (2)	ISO723xC				8	ns
		ISO723xM			0	3	ns
$t_{sk(o)}$	Channel-to-channel output skew (3)	ISO723xC			0	2	ns
		ISO723xM			0	1	ns
t_r	Output signal rise time		See Figure 8		2		ns
t_f	Output signal fall time		See Figure 8		2		ns
t_{PHZ}	Propagation delay, high-level-to-high-impedance output		See Figure 9		15	20	ns
t_{PZH}	Propagation delay, high-impedance-to-high-level output		See Figure 9		15	20	ns
t_{PLZ}	Propagation delay, low-level-to-high-impedance output		See Figure 9		15	20	ns
t_{PZL}	Propagation delay, high-impedance-to-low-level output		See Figure 9		15	20	ns
t_{fs}	Failsafe output delay time from input power loss		See Figure 10		12		µs
$t_{jit(pp)}$	Peak-to-peak eye-pattern jitter	ISO723xM	150 Mbps PRBS NRZ data input, Same polarity inputon all channels, See Figure 12		1		ns

(1) Also referred to as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

7.11 Switching Characteristics: V_{CC1} at 5-V, V_{CC2} at 3.3-V

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay, low-to-high-level output	ISO723xC	See Figure 8	20		50	ns
PWD	Pulse-width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$	ISO723xC	See Figure 8			3	ns
t_{PLH}, t_{PHL}	Propagation delay, low-to-high-level output	ISO723xM	See Figure 8	12		29	ns
PWD	Pulse-width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$	ISO723xM	See Figure 8		1	2	ns
$t_{sk(pp)}$	Part-to-part skew (2)	ISO723xC				10	ns
$t_{sk(pp)}$	Part-to-part skew (2)	ISO723xM			0	5	ns
$t_{sk(o)}$	Channel-to-channel output skew (3)	ISO723xC			0	2.5	ns
$t_{sk(o)}$	Channel-to-channel output skew (3)	ISO723xM			0	1	ns
t_r	Output signal rise time		See Figure 8		2		ns
t_f	Output signal fall time		See Figure 8		2		ns
t_{PHZ}	Propagation delay, high-level-to-high-impedance output		See Figure 9		15	20	ns
t_{PZH}	Propagation delay, high-impedance-to-high-level output		See Figure 9		15	20	ns
t_{PLZ}	Propagation delay, low-level-to-high-impedance output		See Figure 9		15	20	ns
t_{PZL}	Propagation delay, high-impedance-to-low-level output		See Figure 9		15	20	ns
t_{fs}	Failsafe output delay time from input power loss		See Figure 10		18		µs
$t_{jit(pp)}$	Peak-to-peak eye-pattern jitter	ISO723xM	150 Mbps PRBS NRZ data input, Same polarity input on all channels, See Figure 12		1		ns

(1) Also known as pulse skew
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

7.12 Switching Characteristics: V_{CC1} at 3.3-V and V_{CC2} at 5-V

, over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay	ISO723xC	See Figure 8	22		51	ns
PWD	Pulse-width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$	ISO723xC	See Figure 8			3	ns
t_{PLH}, t_{PHL}	Propagation delay	ISO723xM	See Figure 8	12		30	ns
PWD	Pulse-width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$	ISO723xM	See Figure 8		1	2	ns
$t_{sk(pp)}$	Part-to-part skew (2)	ISO723xC				10	ns
		ISO723xM			0	5	ns
$t_{sk(o)}$	Channel-to-channel output skew (3)	ISO723xC			0	2.5	ns
		ISO723xM			0	1	ns
t_r	Output signal rise time		See Figure 8		2		ns
t_f	Output signal fall time		See Figure 8		2		ns
t_{PHZ}	Propagation delay, high-level-to-high-impedance output		See Figure 9		15	20	ns
t_{PZH}	Propagation delay, high-impedance-to-high-level output		See Figure 9		15	20	ns
t_{PLZ}	Propagation delay, low-level-to-high-impedance output		See Figure 9		15	20	ns
t_{PZL}	Propagation delay, high-impedance-to-low-level output		See Figure 9		15	20	ns
t_{fs}	Failsafe output delay time from input power loss		See Figure 10		12		µs
$t_{jit(pp)}$	Peak-to-peak eye-pattern jitter	ISO723xM	150 Mbps PRBS NRZ data input, Same polarity input on all channels, See Figure 12		1		ns

(1) Also known as pulse skew
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

7.13 Switching Characteristics: V_{CC1} and V_{CC2} at 3.3-V

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay	ISO723xC	See Figure 8	25		56	ns
PWD	Pulse-width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$	ISO723xC	See Figure 8			4	ns
t_{pLH}, t_{pHL}	Propagation delay	ISO723xM	See Figure 8	12		34	ns
PWD	Pulse-width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$	ISO723xM	See Figure 8		1	2	ns
$t_{sk(pp)}$	Part-to-part skew (2)	ISO723xC				10	ns
		ISO723xM			0	5	ns
$t_{sk(o)}$	Channel-to-channel output skew (3)	ISO723xC			0	3	ns
		ISO723xM			0	1	ns
t_r	Output signal rise time		See Figure 8		2		ns
t_f	Output signal fall time		See Figure 8		2		ns
t_{PHZ}	Propagation delay, high-level-to-high-impedance output		See Figure 9		15	20	ns
t_{PZH}	Propagation delay, high-impedance-to-high-level output		See Figure 9		15	20	ns
t_{PLZ}	Propagation delay, low-level-to-high-impedance output		See Figure 9		15	20	ns
t_{PZL}	Propagation delay, high-impedance-to-low-level output		See Figure 9		15	20	ns
t_{fs}	Failsafe output delay time from input power loss		See Figure 10		18		µs
$t_{jit(pp)}$	Peak-to-peak eye-pattern jitter	ISO723xM	150 Mbps PRBS NRZ data input, same polarity input on all channels, See Figure 12		1		ns

(1) Also referred to as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

7.14 Typical Characteristics

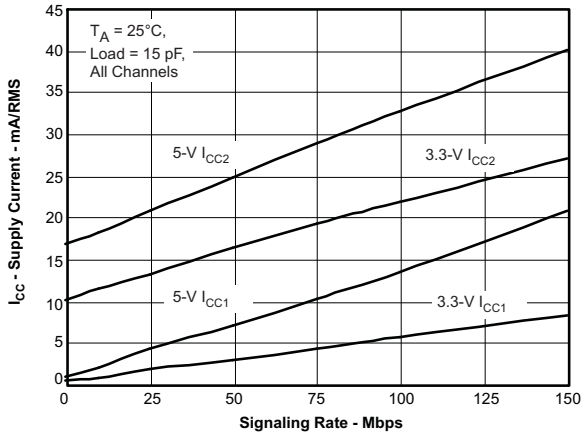


Figure 1. ISO7230C/M RMS Supply Current vs Signaling Rate

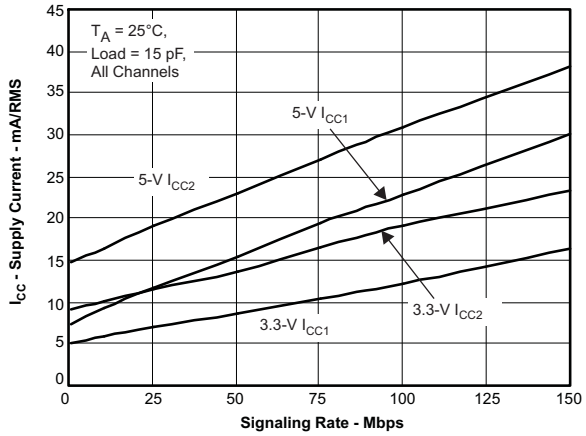


Figure 2. ISO7231C/M RMS Supply Current vs Signaling Rate

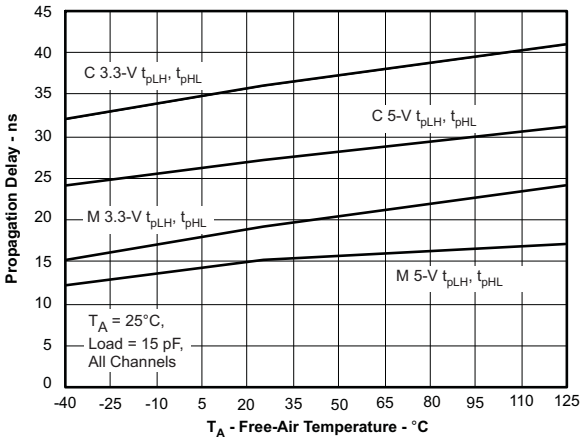


Figure 3. Propagation Delay vs Free-Air Temperature

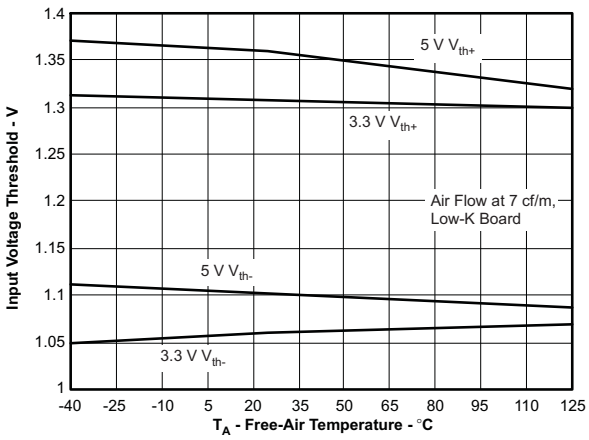


Figure 4. Input Threshold Voltage vs Free-Air Temperature

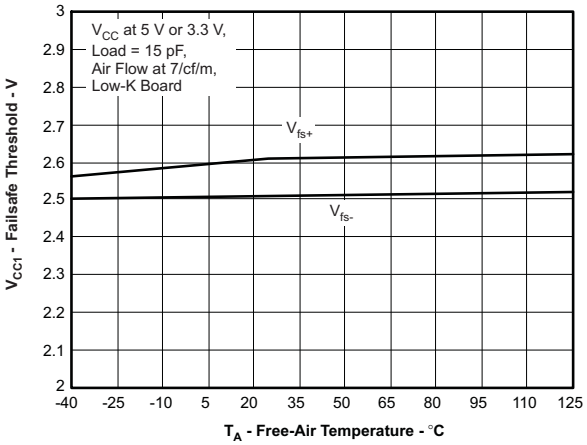


Figure 5. V_{CC1} Fail-Safe Threshold vs Free-Air Temperature

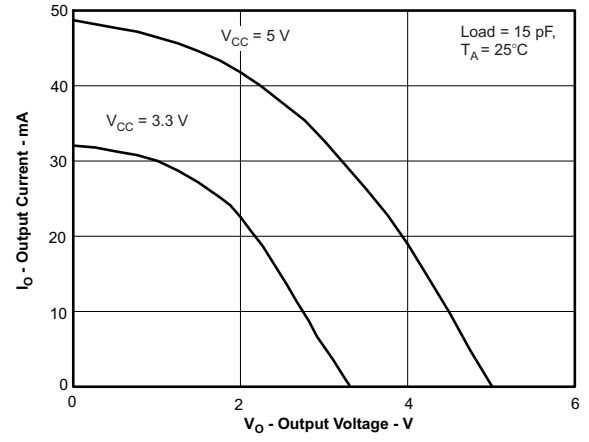


Figure 6. High-Level Output Current vs High-Level Output Voltage

Typical Characteristics (continued)

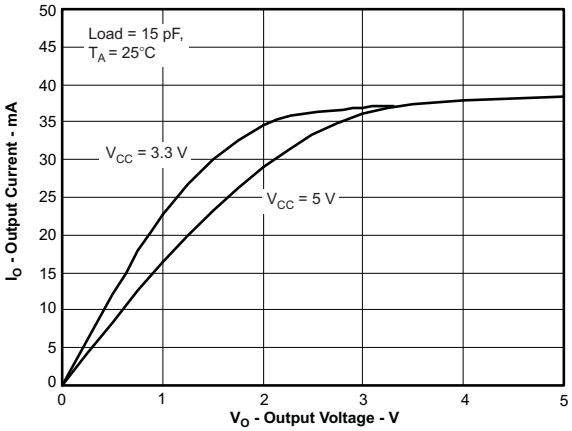
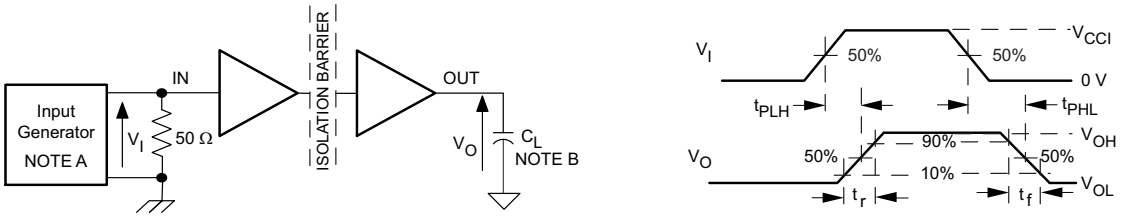


Figure 7. Low-Level Output Current vs Low-Level Output Voltage

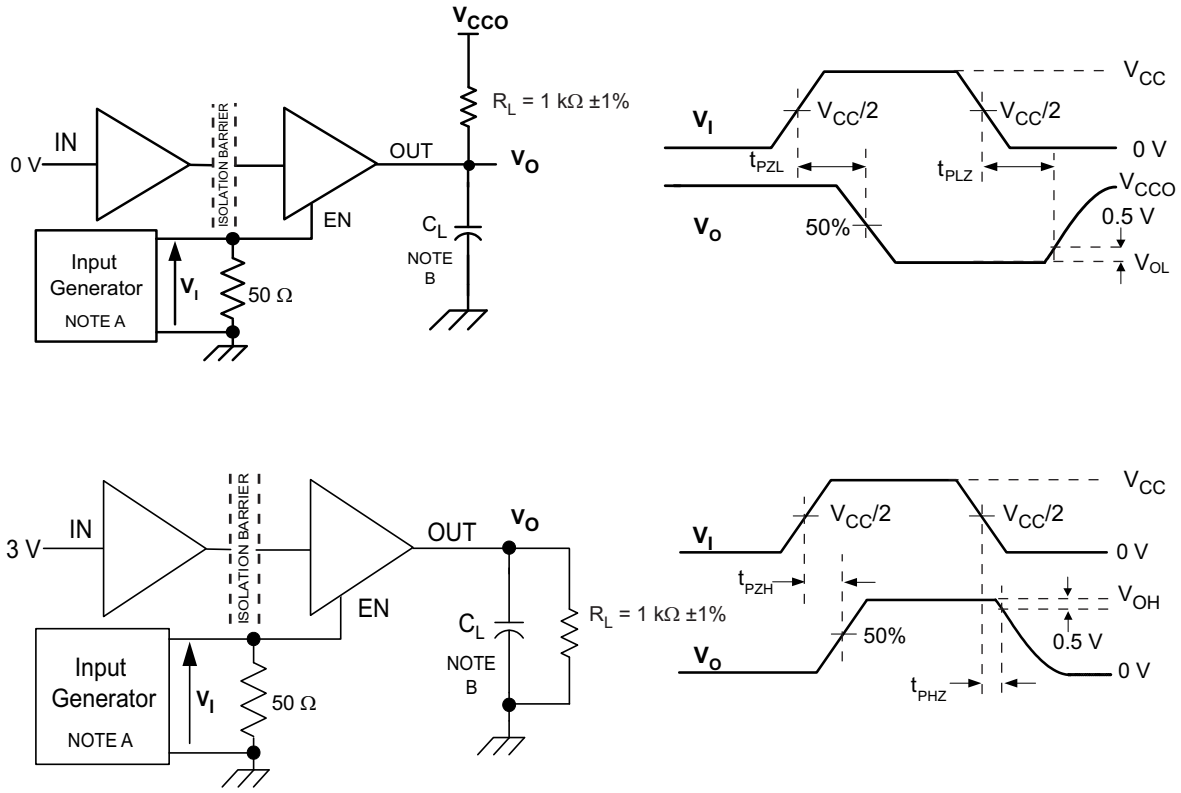
8 Parameter Measurement Information



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, tr ≤ 3 ns, tf ≤ 3 ns, ZO = 50 Ω. At the input, a 50-Ω resistor is required to terminate the Input Generator signal. It is not needed in actual application.

B. CL = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 8. Switching Characteristic Test Circuit and Voltage Waveforms

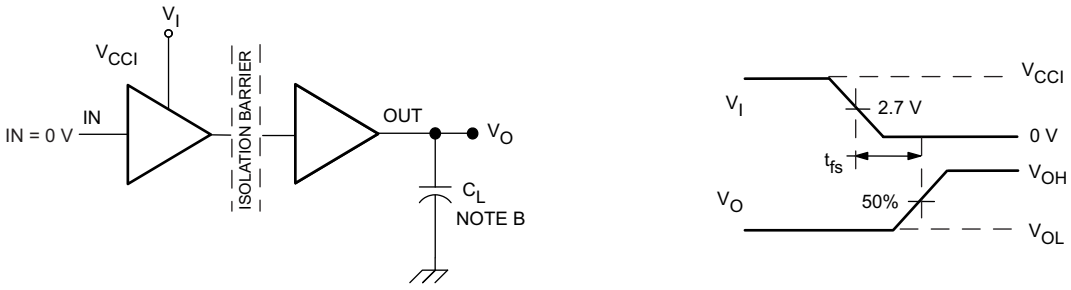


A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50Ω.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 9. Enable/Disable Propagation Delay Time Test Circuit and Waveform

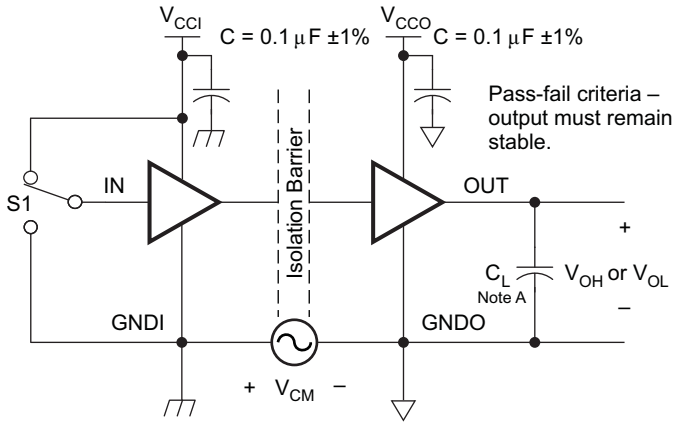
Parameter Measurement Information (continued)



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω.

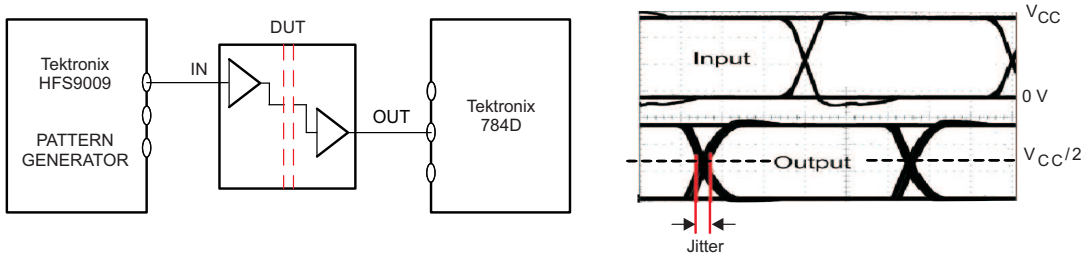
B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 10. Failsafe Delay Time Test Circuit and Voltage Waveforms



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 11. Common-Mode Transient Immunity Test Circuit



NOTE: PRBS bit pattern run length is 2^{16} – 1. Transition time is 800 ps. NRZ data input has no more than five consecutive 1s or 0s.

Figure 12. Peak-to-Peak Eye-Pattern Jitter Test Circuit and Voltage Waveform

9 Detailed Description

9.1 Overview

The isolator in Figure 13 is based on a capacitive isolation barrier technique. The I/O channel of the device consists of two internal data channels, a high-frequency channel (HF) with a bandwidth from 100 kbps up to 150 Mbps, and a low-frequency channel (LF) covering the range from 100 kbps down to DC. In principle, a single-ended input signal entering the HF-channel is split into a differential signal via the inverter gate at the input. The following capacitor-resistor networks differentiate the signal into transients, which then are converted into differential pulses by two comparators. The comparator outputs drive a NOR-gate flip-flop whose output feeds an output multiplexer. A decision logic (DCL) at the driving output of the flip-flop measures the durations between signal transients. If the duration between two consecutive transients exceeds a certain time limit, (as in the case of a low-frequency signal), the DCL forces the output-multiplexer to switch from the high- to the low-frequency channel.

Because low-frequency input signals require the internal capacitors to assume prohibitively large values, these signals are pulse-width modulated (PWM) with the carrier frequency of an internal oscillator, thus creating a sufficiently high frequency signal, capable of passing the capacitive barrier. As the input is modulated, a low-pass filter (LPF) is needed to remove the high-frequency carrier from the actual data before passing it on to the output multiplexer.

9.2 Functional Block Diagram

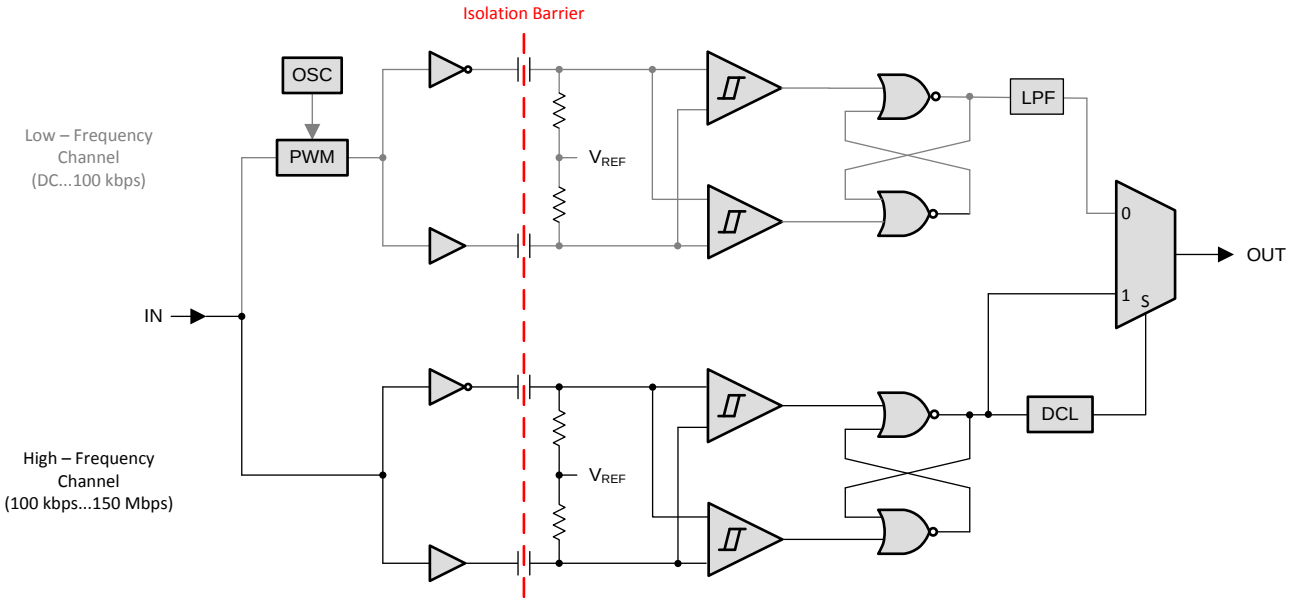


Figure 13. Conceptual Block Diagram of a Digital Capacitive Isolator

9.3 Feature Description

9.3.1 Package Insulation and Safety-Related Specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
L(I01)	Minimum air gap (Clearance)(1)	Shortest terminal-to-terminal distance through air	8			mm
L(I02)	Minimum external tracking (Creepage)(1)	Shortest terminal-to-terminal distance across the package surface	8			mm
CTI	Tracking resistance (comparative tracking index)	DIN EN 60112 (VDE 0303-11); IEC 60112	400			V
DTI	Minimum Internal Gap (Internal Clearance)	Distance through the insulation	0.008			mm
R_{IO}(2)	Isolation resistance	Input to output, V_{IO} = 500 V, T_A = 25°C		>10^{12}		Ω
		Input to output, V_{IO} = 500 V, 100°C ≤ T_A ≤ T_A max		>10^{11}		Ω
C_{IO}(2)	Barrier capacitance Input to output	V_I = 0.4 sin (4E6πt)		2		pF

(1) per JEDEC package dimensions.
(2) All pins on each side of the barrier tied together creating a two-terminal device.

9.3.2 Insulation Characteristics

PARAMETER		TEST CONDITIONS	SPECIFICATION	UNIT
DIN V VDE V 0884-10 (VDE V 0884-10):2006-12(1)				
V_{IORM}	Maximum repetitive peak isolation voltage		560	V_{PK}
V_{PR}	Input to output test voltage	Method b1, V_{PR} = V_{IORM} x 1.875, 100% production test with t = 1 s, Partial discharge < 5 pC	1050	V_{PK}
V_{IOTM}	Maximum transient isolation voltage	V_{TEST} = V_{IOTM}, t = 60 s (qualification), t = 1 s (100% production)	4000	V_{PK}
R_S	Isolation resistance	V_{IO} = 500 V at T_S = 150 °C	>10^9	Ω
	Pollution degree		2	
UL 1577				
V_{ISO}	Withstanding isolation voltage	V_{TEST} = V_{ISO} = 2500 V_{RMS}, t = 60 s (qualification), V_{TEST} = 1.2 x V_{ISO} = 3000 V_{RMS}, t = 1 s (100% production)	2500	V_{RMS}

(1) Climatic classification 40/125/21

Table 1. IEC 60664-1 Ratings Table

PARAMETER	TEST CONDITIONS	SPECIFICATION
Basic isolation group	Material group	II
Installation classification	Rated mains voltage ≤150 V_{RMS}	I-IV
	Rated mains voltage ≤300 V_{RMS}	I-III

9.3.3 Regulatory Information

VDE	CSA	UL
Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 and DIN EN 61010-1 (VDE 0411-1):2011-07	Approved under CSA Component Acceptance Notice 5A and IEC 60950-1	Recognized under UL 1577 Component Recognition Program
Basic insulation; Maximum transient isolation voltage, 4000 V_{PK}; Maximum repetitive peak isolation voltage, 560 V_{PK}	4000 V_{PK} Isolation rating; 384 V_{RMS} Basic insulation working voltage per CSA 60950-1-07+A1 and IEC 60950-1 2nd Ed.+A1	Single protection, 2500 V_{RMS}
File Number: 40016131	Master Contract Number: 220991	File Number: E181974

9.3.4 Safety Limiting Values

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the IO can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	SOIC-16	θ_{JA} = 168°C/W, V_I = 5.5 V, T_J = 170°C, T_A = 25°C			156	mA
			θ_{JA} = 168°C/W, V_I = 3.6 V, T_J = 170°C, T_A = 25°C			239	
T_S	Maximum case temperature	SOIC-16				150	°C

The safety-limiting constraint is the absolute maximum junction temperature specified in the absolute maximum ratings table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the Thermal Characteristics table is that of a device installed in the JESD51-3, Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages and is conservative. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

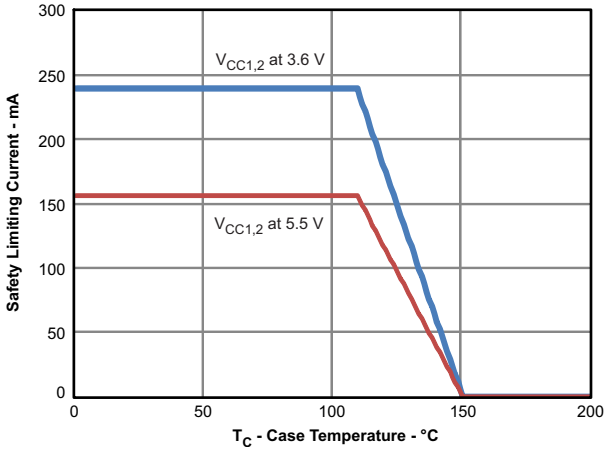


Figure 14. SOIC-16 Θ_{JC} Thermal Derating Curve per VDE

9.4 Device Functional Modes

Table 2. Device Function Table ISO723x (1)

V_{CCI}	V_{CCO}	INPUT (INx)	OUTPUT ENABLE (ENx)	OUTPUT (OUTx)
PU	PU	H	H or Open	H
		L	H or Open	L
		X	L	Z
		Open	H or Open	H
PD	PU	X	H or Open	H
PD	PU	X	L	Z
X	PD	X	X	Undetermined

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}; PU = Powered Up; PD = Powered Down; X = Irrelevant; H = High Level; L = Low Level

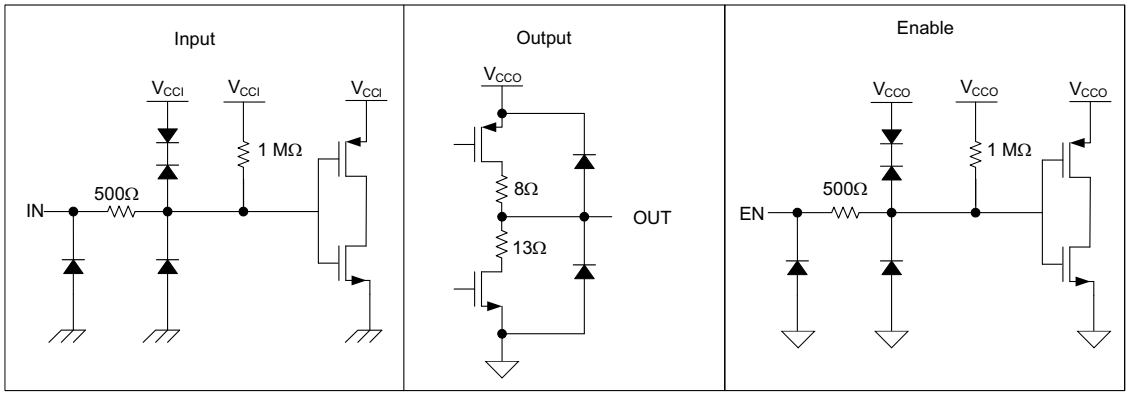


Figure 15. Device I/O Schematics

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

ISO723x utilize single-ended TTL or CMOS-logic switching technologies. The supply voltage range is from 3.15 V to 5.5 V for both supplies, V_{CC1} and V_{CC2}. When designing with digital isolators, it is important to keep in mind that due to the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, µC or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

10.2 Typical Application

ISO7231 combined with Texas Instruments' mixed signal micro-controller, RS-485 transceiver, transformer driver, and voltage regulator can create an isolated RS-485 system as shown in Figure 16.

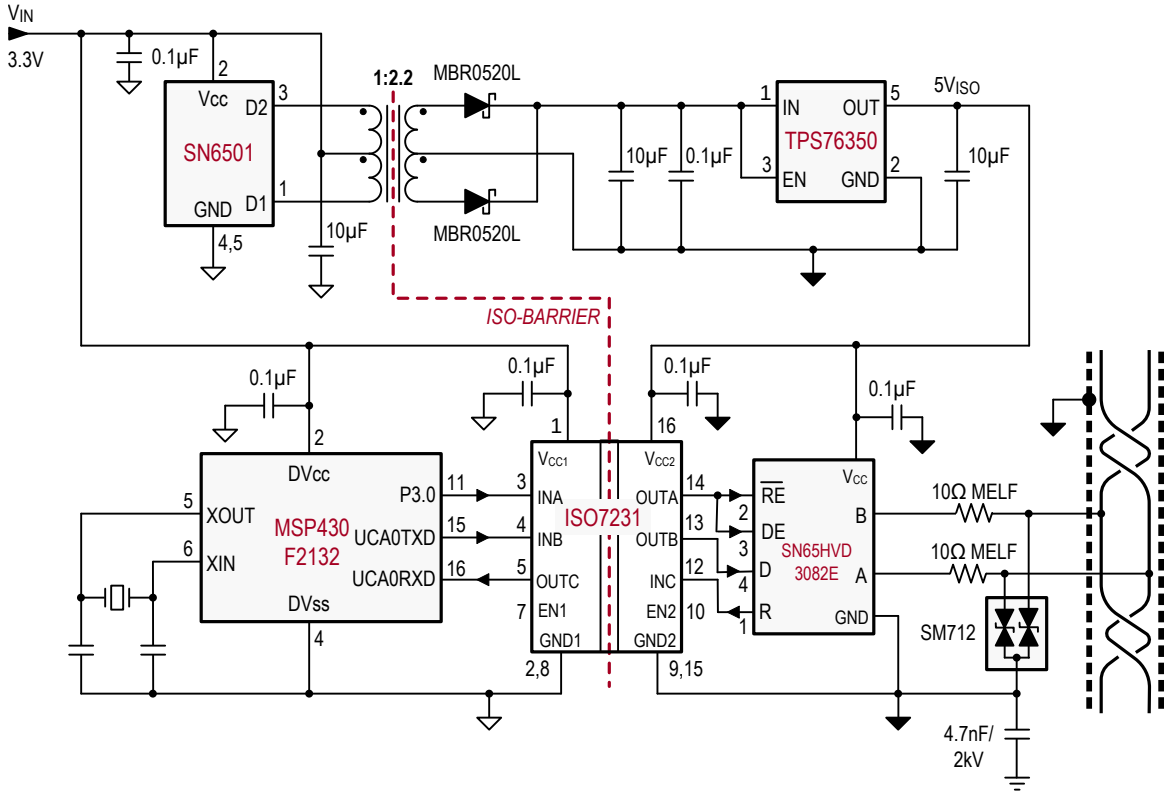


Figure 16. Isolated RS-485 Application Circuit

10.2.1 Design Requirements

Unlike optocouplers, which need external components to improve performance, provide bias, or limit current, ISO723x only needs two external bypass capacitors to operate.

Typical Application (continued)

10.2.2 Detailed Design Procedure

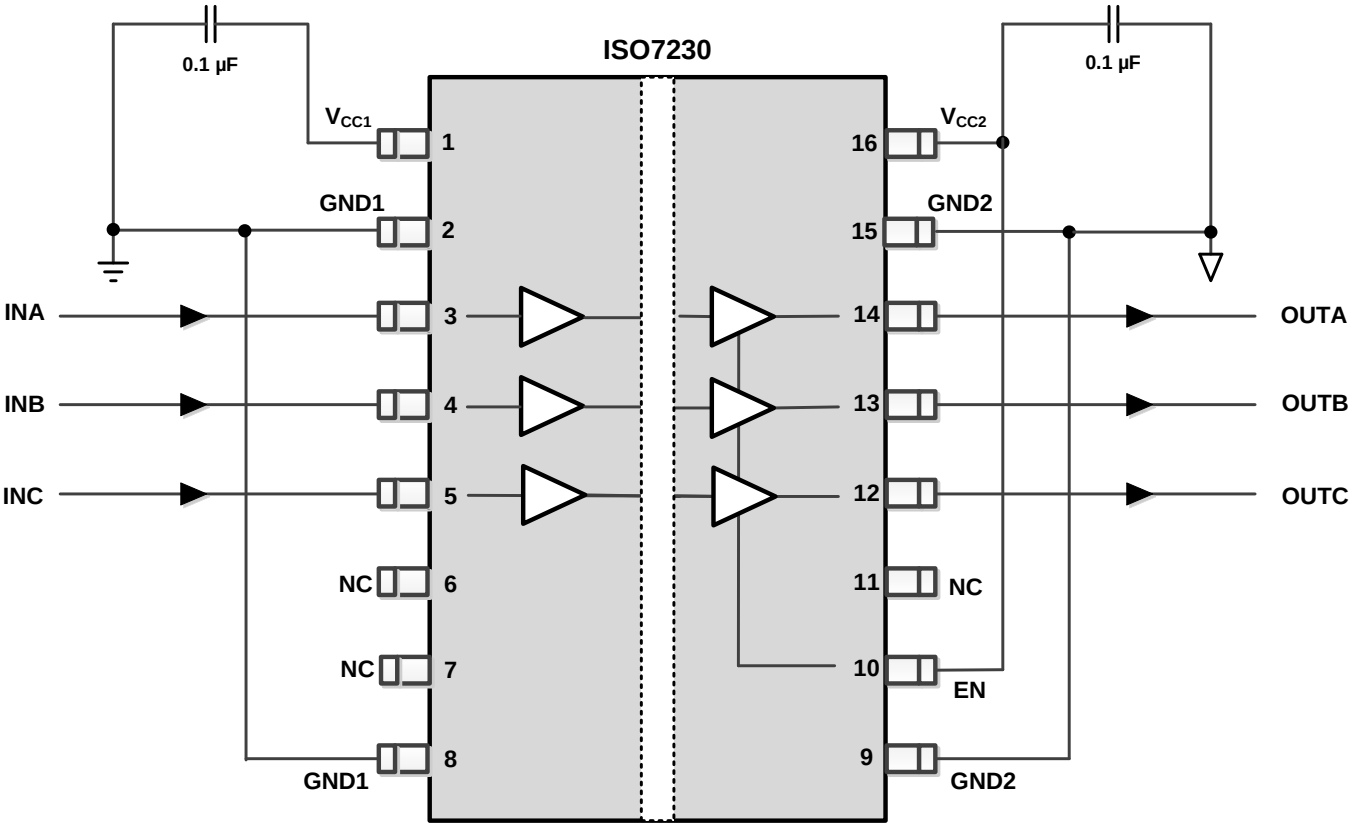


Figure 17. Typical ISO7230 Circuit Hook-up

Typical Application (continued)

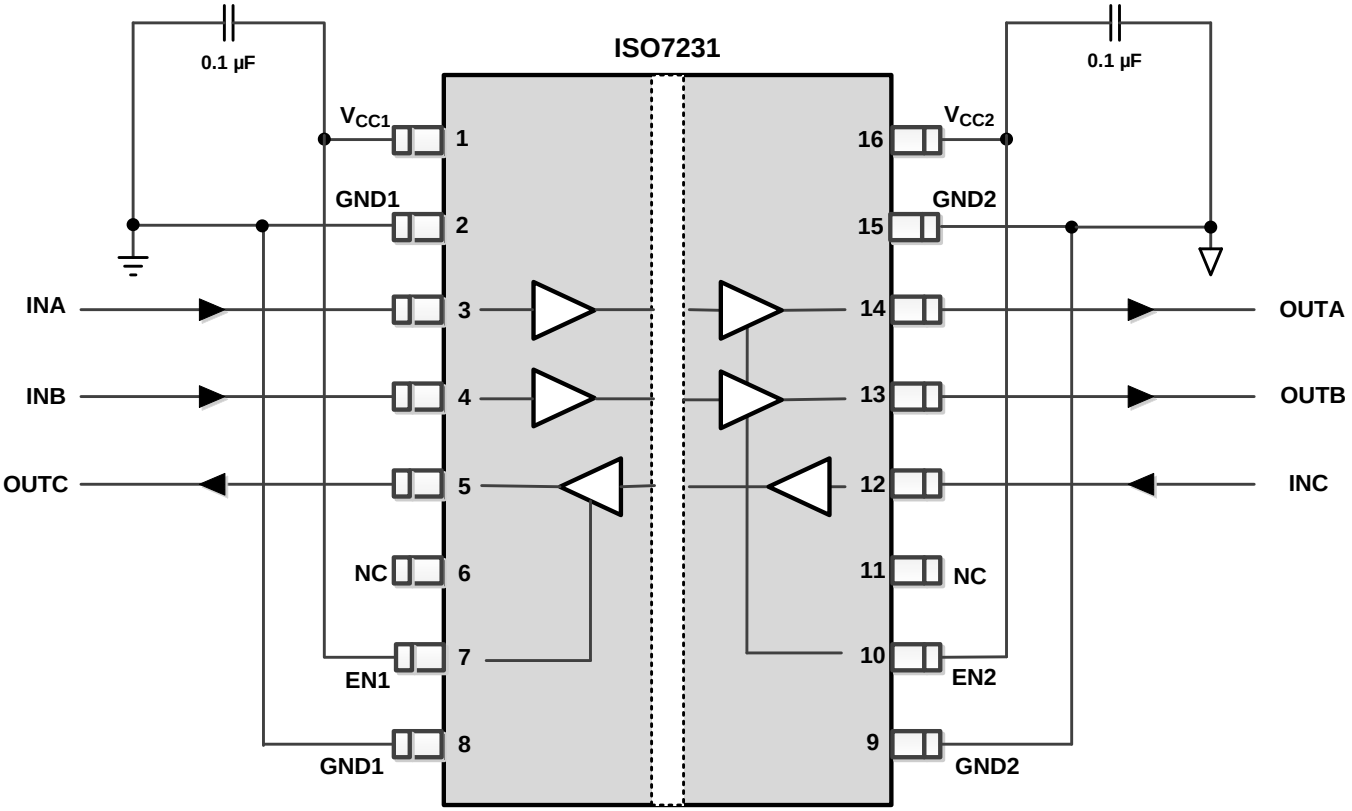


Figure 18. Typical ISO7231 Circuit Hook-up

10.2.3 Application Curve

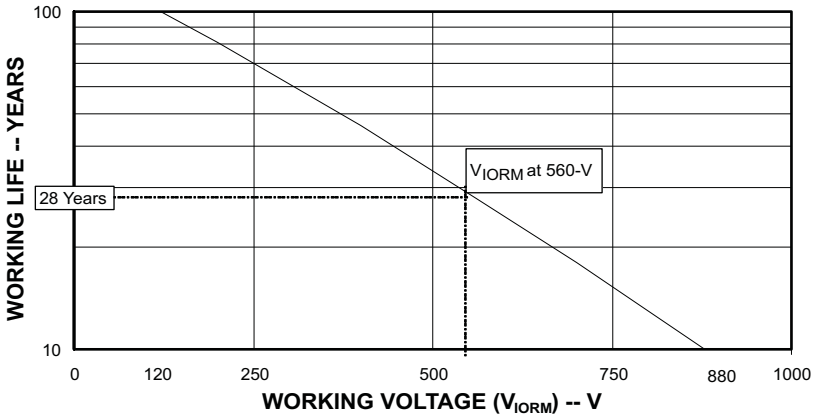


Figure 19. Time Dependant Dielectric Breakdown Testing Results

11 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, a 0.1 µF bypass capacitor is recommended at input and output supply pins (V_{CC1} and V_{CC2}). The capacitors should be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments SN6501 data sheet . For such applications, detailed power supply design and transformer selection recommendations are available in SN6501 data sheet (SLLSEA0).

12 Layout

12.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see Figure 20). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100pF/in^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power/ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly. For detailed layout recommendations, see Application Note SLLA284, *Digital Isolator Design Guide*.

12.1.1 PCB Material

For digital circuit boards operating below 150 Mbps, (or rise and fall times higher than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 epoxy-glass as PCB material. FR-4 (Flame Retardant 4) meets the requirements of Underwriters Laboratories UL94-V0, and is preferred over cheaper alternatives due to its lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and its self-extinguishing flammability-characteristics.

12.2 Layout Example

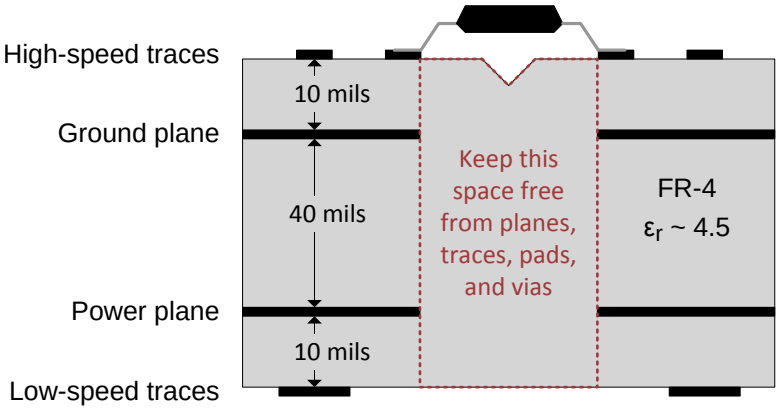


Figure 20. Recommended Layer Stack

13 Device and Documentation Support

13.1 Related Documentation

- *High-Voltage Lifetime of the ISO72x Family of Digital Isolators*, SLLA197
- *ISO72x Digital Isolator Magnetic-Field Immunity*, SLLA181
- *SN6501 Transformer Driver for Isolated Power Supplies*, SLLSEA0
- *Digital Isolator Design Guide*, SLLA284
- *Isolation Glossary*, SLLA353

13.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 3. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
ISO7230C	Click here	Click here	Click here	Click here	Click here
ISO7230M	Click here	Click here	Click here	Click here	Click here
ISO7231C	Click here	Click here	Click here	Click here	Click here
ISO7231M	Click here	Click here	Click here	Click here	Click here

13.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

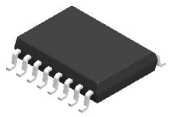
13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

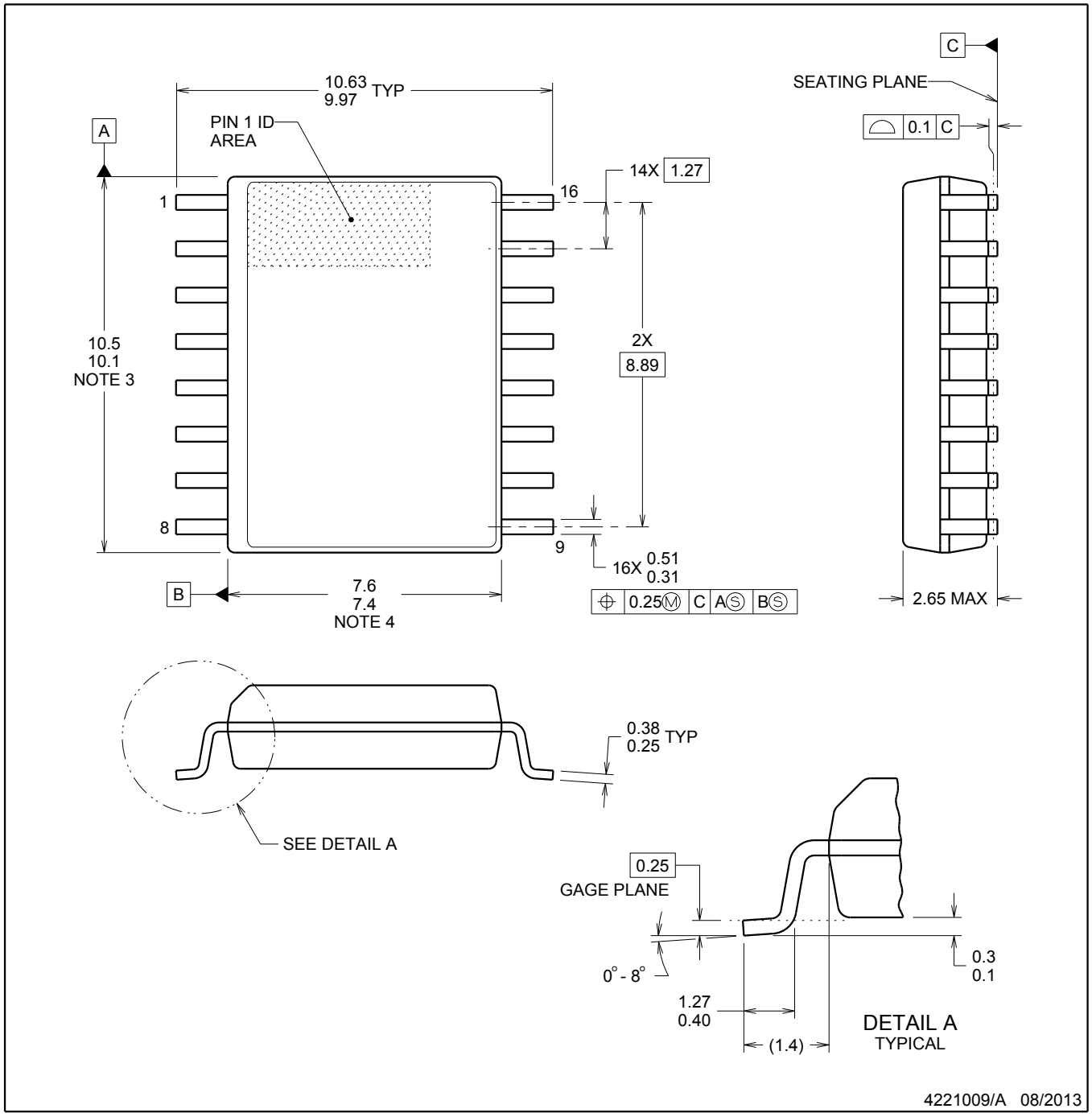
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



DW0016B

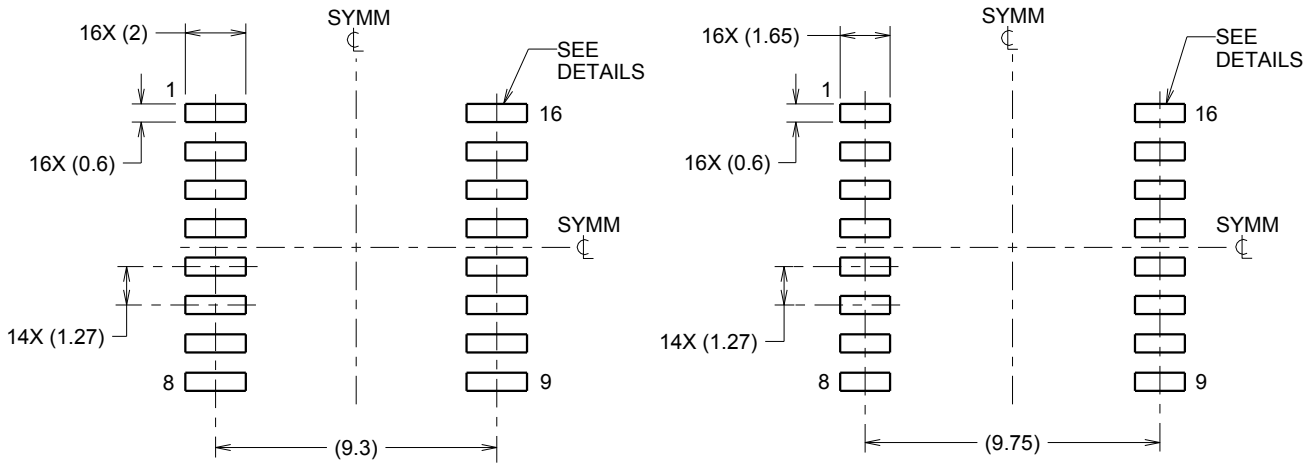
SOIC - 2.65 mm max height

SOIC



NOTES:

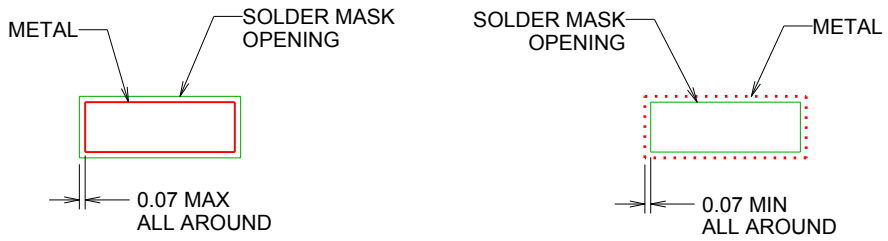
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MO-013, variation AA.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

LAND PATTERN EXAMPLE
SCALE:4X



NON SOLDER MASK DEFINED

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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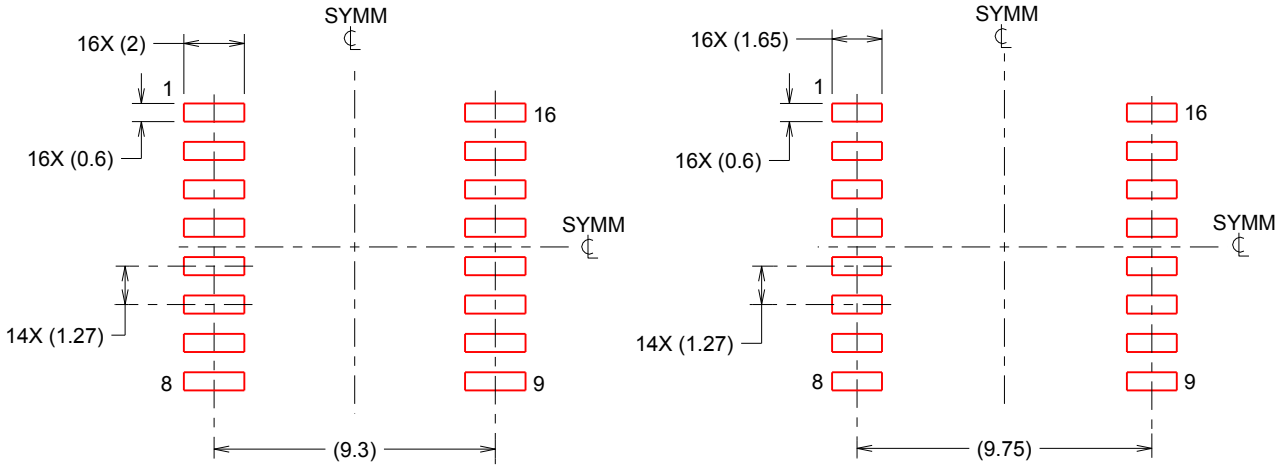
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

DW0016B

SOIC - 2.65 mm max height

SOIC



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO7230CDW	LIFEBUY	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7230C	
ISO7230CDWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7230C	Samples
ISO7230MDW	LIFEBUY	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7230M	
ISO7230MDWR	LIFEBUY	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7230M	
ISO7231CDW	LIFEBUY	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7231C	
ISO7231CDWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7231C	Samples
ISO7231CDWRG4	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7231C	Samples
ISO7231MDW	LIFEBUY	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7231M	
ISO7231MDWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7231M	Samples
ISO7231MDWRG4	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7231M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF ISO7231C :

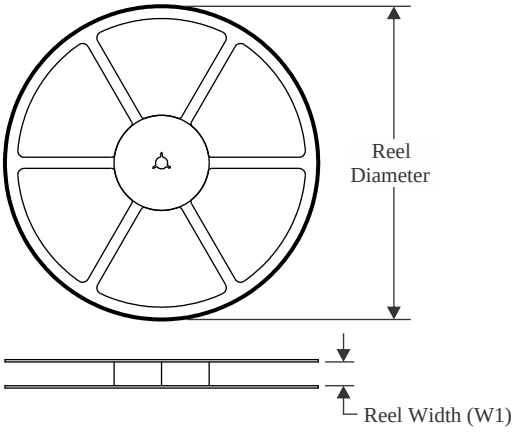
- Automotive : ISO7231C-Q1

NOTE: Qualified Version Definitions:

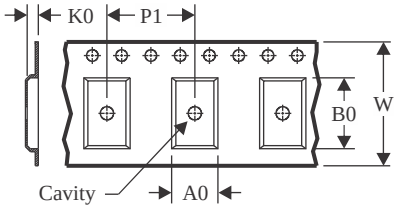
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

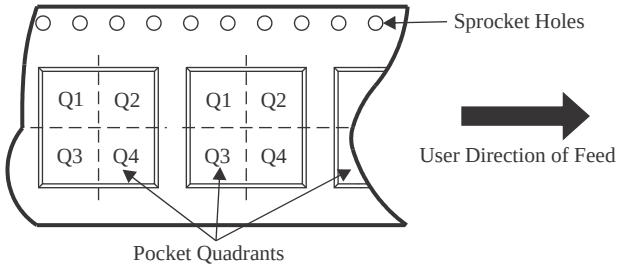


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

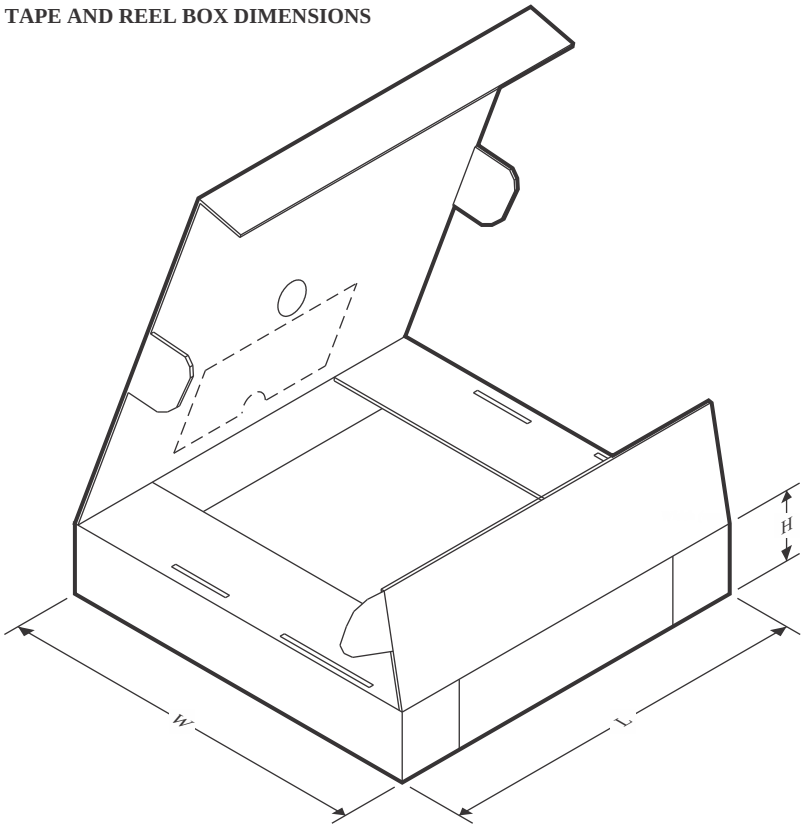
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7230CDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7230MDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7231CDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7231MDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

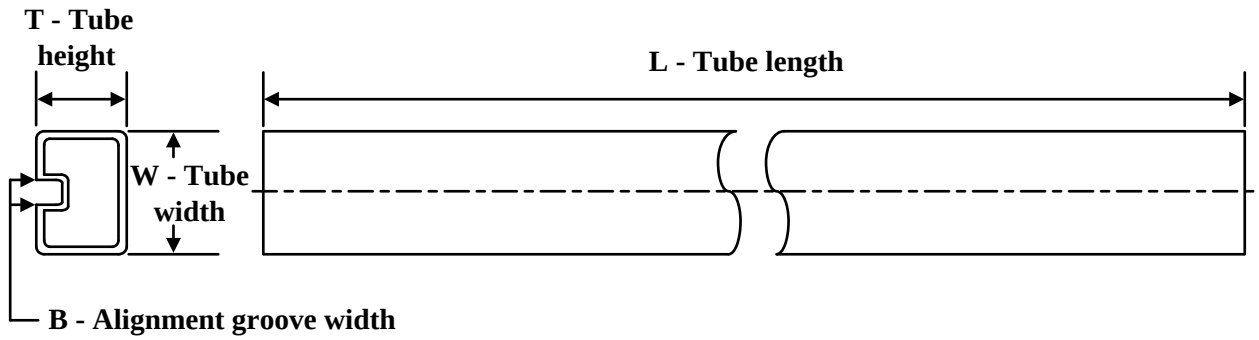
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7230CDWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7230MDWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7231CDWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7231MDWR	SOIC	DW	16	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ISO7230CDW	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO7230MDW	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO7231CDW	DW	SOIC	16	40	506.98	12.7	4826	6.6
ISO7231MDW	DW	SOIC	16	40	506.98	12.7	4826	6.6

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