TEXAS INSTRUMENTS
TPD1E01B04-Q1
SLVSG26A – MAY 2021 – REVISED DECEMBER 2021

TPD1E01B04-Q1 Automotive 0.2-pF, ±3.6-V, ±15-kV ESD Protection Diode in 0402 Package

1 Features

- IEC 61000-4-2 level 4 ESD protection
  - ±15-kV contact discharge
  - ±17-kV air gap discharge
- IEC 61000-4-4 EFT protection
  - 80 A (5/50 ns)
- IEC 61000-4-5 surge protection
  - 2.5 A (8/20 µs)
- IO capacitance:
  - 0.20 pF (typical)
  - 0.23 pF (maximum)
- DC breakdown voltage: 6.4 V (typical)
- Ultra low leakage current: 10-nA (maximum)
- Low ESD clamping voltage: 15 V at 16 A TLP
- Low insertion loss: 20 GHz
- Supports high speed interfaces up to 20 Gbps
- Industry standard 0402 footprint
- AEC-Q101 qualified
  - Device HBM classification level H2
  - Device CDM classification level C5
  - Device operating temperature range: –40°C to +125°C

2 Applications

- End equipment
  - Surround view systems
  - ADAS vision systems
  - Rear view camera
  - Infotainment and cluster
  - Body control module
  - Head units
- Interfaces
  - Automotive SerDes: FPD-Link
  - USB Type-C
  - USB 3.1 Gen 2/3.0/2.0
  - HDMI 2.0/1.4
  - 10/100/1000 Mbps ethernet

3 Description

The TPD1E01B04-Q1 is a bidirectional TVS ESD protection diode for USB Type-C and FPD-Link circuit protection. The TPD1E01B04-Q1 is rated to dissipate ESD strikes at the maximum level specified in the IEC 61000-4-2 international standard (Level 4).

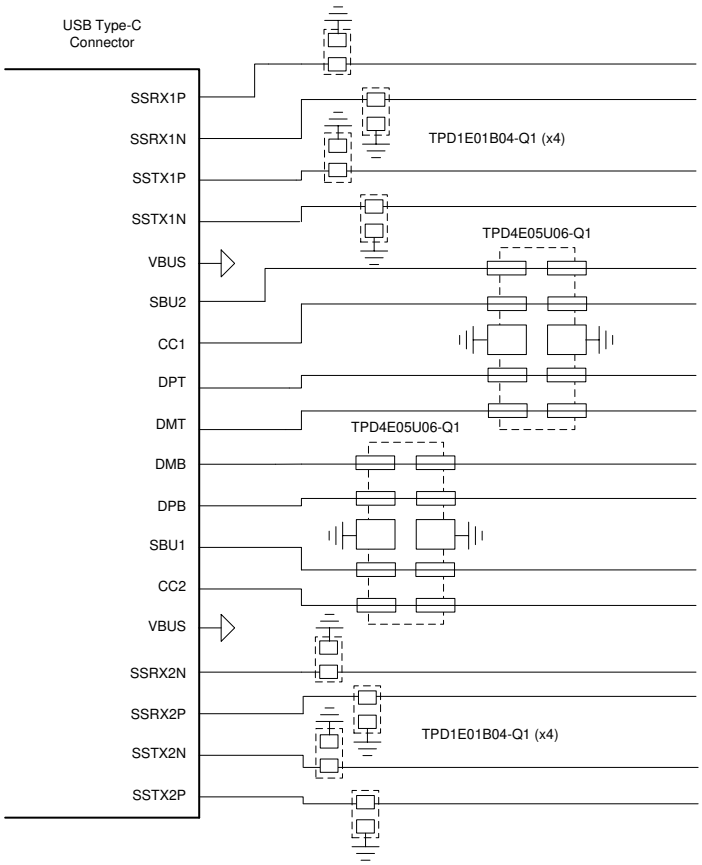
This device features a 0.20-pF (typical) IO capacitance making it ideal for protecting high-speed interfaces up to 20 Gbps such as USB 3.1 Gen2 and FPD-Link. The low dynamic resistance and low clamping voltage ensure system level protection against transient events.

The TPD1E01B04-Q1 is offered in the industry standard 0402 (DPY) package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPD1E01B04-Q1	X1SON (2)	1.00 mm x 0.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Typical Application

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (May 2021) to Revision A (December 2021)	Page
• Changed the status of the data sheet from: *Advanced Information* to: *Production Data*	1

5 Pin Configuration and Functions

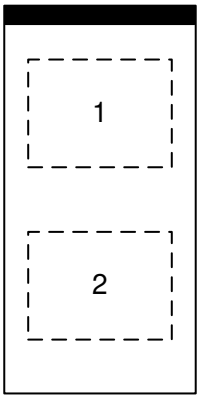


Figure 5-1. DPY Package 2-Pin X1SON Top View

Table 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	IO	I/O	ESD Protected Channel. If used as ESD IO, connect pin 2 to ground
2	IO	I/O	ESD Protected Channel. If used as ESD IO, connect pin 1 to ground

(1) I = input, O = output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Electrical fast transient	IEC 61000-4-5 (5/50 ns) at 25°C		80	A
Peak pulse	IEC 61000-4-5 power (t_p - 8/20 µs) at 25°C		27	W
	IEC 61000-4-5 current (t_p - 8/20 µs) at 25°C		2.5	A
T_A	Operating free-air temperature	–40	125	°C
T_{stg}	Storage temperature	–65	155	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings—AEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q101-001	±2500	V
		Charged device model (CDM), per AEC Q101-005	±1000	

6.3 ESD Ratings—IEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 Contact Discharge, all pins	±15000	V
		IEC 61000-4-2 Air-gap Discharge, all pins	±17000	

6.4 ESD Ratings—ISO Specification

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	ISO 10605, 330-pF, 330-Ω, IO	Contact discharge	± 12500	V
			Air-gap discharge	±15000	

6.5 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IO}	Input pin voltage	–3.6		3.6	V
T_A	Operating free-air temperature	–40		125	°C

6.6 Thermal Information

THERMAL METRIC(1)		TPD1E01B04-Q1 DPY (X1SON) 2 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	442.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	243.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	162.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	154.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	163.0	°C/W

6.6 Thermal Information (continued)

THERMAL METRIC[1]		TPD1E01B04-Q1 DPY (X1SON) 2 PINS	UNIT
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.7 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	I_{IO} < 10 nA	–3.6		3.6	V
V_{BRF}	Breakdown voltage, IO pin to GND	Measured as the maximum voltage before device snaps back into V_{HOLD} voltage		6.4		V
V_{BRR}	Breakdown voltage, GND to IO pin			–6.4		V
V_{HOLD}	Holding voltage	I_{IO} = 1 mA, T_A = 25°C	5	5.9	6.5	V
V_{CLAMP}	Clamping voltage	I_{PP} = 1 A, TLP, from IO to GND		7		V
		I_{PP} = 5 A, TLP, from IO to GND		9.2		
		I_{PP} = 16 A, TLP, from IO to GND		15		
		I_{PP} = 1 A, TLP, from GND to IO		7		
		I_{PP} = 5 A, TLP, from GND to IO		9.2		
		I_{PP} = 16 A, TLP, from GND to IO		15		
I_{LEAK}	Leakage current, IO to GND	V_{IO} = ±2.5 V			10	nA
R_{DYN}	Dynamic resistance	IO to GND		0.57		Ω
		GND to IO		0.57		
C_L	Line capacitance	V_{IO} = 0 V, f = 1 MHz, IO to GND, T_A = 25°C		0.2	0.23	pF

6.8 Typical Characteristics

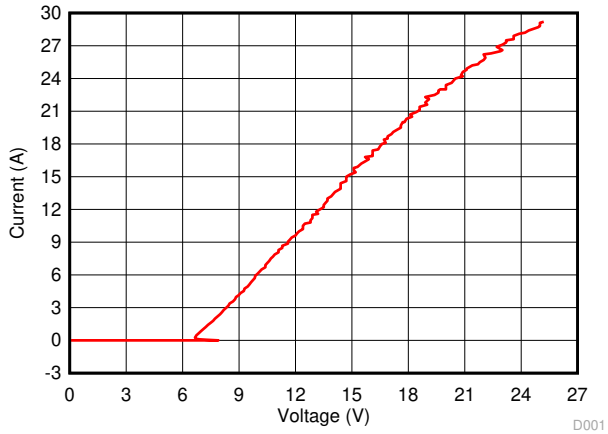


Figure 6-1. Positive TLP Curve

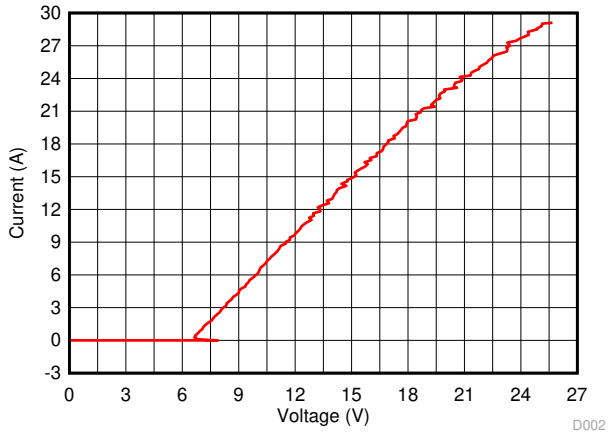


Figure 6-2. Negative TLP Curve

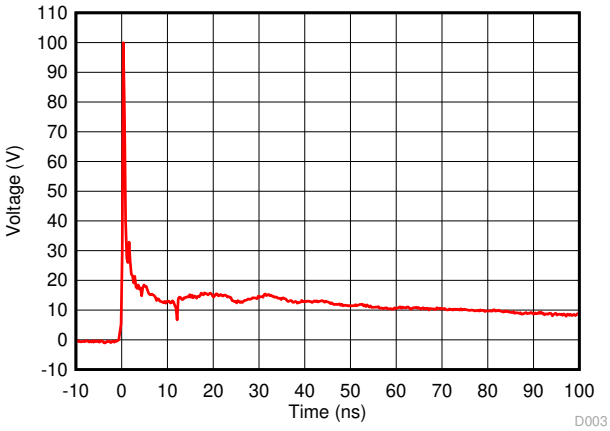


Figure 6-3. 8-kV IEC Waveform

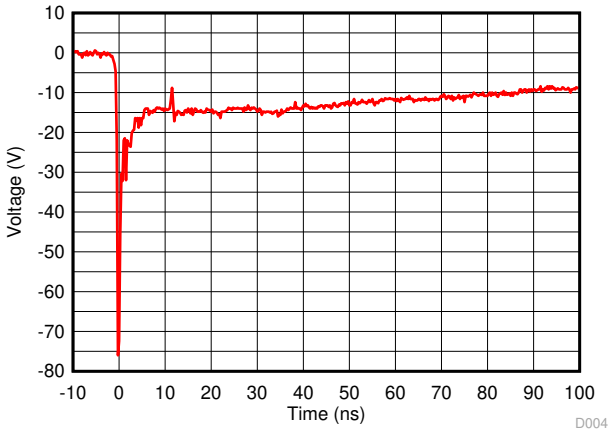


Figure 6-4. –8-kV IEC Waveform

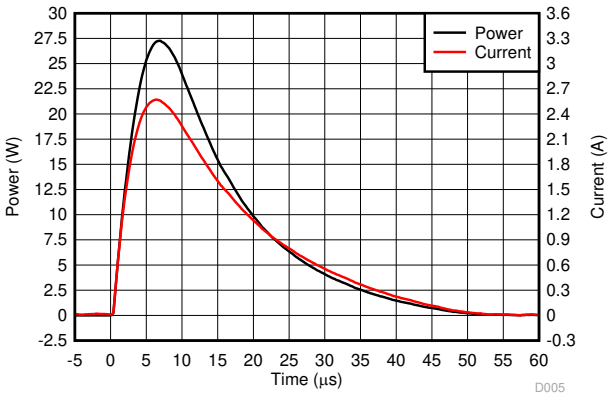


Figure 6-5. Surge Curve (t_p = 8/20µs), IO pin to GND

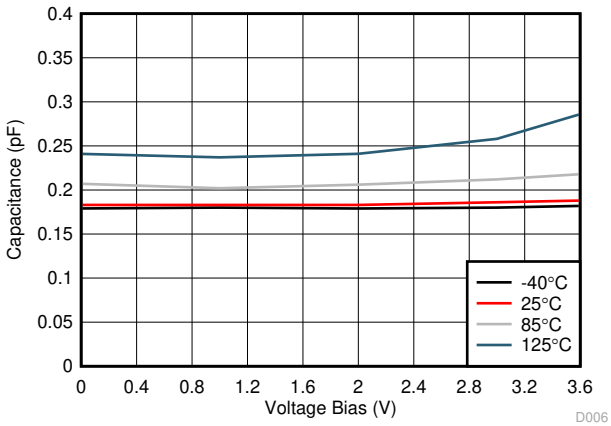


Figure 6-6. Capacitance vs. Bias Voltage

6.8 Typical Characteristics (continued)

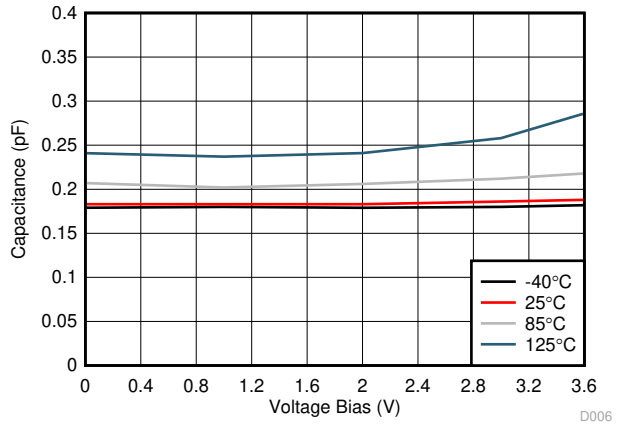


Figure 6-7. Capacitance vs. Bias Voltage (DPY Package)

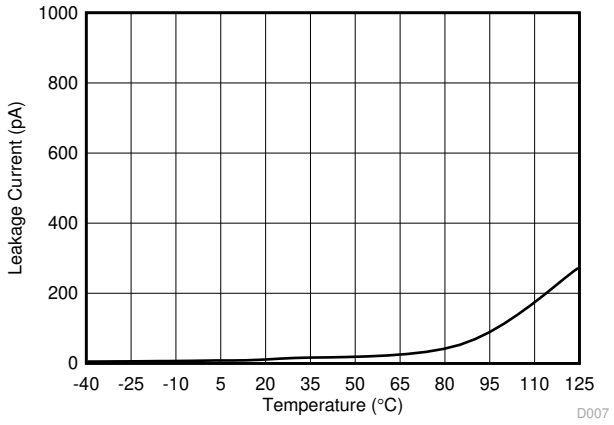


Figure 6-8. Leakage Current vs. Temperature

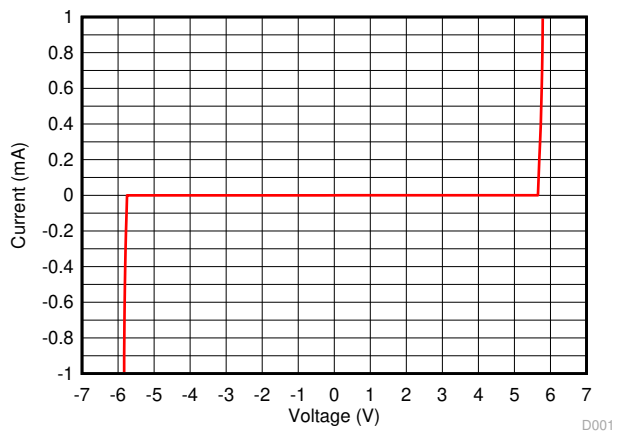


Figure 6-9. DC Voltage Sweep I-V Curve

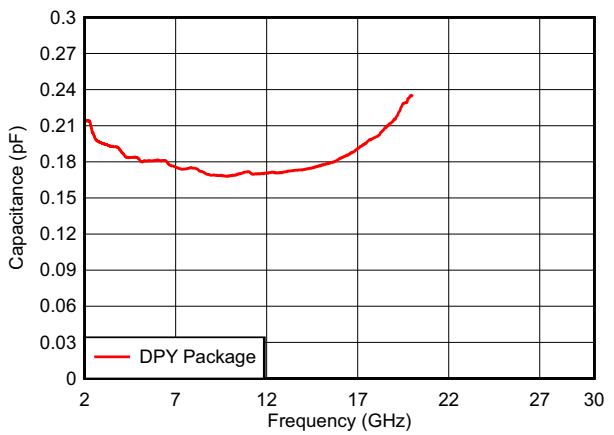


Figure 6-10. Capacitance vs. Frequency

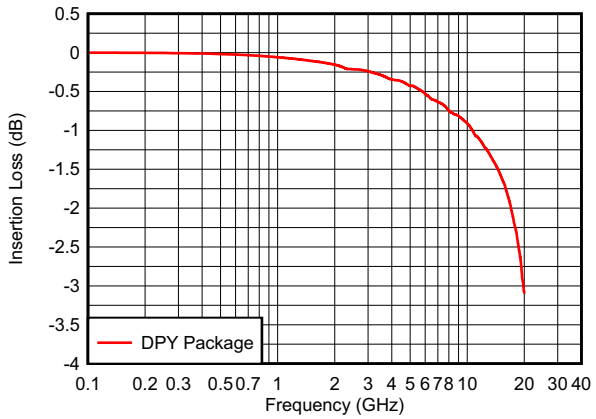


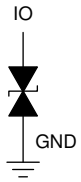
Figure 6-11. Insertion Loss

7 Detailed Description

7.1 Overview

The TPD1E01B04-Q1 device is a bidirectional ESD Protection Diode with ultra-low capacitance. This device can dissipate ESD strikes above the maximum level specified by the IEC 61000-4-2 International Standard. The ultra-low capacitance makes this device ideal for protecting any super high-speed signal pins including Thunderbolt 3. The low capacitance allows for extremely low losses even at RF frequencies such as USB 3.1 Gen 2, Thunderbolt 3, or antenna applications.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 IEC 61000-4-2 ESD Protection

The I/O pins can withstand ESD events up to ±15-kV contact and ±17-kV air gap. An ESD-surge clamp diverts the current to ground.

7.3.2 IEC 61000-4-4 EFT Protection

The I/O pins can withstand an electrical fast transient burst of up to 80 A (5/50 ns waveform, 4 kV with 50-Ω impedance). An ESD-surge clamp diverts the current to ground.

7.3.3 IEC 61000-4-5 Surge Protection

The I/O pins can withstand surge events up to 2.5 A and 27 W (8/20 µs waveform). An ESD-surge clamp diverts this current to ground.

7.3.4 IO Capacitance

The capacitance between each I/O pin to ground is 0.2 pF (typical) and 0.23 pF (maximum). This device supports data rates up to 20 Gbps.

7.3.5 DC Breakdown Voltage

The DC breakdown voltage of each I/O pin is ±6.4 V (typical). This ensures that sensitive equipment is protected from surges above the reverse standoff voltage of ±3.6 V.

7.3.6 Ultra Low Leakage Current

The I/O pins feature an ultra-low leakage current of 10 nA (maximum) at a bias voltage of ±2.5 V.

7.3.7 Low ESD Clamping Voltage

The I/O pins feature an ESD clamp that is capable of clamping the voltage to 9.2 V (I_{PP} = 5 A).

7.3.8 Supports High Speed Interfaces

This device is capable of supporting high speed interfaces up to 20 Gbps, because of the extremely low IO capacitance.

7.3.9 Industrial Temperature Range

This device features an industrial operating range of –40°C to +125°C.

7.3.10 Easy Flow-Through Routing Package

The layout of this device makes it simple and easy to add protection to an existing layout. The packages offers flow-through routing, requiring minimal modification to an existing layout.

7.4 Device Functional Modes

The TPD1E01B04-Q1 device is a passive integrated circuit that triggers when voltages are above V_{BRF} or below V_{BRR}. During ESD events, voltages as high as ±17 kV (air) can be directed to ground through the internal diode network. When the voltages on the protected line fall below the trigger levels of TPD1E01B04-Q1 (usually within 10s of nano-seconds) the device reverts to passive.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPD1E01B04-Q1 is a diode type TVS which is used to provide a path to ground for dissipating ESD events on high-speed signal lines between a human interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP}, to a safe level for the protected IC.

8.2 Typical Application

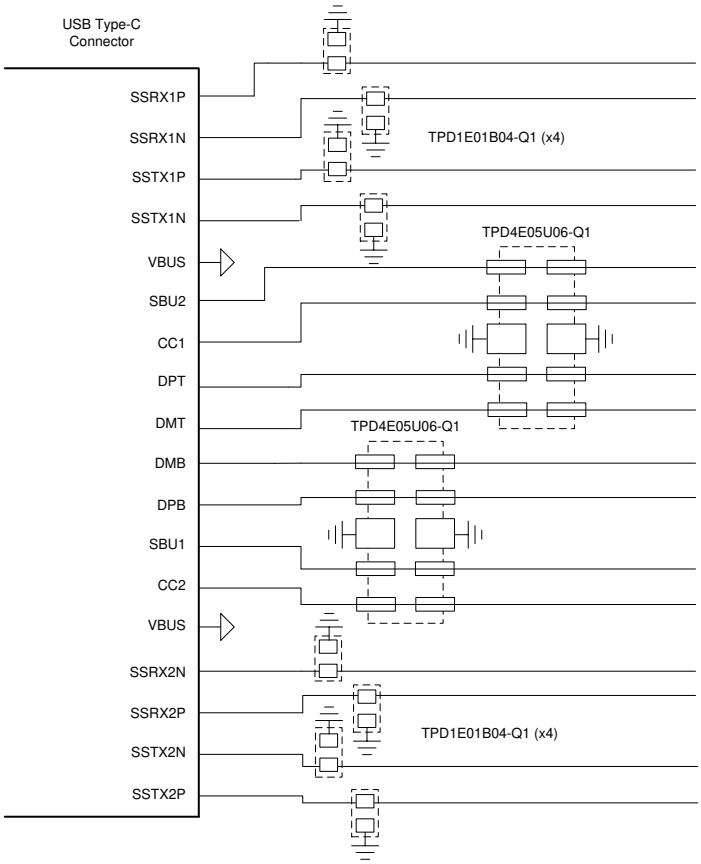


Figure 8-1. USB Type-C for Thunderbolt 3 ESD Schematic

8.2.1 Design Requirements

For this design example eight TPD1E01B04-Q1 devices and two TPD4E05U06-Q1 devices are being used in a USB Type-C for Thunderbolt 3 application. This provides a complete ESD protection scheme.

Given the Thunderbolt 3 application, the parameters listed in Table 8-1 are known.

Table 8-1. Design Parameters

DESIGN PARAMETER	VALUE
Signal range on superspeed Lines	0 V to 3.6 V
Operating frequency on superspeed Lines	up to 10 GHz
Signal range on CC, SBU, and DP/DM Lines	0 V to 5 V
Operating frequency on CC, SBU, and DP/DM Lines	up to 480 MHz

8.2.2 Detailed Design Procedure

8.2.2.1 Signal Range

The TPD1E01B04-Q1 supports signal ranges between –3.6 V and 3.6 V, which supports the SuperSpeed pairs on the USB Type-C application. The TPD4E05U06-Q1 supports signal ranges between 0 V and 5.5 V, which supports the CC, SBU, and DP-DM lines.

8.2.2.2 Operating Frequency

The TPD1E01B04-Q1 has a 0.2 pF (typical) capacitance, which supports the Thunderbolt 3 data rates of 20 Gbps. The TPD4E05U06-Q1 has a 0.5-pF (typical) capacitance, which easily supports the CC, SBU, and DP-DM data rates.

8.2.3 Application Curves

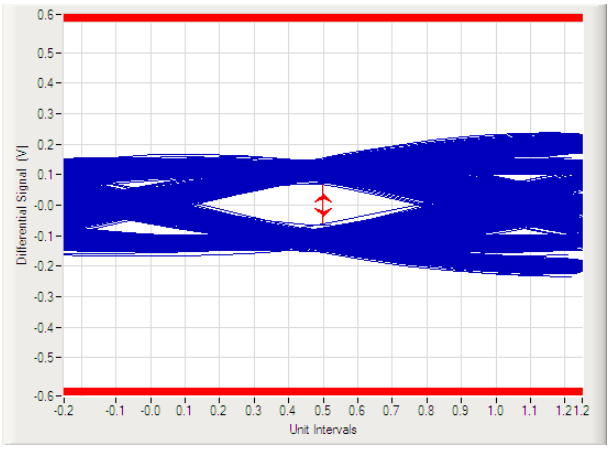


Figure 8-2. USB 3.1 Gen 2 10-Gbps Eye Diagram (Bare Board)

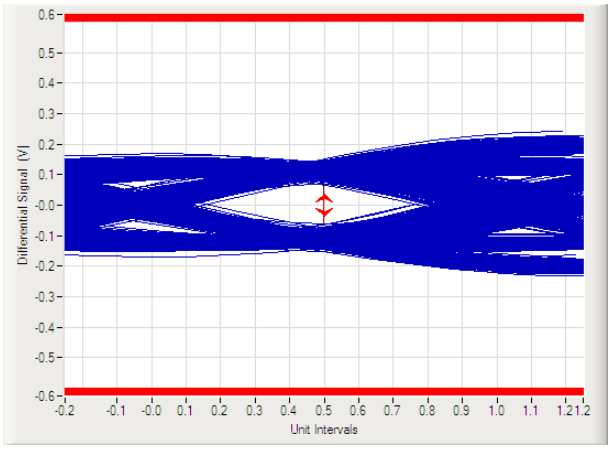


Figure 8-3. USB 3.1 Gen 2 10-Gbps Eye Diagram (with TPD1E01B04-Q1)

9 Power Supply Recommendations

This device is a passive ESD device so there is no need to power it. Take care not to violate the recommended I/O specification to ensure the device functions properly.

10 Layout

10.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

10.2 Layout Example

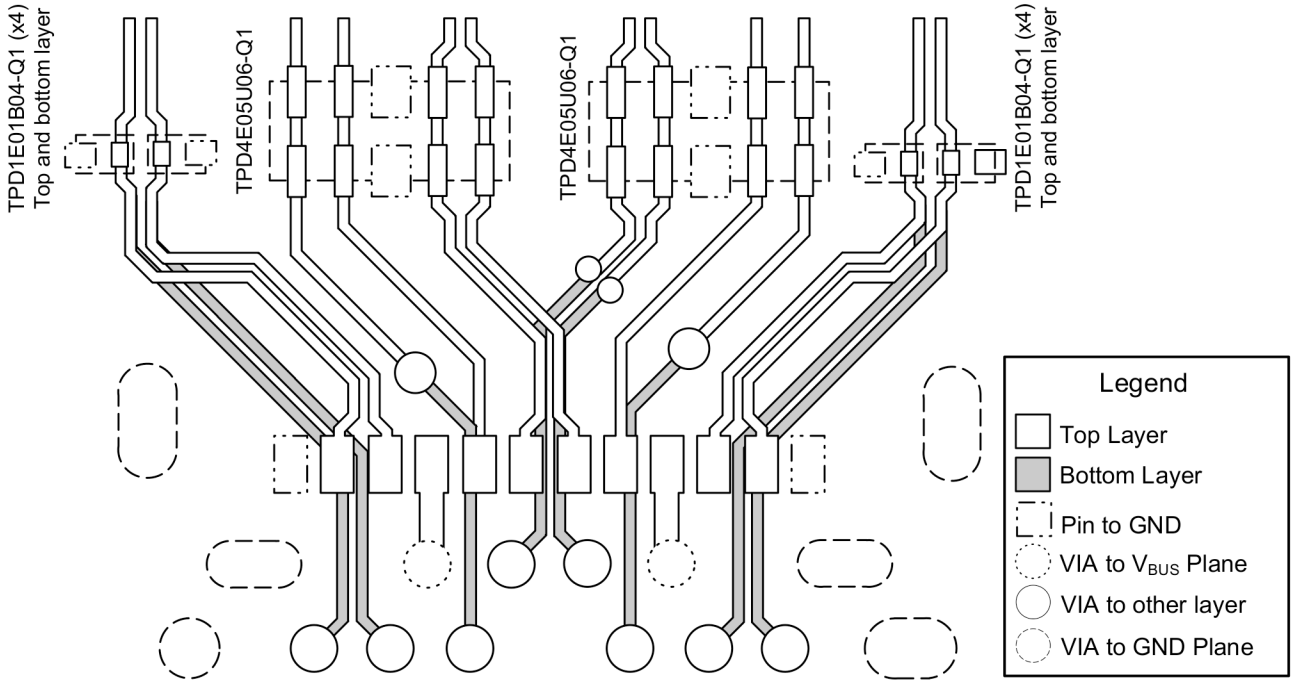


Figure 10-1. USB Type-C Mid-Mount, Hybrid Connector ESD Layout

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Generic ESD Evaluation Module* user's guide

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

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All trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD1E01B04DPYRQ1	ACTIVE	X1SON	DPY	2	10000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	LR	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPD1E01B04-Q1 :

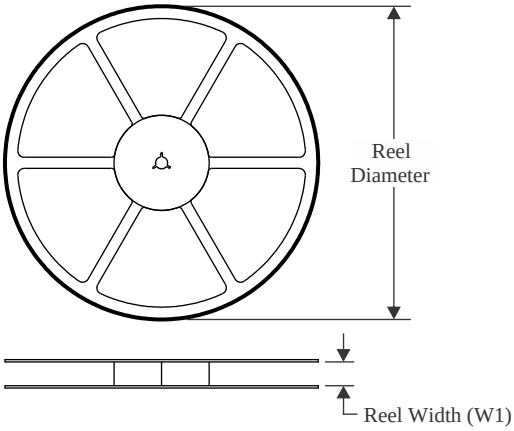
- Catalog : TPD1E01B04

NOTE: Qualified Version Definitions:

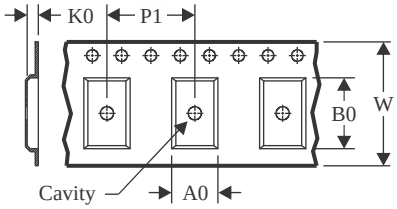
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

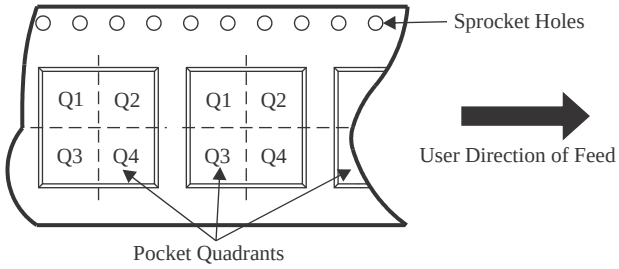


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

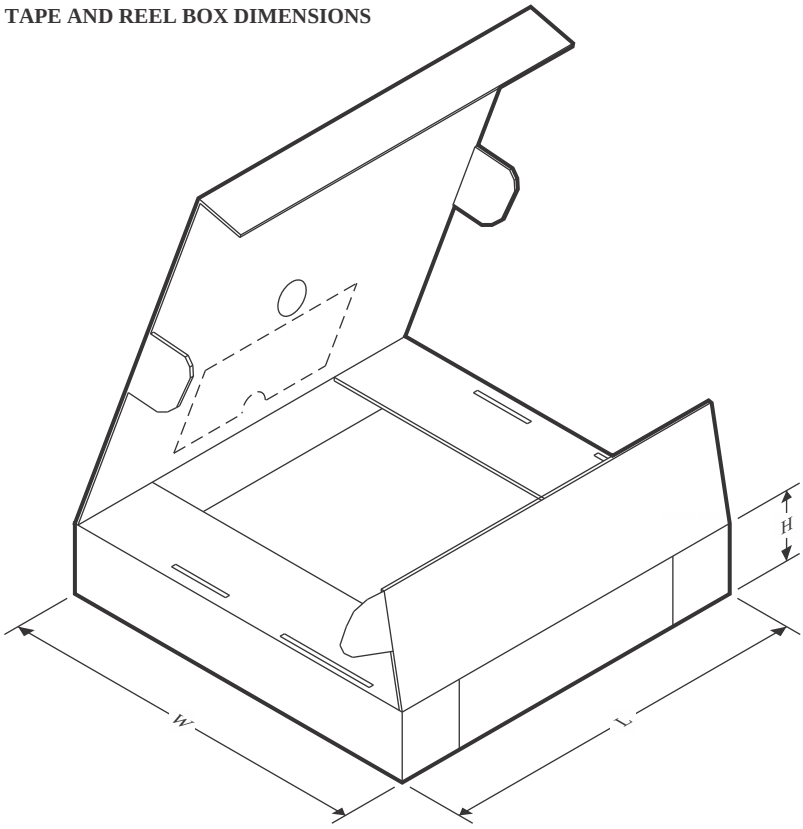
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD1E01B04DPYRQ1	X1SON	DPY	2	10000	178.0	8.4	0.7	1.15	0.47	2.0	8.0	Q1

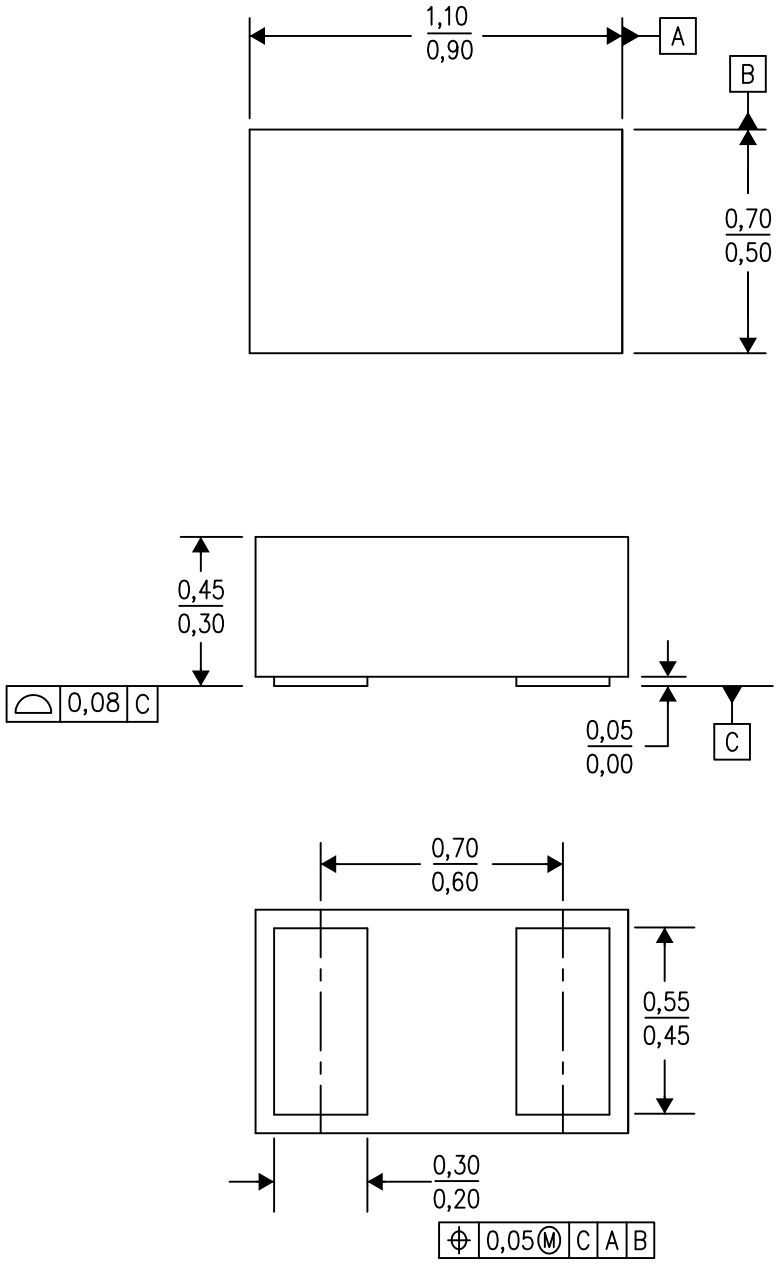
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD1E01B04DPYRQ1	X1SON	DPY	2	10000	205.0	200.0	33.0

DPY (R–PX1SON–N2) PLASTIC SMALL OUTLINE NO–LEAD



4211012/D 08/14

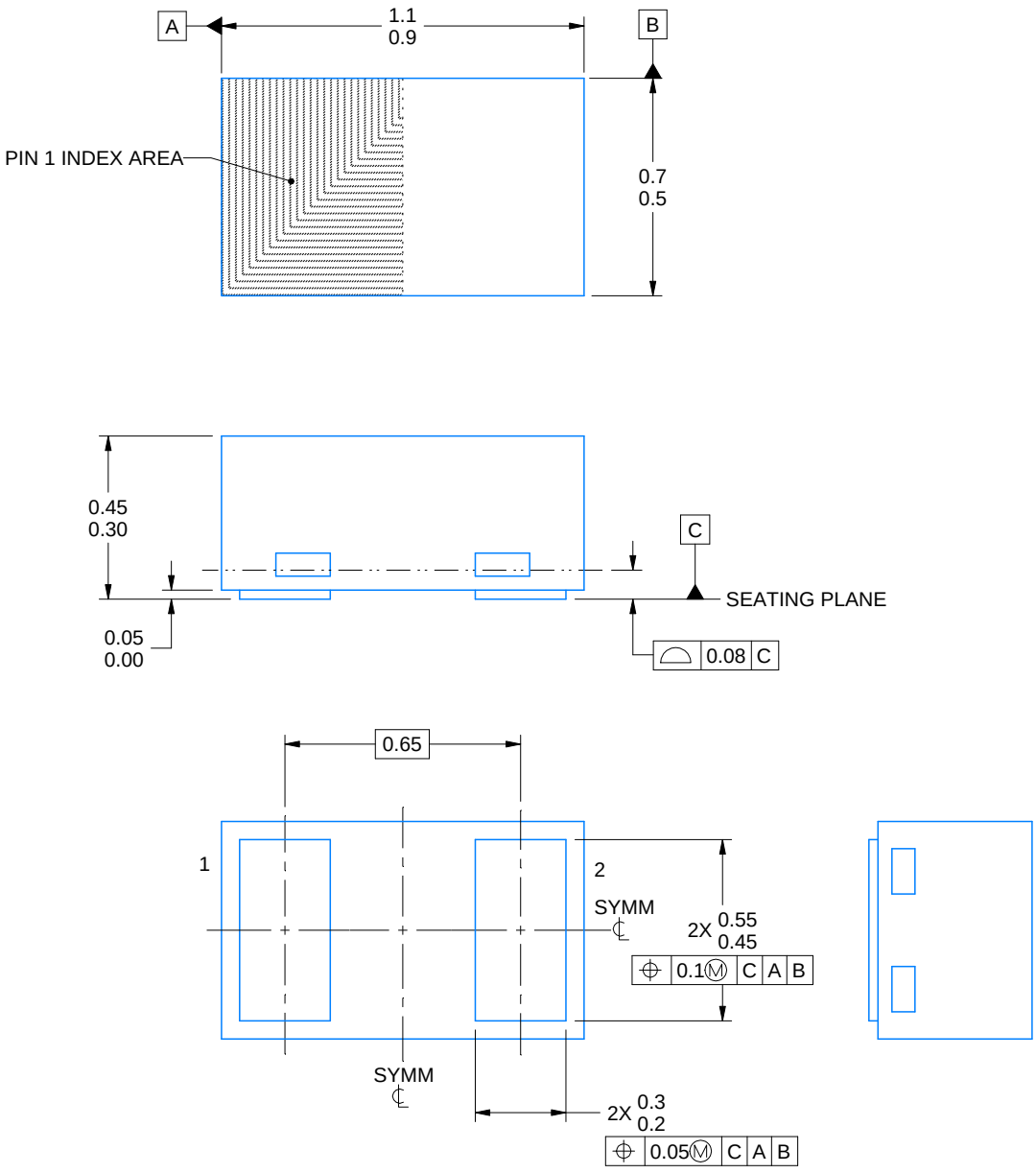
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.

PACKAGE OUTLINE

DPY0002A

X1SON - 0.45 mm max height

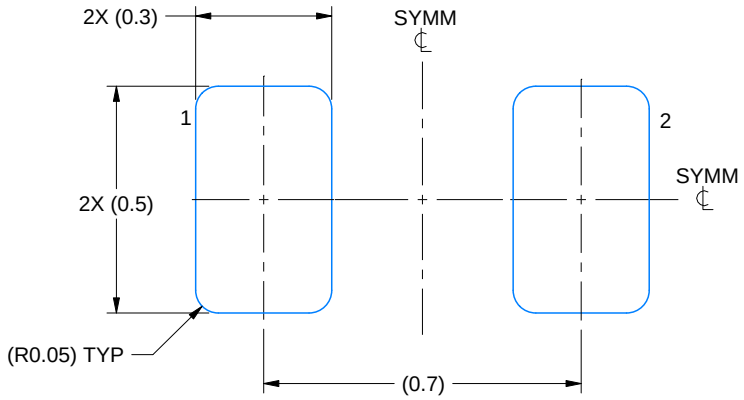
PLASTIC SMALL OUTLINE - NO LEAD



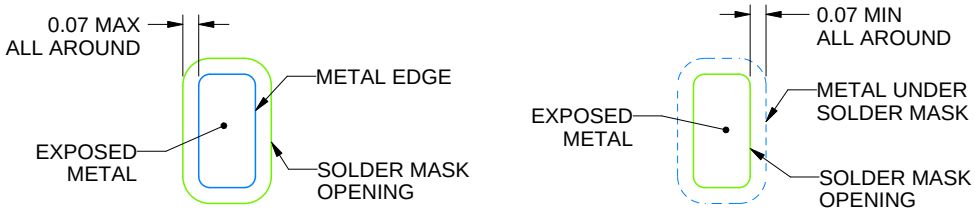
4224561/B 03/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:60X



SOLDER MASK DETAILS

4224561/B 03/2021

NOTES: (continued)

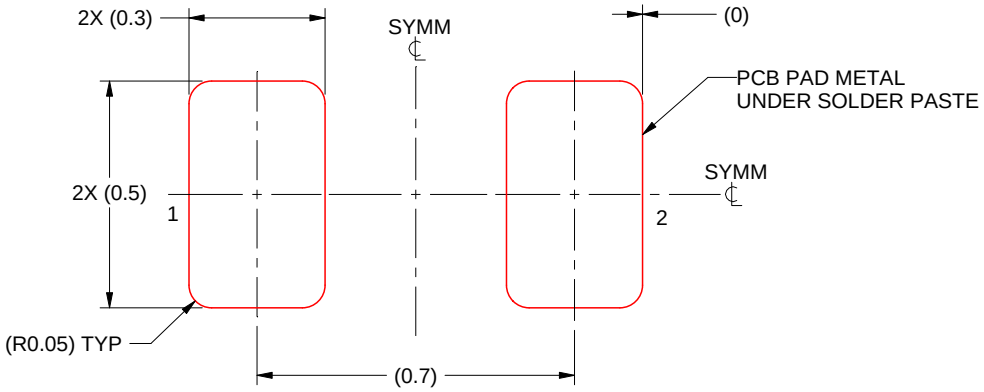
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DPY0002A

X1SON - 0.45 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:60X

4224561/B 03/2021

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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