QUADRUPLE LOW-POWER DIFFERENTIAL RECEIVER

Check for Samples: SN55LBC173-HIREL

FEATURES

- **Meets EIA Standards RS-422-A, RS-423-A, RS-485, and CCITT V.11**
- **Designed to Operate With Pulse Durations as Short as 20 ns**
- **Designed for Multipoint Bus Transmission on Long Bus Lines in Noisy Environments**
- **Input Sensitivity: ±200 mV**
- **Low-Power Consumption: 20 mA (Max)**
- **Open-Circuit Fail-Safe Design**

DESCRIPTION

The SN55LBC173 is a monolithic quadruple differential line receiver with 3-state outputs designed to meet the requirements of the EIA standards RS-422-A, RS-423-A, RS-485, and CCITT V.11. This device is optimized for balanced multipoint bus transmission at data rates up to and exceeding 10 million bits per second. The four receivers share two ORed enable inputs, one active when high, the other active when low. Each receiver features high input impedance, input hysteresis for increased noise immunity, and input sensitivity of ±200 mV over a common-mode input voltage range of 12 V to –7 V. Fail-safe design ensures that if the inputs are open circuited, the output is always high. The SN55LBC173 is designed using the Texas Instruments proprietary LinBiCMOS™ technology that provides low power consumption, high switching speeds, and robustness.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

T_A	PACKAGE	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	KGD	SN55LBC173MKGD1	NA
		SN55LBC173MKGD2	NA

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

BARE DIE INFORMATION

DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION COMPOSITION	BOND PAD THICKNESS
10.5 mils.	Silicon with backgrind	Floating	AlSi(1%)Cu(0.5%)TiW	1850 nm

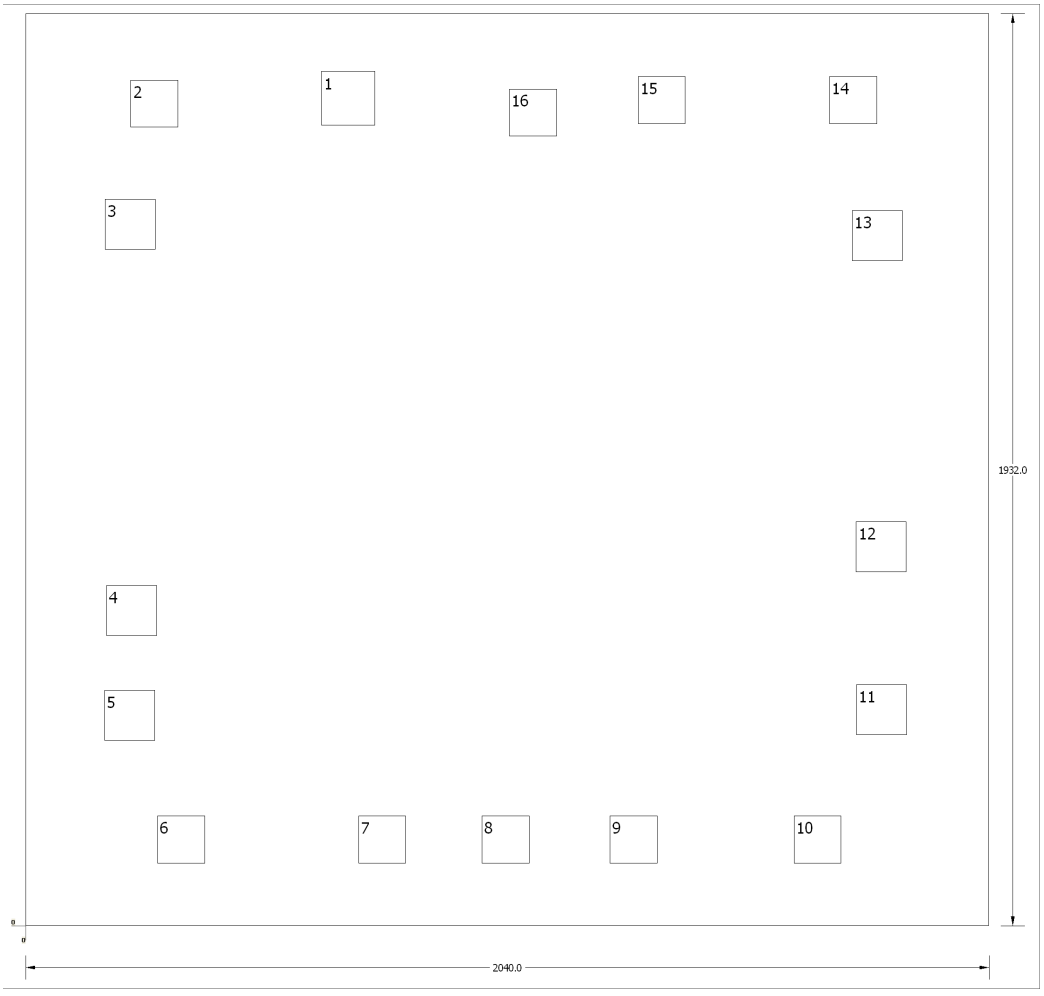


Table 1. Bond Pad Coordinates in Microns

DESCRIPTION	PAD NUMBER	X MIN	Y MIN	X MAX	Y MAX
1B	1	626.5	1695	740.5	1809.5
1A	2	222.5	1690.7	323	1791.3
1Y	3	167.9	1432.1	274.8	1539
G	4	171.4	614.1	278.3	721
2Y	5	166.6	392.1	273.5	499
2A	6	279.2	132	379.7	232.6
2B	7	704.8	132	805.3	232.6
GND	8	966.2	132	1066.7	232.6
3B	9	1237.2	132	1337.7	232.6
3A	10	1626.7	132	1727.2	232.6
3Y	11	1758.7	403.7	1865.6	510.6
$\overline{G}$	12	1758.5	749	1865.4	855.9
4Y	13	1750.1	1408.4	1857	1515.3
4A	14	1702.2	1698.4	1802.7	1799
4B	15	1296.7	1698.4	1397.2	1799
VCC	16	1024.2	1671.9	1124.7	1772.5

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range unless otherwise noted

		Value	UNIT
V_{CC}	Supply voltage range(2)	–0.3 to 7	V
V_I	Input voltage range, (A or B inputs)	±25	V
V_{ID}	Differential input voltage(3)	±25	V
	Data and control voltage range	–0.3 to 7	V
T_A	Operating free-air temperature range	–55 to 125	°C
T_{stg}	Storage temperature range	–65 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.

RECOMMENDED OPERATING CONDITIONS

			MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IC}	Common-mode input voltage		–7		12	
V_{IH}	High-level input voltage	G inputs	2			
V_{IL}	Low-level input voltage				0.8	
V_{ID}	Differential input voltage		–6		6	
I_{OH}	High-level output current				–8	mA
I_{OL}	Low-level output current				16	mA
T_A	Operating free-air temperature		-55		125	°C

ELECTRICAL CHARACTERISTICS

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage		I_O = –8 mA				0.2	V
$V_{IT–}$	Negative-going input threshold voltage		I_O = 8 mA		–0.2			V
V_{hys}	Hysteresis voltage ($V_{IT+} – V_{IT–}$)					45		mV
V_{IK}	Enable input clamp voltage		I_I = – 18 mA			–0.9	–1.5	V
V_{OH}	High-level output voltage		V_{ID} = –200 mV, I_{OH} = –8 mA		3.5	4.5		V
V_{OL}	Low-level output voltage		V_{ID} = –200 mV, I_{OL} = 8 mA			0.3	0.5	V
			V_{ID} = –200 mV, I_{OL} = 8 mA, T_A = 125°				0.7	
I_{OZ}	High-impedance-state output current		V_O = 0 V to V_{CC}				±20	µA
I_I	Bus input current	A or B inputs	V_{IH} = 12 V, V_{CC} = 5 V	Other inputs at 0 V		0.7	1.15	mA
			V_{IH} = 12 V, V_{CC} = 0 V			0.8	1.15	
			V_{IH} = –7 V, V_{CC} = 5 V			–0.5	–0.9	
			V_{IH} = –7 V, V_{CC} = 0 V			–0.4	–0.9	
I_{IH}	High-level input current		V_{IH} = 5 V				±20	µA
I_{IL}	Low-level input current		V_{IL} = 0 V				–20	µA
I_{OS}	Short-circuit output current		V_O = 0			–80	–120	mA
I_{CC}	Supply current		Outputs enabled, I_O = 0, V_{ID} = 5 V			11	20	mA
			Outputs disabled			0.9	1.4	

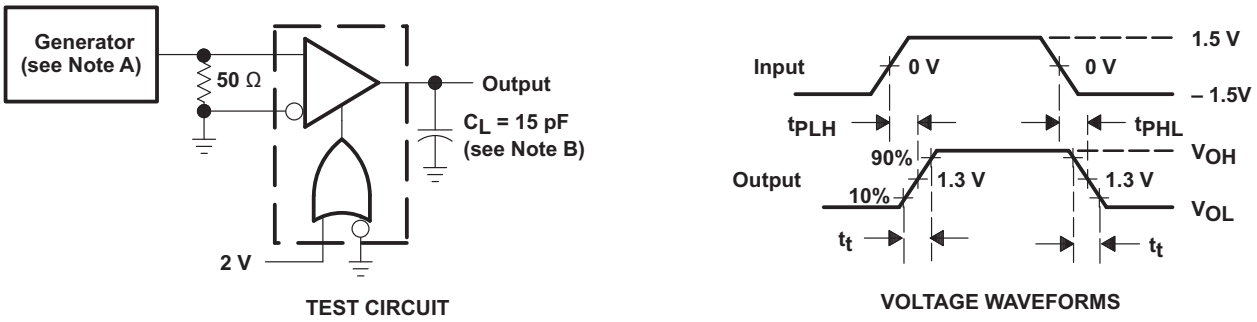
(1) All typical values are at 25°C and with a 5 V supply.

SWITCHING CHARACTERISTICS

V_{CC} = 5 V, C_L = 15 pF, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level output	V_{ID} = –1.5 V to 1.5 V, See Figure 1	25°C	11	22	30	ns
			–55°C to 125°C	11		35	
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = –1.5 V to 1.5 V, See Figure 1	25°C	11	22	35	ns
			–55°C to 125°C	11		35	
t_{PZH}	Output enable time to high level	See Figure 2	25°C		17	40	ns
			–55°C to 125°C			45	
t_{PZL}	Output enable time to low level	See Figure 3	25°C		18	30	ns
			–55°C to 125°C			35	
t_{PHZ}	Output disable time from high level	See Figure 2	25°C		30	40	ns
			–55°C to 125°C			55	
t_{PLZ}	Output disable time from low level	See Figure 3	25°C		25	40	ns
			–55°C to 125°C			45	
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} – t_{PLH}\|$)	See Figure 1	25°C		0.5	6	ns
			–55°C to 125°C			7	
t_t	Transition time	See Figure 1	25°C		5	10	ns
			–55°C to 125°C			16	

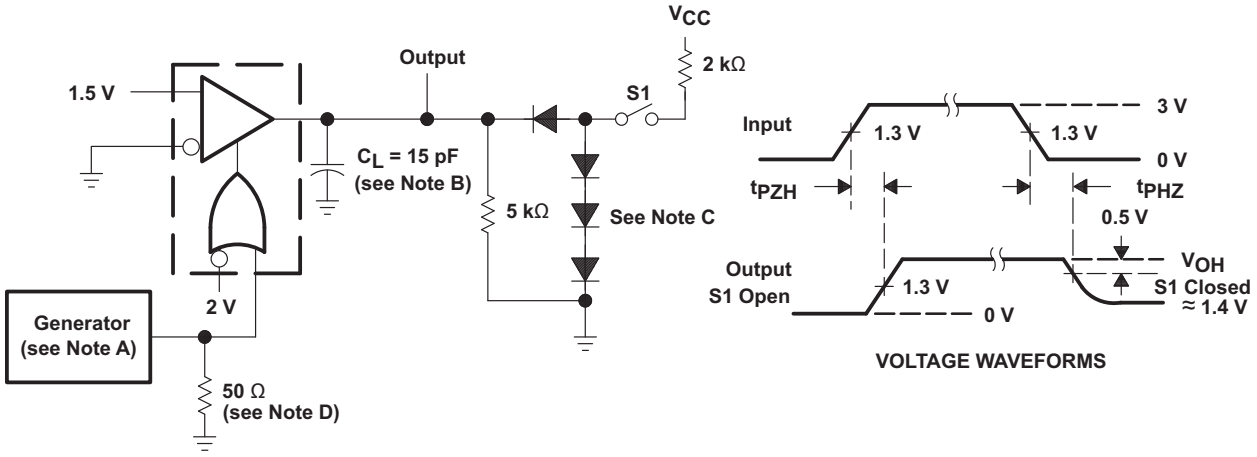
PARAMETER MEASUREMENT INFORMATION



A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle ≤ 50%, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

B. C_L includes probe and jig capacitance.

Figure 1. t_{pd} and t_t Test Circuit and Voltage Waveforms



A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle ≤ 50%, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

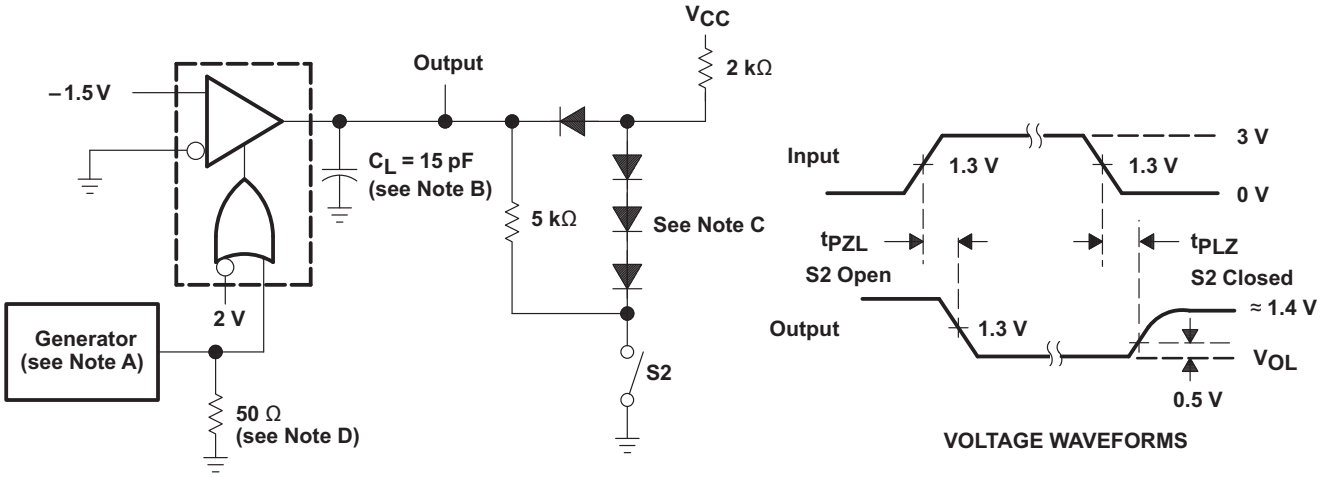
B. C_L includes probe and jig capacitance.

C. All diodes are 1N916 or equivalent.

D. To test the active-low enable $\overline{G}$, ground G and apply an inverted input waveform to $\overline{G}$.

Figure 2. t_{PHZ} and t_{PZH} Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)



TEST CIRCUIT

VOLTAGE WAVEFORMS

A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle ≤ 50%, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

B. C_L includes probe and jig capacitance.

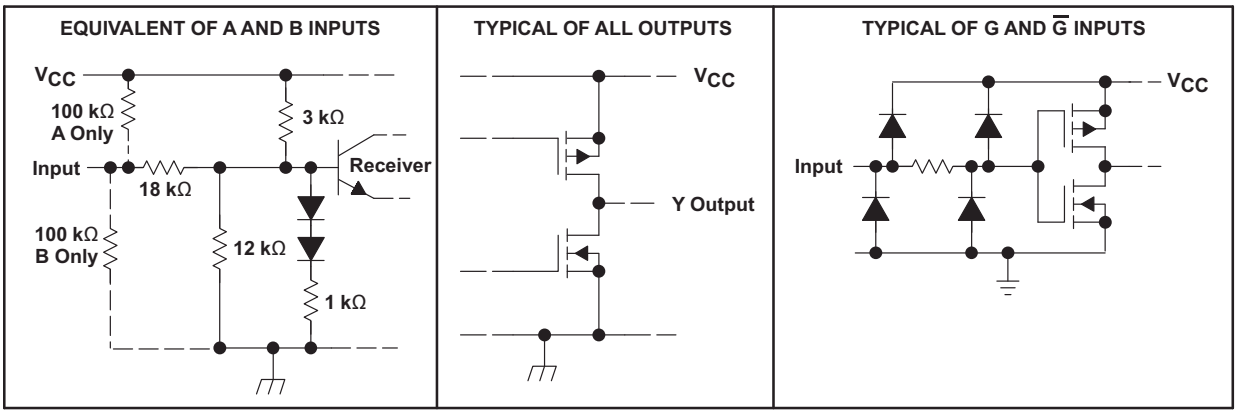
C. All diodes are 1N916 or equivalent.

D. To test the active-low enable $\overline{G}$, ground G and apply an inverted input waveform to $\overline{G}$.

Figure 3. t_{PZL} and t_{PLZ} Test Circuit and Voltage Waveforms

DEVICE INFORMATION

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



FUNCTION TABLE (EACH RECIEVER)

DIFFERENTIAL INPUTS	ENABLES		OUTPUT
A - B	G	$\overline{G}$	Y
$V_{ID} \geq 0.2$ V	H	X	H
	X	L	H
$-0.2 < V_{ID} < 0.2$ V	H	X	?
	X	L	?
$V_{ID} \leq -0.2$ V	H	X	L
	X	L	L
X	L	H	Z
Open circuit	H	X	H
	X	L	H

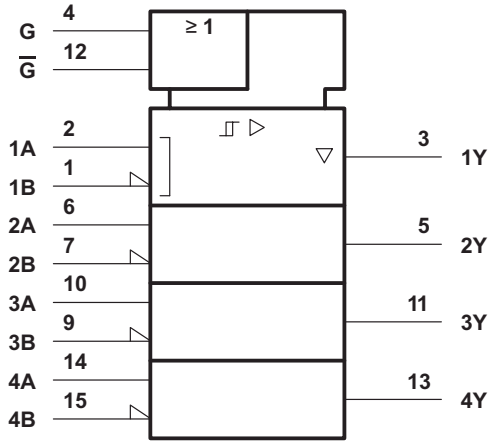


Figure 4. Logic Symbol

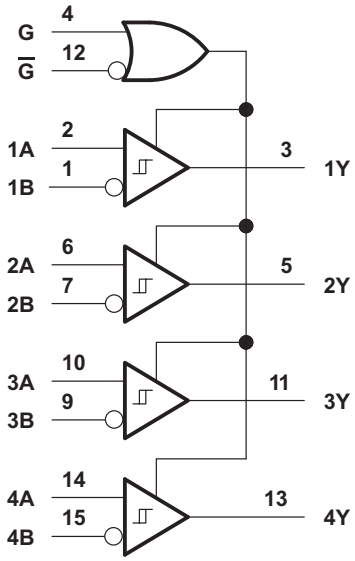


Figure 5. Logic Diagram (Positive Logic)

TYPICAL CHARACTERISTICS

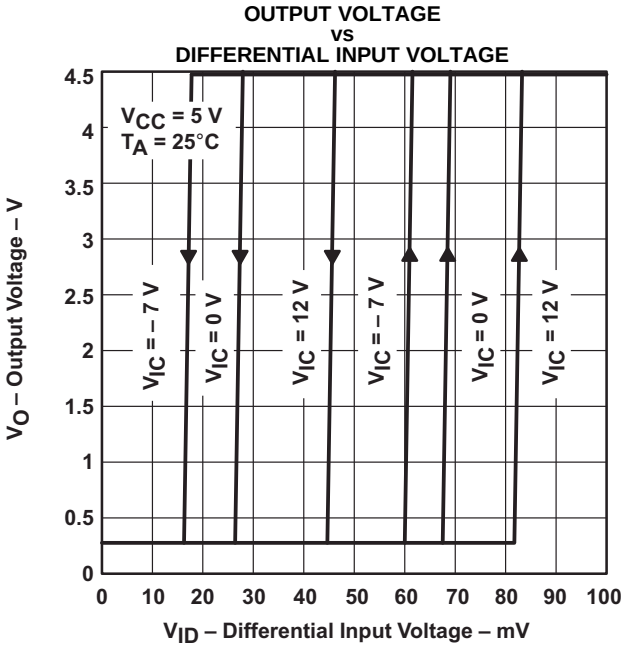


Figure 6.

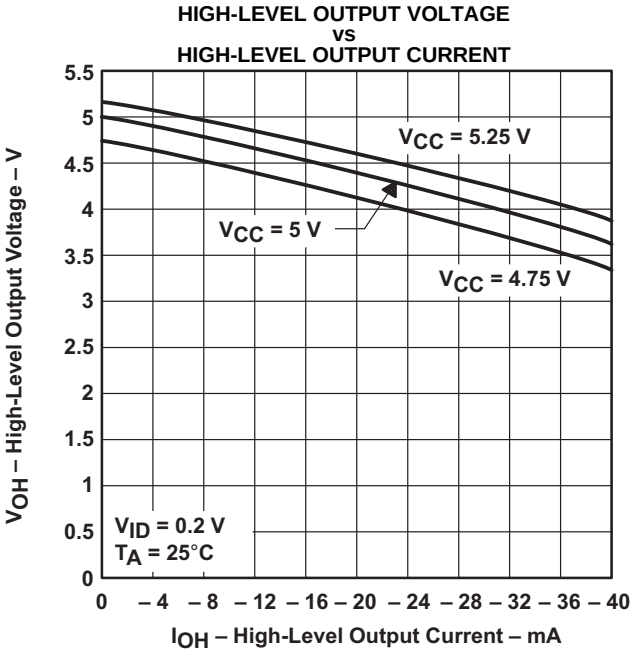


Figure 7.

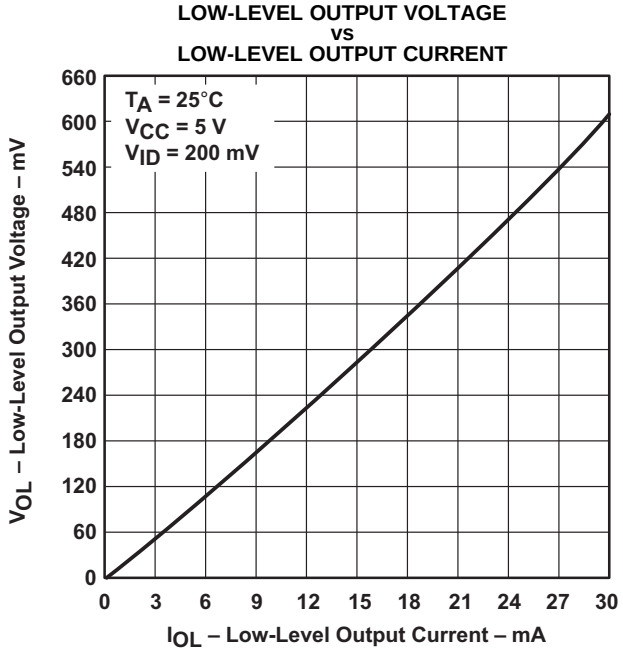


Figure 8.

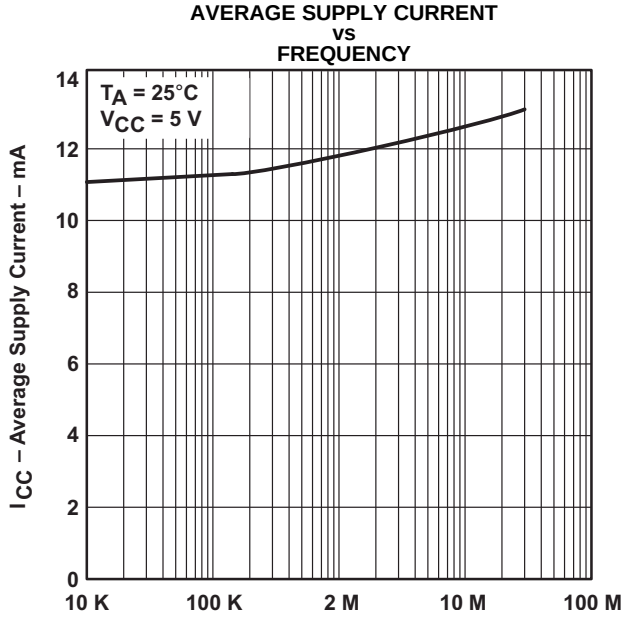


Figure 9.

TYPICAL CHARACTERISTICS (continued)

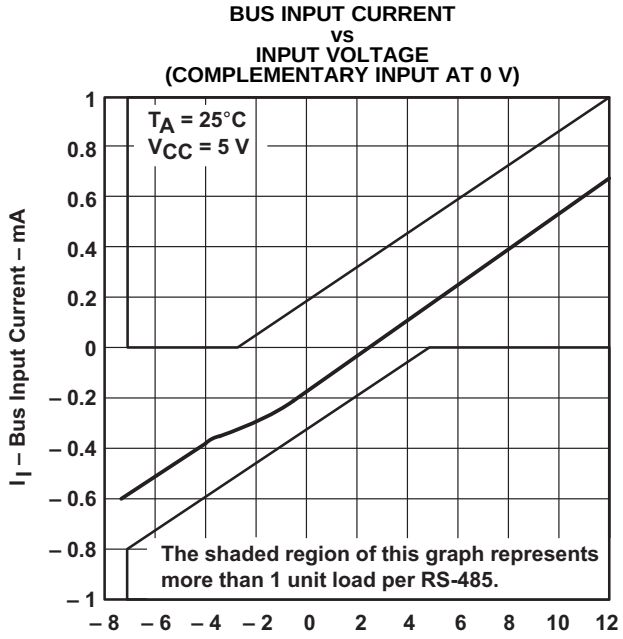


Figure 10.

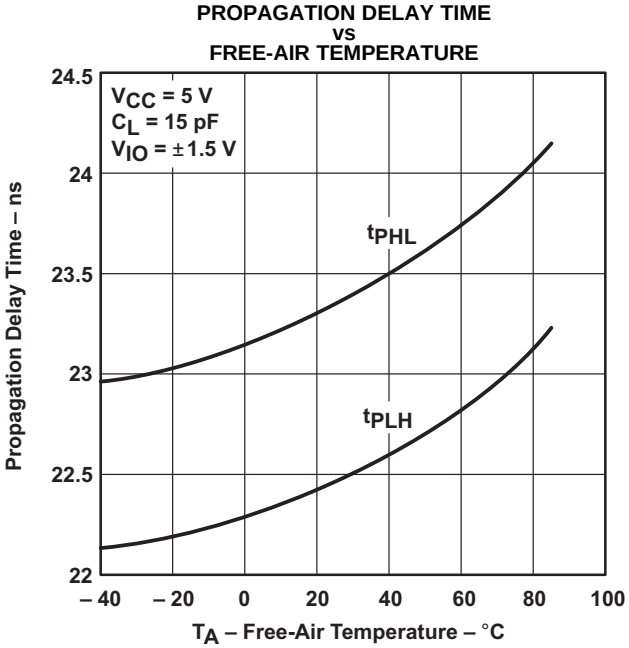


Figure 11.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN55LBC173MKGD1	ACTIVE	XCEPT	KGD	0	100	RoHS & Green	Call TI	N / A for Pkg Type	-55 to 125		Samples
SN55LBC173MKGD2	ACTIVE	XCEPT	KGD	0	10	TBD	Call TI	Call TI	-55 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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