ESP8684 Series

Hardware Design Guidelines

Introduction

Hardware design guidelines give advice on how to integrate ESP8684 into other products. ESP8684 is a series of ultra-low-power Wi-Fi and Bluetooth® 5 (LE) SoCs.

These guidelines will help to ensure optimal performance of your product with respect to technical accuracy and conformity to Espressif's standards.

Version 1.4
Espressif Systems

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1 Overview

Note:

Check the link or the QR code to make sure that you use the latest version of this document:
https://espressif.com/sites/default/files/documentation/esp8684_hardware_design_guidelines_en.pdf

ESP8684 series is an ultra-low-power MCU-based SoC solution that supports 2.4 GHz Wi-Fi and Bluetooth® Low Energy (Bluetooth LE). With its state-of-the-art power and RF performance, this SoC is an ideal choice for a wide variety of application scenarios relating to Internet of Things (IoT), smart home, industrial automation, health care, and consumer electronics.

At the core of this chip is a 32-bit RISC-V single-core processor that operates at up to 120 MHz. The chip supports application development, without the need for a host MCU.

ESP8684 series provides a highly-integrated way to implement Wi-Fi and Bluetooth LE technologies using a complete RF subsystem, including a antenna switch, RF balun, power amplifier, low noise amplifier (LNA), filter, power management unit, calibration circuits, etc. As a result, PCB size has been greatly reduced.

With its advanced calibration circuitry, ESP8684 can dynamically adjust itself to remove external circuit imperfections or adapt to changes in external conditions. As such, the mass production of ESP8684 series does not require expensive and specialized Wi-Fi test equipment.

For more information about ESP8684 series, please refer to *ESP8684 Series Datasheet*.

Note:

Unless otherwise specified, "ESP8684" used in this document refers to the series of chips, instead of a specific chip variant.

2 Schematic Checklist

The integrated circuitry of ESP8684 requires only 15 electrical components (resistors, capacitors, and inductors) and one crystal. The high integration of ESP8684 allows for simple peripheral circuit design. This chapter details ESP8684 schematics.

ESP8684 schematic is shown in Figure 1.

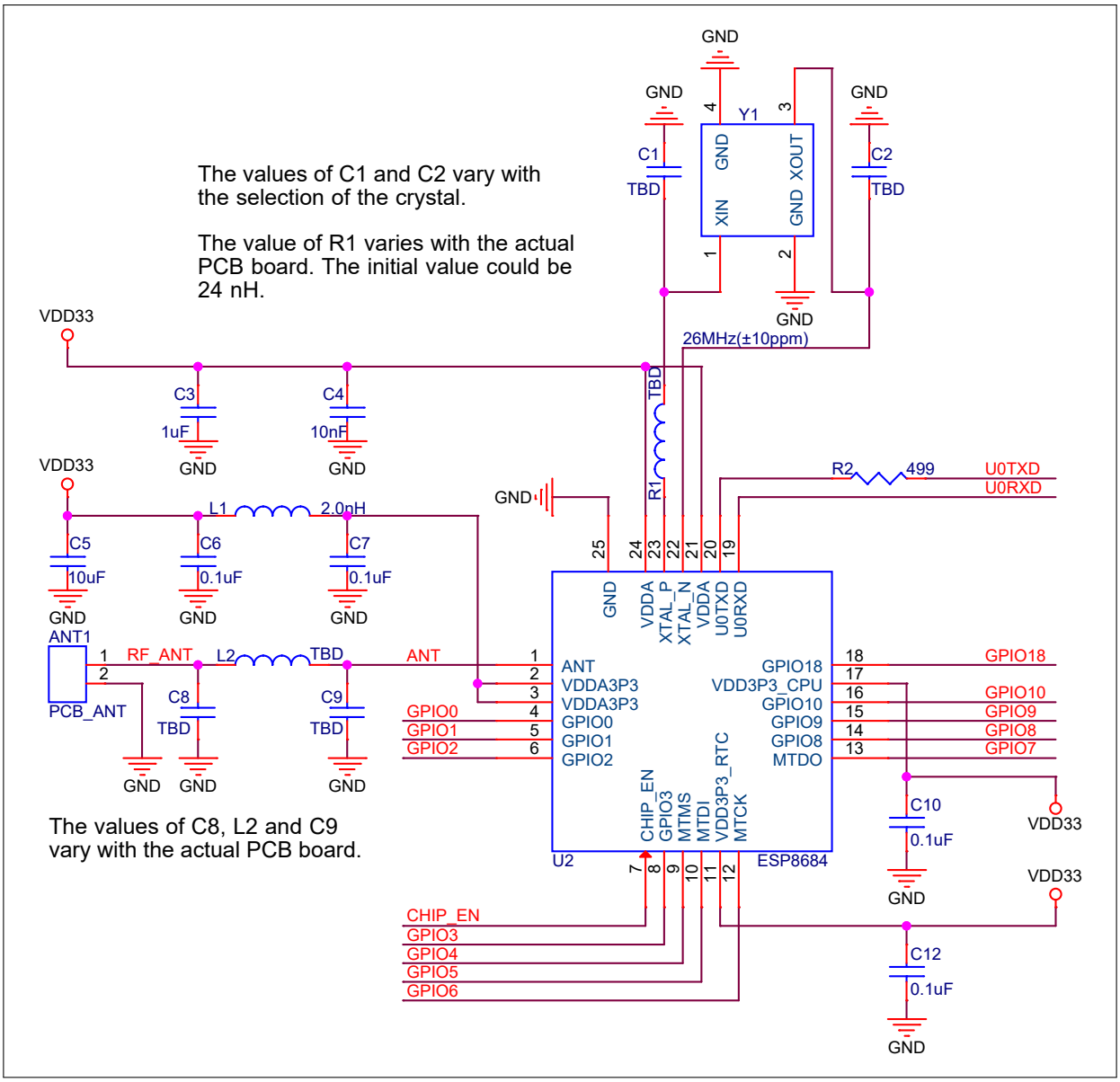

Figure 1: ESP8684 Schematic

Any basic ESP8684 circuit design may be broken down into the following major sections:

- Power supply
- Power-on sequence and system reset
- Flash
- Clock source
- RF
- UART
- ADC
- Strapping pins

- GPIO

The rest of this document details the specifics of circuit design for each of these sections.

2.1 Power Supply

Details of using power supply pins can be found in Section *Power Scheme* in *ESP8684 Series Datasheet*.

2.1.1 Digital Power Supply

ESP8684 has pin 17 VDD3P3_CPU that supplies power to CPU IO, in a voltage range of 3.0 V ~ 3.6 V. It is recommended to add an extra 0.1 μF filter capacitor close to this digital power supply pin.

The schematic for the digital power supply pins is shown in Figure 2.

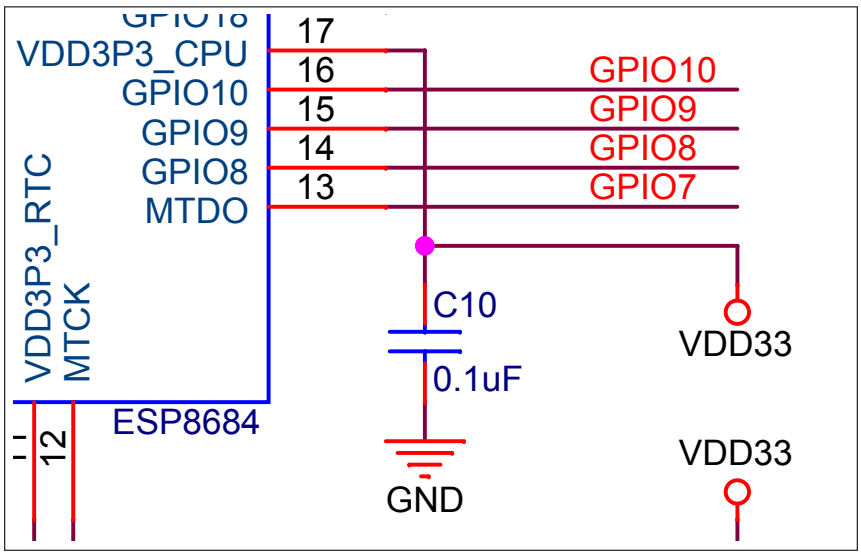

Figure 2: Schematic for the Digital Power Supply Pins

2.1.2 Analog Power Supply

Pin 2 and 3 (both labelled VDDA3P3), pin 21 and 24 (both VDDA) are the analog power supply pins, working at 3.0 V ~ 3.6 V.

It should be noted that the sudden increase in current draw, when ESP8684 is transmitting signals, may cause a power rail collapse. Therefore, it is highly recommended to add another 10 μF capacitor to the power trace, which can work in conjunction with the 0.1 μF capacitor. In addition, a LC filter circuit needs to be added near VDDA3P3 pins so as to suppress high-frequency harmonics. The recommended rated current of the inductor is 500 mA or above. Refer to Figure 3 and place the appropriate decoupling capacitor near each analog power pin.

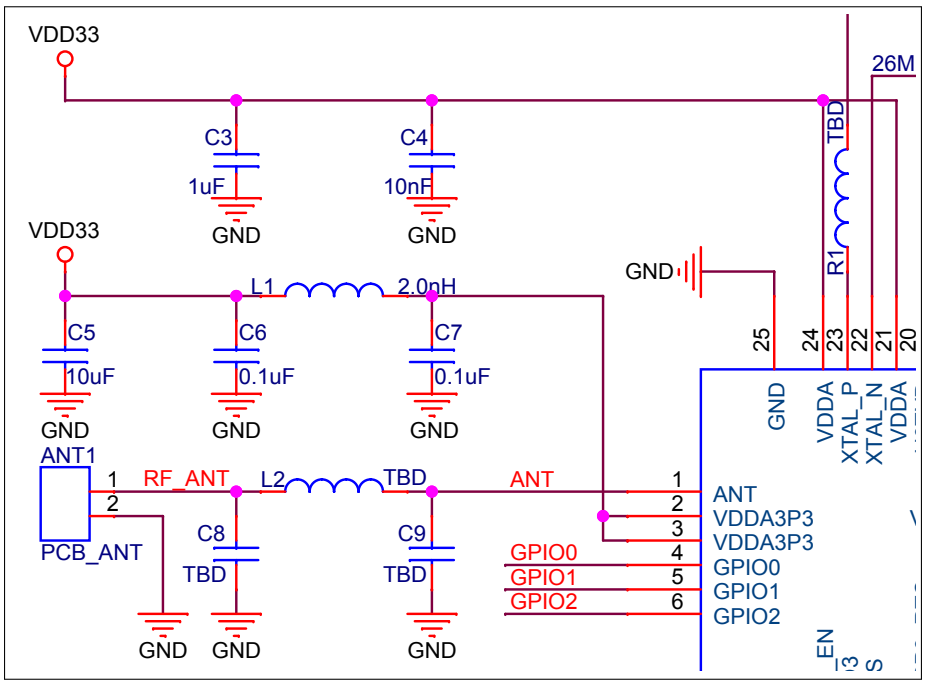

Figure 3: Schematic for the Analog Power Supply Pins

2.1.3 RTC Power Supply

The pin 11 VDD3P3_RTC of ESP8684 series of chips is RTC and analog power supply pin. It is recommended to place a 0.1 μf decoupling capacitor near this pin in the circuit.

Please note that this power supply cannot be used as backup power.

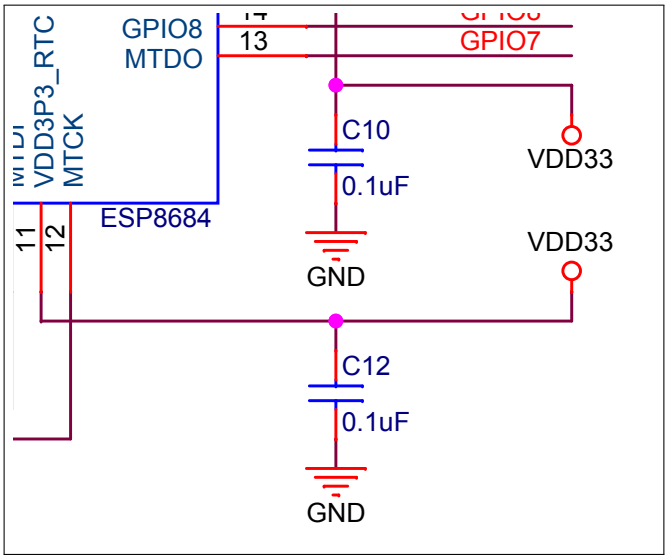

Figure 4: ESP8684 RTC Power Supply

Notice:

- The recommended power supply voltage for ESP8684 is 3.3 V and the output current is no less than 500 mA.
- It is suggested to add an ESD protection diode at the power entrance.

2.2 Power-up Timing and System Reset

2.2.1 Power-up Timing

ESP8684 uses a 3.3 V system power supply. The chip should be activated after the power rails have stabilized. This is achieved by delaying the activation of CHIP_EN after the 3.3 V rails have been brought up. More details can be found in Section 2.2.3.

Notice:

To ensure that stable power is supplied to the chip during power-up, it is advised to add an RC delay circuit at the CHIP_EN pin. The recommended setting for the RC delay circuit is usually R = 10 kΩ and C = 1 μF. However, specific parameters should be adjusted based on the characteristics of the power supply and the power-up and reset sequence timing of the chip.

2.2.2 System Reset

CHIP_EN serves as the reset pin of ESP8684. The reset voltage (V_{IL_nRST}) should be in the range of (–0.3 ~ 0.25 × VDD) V. VDD is the I/O voltage for a particular power domain of pins. To avoid reboots caused by external interferences, make the CHIP_EN trace as short as possible. Also, add a pull-up resistor as well as a capacitor to the ground whenever possible.More details can be found in Section 2.2.3.

Notice:

CHIP_EN pin must not be left floating.

2.2.3 Power-up and Reset Timing

Figure 5 shows the power-up and reset timing of ESP8684 series of chips. Details about the parameters are listed in Table 1.

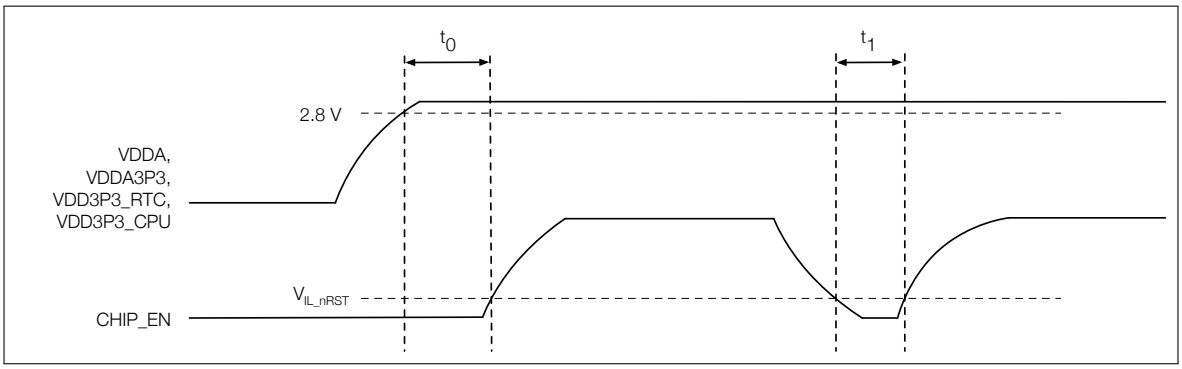

Figure 5: ESP8684 Power-up and Reset Timing

Table 1: Description of ESP8684 Power-up and Reset Timing Parameters

Parameter	Description	Min (μs)
t_0	Time between bringing up the VDDA, VDDA3P3, VDD3P3_RTC, and VDD3P3_CPU rails, and activating CHIP_EN	50
t_1	Duration of CHIP_EN signal level < V_{IL_nRST} to reset the chip	50

2.3 Flash

ESP8684 series is embedded with flash. If external flash is needed, please connect to the free GPIOs.

2.4 Clock Source

ESP8684 has two clock sources:

- External crystal oscillator clock source
- RTC clock source

2.4.1 External Clock Source (compulsory)

Currently, the ESP8684 firmware only supports 26 MHz crystal.

Crystal

The circuit for the crystal is shown in Figure 6. The specific capacitive values of C1 and C2 depend on further testing of the overall performance of the whole circuit. In order to reduce the drive strength of the crystal and minimize the impact of crystal harmonics on RF performance, please add a series inductor (initially of 24 nH) on the XTAL_P clock trace. Note that the accuracy of the selected crystal should be within ±10 ppm at room temperature.

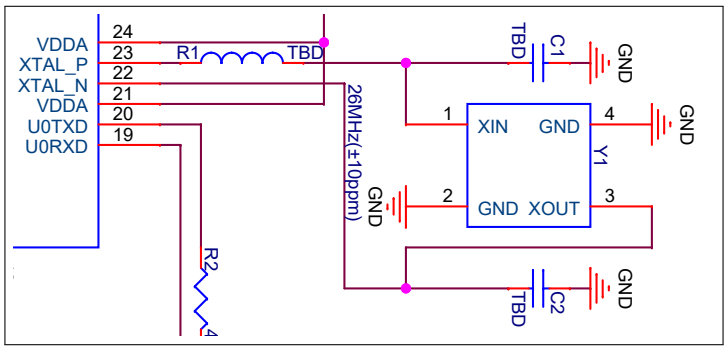

Figure 6: Schematic for the Crystal

Notice:

Defects in the manufacturing of crystal and oscillators (for example, large frequency deviation of more than ±10 ppm, unstable performance within operating temperature range, etc) may lead to the malfunction of ESP8684, resulting in a decrease of the RF performance.

2.4.2 RTC (optional)

ESP8684 supports an external clock signal (e.g., an oscillator) input through GPIO0 to act as the RTC sleep clock and the typical clock frequency is 32.768 kHz. The amplitude of the input clock signal should be the same as the amplitude requirement of the GPIO input signal.

2.5 RF

The RF circuit of the ESP8684 series of chips is mainly composed of three parts, the RF traces on the PCB board, the chip matching circuit, the antenna and the antenna matching circuit.

For the RF traces on the PCB board, 50 Ω impedance control is required.

Chip matching circuit must be placed close to the chip. It is mainly used to adjust the impedance point and suppress harmonics. The CLC structure is preferred, and a set of LC can be added if space permits. The CLC matching circuit is shown in Figure 7.

For the antenna and the antenna matching circuit, to ensure the radiation performance, the antenna's characteristic impedance must be around 50 Ω. Adding a CLC matching circuit near the antenna is recommended to adjust the antenna. However, if the available space is limited and the antenna impedance point can be guaranteed to be 50 Ω by simulation, then there is no need to add a matching circuit near the antenna.

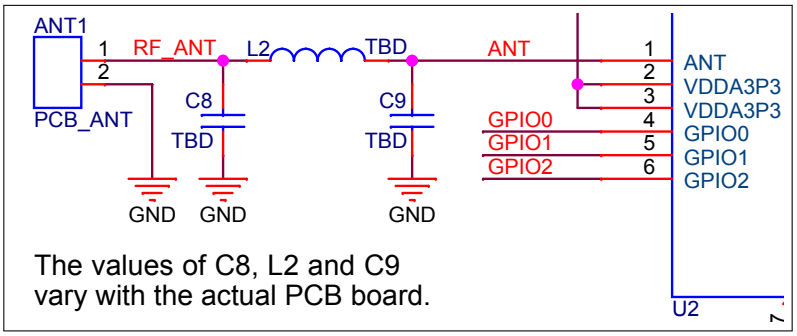

Figure 7: Schematic for RF Matching

Figure 8 shows the general process of RF tuning. Please be noted the matching parameters are subject to the RF tuning of PCB board, which depends greatly on the antenna and PCB layout. The initial value can be 0 Ω. For ESP8684 series of chips, it is recommended to set the S11 parameter in the figure below to 35+j0 and the center frequency is 2442 MHz.

If the RF function is not required, the RF pin can be left floating.

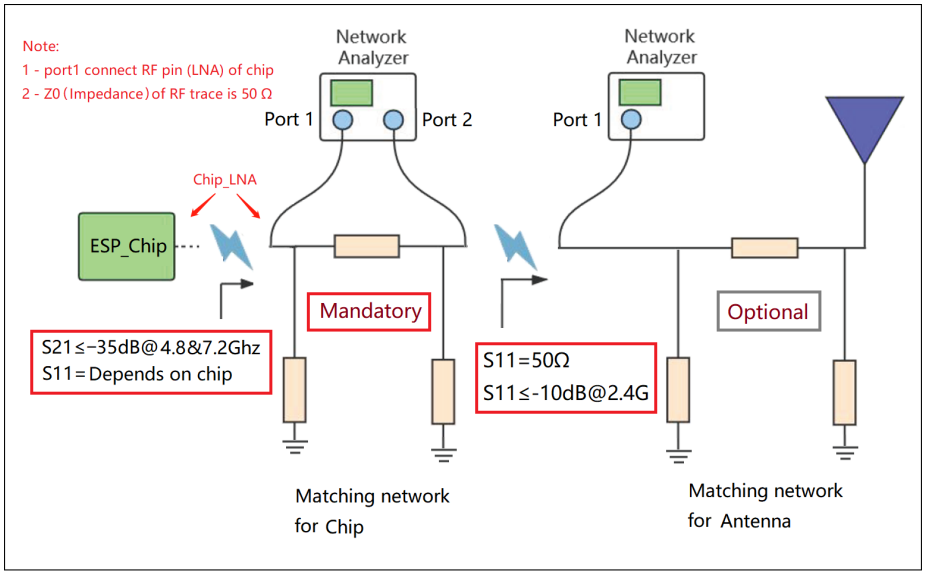

Figure 8: RF Tuning Diagram

2.6 UART

It is recommended to connect a 499 Ω series resistor to the U0TXD line in order to suppress the 80 MHz harmonics.

2.7 ADC

It is recommended to add a 0.1 μF filter capacitor between pins and ground when using the ADC function.

2.8 Strapping Pins

Note:
The content below is excerpted from Section Strapping Pins in *ESP8684 Series Datasheet*.

ESP8684 series has two strapping pins:

- GPIO8
- GPIO9

Software can read the values of GPIO8 and GPIO9 from GPIO_STRAPPING field in GPIO_STRAP_REG register. For register description, please refer to Section GPIO Matrix Register Summary in *ESP8684 Technical Reference Manual*.

During the chip's power-on reset, RTC watchdog reset, and brownout reset, the latches of the strapping pins sample the voltage level as strapping bits of "0" or "1", and hold these bits until the chip is powered down or shut down.

By default, GPIO9 is connected to the internal weak pull-up resistor. If GPIO9 is not connected or connected to an external high-impedance circuit, the latched bit value will be "1".

To change the strapping bit values, you can apply the external pull-down/pull-up resistances, or use the host MCU's GPIOs to control the voltage level of these pins when powering on ESP8684.

After reset, the strapping pins work as normal-function pins.

Table 2 lists detailed booting configurations of the strapping pins.

Table 2: Strapping Pins

Booting Mode [1]			
Pin	Default	SPI Boot	Download Boot
GPIO8	N/A	Don't care	1
GPIO9	Internal weak pull-up	1	0
Enabling/Disabling ROM Messages Print During Booting			
Pin	Default	Functionality	

GPIO8	N/A	When the value of eFuse field EFUSE_UART_PRINT_CONTROL is 0 (default), print is enabled and not controlled by GPIO8. 1, if GPIO8 is 0, print is enabled; if GPIO8 is 1, it is disabled. 2, if GPIO8 is 0, print is disabled; if GPIO8 is 1, it is enabled. 3, print is disabled and not controlled by GPIO8.

[1] The strapping combination of GPIO8 = 0 and GPIO9 = 0 is invalid and will trigger unexpected behavior.

Figure 9 shows the setup and hold times for the strapping pins before and after the CHIP_EN signal goes high. Details about the parameters are listed in Table 3.

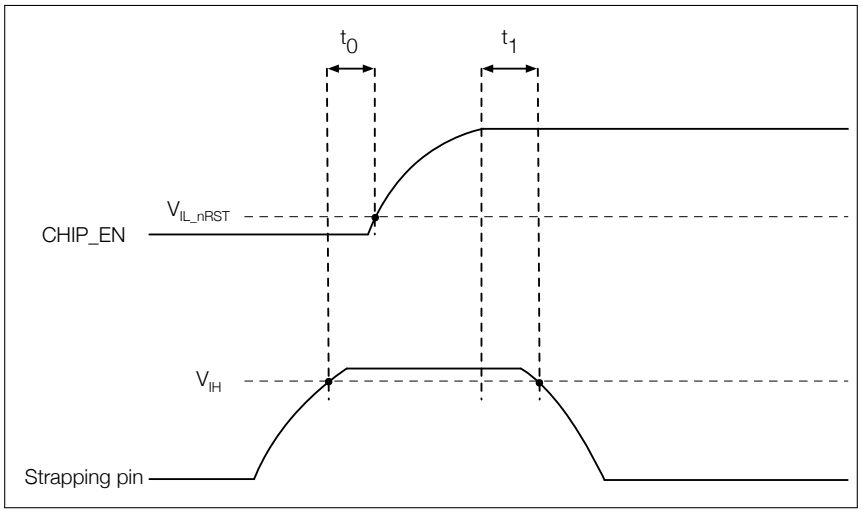

Figure 9: Setup and Hold Times for the Strapping Pins

Table 3: Parameter Descriptions of Setup and Hold Times for the Strapping Pins

Parameter	Description	Min (ms)
t_0	Setup time before CHIP_EN goes from low to high	0
t_1	Hold time after CHIP_EN goes high	3

2.9 GPIO

Note:
The content below is excerpted from Section General Purpose Input / Output Interface (GPIO) in *ESP8684 Technical Reference Manual*.

ESP8684 series has 14 GPIO pins which can be assigned various functions by configuring corresponding registers. Besides digital signals, some GPIOs can be also used for analog functions, such as ADC.

All GPIOs have selectable internal pull-up or pull-down, or can be set to high impedance. When these GPIOs are configured as an input, the input value can be read by software through the register. Input GPIOs can also be set to generate edge-triggered or level-triggered CPU interrupts. All digital IO pins are bi-directional, non-inverting

and tristate, including input and output buffers with tristate control. These pins can be multiplexed with other functions, such as the UART, SPI, etc. For low-power operations, the GPIOs can be set to holding state.

The IO MUX and the GPIO matrix are used to route signals from peripherals to GPIO pins. Together they provide highly configurable I/O. Using GPIO Matrix, peripheral input signals can be configured from any IO pins while peripheral output signals can be configured to any IO pins. Table 4 shows the IO MUX functions of each pin.

For more information about IO MUX and GPIO matrix, please refer to Chapter IO MUX and GPIO Matrix (GPIO, IO_MUX) in *ESP8684 Technical Reference Manual*.

Table 4: IO MUX Pin Functions

Pin Name	No.	Function 0	Function 1	Function 2	Reset	Notes
GPIO0	4	GPIO0	GPIO0	—	0	R, G
GPIO1	5	GPIO1	GPIO1	—	0	R, G
GPIO2	6	GPIO2	GPIO2	FSPIQ	1	R
GPIO3	8	GPIO3	GPIO3	—	1	R, G
MTMS	9	MTMS	GPIO4	FSPIHD	1	R
MTDI	10	MTDI	GPIO5	FSPIWP	1	R, G
MTCK	12	MTCK	GPIO6	FSPICLK	1*	—
MTDO	13	MTDO	GPIO7	FSPID	1	—
GPIO8	14	GPIO8	GPIO8	—	1	—
GPIO9	15	GPIO9	GPIO9	—	3	—
GPIO10	16	GPIO10	GPIO10	FSPICS0	1	—
GPIO18	18	GPIO18	GPIO18	—	0	—
U0RXD	19	U0RXD	GPIO19	—	3	—
U0TXD	20	U0TXD	GPIO20	—	4	—

Reset

The default configuration of each pin after reset:

- **0** - input disabled, in high impedance state (IE = 0)
- **1** - input enabled, in high impedance state (IE = 1)
- **2** - input enabled, pull-down resistor enabled (IE = 1, WPD = 1)
- **3** - input enabled, pull-up resistor enabled (IE = 1, WPU = 1)
- **4** - output enabled, pull-up resistor enabled (OE = 1, WPU = 1)
- **0*** - input disabled, pull-up resistor enabled (IE = 0, WPU = 0). See details in Notes
- **1*** - When the value of eFuse bit EFUSE_DIS_PAD_JTAG is
  0, input enabled, pull-up resistor enabled (IE = 1, WPU = 1)
  1, input enabled, in high impedance state (IE = 1)

We recommend pulling high or low GPIO pins in high impedance state to avoid unnecessary power consumption. You may add pull-up and pull-down resistors in your PCB design referring to Table DC Characteristics (3.3 V, 25 °C) in *ESP8684 Series Datasheet*, or enable internal pull-up and pull-down resistors during software initialization.

Notes

- **R** - These pins have analog functions.
- **G** - These pins have glitches during power-up. See details in Table 5.

Table 5: Power-Up Glitches on Pins

Pin	Glitch[1]	Typical Time Period (μs)
GPIO0	Low-level glitch	40
GPIO1	Low-level glitch	60
GPIO3	Low-level glitch	40
MTDI	Low-level glitch	60

[1] Low-level glitch: the pin is at a low level during the time period;

3 PCB Layout Design

This chapter introduces the key points of how to design an ESP8684 PCB layout using the ESP8684-MINI-1 module as an example.

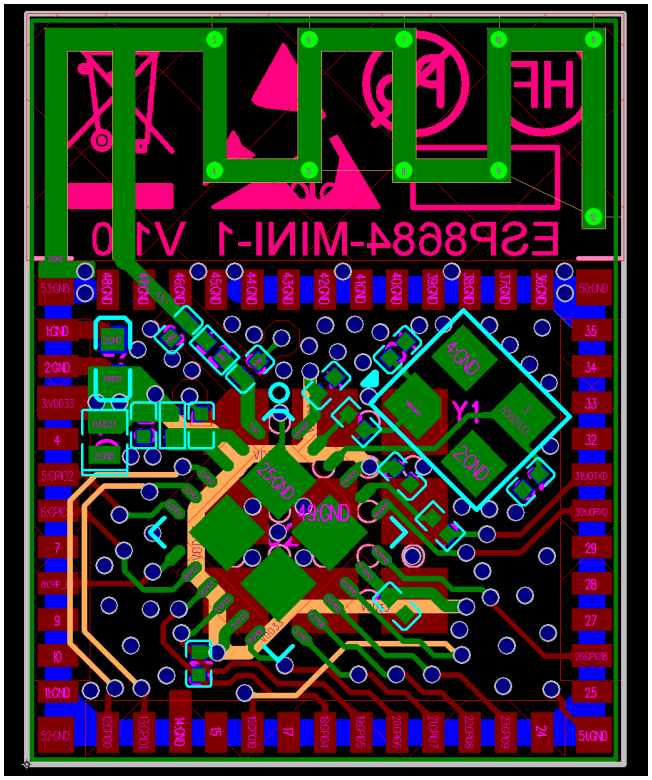

Figure 10: ESP8684 PCB Layout

3.1 General Principles of PCB Layout

It is recommended to use a four-layer PCB design:

- Layer 1 (TOP): Signal traces and components
- Layer 2 (GND): No signal traces here to ensure a complete GND plane
- Layer 3 (POWER): Route power traces here.
- Layer 4 (BOTTOM): It is not recommended to place any components on this layer. It is acceptable to route signal traces on this layer when GND plane is applied.

A two-layer PCB design can also be used:

- Layer 1 (TOP): Signal traces and components
- Layer 2 (BOTTOM): Do not place any components on this layer and keep traces to a minimum. Ideally, it should be a complete GND plane.

3.2 Positioning a Module on a Base Board

If module-on-board design is adopted, attention should be paid while positioning the module on the base board. The interference of the base board on the module's antenna performance should be minimized.

The module should be placed as close to the edge of the base board as possible. On-board PCB antenna should be placed outside the base board whenever possible. In addition, the feed point of the antenna should be closest to the board. In the following example figures, positions with mark ✓are strongly recommended, while positions without a mark are not recommended.

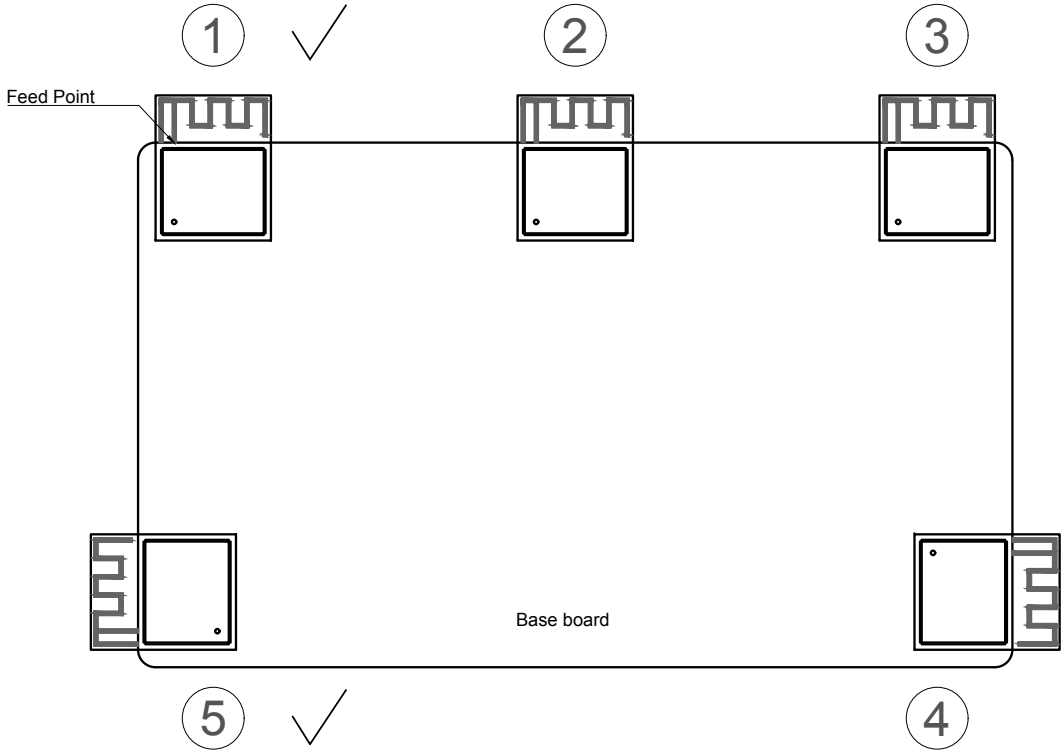

Figure 11: Placement of ESP8684 Modules on Base Board

If PCB antenna could not be outside the board, please ensure a large clear region at least 15 mm around antenna area (no copper, routing, components on it), as shown in Figure 12. If there is base board under the antenna area, it is recommended to cut it off to minimize its impact on the antenna.

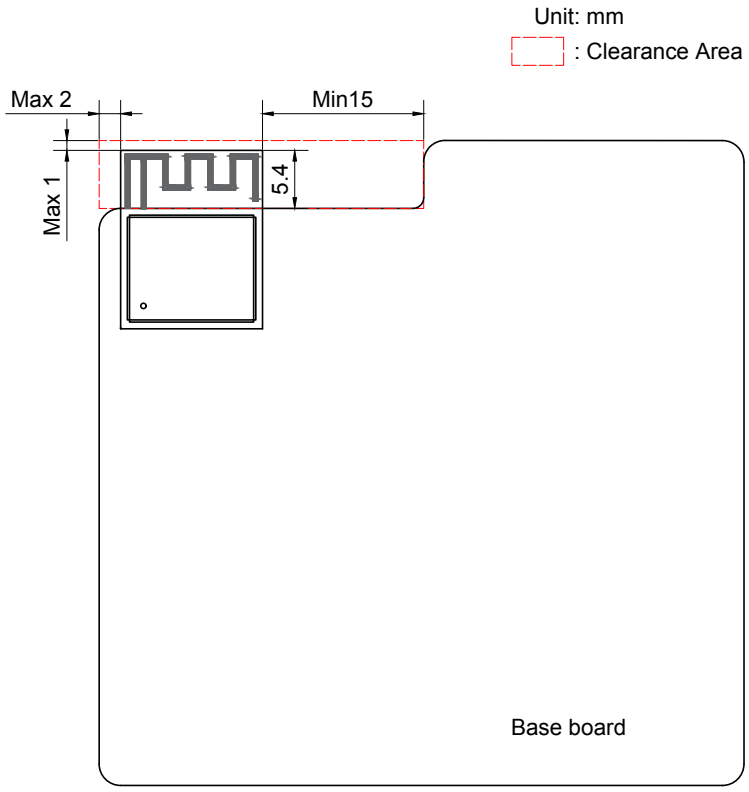

Figure 12: Keepout Zone for ESP8684 Module's Antenna on the Base Board

When designing an end product, attention should be paid to the interference caused by the housing of the antenna and it is recommended to carry out RF verification.

As a conclusion, please be noted it is necessary to test the throughput and communication signal range of the whole product to ensure real product performance.

3.3 Power Supply

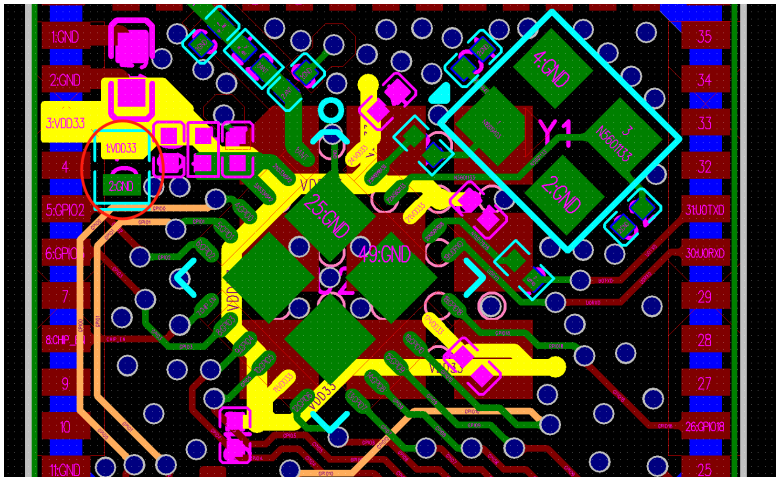

Figure 13: ESP8684 Power Traces in a Four-layer PCB Design

- Four-layer PCB design is recommended over a two-layer design. The power traces should be routed on Layer 3 whenever possible. Vias are required for the power traces to go through the layers and get

connected to the pins on the top layer. There should be at least two vias if the main power traces need to cross layers. The drill diameter on other power traces should be no smaller than the width of the power traces.

- The 3.3 V power traces, highlighted in yellow, are routed as shown in Figure 13. The width of the main power traces should be no less than 20 mil. The width of the power traces for VDDA3P3 pins should be no less than 15 mil. Recommended width of other power traces is 10 mil.
- The ESD protection diode is placed next to the power port (circled in red in the top left quarter of Figure 13). The power trace should have a 10 µF capacitor on its way to the chip, to be used in conjunction with a 0.1 µF capacitor. Then the power traces are divided into two ways from here and form a star-shape topology, thus reducing the coupling between different power pins. Note that all decoupling capacitors should be placed close to the power pin, and ground vias should be added close to the capacitor's ground pin to ensure a short return path.
- As shown in Figure 14, it is recommended to connect the capacitor to ground in the LC filter circuit near VDDA3P3 pins to the fourth layer through a via, and maintain a keep-out area on other layers.
- The power trace begins at the power entrance and reaches VDDA3P3. It is required to add GND isolation between this power trace and the GPIO traces on the left, and place vias whenever possible.
- The ground pad at the bottom of the chip should be connected to the ground plane through at least nine ground vias.

Note:
If you need to solder the module on another board, it is recommended to employ a four-grid EPAD on the solder mask and paste mask, cover the gaps with ink, and place ground vias in the gaps, as shown in Figure 13. This can avoid tin leakage when soldering the module.

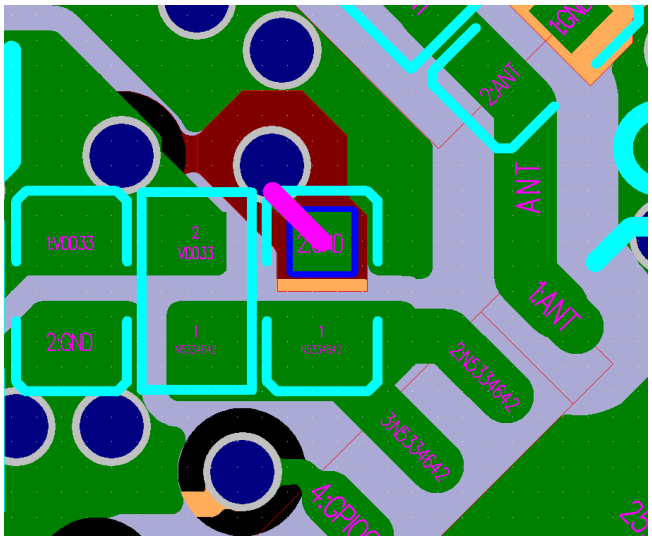

Figure 14: ESP8684 Analog Power Traces in a Four-layer PCB Design

3.4 Crystal Oscillator

Figure 15 shows the reference design of the crystal oscillator. In addition, the following should be noted:

- The crystal oscillator should be placed far from the clock pin to avoid the interference on the chip. **The gap**

should be at least 2.0 mm. It is good practice to add high-density ground via stitching around the clock trace for better isolation.

- There should be no vias for the clock input and output traces, which means the traces cannot cross layers.
- The external regulating capacitor should be placed on the near left or right side of the crystal oscillator, and at the end of the clock trace whenever possible, to make sure the ground pad of the capacitor is close to that of the crystal oscillator.
- Do not route high-frequency digital signal traces under the crystal oscillator. It is best not to route any signal trace under the crystal oscillator. The vias on the power traces on both sides of the crystal clock trace should be placed as far away from the clock trace as possible, and the two sides of the clock trace should be surrounded by grounding copper.
- As the crystal oscillator is a sensitive component, do not place any magnetic components nearby that may cause interference, for example large inductance component, and ensure that there is a clean large-area ground plane around the crystal oscillator.

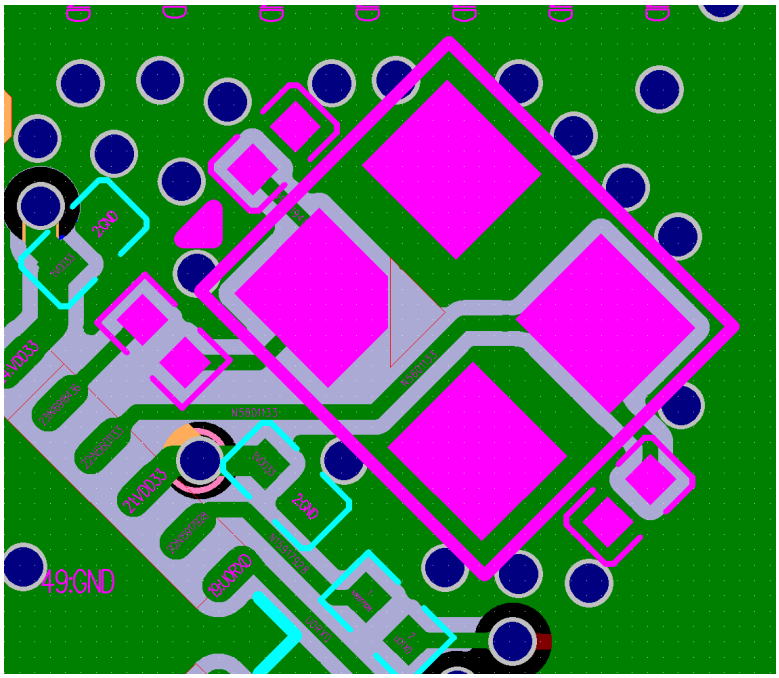

Figure 15: ESP8684 Crystal Oscillator Layout

3.5 RF

The RF trace is routed as shown highlighted in pink in Figure 16.

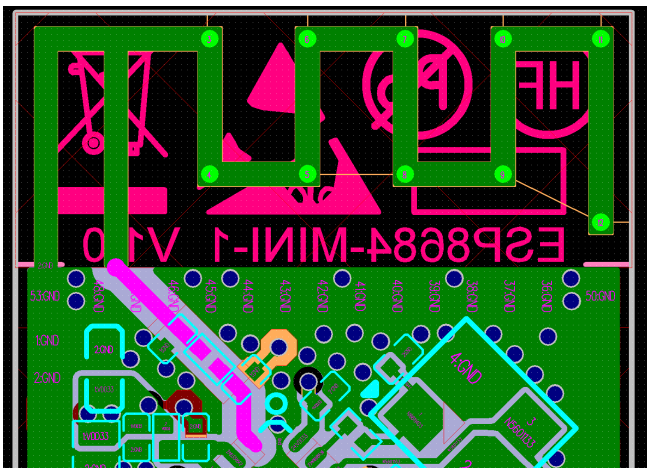

Figure 16: ESP8684 RF Layout in a Four-layer PCB Design

- The RF trace should have 50 Ω single-ended characteristic impedance. The reference plane is the second layer. A π-type matching circuit should be added on the RF trace and placed close to the chip, in a zigzag.
- For designing the RF trace at 50 Ω single-ended impedance, please refer to the PCB stack-up design shown in Figure 17.

Thickness (mm)	Impedance (Ohm)	Gap (mil)	Width (mil)	Gap (mil)
-	50	12.2	12.6	12.2

Stack up	Material	Base copper (oz)	Thickness (mil)	DK
SM			0.4	4
L1_Top	Finished copper 1 oz	0.33	0.8	
PP	7628 TG150 RC50%		8	4.39
L2_Gnd		1	1.2	
Core	Core		Adjustable	4.43
L3_Power		1	1.2	
PP	7628 TG150 RC50%		8	4.39
L4_Bottom	Finished copper 1 oz	0.33	0.8	
SM			0.4	4

Figure 17: ESP8684 PCB Stack up Design

- The RF trace should have consistent width and not branch out. It should be as short as possible with dense ground vias around for inteference shielding.
- The RF trace should be routed on the outer layer without vias, i.e., should not cross layers. The RF trace should be routed at a 135° angle, or with circular arcs if trace bends are required.
- Please add a stub between the ground and the capacitors near the chip to suppress second harmonics. It is preferable to keep the stub length 15 mil, and determine the stub width according to the number of PCB layers, so that the characteristic impedance of the stub is 100 Ω ± 10%. In addition, please connect the stub via to the third layer, and maintain a keep-out area on the first and second layers. The trace highlighted in Figure 18 is the stub. Note that a stub is not required for package types above 0201.
- The ground plane on the adjacent layer needs to be complete. Do not route any traces under the RF trace whenever possible.

- There should be no high-frequency signal traces routed close to the RF trace. The RF antenna should be placed away from high-frequency components, such as crystals, DDR, high-frequency clocks, etc. In addition, the USB port, USB-to-serial chip, UART signal lines (including traces, vias, test points, header pins, etc.) must be as far away from the antenna as possible. The UART signal line should be surrounded by ground copper and ground vias.

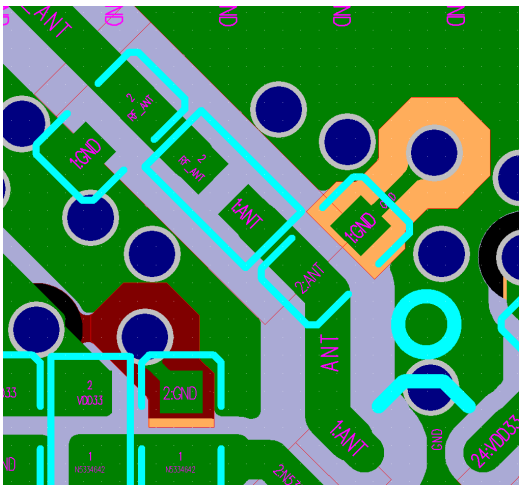

Figure 18: ESP8684 Stub in a Four-layer PCB Design

3.6 UART

The series resistor on the U0TXD trace needs to be placed close to the chip and away from the crystal. The U0TXD and U0RXD traces on the top layer should be as short as possible, surrounded by ground copper and ground vias.

3.7 Typical Layout Problems and Solutions

3.7.1 Q: The current ripple is not large, but the TX performance of RF is rather poor.

Analysis:

The current ripple has a strong impact on the RF TX performance. It should be noted that the ripple must be tested when ESP8684 is in the normal working mode. The ripple increases when the power gets high in a different mode.

Generally, the peak-to-peak value of the ripple should be <80 mV when ESP8684 sends MCS7@11n packets, and <120 mV when ESP8684 sends 11m@11b packets.

Solution:

Add a 10 μF filter capacitor to the branch of the power trace (the branch powering the chip's analog power pin). The 10 μF capacitor should be as close to the analog power pin as possible for small and stable current ripples.

3.7.2 Q: The power ripple is small, but RF TX performance is poor.

Analysis:

The RF TX performance can be affected not only by power ripples, but also by the crystal itself. Poor quality and big frequency offsets of the crystal decrease the RF TX performance. The crystal clock may be corrupted by other interfering signals, such as high-speed output or input signals. In addition, high-frequency signal traces, such as the SDIO traces and UART traces under the crystal, could also result in the malfunction of the crystal. Besides, sensitive components or radiation components, such as inductors and antennas, may also decrease the RF performance.

Solution:

This problem is caused by improper layout and can be solved by re-layout. Please see Section 3.4 for details.

3.7.3 Q: When ESP8684 sends data packages, the power value is much higher or lower than the target power value, and the EVM is relatively poor.

Analysis:

The disparity between the tested value and the target value may be due to signal reflection caused by the impedance mismatch on the transmission line connecting the RF pin and the antenna. Besides, the impedance mismatch will affect the working state of the internal PA, making the PA prematurely access the saturated region in an abnormal way. The EVM becomes poor as the signal distortion happens.

Solution:

Match the antenna's impedance with the π-type circuit on the RF trace, so that impedance of the antenna as seen from the RF pin matches closely with that of the chip. This reduces reflections to the minimum.

3.7.4 Q: TX performance is not bad, but the RX sensitivity is low.

Analysis:

Good TX performance indicates proper RF impedance matching. Poor RX sensitivity may result from external coupling to the antenna. For instance, the crystal signal harmonics could couple to the antenna. If the TX and RX traces of UART cross over with RF trace, they will affect the RX performance, as well. If there are many high-frequency interference sources on the board, signal integrity should be considered.

Solution:

Keep the antenna away from crystals. Do not route high-frequency signal traces close to the RF trace. Please see Section 3.5 for details.

4 Hardware Development

4.1 ESP8684 Modules

For a list of ESP8684 modules please check Modules section of Espressif website.

To review module reference designs please check Documentation section of Espressif website.

Notes on Using Modules

- The module uses one single pin as the power supply pin. You can connect the module to a 3.3 V power supply that can drive at least 500 mA output current. The 3.3 V power supply works both for the analog circuit and the digital circuit.
- The EN pin is used for enabling the module. Set the EN pin high for normal working mode. There is no RC delay circuit on the module. It is recommended to add an external RC delay circuit to the module. For details please refer to Section 2.2.
- Lead the GND, RXD, TXD pins out and connect them to a USB-to-UART converter for firmware download, log-printing and communication.

By default, the initial firmware has already been downloaded in the flash. If you need to download different firmware, please follow the steps below:

1. Set the module to UART Download mode by pulling IO9 (pulled up by default) low and IO8 high.
2. Power on the module and check whether the module has entered UART Download mode via serial port.
3. Download your firmware into flash using Flash Download Tool.
4. After firmware has been downloaded, pull IO9 high to enter SPI Boot mode.
5. Power on the module again. The chip will read and execute the new firmware during initialization.

Notice:

- During the whole process, you can check the status of the chip with the log printed through UART. If the firmware cannot be downloaded or executed, you can check if the working mode is normal during the chip initialization by looking at the log.
- The serial port cannot be used for both the log-print and flash-download tools simultaneously.

4.2 ESP8684 Development Boards

For a list of the latest designs of ESP8684 boards please check Development Boards section of Espressif website.

5 Hardware Design Checklist Form

To verify the compliance of your design with all the important hardware design guidelines, please refer to the checklist in *Espressif Hardware Examination Form*:
https://www.espressif.com/en/contact-us/technical-inquiries/hardware-issues

In case of doubt or discrepancy between this document and the checklist, this document shall prevail.

6 Related Documentation and Resources

Related Documentation

- ESP8684 Series Datasheet – Specifications of the ESP8684 hardware.
- ESP8684 Technical Reference Manual – Detailed information on how to use the ESP8684 memory and peripherals.
- *Certificates*
  https://espressif.com/en/support/documents/certificates
- *Documentation Updates and Update Notification Subscription*
  https://espressif.com/en/support/download/documents

Developer Zone

- *ESP-IDF* and other development frameworks on GitHub.
  https://github.com/espressif
- *ESP32 BBS Forum* – Engineer-to-Engineer (E2E) Community for Espressif products where you can post questions, share knowledge, explore ideas, and help solve problems with fellow engineers.
  https://esp32.com/
- *The ESP Journal* – Best Practices, Articles, and Notes from Espressif folks.
  https://blog.espressif.com/
- See the tabs *SDKs and Demos*, *Apps*, *Tools*, *AT Firmware*.
  https://espressif.com/en/support/download/sdks-demos

Products

- *ESP8684 Series SoCs* – Browse through all ESP8684 SoCs.
  https://espressif.com/en/products/socs?id=ESP8684
- *ESP8684 Series Modules* – Browse through all ESP8684-based modules.
  https://espressif.com/en/products/modules?id=ESP8684
- *ESP8684 Series DevKits* – Browse through all ESP8684-based devkits.
  https://espressif.com/en/products/devkits?id=ESP8684
- *ESP Product Selector* – Find an Espressif hardware product suitable for your needs by comparing or applying filters.
  https://products.espressif.com/#/product-selector?language=en

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Glossary

CLC	Capacitor-Inductor-Capacitor
DDR	Double-Data Rate
ESD	Electrostatic Discharge
GND	Ground
LC	Inductor-Capacitor
PA	Power Amplifier
RC	Resistor-Capacitor
RTC	Real-Time Clock
RX	Receive
SiP	System-in-Package
TX	Transmit
Zero-ohm resistor	A zero-ohm resistor is a placeholder on the circuit so that another higher ohm resistor can replace it, depending on design cases.

Revision History

Date	Version	Release Notes
2023-01-04	v1.4	• Updated *RTC Power Supply* • Updated *Flash* • Updated *External Clock Source (compulsory)*
2022-10-13	v1.3	Updated *RF*
2022-07-01	v1.2	• Added 26 MHz crystal • Updated *ESP8684 Schematic* • Updated *Schematic for the Analog Power Supply Pins* • Updated *Schematic for the Crystal*
2022-05-20	v1.1	Added section *RTC (optional)*
2022-05-05	v1.0	First release
2022-01-10	v0.1	Draft

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