Low Voltage Supervisory Circuit with Watchdog and Manual Reset

Features

- Precision low voltage monitoring
- 200 ms (typical) reset timeout
- Watchdog timer with 1.6 sec timeout
- Manual reset input
- Reset output stage
- Push-pull active-low
- Low power consumption: 2.2 µA
- Guaranteed reset output valid to V_{CC} = 1 V
- Power supply glitch immunity
- Specified from −40°C to +125°C
- 5-lead SOT-23 package

Applications

- Microprocessor systems
- Computers
- Controllers
- Intelligent instruments
- Portable equipment

Description

The TPV6823 is a supervisory circuit that monitors power supply voltage levels and provides a power-on reset signal.

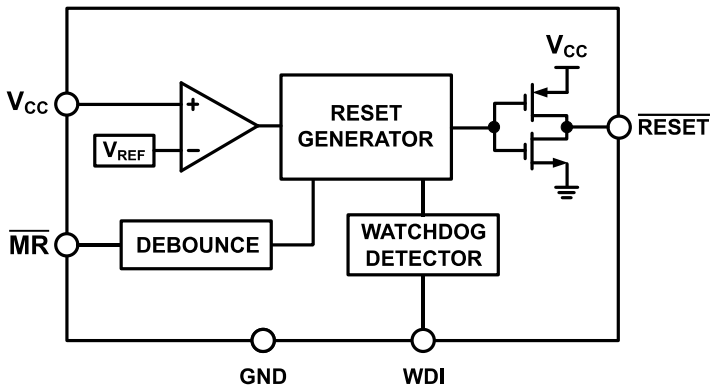
It also has on-chip watchdog timer, which can give out a reset signal if the microprocessor fails to strobe watchdog timer within a preset timeout period.

A reset signal can also be asserted by an external manual reset input.

The reset and watchdog timeout periods are fixed at 200 ms (typical) and 1.6 sec (typical), respectively.

The TPV6823 is available in a 5-lead SOT-23 package and typically consumes only 2.2 µA, suitable for use in low power, portable applications.

Typical Application Circuit



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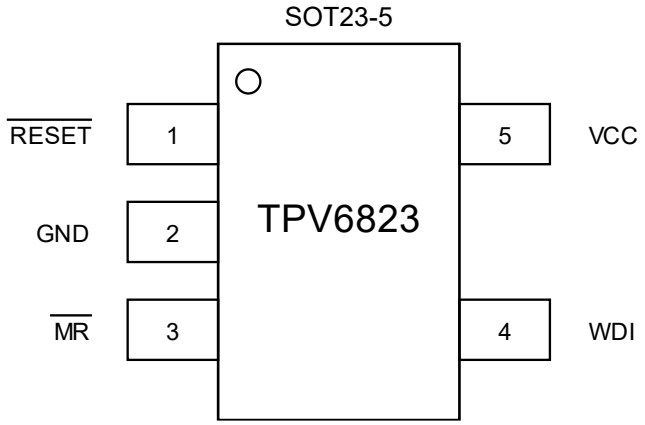
Revision History

Date	Revision	Notes
2018-12-10	Rev.A.0	First Release Version
2019-04-15	Rev.A.1	Update package POD information
2019-05-28	Rev.A.2	Add WDI pulse interval spec
2021-08-26	Rev.A.3	Update Format and add Application Note
2021-11-22	Rev.A.4	Correct POD

Pin Configuration and Functions



Pin Functions

Pin		I/O	Description
No.	Name		
1	$\overline{\text{RESET}}$	O	Active-Low Reset Push-Pull Output Stage. Asserted whenever V_{CC} is below the reset threshold, V_{TH}.
2	GND	-	Ground.
3	$\overline{\text{MR}}$	I	Manual Reset Input. This is an active-low input, which, when forced low for at least 1 μs, generates a reset. It features a 50 kΩ internal pull-up.
4	WDI	I	Watchdog Input. Generates a reset if the voltage on the pin remains low or high for the duration of the watchdog timeout. The timer is cleared if a logic transition occurs on this pin or if a reset is generated.
5	VCC	–	Power Supply Voltage Being Monitored.

Specifications

Absolute Maximum Ratings

Parameter		Min	Max	Unit
Input Voltage	VCC	−0.3	6	V
Output Current	$\overline{\text{RESET}}$		20	mA
T_J	Maximum Junction Temperature	−40	125	°C
T_{STG}	Storage Temperature Range	−65	150	°C
T_L	Lead Temperature (Soldering 10 sec)		260	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

(1) This data was taken with the JEDEC low effective thermal conductivity test board.

(2) This data was taken with the JEDEC standard multilayer test boards.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001(1)	4000	V
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002(2)	2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Electrical Characteristics

All test condition is V_{CC} = 1.53 V to 5.5 V, T_A = −40°C to +125°C, unless otherwise noted.

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
Supply Voltage and Current							
V_{CC}	VCC Operating Voltage Range			1		5.5	V
I_{CC}	Supply Current		WDI and MR unconnected (VCC=1.8V)		2.2	10	μA
			WDI and MR unconnected (VCC=5V)		6	15	μA
V_{TH}	Reset Threshold Voltage	TPV6823V		1.51	1.58	1.63	V
		TPV6823W		1.62	1.67	1.71	V
		TPV6823Y		2.12	2.19	2.25	V
		TPV6823Z		2.25	2.32	2.38	V
		TPV6823R		2.55	2.63	2.70	V
		TPV6823S		2.85	2.93	3.00	V
		TPV6823T		3.00	3.08	3.15	V
		TPV6823M		4.25	4.38	4.5	V
		TPV6823L		4.5	4.63	4.75	V
	Reset Threshold Temperature Coefficient				60		ppm/°C
V_{HYS}	Reset Threshold Hysteresis				$2\times\frac{V_{TH}}{1000}$		mV
t_{RD}	VCC To Reset Delay		V_{TH} – V_{CC} = 100mV		20		μs
t_{RP}	Reset Timeout Period			140	200	280	ms
V_{OL}	Reset Output Voltage Low (Push-Pull)		V_{CC} ≥ 1V, I_{SINK} = 50μA			0.3	V
V_{OH}	Reset Output Voltage High (Push-Pull Only)		V_{CC} ≥ 1.8V, I_{SOURCE} = 200μA	0.8 × V_{CC}			V
$\overline{MR}$ Pin							
V_{IL_MR}	Input Threshold Voltage Low for $\overline{MR}$					0.3 × V_{CC}	V
V_{IH_MR}	Input Threshold Voltage High for $\overline{MR}$			0.7 × V_{CC}			V
t_{PW_MR}	$\overline{MR}$ Input Pulse Width			1			μs
t_{GR_MR}	$\overline{MR}$ Glitch Rejection				100		ns
t_{d_MR}	$\overline{MR}$ to Reset Delay				200		ns
R_{PU_MR}	$\overline{MR}$ Pull-Up Resistance				50		kΩ

***Note:** 100% tested at T_A = 25°C.

Electrical Characteristics

All test condition is V_{CC} = 1.53 V to 5.5 V, T_A = −40°C to +125°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
WDI Pin						
t_{WD}	Watchdog Timeout Period		1.12	1.6	2.4	s
t_{PW_WD}	WDI Pulse Width 50 ns		50			ns
t_{int_WD}	WDI Pulse Interval		12			ms
V_{IL_WD}	WDI Input Threshold VIL				0.3 × V_{CC}	V
V_{IH_WD}	WDI Input Threshold VIH		0.7 × V_{CC}			V
I_{WDI}	WDI Input Current	V_{WDI} = V_{CC}		20		μA
		V_{WDI} = 0		−15		μA

***Note:** 100% tested at T_A = 25°C.

Typical Performance Characteristics

All test condition: V_{CC} = 3.3 V, T_A = +25°C, RL = 150Ω to GND, unless otherwise noted.

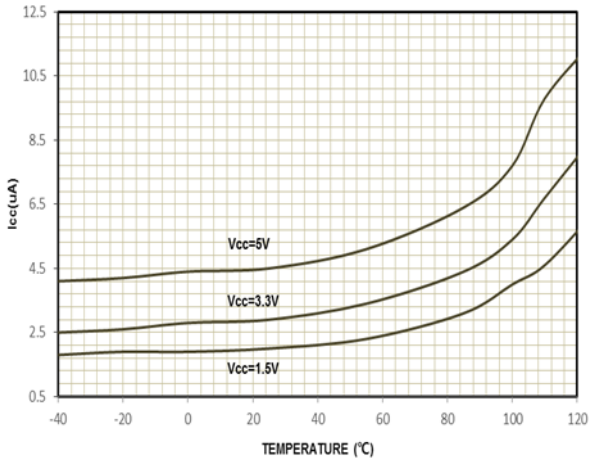


Figure 1 Supply Current vs. Temperature

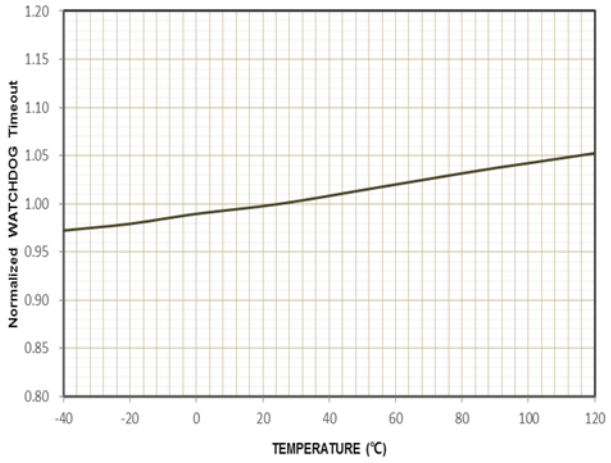


Figure 2 Normalized Watchdog Timeout Period vs. Temperature

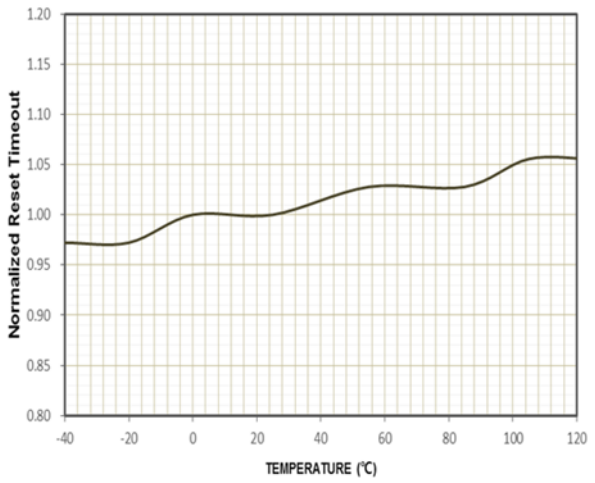


Figure 3 Normalized Reset Timeout Period vs. Temperature

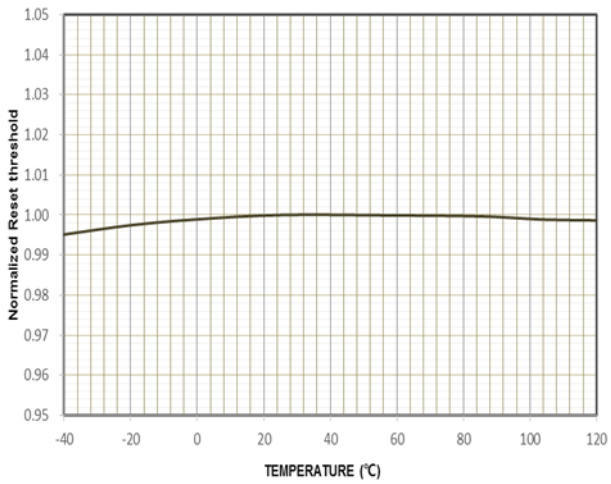


Figure 4 Normalized Reset Threshold vs Temperature

Typical Performance Characteristics (Continued)

All test condition: V_{CC} = 3.3 V, T_A = +25°C, RL = 150Ω to GND, unless otherwise noted.

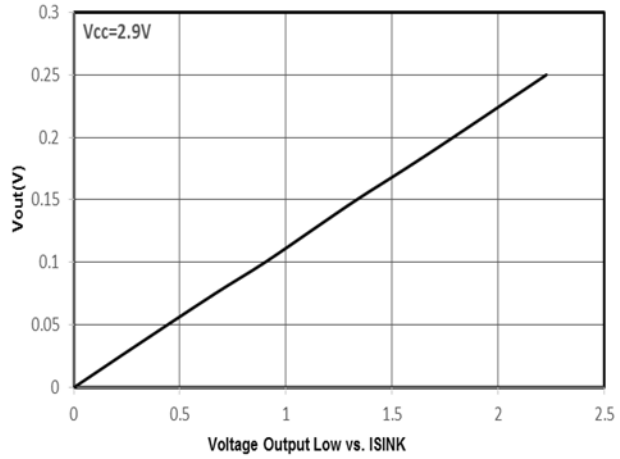


Figure 5 Voltage Output Low vs. I_{SINK}

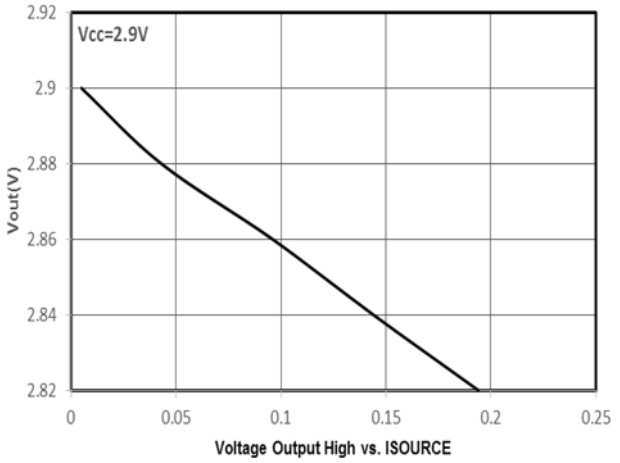


Figure 6 Voltage Output Low vs. I_{SOURCE}

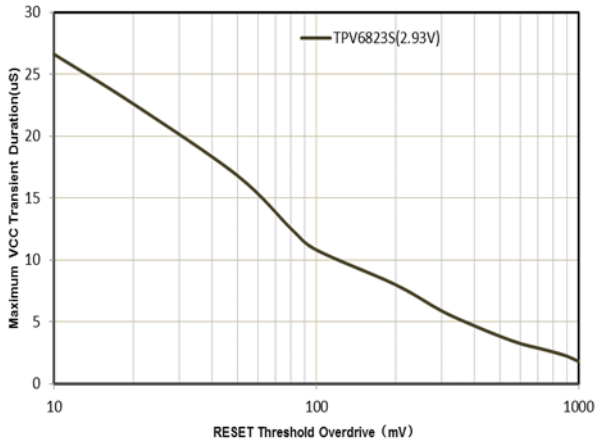


Figure 7 Maximum VCC Transient Duration vs. Reset Threshold Overdrive

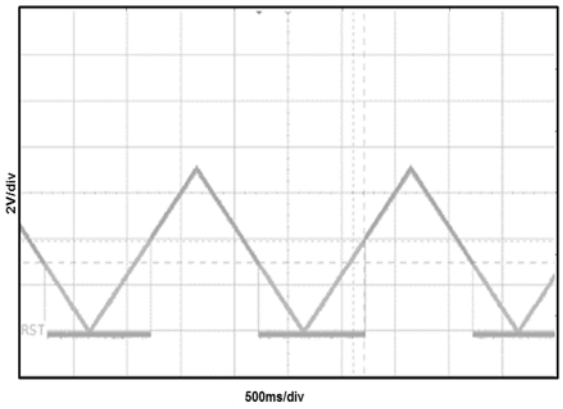


Figure 8 Reset Output Voltage vs. Supply Voltage

Detailed Description

Theory of Operation

The TPV6823 provides supply voltage supervision as well as manual reset and watchdog functions.

A reset signal is asserted when the supply voltage is below a preset threshold. In addition, the TPV6823 allows supply voltage stabilization with a fixed timeout before the reset de-asserts after the supply voltage rises above the threshold.

A watchdog timer detects if the microprocessor code breaks down or becomes stuck in an infinite loop. If this happens, the watchdog timer asserts a reset pulse, which restarts the microprocessor in a known state.

A manual reset input is available to reset the microprocessor, for example, by using an external push-button.

RESET OUTPUT

The TPV6823 features an active-low push-pull output. For active-low output, the reset signal is guaranteed to be logic low for V_{CC} down to 1 V. The reset output is asserted when V_{CC} is below the reset threshold (V_{TH}), when $\overline{MR}$ is driven low, or when WDI is not serviced within the watchdog timeout period (t_{WD}). Reset remains asserted for the duration of the reset active timeout period (t_{RP}) after V_{CC} rises above the reset threshold, after $\overline{MR}$ transitions from low to high, or after the watchdog timer times out. Figure 9 shows the reset outputs.

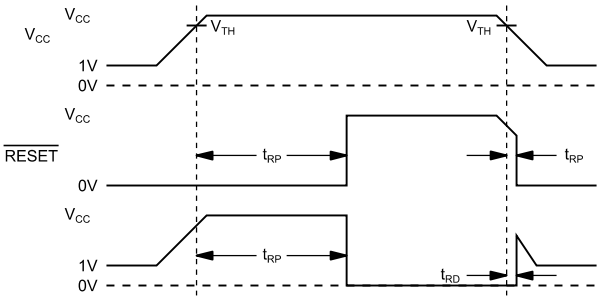


Figure 9 Reset Timing Diagram

MANUAL RESET INPUT

The TPV6823 features a manual reset input ($\overline{MR}$), which, when driven low, asserts the reset output. When $\overline{MR}$ transitions from low to high, reset remains asserted for the duration of the reset active timeout period before de-asserting.

The $\overline{MR}$ input has an internal pull-up resistor so that the input is always high when unconnected. Noise immunity is provided on the $\overline{MR}$ input, and fast, negative-going transients are ignored. A 0.1 µF capacitor between $\overline{MR}$ and ground provides additional noise immunity.

WATCHDOG INPUT

The TPV6823 features a watchdog timer, which monitors microprocessor activity. A timer circuit is cleared with every low-to-high or high-to-low logic transition on the watchdog input pin (WDI). If the timer counts through the preset watchdog timeout period (t_{WD}), reset is asserted. The microprocessor is required to toggle the WDI pin to avoid being reset.

In addition to logic transitions on WDI, the watchdog timer is also cleared by a reset assertion due to an under-voltage condition on V_{CC} or $\overline{MR}$ being pulled low. When reset is asserted, the watchdog timer is cleared and does not begin counting again until reset de-asserts. The watchdog timer can be disabled by leaving WDI

floating or by three-stating the WDI driver.

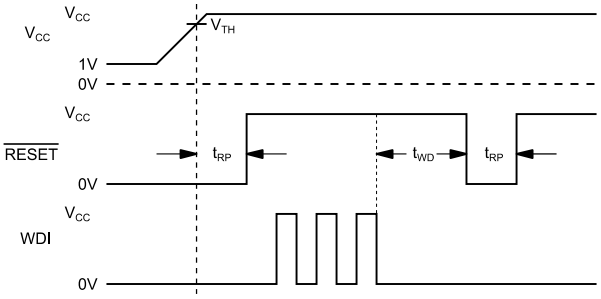


Figure 10 Watchdog Timing Diagram

Application Note

Power up/down Restriction:

When power supply ramps up very slow at high temperature, there may be a certain percentage of the chips are probabilistic abnormal (With abnormal current appears around 0.6V, internal LDO is pulled down, and then the $\overline{\text{RESET}}$ output is incorrect). Through simulation and experiment, certain requirements of power supply up and down should be followed to avoid this kind of issue.

The requirements are shown in Figure 11:

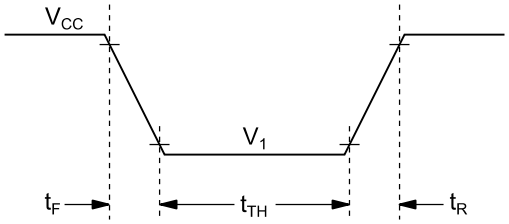


Figure 11 Power Supply Requirements

1. V_1 < 200mV
2. t_{TH} > 40ms,
3. t_R > 0.2V/ms
4. In power up duration (t_R), Ripple or noise on V_{CC} should be < 100mV

WDI Restriction:

If WDI is kept to be low or high longer than t_{WD} then the $\overline{\text{RESET}}$ signal is triggered to be low. Only in this case, if WDI is toggled when $\overline{\text{RESET}}$ is low, the $\overline{\text{RESET}}$ will be kept low, until WDI is not toggled and kept to be low or high longer than t_{RP}, and then $\overline{\text{RESET}}$ will recover to high again.

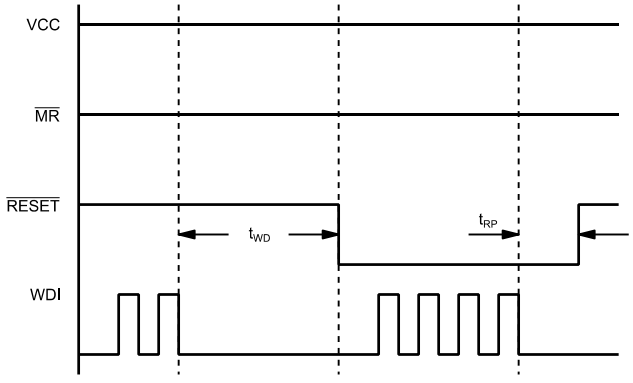
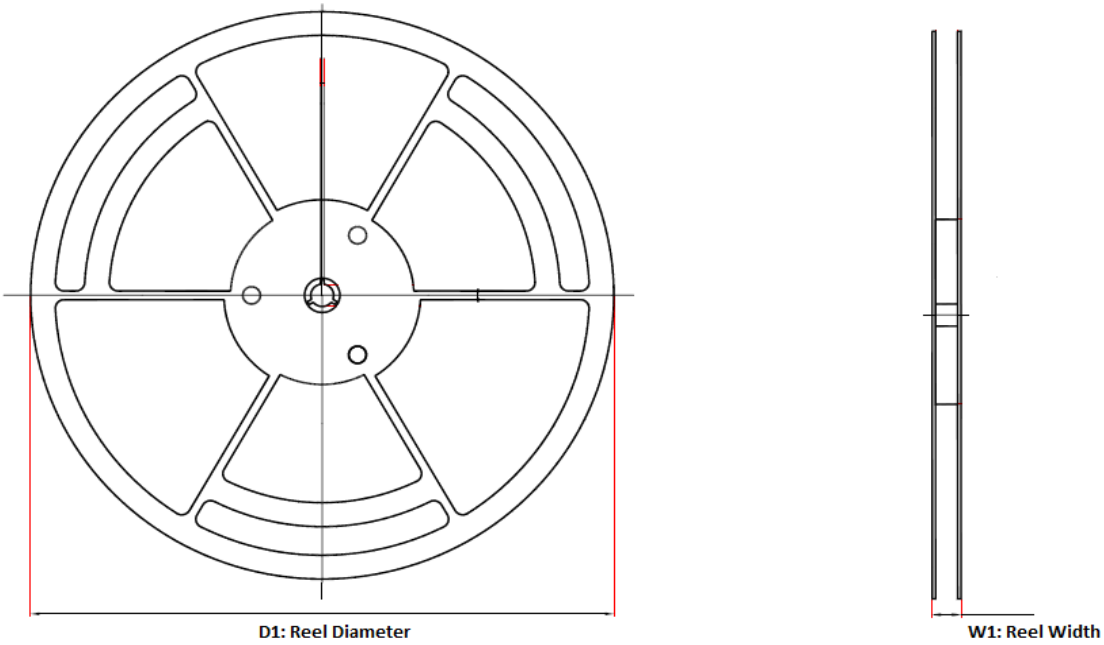


Figure 12 Watchdog Requirements

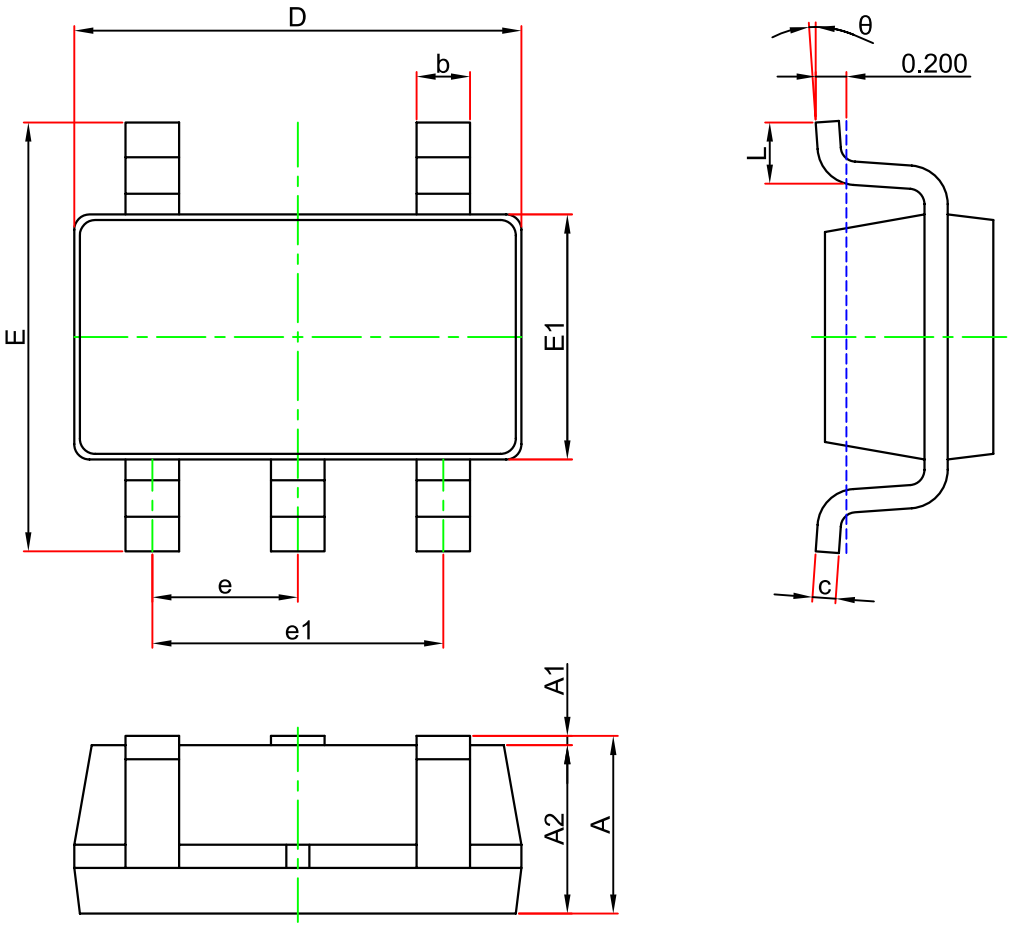
Tape and Reel Information



Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPV6823V-TR	SOT23-5	180	13.1	3.2	3.2	1.4	4	8	Q3
TPV6823W-TR	SOT23-5	180	13.1	3.2	3.2	1.4	4	8	Q3
TPV6823Y-TR	SOT23-5	180	13.1	3.2	3.2	1.4	4	8	Q3
TPV6823Z-TR	SOT23-5	180	13.1	3.2	3.2	1.4	4	8	Q3
TPV6823R-TR	SOT23-5	180	13.1	3.2	3.2	1.4	4	8	Q3
TPV6823S-TR	SOT23-5	180	13.1	3.2	3.2	1.4	4	8	Q3
TPV6823T-TR	SOT23-5	180	13.1	3.2	3.2	1.4	4	8	Q3
TPV6823M-TR	SOT23-5	180	13.1	3.2	3.2	1.4	4	8	Q3
TPV6823L-TR	SOT23-5	180	13.1	3.2	3.2	1.4	4	8	Q3

Package Outline Dimensions

SOT23-5



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E1	1.500	1.700	0.059	0.067
E	2.650	2.950	0.104	0.116
e	0.950 (BSC)		0.037 (BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transpor Quar
TPV6823V-TR	−40°C to 125°C	SOT23-5	V1V	1	Tape and R
TPV6823W-TR	−40°C to 125°C	SOT23-5	V1W	1	Tape and R
TPV6823Y-TR	−40°C to 125°C	SOT23-5	V1Y	1	Tape and R
TPV6823Z-TR	−40°C to 125°C	SOT23-5	V1Z	1	Tape and R
TPV6823R-TR	−40°C to 125°C	SOT23-5	V1R	1	Tape and R
TPV6823S-TR	−40°C to 125°C	SOT23-5	V1S	1	Tape and R
TPV6823T-TR	−40°C to 125°C	SOT23-5	V1T	1	Tape and R
TPV6823M-TR	−40°C to 125°C	SOT23-5	V1M	1	Tape and R
TPV6823L-TR	−40°C to 125°C	SOT23-5	V1L	1	Tape and R

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.