TL103Wx Dual Operational Amplifiers With Internal Reference

1 Features

- New TL103WB, a pin-compatible upgrade to the TL103W and TL103WA
- Improved specifications of B version amplifiers:
  - Supply range: 3 V to 36 V
  - Low maximum input offset voltage: ±3 mV (25°C) and ±4 mV (full temperature)
  - Gain bandwidth: 1.2 MHz
  - Total supply current: 600 µA
  - EMI rejection: integrated RF and EMI filter
  - Temperature range: -40°C to 125°C
- Improved specifications of B version reference:
  - Fixed 2.5-V reference
  - Tight tolerance maximum of 0.4% (25°C) and 0.8% (full temperature)
  - Wide sink-current range: 0.5 mA (typical) to 100 mA

2 Applications

- Battery chargers
- Switch-mode power supplies
- Linear voltage regulation
- Data-acquisition systems

3 Description

The TL103Wx devices combine the building blocks of a dual operational amplifier and a fixed voltage reference – both of which are often used in the control circuitry of both switch-mode and linear power supplies. OP AMP1 has its non-inverting input internally tied to a fixed 2.5-V reference, while OP AMP2 is independent, with both inputs uncommitted.

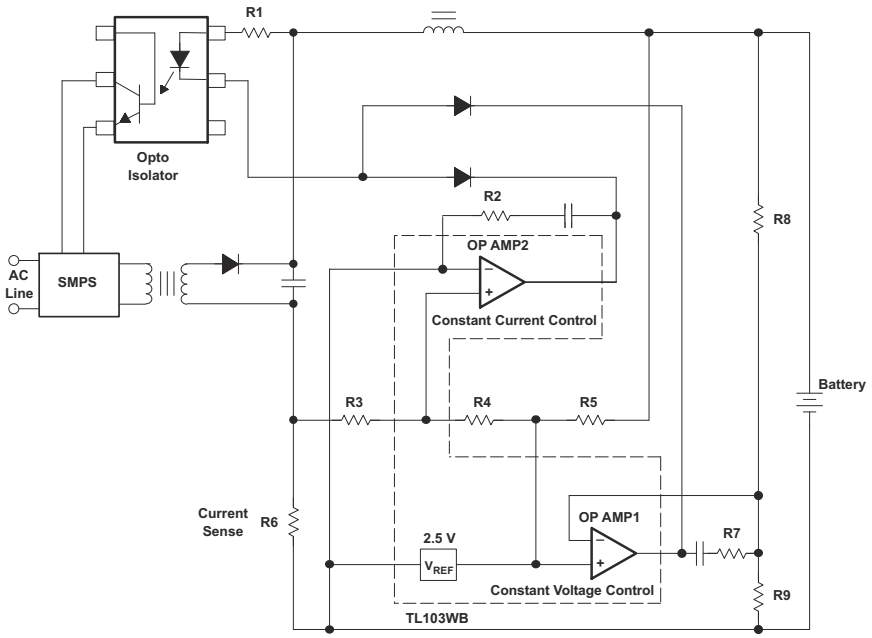
The upgraded TL103WB features improvements such as a wider supply range (up to 36 V), lower supply current (300 µA) and tighter voltage regulation. This regulation can be achieved through low offset voltages for both operational amplifiers (0.3 mV typical) and tight tolerances for the voltage reference (0.4% at 25°C and 0.8% over operating temperature range).

The TL103WB has a widened temperature range of –40°C to 125°C.

Device Information

PART NUMBER	CHANNEL COUNT	PACKAGE(1)	PACKAGE SIZE(3)
TL103W TL103WA TL103WB	Dual + Reference	D (SOIC, 8)(2)	4.9 mm × 6 mm
		DDF (SOT-23, 8) (2)	2.9 mm × 2.8 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) This package is preview only.
(3) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application Circuit

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision M (October 2016) to Revision N (August 2023) — **Page**

- Updated *Features* section to highlight TL103WB....1
- Updated the numbering format for tables, figures, and cross-references throughout the document....1
- Added the *TL103WB* device information throughout the document....1
- Updated *Description* section....1
- Updated *Device Information* table to include channel count....1
- Removed DRJ package details and added DDF package for preview....3
- Updated formatting for *Electrical Characteristics* tables....5
- Updated typical dynamic impedance from 0.2 Ω to 0.4 Ω in *Electrical Characteristics* tables....5

Changes from Revision L (February 2016) to Revision M (October 2016) — **Page**

- Changed positive and negative terminals OP AMP 2 in the D Package image of *Pin Configuration and Functions*....3

Changes from Revision K (October 2010) to Revision L (February 2016) — **Page**

- Added the *Device Information* table, *Pin Configuration and Functions*, *ESD Ratings*, *Thermal Information*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections....1
- Changed *Features* from: 2 kV ESD Protection (HBM) to: 2.5-kV ESD Protection (HBM)....1
- Changed the Zener diode component to V_{REF} in the *Typical Application Circuit*....1
- Changed the Zener diode component to V_{REF} in the D Package of *Pin Configuration and Functions*....3

5 Pin Configuration and Functions

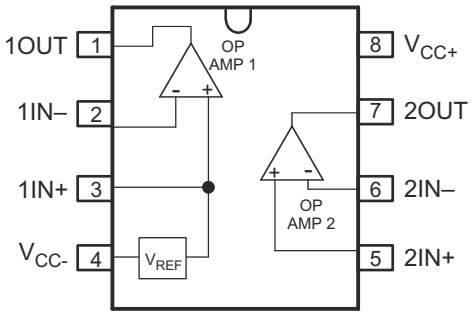


Figure 5-1. D and DDF Packages, 8-Pin SOIC and SOT-23-THN (Top View)

Table 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
1OUT	1	O	Opamp 1 output
1IN–	2	I	Opamp 1 inverting input
1IN+	3	I	Opamp 1 non-inverting input and Shunt reference cathode terminal
$V_{CC–}$	4	I	Negative Supply Voltage
2IN+	5	I	Opamp 2 non-inverting input
2IN–	6	I	Opamp 2 inverting input
2OUT	7	O	Opamp 2 output
V_{CC+}	8	I	Positive Supply Voltage

(1) I = input, O = output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
$V_{CC±}$	Supply voltage	TL103W/TL103WA	0	36	V
		TL103WB	0	40	
V_{ID}	Operational amplifier input differential voltage			36	V
V_I	Operational amplifier input voltage range	TL103W/TL103WA	-0.3	36	V
		TL103WB	-0.3	40	
I_{KA}	Voltage reference cathode current			100	mA
T_J	Maximum junction temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
$V_{CC±}$	Supply voltage	TL103W/TL103WA	3	32	V
		TL103WB	3	36	
V_{ICR}	Input common-mode voltage range		V_{CC-}	(V_{CC+}) - 2	V
I_K	Cathode current		1	100	mA
T_A	Operating free-air temperature	TL103W/TL103WA	–40	105	°C
		TL103WB	–40	125	

6.4 Thermal Information

THERMAL METRIC(1)		TL103Wx D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	97	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics: OP AMP1 (V_{REF} at Non-Inverting Input)

V_{CC+} = 5 V, V_{CC-} = GND, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			T_A	MIN	TYP	MAX	UNIT
AMPLIFIER									
V_{IO}	Input offset voltage	V_{ICM} = 0 V		TL103W			±1	±4	mV
					Full range			±5	
				TL103WA			±0.5	±3.0	
					Full range			±5	
				TL103WB			±0.3	±3.0	
					Full range			±4	
αV_{IO}	Input offset-voltage drift			TL103W/TL103WA	Full range		±7		µV/°C
				TL103WB	Full range		±3.5		
I_{IB}	Input bias current (negative input)			TL103W/TL103WA			±20		nA
				TL103WB			±10		
A_{VD}	Large-signal voltage gain	V_{CC+} = 15 V, R_L = 2 kΩ, V_{ICM} = 0 V		TL103W/TL103WA			100		V/mV
				TL103WB			140		
k_{SVR}	Supply-voltage rejection ratio	V_{CC+} = 5 V to 30 V, V_{ICM} = 0 V		TL103W/TL103WA		65	100		dB
				TL103WB		80	114		
I_O	Output current	V_{CC+} = 15 V, V_O = 2 V, V_{ID} = 1 V	Source(1)			20	40		mA
			Sink(1)			10	12		
		V_{CC+} = 15 V, V_O = 0.2 V, V_{ID} = -1 V	Sink(1)	TL103W/TL103WA		12	50		µA
				TL103WB		60	100		
I_{SC}	Short-circuit to GND	V_{CC+} = 15 V					±40	±60	mA
V_O	Voltage output swing from rail	V_{CC+} = 30 V, R_L = 2 kΩ	Positive Rail (V_{CC+})	TL103W/TL103WA		26	27		V
					Full range	26			
				TL103WB		27.4	28.4		
					Full range	27.4			
		V_{CC+} = 30 V, R_L = 10 kΩ	Positive Rail (V_{CC+})	TL103W/TL103WA		27	28		
					Full range	27			
				TL103WB		27.6	28.6		
					Full range	27.6			
			Negative Rail (V_{CC-})				5	20	mV
					Full range			20	
SR	Slew rate at unity gain	V_{CC+} = 15 V, C_L = 100 pF, R_L = 2 kΩ, V_I = 0.5 V to 2 V, unity gain		TL103W/TL103WA		0.2	0.4		V/µs
				TL103WB		0.2	0.5		
GBW	Gain bandwidth product	V_{CC+} = 30 V, V_I = 10 mV, C_L = 100 pF, R_L = 2 kΩ, f = 100 kHz		TL103W/TL103WA		0.5	0.9		MHz
				TL103WB		0.5	1.2		
THD	Total harmonic distortion	V_{CC+} = 30 V, V_O = 2 V_{PP}, C_L = 100 pF, R_L = 2 kΩ, f = 1 kHz, A_V = 20 dB		TL103W/TL103WA			0.02		%
				TL103WB			TBD		
I_{CC}	Total supply current, excluding cathode-current reference (both amplifiers)	V_{CC+} = 5 V, no load		TL103W/TL103WA			0.7	1.2	mA
		V_{CC+} = 30 V, no load			Full range			2	
		V_{CC+} = 5 V, no load		TL103WB			0.6	0.92	
		V_{CC+} = 30 V, no load			Full range			1.6	
VOLTAGE REFERENCE									
V_{ref}	Reference Voltage	I_K = 10 mA		TL103W		2.482	2.5	2.518	V
					Full Range	2.465		2.535	V
				TL103WA/TL103WB		2.49	2.5	2.51	V
					Full Range	2.48		2.52	V
ΔV_{ref}	Reference input voltage deviation over temperature range	I_K = 10 mA			Full Range		7	30	mV
I_{min}	Minimum cathode current for regulation						0.5	1	mA
$\|Z_{KA}\|$	Dynamic impedance	I_{KA} = 1 mA to 100 mA, f < 1 kHz					0.4	0.5	Ω

(1) Specified by characterization only

6.6 Electrical Characteristics: OP AMP2 (Independent Amplifier)

V_{CC+} = 5 V, V_{CC-} = GND, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{ICM} = 0 V		TL103W			±1	±4	mV
					Full range			±5	
				TL103WA			±0.5	±3.0	
					Full range			±5	
				TL103WB			±0.3	±3.0	
					Full range			±4	
αV_{IO}	Input offset-voltage drift			TL103W/TL103WA	Full range		±7		µV/°C
				TL103WB	Full range		±3.5		
I_{IO}	Input offset current			TL103W/TL103WA			±2	±75	nA
					Full range			±150	
				TL103WB			±0.5	±4	
					Full range			±5	
I_{IB}	Input bias current			TL103W/TL103WA			±20	±150	nA
					Full range			±200	
				TL103WB			±10	±10	
					Full range			±50	
A_{VD}	Large-signal voltage gain	V_{CC+} = 15 V, R_L = 2 kΩ, VO = 1.4 V to 11.4 V		TL103W/TL103WA		50	100		V/mV
						25	100		
				TL103WB		70	140		
						35	140		
k_{SVR}	Supply-voltage rejection ratio	V_{CC+} = 5 V to 30 V		TL103W/TL103WA		65	100		dB
				TL103WB		80	114		
V_{ICR}	Input common-mode voltage range	V_{CC+} = 30 V				V_{CC-}		(V_{CC+}) – 1.5	V
					Full range	V_{CC-}		(V_{CC+}) – 2	
CMRR	Common-mode rejection ratio	V_{CC+} = 30 V		TL103W/TL103WA		70	85		dB
					Full range	60			
I_O	Output current	V_{CC+} = 15 V, V_O = 2 V	Source, V_{ID} = 1 V[1]			20	40		mA
			Sink, V_{ID} = -1 V[1]			10	12		
		V_{CC+} = 15 V, V_O = 0.2 V, V_{ID} = -1 V	Sink[1]	TL103W/TL103WA		12	50		µA
				TL103WB		60	100		
I_{SC}	Short-circuit to GND	V_{CC+} = 15 V					±40	±60	mA
V_O	Voltage output swing from rail	V_{CC+} = 30 V, R_L = 2 kΩ	Positive Rail (V_{CC+})	TL103W/TL103WA		26	27		V
					Full range	26			
				TL103WB		27.4	28.4		
					Full range	27.4			
		V_{CC+} = 30 V, R_L = 10 kΩ	Positive Rail (V_{CC+})	TL103W/TL103WA		27	28		
					Full range	27			
				TL103WB		27.6	28.6		
					Full range	27.6			
			Negative Rail (V_{CC-})				5	20	mV
					Full range			20	
SR	Slew rate at unity gain	V_{CC+} = 15 V, C_L = 100 pF, R_L = 2 kΩ, V_I = 0.5 V to 2 V, unity gain		TL103W/TL103WA		0.2	0.4		V/µs
				TL103WB		0.2	0.5		
GBW	Gain bandwidth product	V_{CC+} = 30 V, V_I = 10 mV, C_L = 100 pF, R_L = 2 kΩ, f = 100 kHz		TL103W/TL103WA		0.5	0.9		MHz
				TL103WB		0.5	1.2		
THD	Total harmonic distortion	V_{CC+} = 30 V, V_O = 2 V_{PP}, C_L = 100 pF, R_L = 2 kΩ, f = 1 kHz, A_V = 20 dB		TL103W/TL103WA			0.02		%
				TL103WB			TBD		
V_n	Equivalent input noise voltage	V_{CC+} = 30 V, R_S = 100 Ω, f = 1 kHz		TL103W/TL103WA			50		nV/√Hz
				TL103WB			38		

6.6 Electrical Characteristics: OP AMP2 (Independent Amplifier) (continued)

V_{CC+} = 5 V, V_{CC-} = GND, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
I_{CC}	Total supply current, excluding cathode-current reference (both amplifiers)	V_{CC+} = 5 V, no load	TL103W/TL103WA			0.7	1.2	mA
		V_{CC+} = 30 V, no load		Full range			2	
		V_{CC+} = 5 V, no load	TL103WB			0.6	0.92	
		V_{CC+} = 30 V, no load		Full range			1.6	

(1) Specified by characterization only

6.7 Typical Characteristics: TL103WB

at $T_A \cong 25°C$, V_{CC} = 36 V (±18 V), $V_{CM} = V_{CC} / 2$, R_{LOAD} = 10 kΩ connected to $V_{CC} / 2$ (unless otherwise noted)

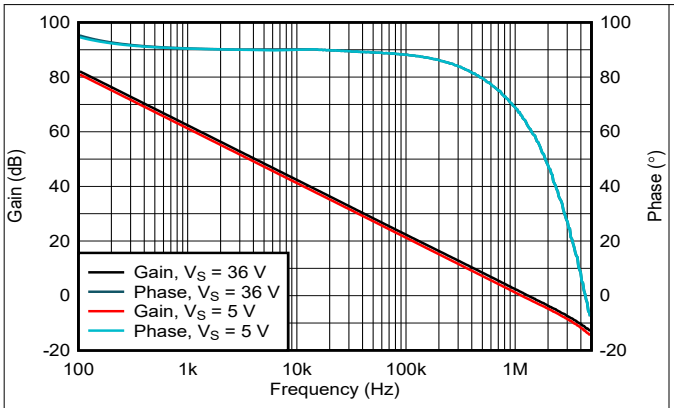


Figure 6-1. Open-Loop Gain and Phase vs Frequency

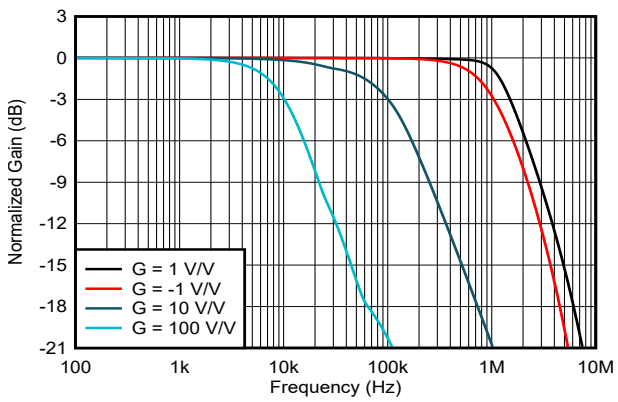


Figure 6-2. Closed-Loop Gain vs Frequency

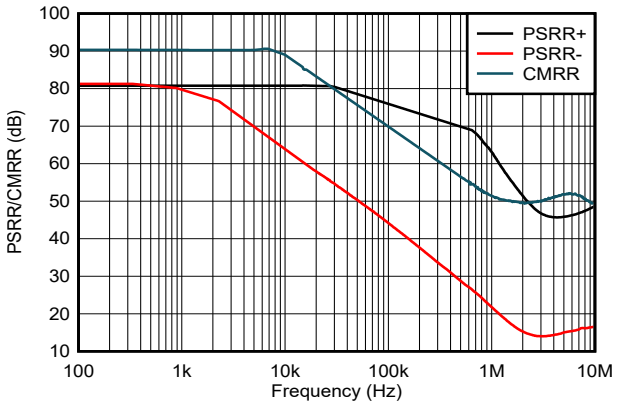


Figure 6-3. CMRR and PSRR vs Frequency

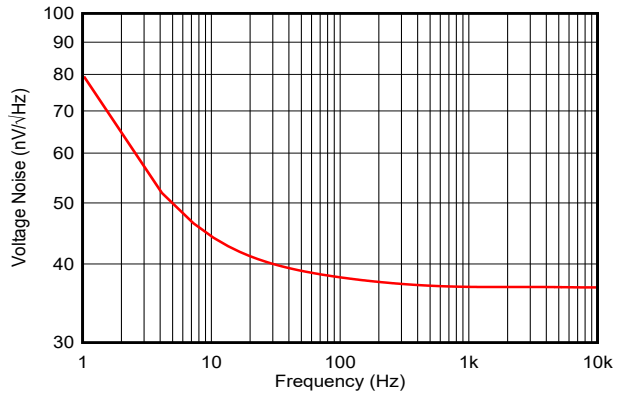


Figure 6-4. Input Voltage Noise Spectral Density vs Frequency

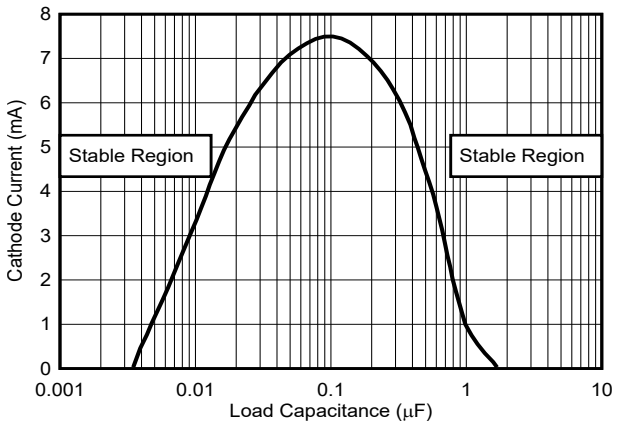


Figure 6-5. Reference Stability vs Capacitive Load

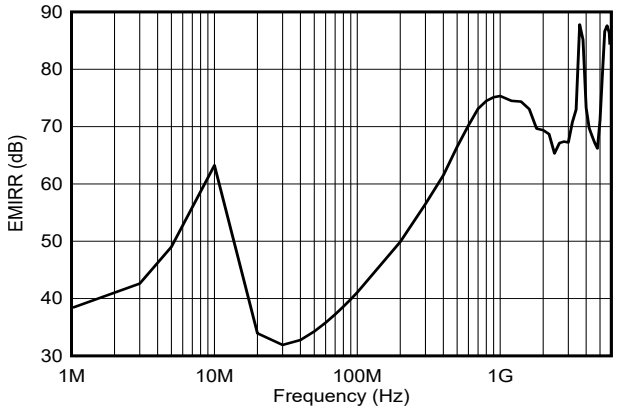


Figure 6-6. EMIRR (Electromagnetic Interference Rejection Ratio) vs Frequency

7 Device and Documentation Support

7.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

7.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

7.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL103WAID	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	Z103WA	
TL103WAIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	Z103WA	Samples
TL103WID	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	Z103W	
TL103WIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	Z103W	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

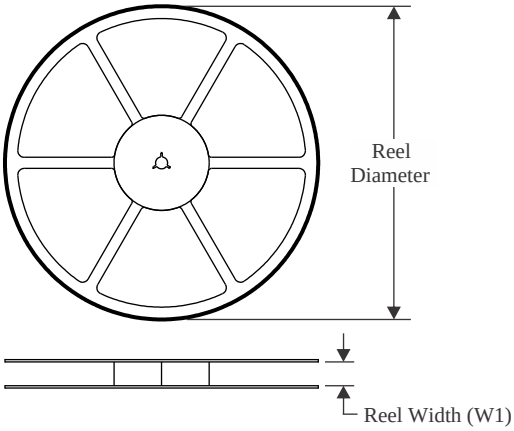
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

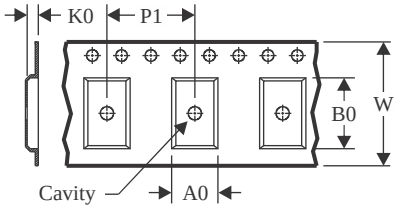
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

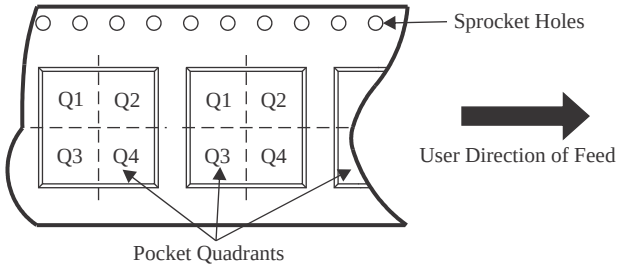


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

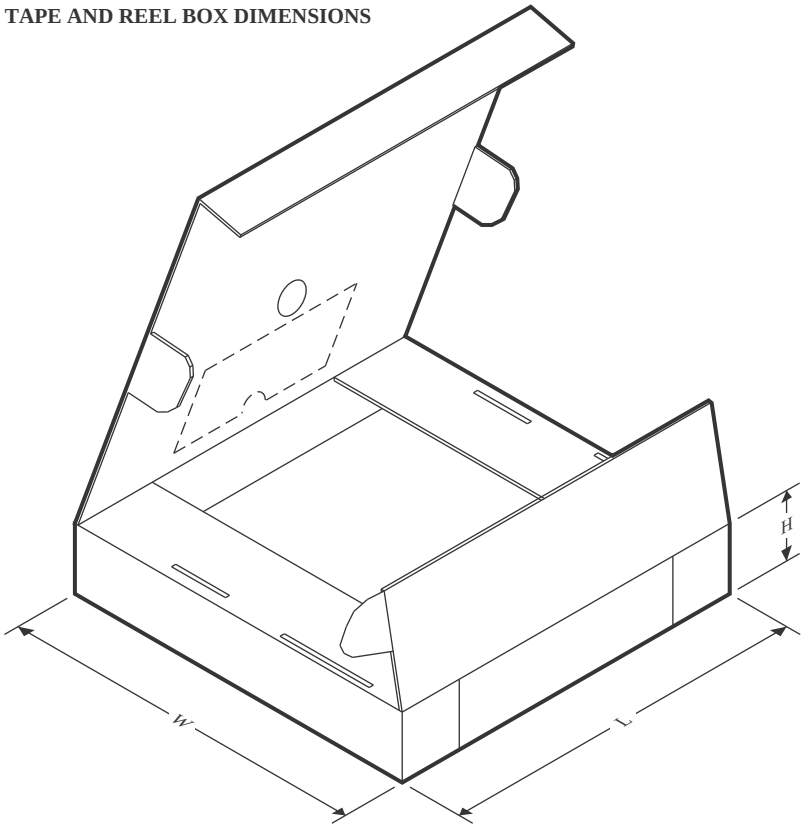
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL103WAIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL103WIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

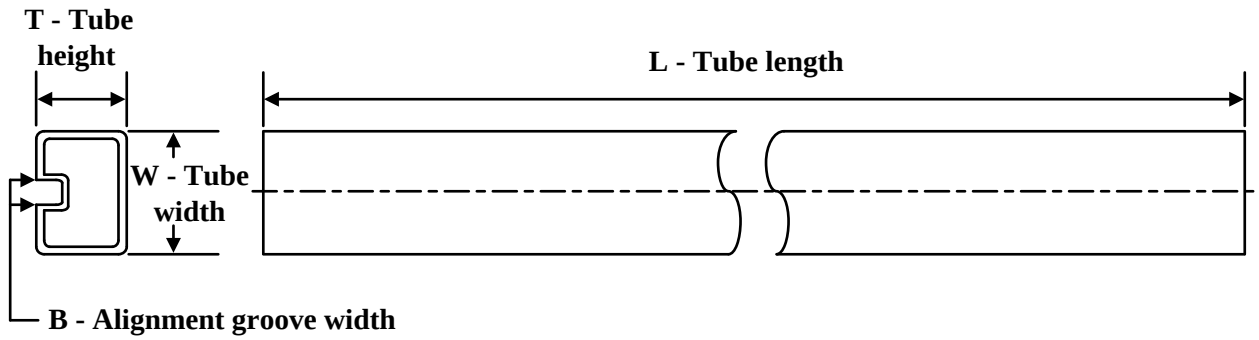
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

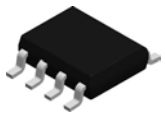
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL103WAIDR	SOIC	D	8	2500	340.5	336.1	25.0
TL103WIDR	SOIC	D	8	2500	340.5	336.1	25.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TL103WAID	D	SOIC	8	75	507	8	3940	4.32
TL103WID	D	SOIC	8	75	507	8	3940	4.32

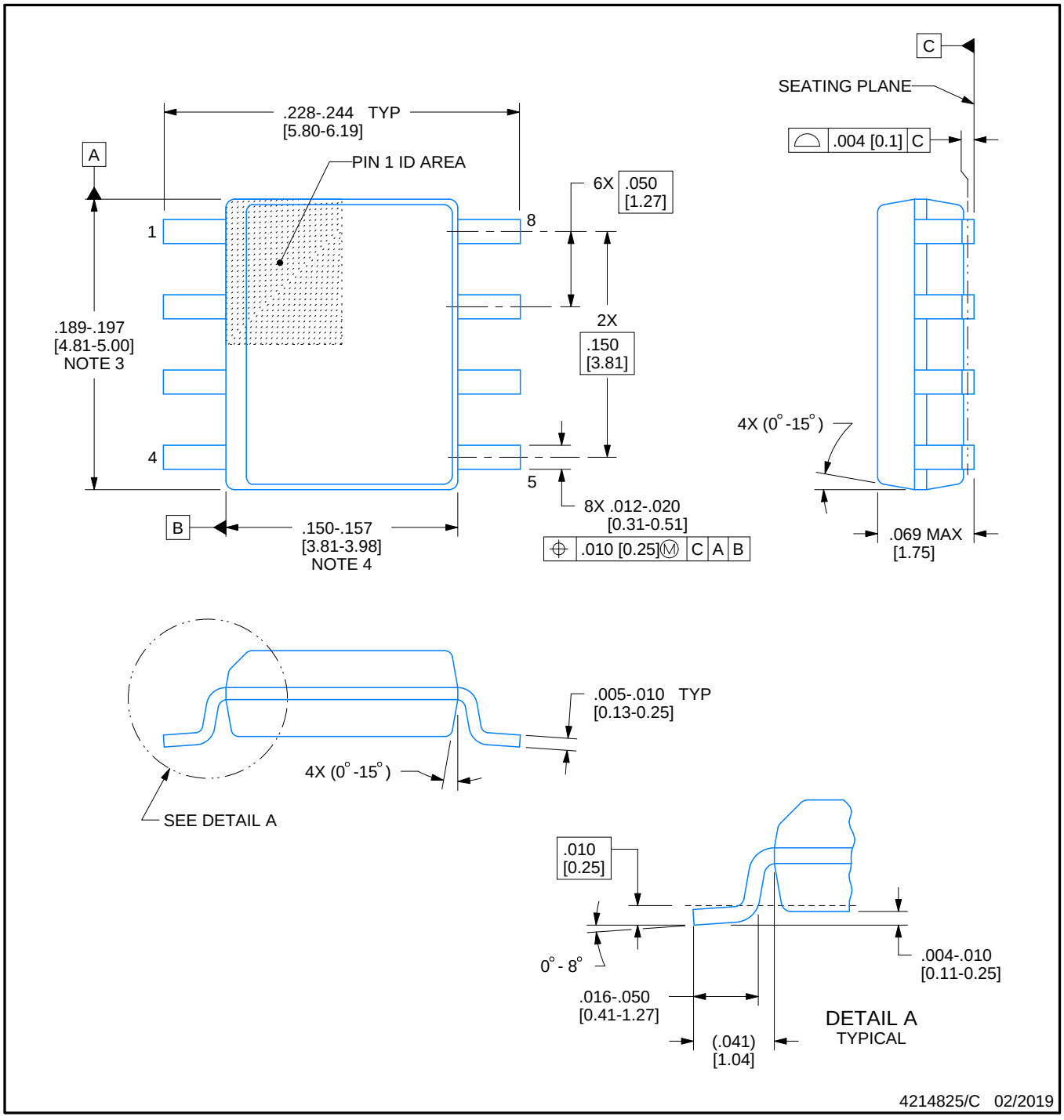


PACKAGE OUTLINE

D0008A

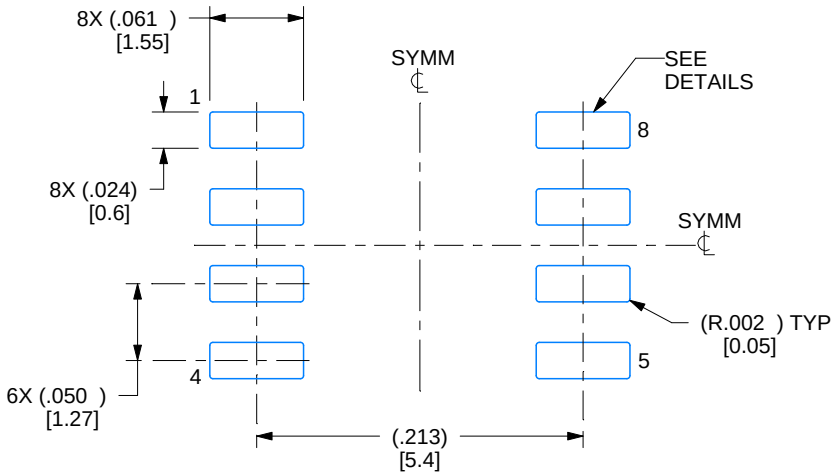
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

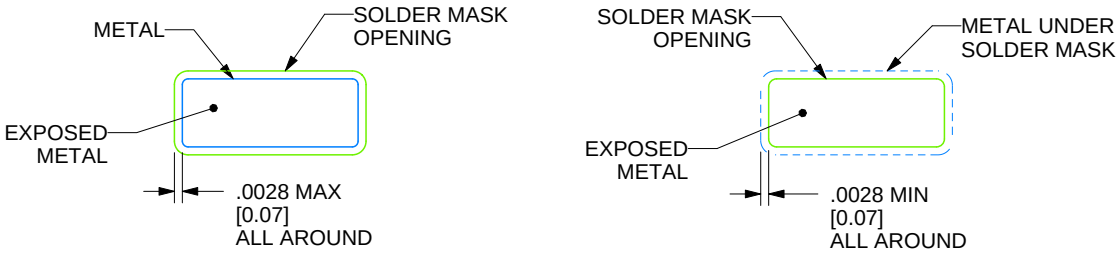


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

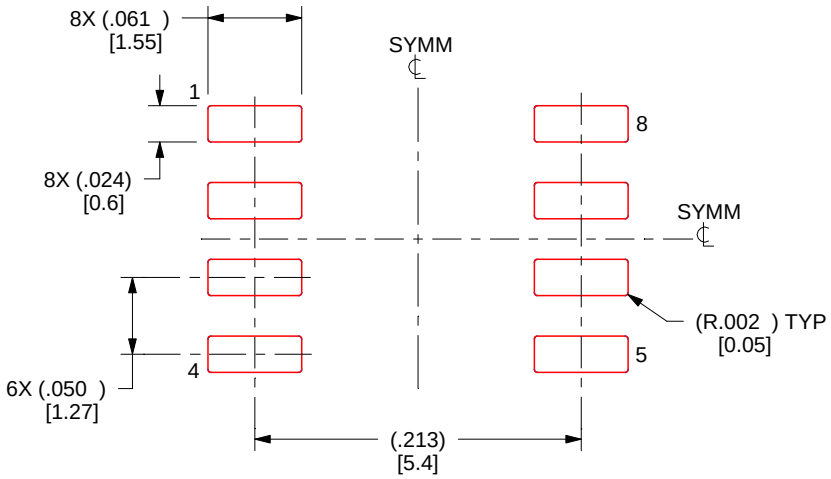
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265