ONET8501PB 11.3-Gbps Rate-Selectable Limiting Amplifier

1 Features

- Up to 11.3-Gbps Operation
- 2-Wire Digital Interface
- Digitally Selectable Input Bandwidth
- Adjustable LOS Threshold
- Digitally Selectable Output Voltage
- Digitally Selectable Output Preemphasis
- Adjustable Input Threshold Voltage
- Low Power Consumption
- Input Offset Cancellation
- CML Data Outputs With On-Chip 50-Ω Back-Termination to VCC
- Single 3.3-V Supply
- Output Disable
- Surface Mount Small Footprint 3-mm × 3-mm, 16-Pin, RoHS compliant VQFN Package

2 Applications

- 10-Gigabit Ethernet Optical Receivers
- 2x, 4x, 8x, and 10x Fiber Channel Optical Receivers
- SONET OC-192/SDH-64 Optical Receivers
- SFP+ and XFP Transceiver Modules
- XENPAK, XPAK, X2, and 300-Pin MSA Transponder Modules
- Cable Drivers and Receivers

3 Description

The ONET8501PB device is a high-speed, 3.3-V limiting amplifier for multiple fiber optic and copper cable applications with data rates from 2 Gbps up to 11.3 Gbps.

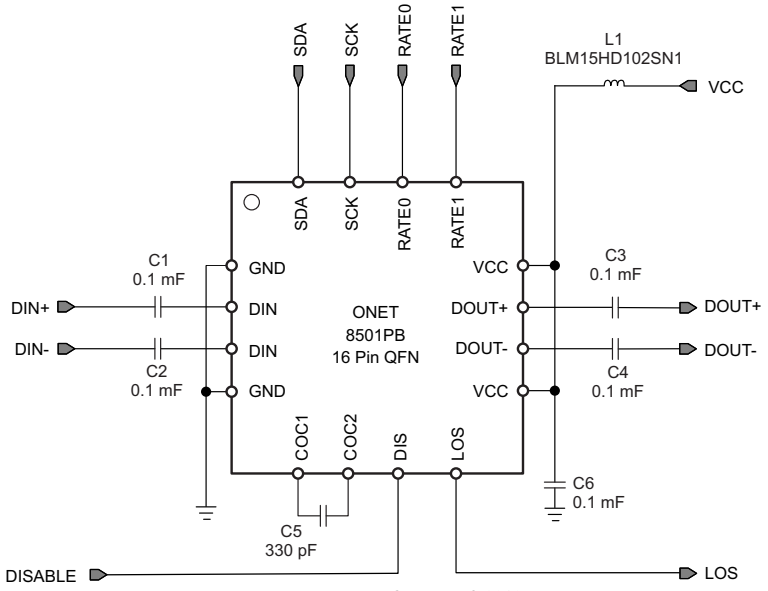
The device provides a two-wire serial interface which allows digital control of the bandwidth, output amplitude, output preemphasis, input threshold voltage (slice level), and the loss of signal assert level. Predetermined settings for bandwidth and LOS assert levels can also be selected with external rate selection pins.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ONET8501PB	VQFN (16)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuit



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4 Revision History

Changes from Original (July 2008) to Revision A **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

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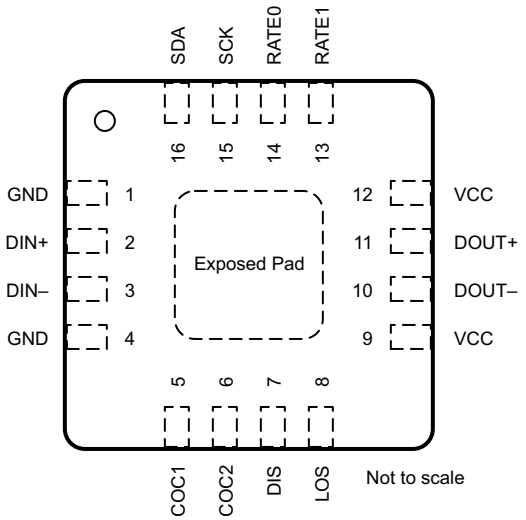
5 Description (continued)

The ONET8501PB provides a gain of about 34 dB which ensures a fully differential output swing for input signals as low as 20 mV_{pp}. The output amplitude can be adjusted to 350 mV_{pp}, 650 mV_{pp}, or 850 mV_{pp}. To compensate for frequency-dependent loss of microstrips or striplines connected to the output of the device, programmable preemphasis is included in the output stage. A settable loss of signal detection and output disable are also provided.

The device, available in RoHS compliant small footprint 3-mm × 3-mm, 16-pin VQFN package, typically dissipates less than 170 mW and is characterized for operation from –40°C to 100°C.

6 Pin Configuration and Functions

RGT Package
16-Pin VQFN
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
COC1	5	Analog	Offset cancellation filter capacitor plus terminal. An external capacitor can be connected between this pin and COC2 to reduce the low frequency cutoff. To disable the offset cancellation loop, connect COC1 and COC2 together.
COC2	6	Analog	Offset cancellation filter capacitor minus terminal. An external capacitor can be connected between this pin and COC1 to reduce the low frequency cutoff. To disable the offset cancellation loop, connect COC1 and COC2 together.
DIN+	2	Analog-input	Noninverted data input. Differentially 100 Ω terminated to DIN–.
DIN–	3	Analog-input	Inverted data input. Differentially 100 Ω terminated to DIN+.
DIS	7	Digital-input	Disables the output stage when set to a high level.
DOUT–	10	CML-out	Inverted data output. On-chip 50 Ω back-terminated to VCC.
DOUT+	11	CML-out	Noninverted data output. On-chip 50 Ω back-terminated to VCC.
GND	1,4, EP	Supply	Circuit ground. Exposed die pad (EP) must be grounded.
LOS	8	Open-drain MOS	High level indicates that the input signal amplitude is below the programmed threshold level. Open-drain output. Requires an external 10-kΩ pullup resistor to VCC for proper operation.
RATE1	13	Digital-input	Bandwidth selection for noise suppression.
RATE0	14	Digital-input	Bandwidth selection for noise suppression.
SCK	15	Digital-input	Serial interface clock input. Connect a pullup resistor (10 kΩ typical) to VCC.
SDA	16	Digital-input	Serial interface data input. Connect a pullup resistor (10 kΩ typical) to VCC.
VCC	9, 12	Supply	3.3-V ± 10% supply voltage.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage(2)	–0.3	4	V
V_{DIN+}, $V_{DIN–}$	Voltage at DIN+, DIN–(2)	0.5	4	V
V_{LOS}, V_{COC1}, V_{COC2}, V_{DOUT+}, $V_{DOUT–}$, V_{DIS}, V_{RATE0}, V_{RATE1}, V_{SDA}, V_{SCK}	Voltage at LOS, COC1, COC2, DOUT+, DOUT–, DIS, RATE0, RATE1, SDA, SCK(2)	–0.3	4	V
$V_{DIN,DIFF}$	Differential voltage between DIN+ and DIN–		±2.5	V
I_{DIN+}, $I_{DIN–}$, I_{DOUT+}, $I_{DOUT–}$	Continuous current at inputs and outputs		25	mA
T_{LEAD}	Lead temperature 1.6mm (1/16 inch) from case for 10 s		260	°C
T_A	Characterized free-air operating temperature	–40	100	°C
$T_{J,max}$	Maximum junction temperature		125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	2.95	3.3	3.6	V
T_A	Operating free-air temperature	–40		100	°C
	DIGITAL input high voltage	2			V
	DIGITAL input low voltage			0.8	V

7.4 DC Electrical Characteristics

Over recommended operating conditions, outputs connected to a 50-Ω load, AMP1 = 0, AMP0 = 1 (Register 3) unless otherwise noted. Typical operating condition is at V_{CC} = 3.3 V and T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		2.95	3.3	3.6	V
I_{VCC}	Supply current	DIS = 0, CML currents included		50	63	mA
R_{IN}	Data input resistance	Differential		100		Ω
R_{OUT}	Data output resistance	Single-ended, referenced to V_{CC}		50		Ω
	LOS HIGH voltage	I_{SOURCE} = 50 µA with 10-kΩ pullup to V_{CC}	2.4			V
	LOS LOW voltage	I_{SINK} = 10 mA with 10-kΩ pullup to V_{CC}			0.4	V

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7.5 AC Electrical Characteristics

Over recommended operating conditions, outputs connected to a 50-Ω load, AMP1 = 0, AMP0 = 1 (Register 3) and maximum bandwidth unless otherwise noted. Typical operating condition is at V_{CC} = 3.3 V and T_A = 25°C.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
f_{3dB-H}	–3-dB bandwidth default settings	RATE1 = 1, RATE0 = 0	7.5	9		GHz
		RATE1 = 1, RATE0 = 1		8.4		
		RATE1 = 0, RATE0 = 1		7.6		
		RATE1 = 0, RATE0 = 0		2.4		
f_{3dB-L}	Low frequency –3-dB bandwidth	With 330-pF COC capacitor		10	45	kHz
$V_{IN,MIN}$	Data input sensitivity	PRBS31 pattern at 11.3 Gbps, BER < 10^{-12}		5	9	mV_{pp}
		V_{OD-min} ≥ 0.95 × V_{OD} (output limited)		20	30	
		PRBS31 pattern at 8.5 Gbps, BER < 10^{-12}, RATE1 = 1, RATE0 = 0		4		
		PRBS31 pattern at 4.25 Gbps, BER < 10^{-12}, RATE1 = 1, RATE0 = 1		4		
		PRBS31 pattern at 2.125 Gbps, BER < 10^{-12}, RATE1 = 0, RATE0 = 1		4		
SDD11	Differential input return gain	0.01 GHz < f < 3.9 GHz		–16		dB
		3.9 GHz < f < 12.1 GHz		See (1)		
SDD22	Differential output return gain	0.01 GHz < f < 3.9 GHz		–16		dB
		3.9 GHz < f < 12.1 GHz		See(1)		
SCD11	Differential to common-mode conversion gain	0.01 GHz < f < 12.1 GHz		–15		dB
SCC22	Common-mode output return gain	0.01 GHz < f < 7.5 GHz		–13		dB
		7.5 GHz < f < 12.1 GHz		–9		
A	Small signal gain		29	34		dB
$V_{IN,MAX}$	Data input overload		2000			mV_{pp}
DJ	Deterministic jitter at 11.3 Gbps	V_{IN} = 15 mV_{pp}, K28.5 pattern		3	8	ps_{pp}
		V_{IN} = 30 mV_{pp}, K28.5 pattern		3	10	
		V_{IN} = 2000 mV_{pp}, K28.5 pattern		6	15	
	Deterministic jitter at 8.5 Gbps	V_{IN} = 30 mV_{pp}, K28.5 pattern, RATE1 = 1, RATE0 = 0		4		ps_{pp}
	Deterministic jitter at 4.25 Gbps	V_{IN} = 30 mV_{pp}, K28.5 pattern, RATE1 = 1, RATE0 = 1		6		ps_{pp}
	Deterministic jitter at 2.125 Gbps	V_{IN} = 30 mV_{pp}, K28.5 pattern, RATE1 = 0, RATE0 = 1		8		ps_{pp}
RJ	Random jitter	V_{IN} = 30 mV_{pp}		1		ps_{rms}
V_{OD}	Differential data output voltage	V_{IN} > 30 mV_{pp}, DIS = 0, AMP1 = 0, AMP0 = 0	250	350	450	mV_{pp}
		V_{IN} > 30 mV_{pp}, DIS = 0, AMP1 = 0, AMP0 = 1	500	650	800	
		V_{IN} > 30 mV_{pp}, DIS = 0, AMP1 = 1, AMP0 = 1	650	850	1050	
		DIS = 1			5	mV_{rms}
V_{PREEM}	Output preemphasis step size			1		dB
t_R	Output rise time	20% to 80%, V_{IN} > 30 mV_{pp}		28	40	ps
t_F	Output fall time	20% to 80%, V_{IN} > 30 mV_{pp}		28	40	ps
CMOV	AC common-mode output voltage	PRBS31 pattern; AMP1 = 0, AMP0 = 1			7	mV_{rms}
V_{TH}	LOW LOS assert threshold range min	K28.5 pattern at 11.3 Gbps, LOSRNG = 0		15		mV_{pp}
	LOW LOS assert threshold range max	K28.5 pattern at 11.3 Gbps, LOSRNG = 0		35		
V_{TH}	HIGH LOS assert threshold range min	K28.5 pattern at 11.3 Gbps, LOSRNG = 1		35		mV_{pp}
	HIGH LOS assert threshold range max	K28.5 pattern at 11.3 Gbps, LOSRNG = 1		80		
	LOS threshold variation	Versus temperature at 11.3 Gbps		1.5		dB
		Versus supply voltage V_{CC} at 11.3 Gbps		1		
		Versus data rate		1.5		
	LOS hysteresis (electrical)	K28.5 pattern at 11.3 Gbps	2	4	6	dB
T_{LOS_AST}	LOS assert time		2.5	10	80	µs
T_{LOS_DEA}	LOS deassert time		2.5	10	80	µs
T_{DIS}	Disable response time			20		ns

(1) Differential Return Gain given by SDD11, SDD22 = –11.6 + 13.33 $\log_{10}$(f/8.25), f in GHz

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7.6 Typical Characteristics

Typical operating condition is at V_{CC} = 3.3 V, T_A = 25°C, AMP1 = 0, AMP0 = 1 (Register 3), and maximum bandwidth unless otherwise noted.

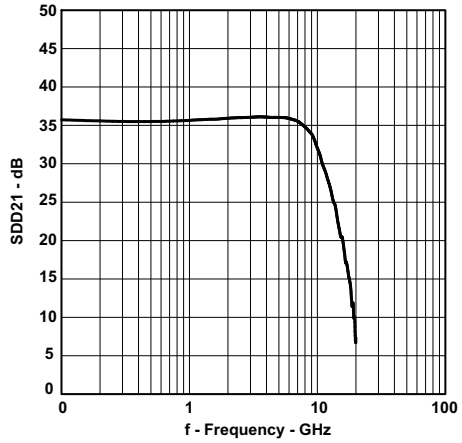

Figure 1. Frequency Response

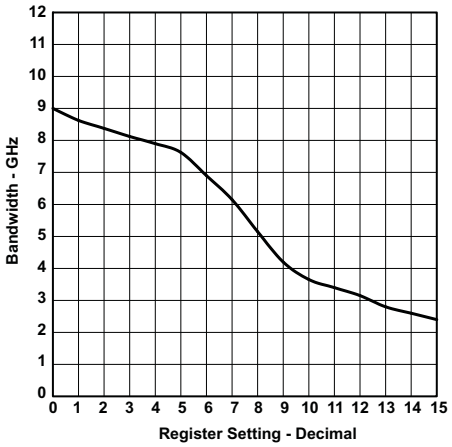

Figure 2. Bandwidth vs Register Setting

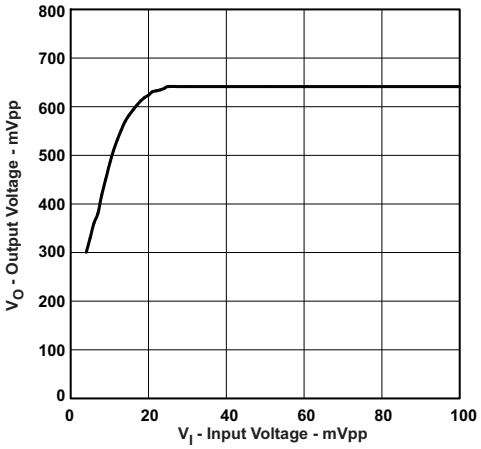

Figure 3. Transfer Function

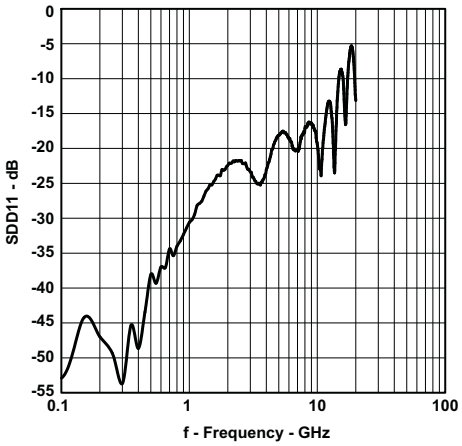

Figure 4. Differential Input Return Gain vs Frequency

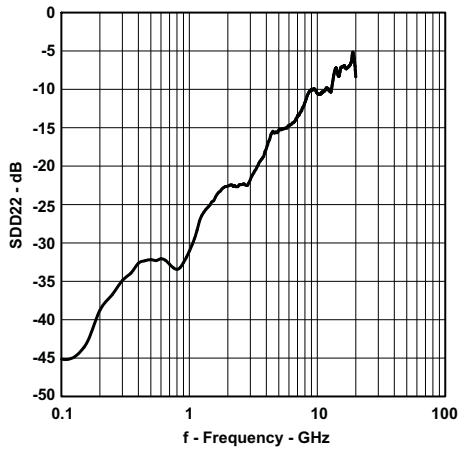

Figure 5. Differential Output Return Gain vs Frequency

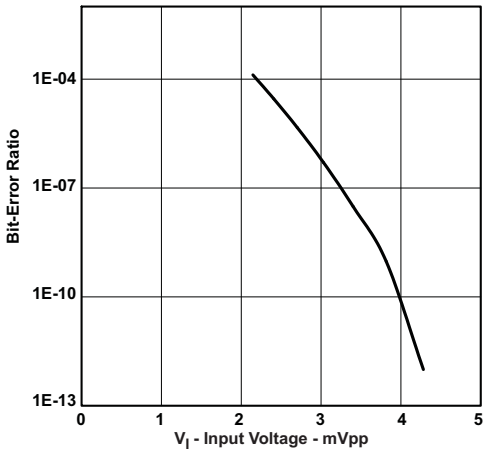

Figure 6. BIT-Error Ratio vs Input Voltage (11.3 GBPS)

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Typical Characteristics (continued)

Typical operating condition is at V_{CC} = 3.3 V, T_A = 25°C, AMP1 = 0, AMP0 = 1 (Register 3), and maximum bandwidth unless otherwise noted.

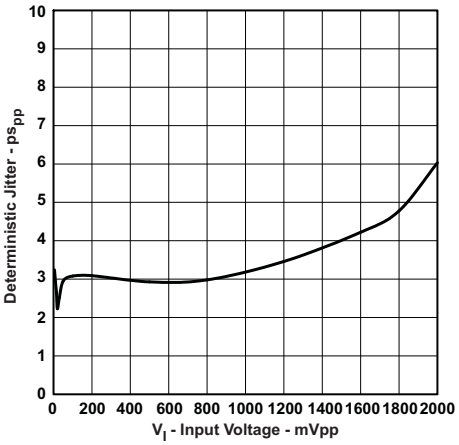


Figure 7. Deterministic Jitter vs Input Voltage

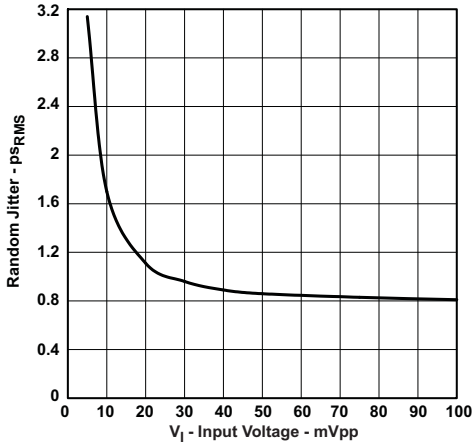


Figure 8. Random Jitter vs Input Voltage

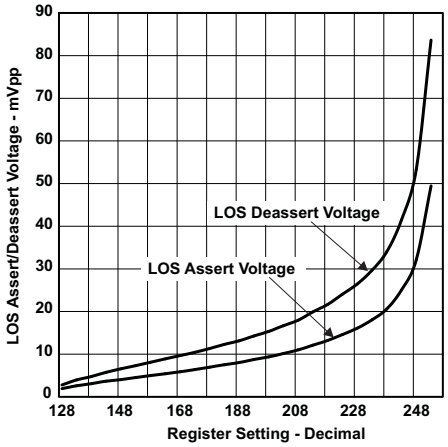


Figure 9. LOS Assert/Deassert Voltage vs Register Setting LOSRNG = 0

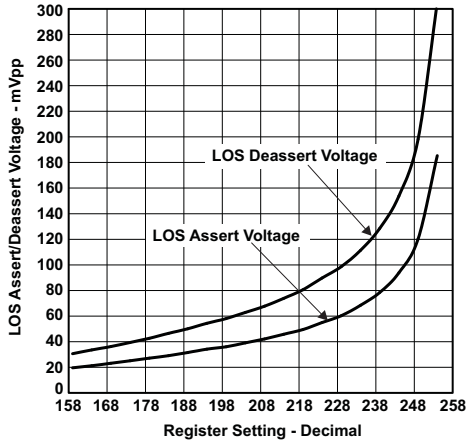


Figure 10. LOS Assert/Deassert Voltage vs Register Setting LOSRNG = 1

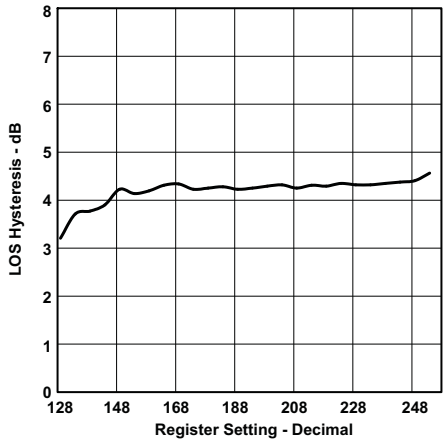


Figure 11. LOS Hysteresis vs Register Setting LOSRNG = 0

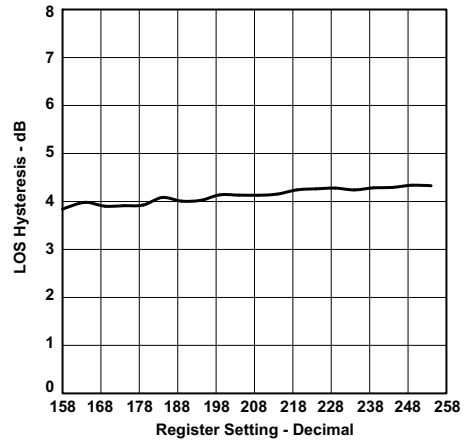


Figure 12. LOS Hysteresis vs Register Setting LOSRNG = 1

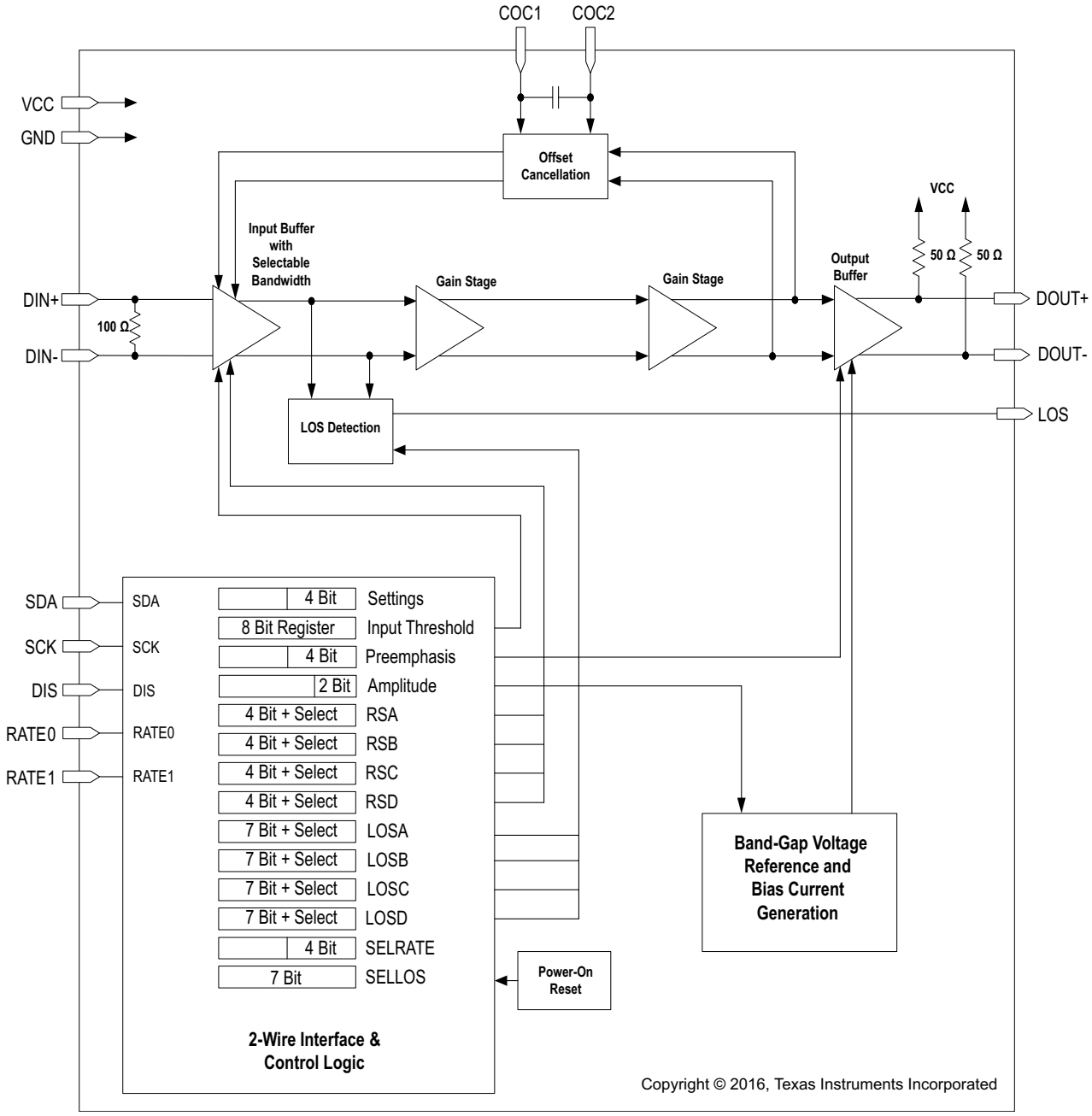
8 Detailed Description

8.1 Overview

This compact, low-power, 11.3-Gbps limiting amplifier consists of a high-speed data path with offset cancellation block (DC feedback) combined with an analog settable input threshold adjust, a loss-of-signal detection block using two peak detectors, a two-wire interface with a control-logic block and a band-gap voltage reference and bias current generation block.

See *Functional Block Diagram* for a simplified block diagram of the ONET8501PB.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 High-Speed Data Path

The high-speed data signal is applied to the data path by means of input signal pins DIN+ / DIN–. The data path consists of a 100-Ω differential termination resistor followed by a digitally controlled bandwidth switch input buffer for rate select. The RATE1 and RATE0 pins can be used to control the bandwidth of the filter. Default bandwidth settings are used; however, these can be changed using registers 4 through 7 through the serial interface. For details regarding the rate selection, see Table 19. A gain stage and an output buffer stage follow the input buffer, which together provide a gain of 34 dB. The device can accept input amplitude levels from 5 mV_{pp} up to 2000 mV_{pp}. The amplified data output signal is available at the output pins DOUT+ and DOUT, which includes on-chip 2 × 50-Ω back-termination to VCC.

Offset cancellation compensates for internal offset voltages and thus ensures proper operation even for very small input data signals. The offset cancellation can be disabled so that the input threshold voltage can be adjusted to optimize the bit error rate or change the eye crossing to compensate for input signal pulse width distortion. The offset cancellation can be disabled by setting OCDIS = 1 (bit 1 of register 0). The input threshold level can be adjusted using register settings THADJ[0..7] (register 1). For details regarding input threshold adjust, see Table 19.

The low frequency cutoff is as low as 80 kHz with the built-in filter capacitor. For applications, which require even lower cutoff frequencies, an additional external filter capacitor may be connected to the COC1 and COC2 pins. A value of 330 pF results in a low frequency cutoff of 10 kHz.

8.3.2 Band-gap Voltage and Bias Generation

The ONET8501PB limiting amplifier is supplied by a single 3.3-V supply voltage connected to the VCC pins. This voltage is referred to ground (GND).

On-chip band-gap voltage circuitry generates a reference voltage, independent of supply voltage, from which all other internally required voltages and bias currents are derived.

8.4 Device Functional Modes

8.4.1 High-Speed Output Buffer

The output amplitude of the buffer can be set to 350 mV_{pp}, 650 mV_{pp}, or 850 mV_{pp} using register settings AMP[0..1] (register 3) through the serial interface. To compensate for frequency dependant losses of transmission lines connected to the output, the ONET8501PB has adjustable preemphasis of the output stage. The preemphasis can be set from 0 to 8 dB in 1-dB steps using register settings PEADJ[0..3] (register 2).

8.4.2 Rate Select

There are 16 possible internal filter settings (4 bit) to adjust the small signal bandwidth to the data rate. For fast rate selection, 4 default values can be selected with the RATE1 and RATE0 pins. Using the serial interface, the bandwidth settings can be customized instead of using the default values. The default bandwidths and the registers used to change the bandwidth settings are shown in Table 1.

Table 1. Rate Selection Default Settings and Registers Used for Adjustment

RATE1	RATE0	DEFAULT BANDWIDTH (GHz)	REGISTER USED FOR ADJUSTMENT
0	0	2.4	RSA (Register 4)
0	1	7.6	RSB (Register 5)
1	1	8.4	RSC (Register 6)
1	0	9	RSD (Register 7)

If the rate select register selection bit is set LOW, for example RSASEL = 0 (bit 7 of register 4), then the default bandwidth for that register is used. If the register selection bit is set HIGH, for example RSASEL = 1 (bit 7 of register 4), then the content of RSA[0..3] (register 4) is used to set the input filter bandwidth when RATE0 = 0 and RATE1 = 0. The settings of the rate selection registers RSA, RSB, RSC, RSD, and the corresponding filter bandwidths are shown in Table 2.

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Table 2. Available Bandwidth Settings

RSX3	RSX2	RSX1	RSX0	TYPICAL BANDWIDTH (GHz)
0	0	0	0	9
0	0	0	1	8.6
0	0	1	0	8.4
0	0	1	1	8.1
0	1	0	0	7.9
0	1	0	1	7.6
0	1	1	0	6.9
0	1	1	1	6.2
1	0	0	0	5.2
1	0	0	1	4.2
1	0	1	0	3.7
1	0	1	1	3.4
1	1	0	0	3.2
1	1	0	1	2.8
1	1	1	0	2.6
1	1	1	1	2.4

The RATE1 and RATE0 pins do not have to be used if the serial interface is being used. If RATE1 is not connected it is internally pulled HIGH and if RATE0 is not connected it is internally pulled LOW, thus selecting register 7. Therefore, changing the contents of RSD[0..3] (register 7) through the serial interface can be used to adjust the bandwidth.

8.4.3 Loss-of-Signal Detection

The loss of signal detection is done by 2 separate level detectors to cover a wide dynamic range. The peak values of the input signal and the output signal of the gain stage are monitored by the peak detectors. The peak values are compared to a predefined loss of signal threshold voltage inside the loss of signal detection block. As a result of the comparison, the LOS signal, which indicates that the input signal amplitude is below the defined threshold level, is generated. The LOS assert level is settable through the serial interface. There are 2 LOS ranges settable with the LOSRNG bit (bit 2 register 0) through the serial interface. By setting the bit LOSRNG = 1, the high range of the LOS assert values are used (35 mV_{pp} to 80 mV_{pp}) and by setting the bit LOSRNG = 0, the low range of the LOS assert values are used (15 mV_{pp} to 35 mV_{pp}).

There are 128 possible internal LOS settings (7 bit) for each LOS range to adjust the LOS assert level. For fast LOS selection, 4 default values can be selected with the RATE1 and RATE0 pins; however, the LOS settings can be customized instead of using the default values. The default LOS assert levels and the registers used to change the LOS settings are shown in Table 3.

Table 3. LOS Assert Level Default Settings and Registers Used for Adjustment

RATE1	RATE0	DEFAULT LOS ASSERT LEVEL (mV_{pp})	REGISTER USED FOR ADJUSTMENT
0	0	15	LOSA (Register 8)
0	1	18	LOSB (Register 9)
1	1	26	LOSC (Register 10)
1	0	26	LOSD (Register 11)

If the LOS register selection bit is set low, for example LOSASEL = 0 (bit 7 of register 8), then the default LOS assert level for that register is used. If the register selection bit is set high, for example LOSASEL = 1 (bit 7 of register 8), then the content of LOSA[0..6] (register 8) is used to set the LOS assert level when RATE1 = 0 and RATE0 = 0. The RATE1 and RATE0 pins do not have to be used if the serial interface is being used. If RATE1 is not connected it is internally pulled HIGH and if RATE0 is not connected it is internally pulled LOW, thus selecting register 11. Therefore, changing the content of LOSD[0..6] (register 11) through the serial interface can be used to adjust the LOS assert level.

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8.5 Programming

8.5.1 2-Wire Interface and Control Logic

The ONET8501PB uses a 2-wire serial interface for digital control. The two circuit inputs, SDA and SCK, are driven, respectively, by the serial data and serial clock from a microcontroller, for example. Both inputs include 100-kΩ pullup resistors to VCC. For driving these inputs, TI recommends an open-drain output.

The 2-wire interface allows write access to the internal memory map to modify control registers and read access to read out control and status signals. The ONET8501PB is a slave device only which means that it can not initiate a transmission itself; it always relies on the availability of the SCK signal for the duration of the transmission. The master device provides the clock signal as well as the START and STOP commands. The protocol for a data transmission is as follows:

1. START command
2. 7-bit slave address (1000100) followed by an eighth bit which is the data direction bit (R/W). A zero indicates a WRITE and a 1 indicates a READ.
3. 8-bit register address
4. 8-bit register data word
5. STOP command

Regarding timing, the ONET8501PB is I^2C compatible. The typical timing is shown in Figure 13 and a complete data transfer is shown in Figure 14. Parameters for Figure 13 are defined in Table 4.

Bus Idle: Both SDA and SCK lines remain HIGH

Start Data Transfer: A change in the state of the SDA line, from HIGH to LOW, while the SCK line is HIGH, defines a START condition (S). Each data transfer begins with a START condition.

Stop Data Transfer: A change in the state of the SDA line from LOW to HIGH while the SCK line is HIGH defines a STOP condition (P). Each data transfer ends with a STOP condition; however, if the master still wishes to communicate on the bus, it can generate a repeated START condition and address another slave without first generating a STOP condition.

Data Transfer: Only one data byte can be transferred between a START and a STOP condition. The receiver acknowledges the transfer of data.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge bit. The transmitter releases the SDA line and a device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge clock pulse. Setup and hold times must be taken into account. When a slave-receiver doesn't acknowledge the slave address, the data line must be left HIGH by the slave. The master can then generate a STOP condition to abort the transfer. If the slave-receiver does acknowledge the slave address but some time later in the transfer cannot receive any more data bytes, the master must abort the transfer. This is indicated by the slave generating the not acknowledge on the first byte to follow. The slave leaves the data line HIGH and the master generates the STOP condition.

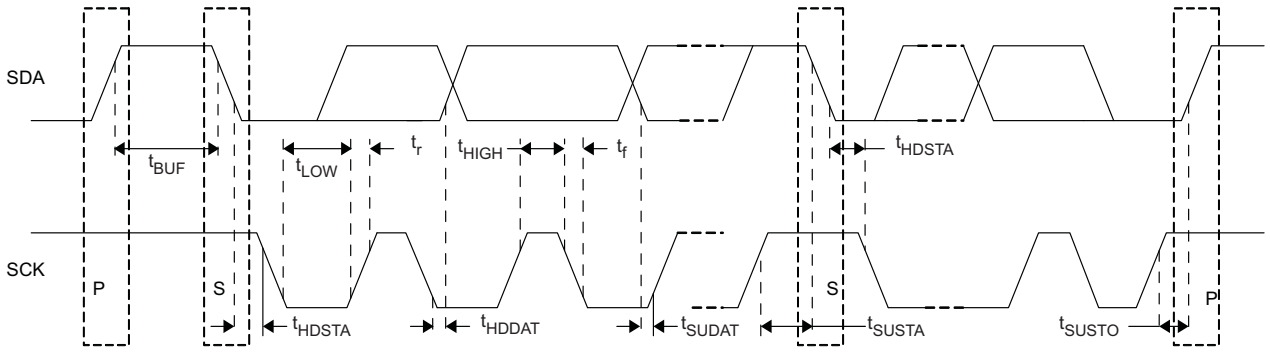

Figure 13. I^2C Timing Diagram

Programming (continued)

Table 4. Timing Diagram Definitions

PARAMETER		MIN	MAX	UNIT
f_{SCK}	SCK clock frequency		400	kHz
t_{BUF}	Bus free time between START and STOP conditions	1.3		µs
t_{HDSTA}	Hold time after repeated START condition. After this period, the first clock pulse is generated	0.6		µs
t_{LOW}	Low period of the SCK clock	1.3		µs
t_{HIGH}	High period of the SCK clock	0.6		µs
t_{SUSTA}	Setup time for a repeated START condition	0.6		µs
t_{HDDAT}	Data HOLD time	0		µs
t_{SUDAT}	Data setup time	100		ns
t_R	Rise time of both SDA and SCK signals		300	ns
t_F	Fall time of both SDA and SCK signals		300	ns
t_{SUSTO}	Setup time for STOP condition	0.6		µs

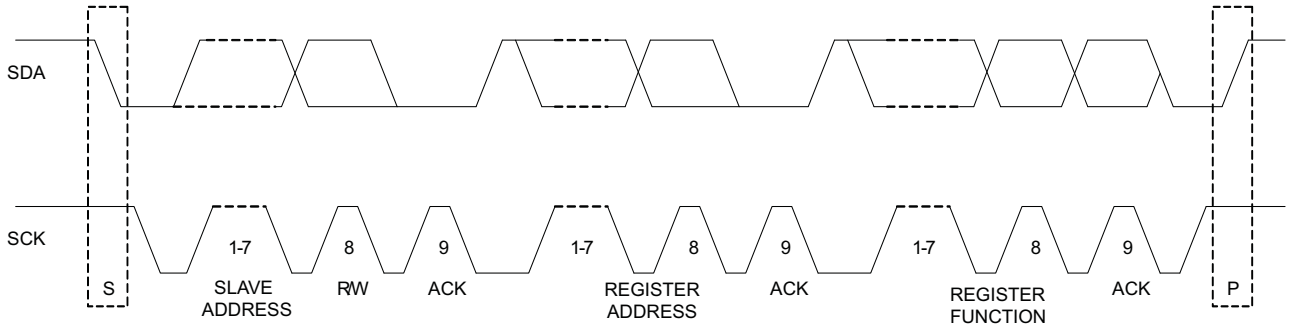

Figure 14. I²C Data Transfer

8.6 Register Maps

The register mapping for read and write register addresses 0 (0x00) through 11 (0x0B) are shown in Table 5 through Table 16. The register mapping for the read only register addresses 14 (0x0E) and 15 (0x0F) are shown in Table 17 and Table 18.

Table 19 describes the circuit functionality based on the register settings.

8.6.1 Register 0 (0x00) Mapping – Control Settings

Table 5. Register 0 (0x00) Mapping – Control Settings

REGISTER ADDRESS 0 (0X00)							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
—	—	—	—	DIS	LOSRNG	OCDIS	I2CDIS

8.6.2 Register 1 (0x01) Mapping – Input Threshold Adjust

Table 6. Register 1 (0x01) Mapping – Input Threshold Adjust

REGISTER ADDRESS 1 (0X01)							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
THADJ7	THADJ6	THADJ5	THADJ4	THADJ3	THADJ2	THADJ1	THADJ0

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8.6.3 Register 2 (0x02) Mapping – Preemphasis Adjust

Table 7. Register 2 (0x02) Mapping – Preemphasis Adjust

REGISTER ADDRESS 2 (0X02)							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
—	—	—	—	PEADJ3	PEADJ2	PEADJ1	PEADJ0

8.6.4 Register 3 (0x03) Mapping – Output Amplitude Adjust

Table 8. Register 3 (0x03) Mapping – Output Amplitude Adjust

REGISTER ADDRESS 3 (0X03)							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
—	—	—	—	—	—	AMP1	AMP0

8.6.5 Register 4 (0x04) Mapping – Rate Selection Register A

Table 9. Register 4 (0x04) Mapping – Rate Selection Register A

register address 4 (0x04)							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RSASEL	—	—	—	RSA3	RSA2	RSA1	RSA0

8.6.6 Register 5 (0x05) Mapping – Rate Selection Register B

Table 10. Register 5 (0x05) Mapping – Rate Selection Register B

REGISTER ADDRESS 5 (0X05)							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RSBSEL	—	—	—	RSB3	RSB2	RSB1	RSB0

8.6.7 Register 6 (0x06) Mapping – Rate Selection Register C

Table 11. Register 6 (0x06) Mapping – Rate Selection Register C

REGISTER ADDRESS 6 (0X06)							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RSCSEL	—	—	—	RSC3	RSC2	RSC1	RSC0

8.6.8 Register 7 (0x07) Mapping – Rate Selection Register D

Table 12. Register 7 (0x07) Mapping – Rate Selection Register D

REGISTER ADDRESS 7 (0X07)							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RSDSEL	—	—	—	RSD3	RSD2	RSD1	RSD0

8.6.9 Register 8 (0x08) Mapping – LOS Assert Level Register A

Table 13. Register 8 (0x08) Mapping – LOS Assert Level Register A

REGISTER ADDRESS 8 (0X08)							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
LOSASEL	LOSA6	LOSA5	LOSA4	LOSA3	LOSA2	LOSA1	LOSA0

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8.6.10 Register 9 (0x09) Mapping – LOS Assert Level Register B

Table 14. Register 9 (0x09) Mapping – LOS Assert Level Register B

REGISTER ADDRESS 9 (0X09)							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
LOSBSEL	LOSB6	LOSB5	LOSB4	LOSB3	LOSB2	LOSB1	LOSB0

8.6.11 Register 10 (0x0A) Mapping – LOS Assert Level Register C

Table 15. Register 10 (0x0A) Mapping – LOS Assert Level Register C

REGISTER ADDRESS 10 (0X0A)							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
LOSCSEL	LOSC6	LOSC5	LOSC4	LOSC3	LOSC2	LOSC1	LOSC0

8.6.12 Register 11 (0x0B) Mapping – LOS Assert Level Register D

Table 16. Register 11 (0x0B) Mapping – LOS Assert Level Register D

REGISTER ADDRESS 11 (0X0B)							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
LOSDSEL	LOSD6	LOSD5	LOSD4	LOSD3	LOSD2	LOSD1	LOSD0

8.6.13 Register 14 (0x0E) Mapping – Selected Rate Setting (Read Only)

Table 17. Register 14 (0x0E) Mapping – Selected Rate Setting (Read Only)

REGISTER ADDRESS 14 (0X0E)							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
—	—	—	—	SELRATE3	SELRATE2	SELRATE1	SELRATE0

8.6.14 Register 15 (0x0F) Mapping – Selected LOS Level (Read Only)

Table 18. Register 15 (0x0F) Mapping – Selected LOS Level (Read Only)

REGISTER ADDRESS 15 (0X0F)							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
—	SELLOS6	SELLOS5	SELLOS4	SELLOS3	SELLOS2	SELLOS1	SELLOS0

Table 19. Register Functionality

SYMBOL	REGISTER BIT	FUNCTION
DIS	Output disable bit 3	**Output disable bit:** 1 = output disabled 0 = output enabled
LOSRNG	LOS Range bit 2	**LOS range bit:** 1 = high LOS assert voltage range 0 = low LOS assert voltage range
OCDIS	Offset cancellation disable bit 1	**Offset cancellation disable bit:** 1 = offset cancellation is disabled 0 = offset cancellation is enabled
I2CDIS	I^2C disable bit 0	**I^2C disable bit:** 1 = I^2C is disabled. 0 = I^2C is enabled. This is the default setting.

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Table 19. Register Functionality (continued)

SYMBOL	REGISTER BIT	FUNCTION			
THADJ7	Input threshold adjust bit 7 (MSB)	**Input threshold adjustment setting:**			
THADJ6	Input threshold adjust bit 6	Maximum positive shift for 00000001 (1)			
THADJ5	Input threshold adjust bit 5	Minimum positive shift for 01111111 (127)			
THADJ4	Input threshold adjust bit 4	Zero shift for 10000000 (128)			
THADJ3	Input threshold adjust bit 3	Minimum negative shift for 10000001 (129)			
THADJ2	Input threshold adjust bit 2	Maximum negative shift for 11111111 (255)			
THADJ1	Input threshold adjust bit 1				
THADJ0	Input threshold adjust bit 0 (LSB)				
PEADJ3	Preemphasis adjust bit 3 (MSB)	**Preemphasis setting:**			
PEADJ2	Preemphasis adjust bit 2		Preemphasis (dB)	Register Setting	
PEADJ1	Preemphasis adjust bit 1		0	0000	
PEADJ0	Preemphasis adjust bit 0 (LSB)		1	0001	
			2	0011	
			3	0100	
			4	0101	
			5	0111	
			6	1100	
			7	1101	
			8	1111	
AMP1	Output amplitude adjustment bit 1	**Output amplitude adjustment:**			
AMP0	Output amplitude adjustment bit 0	00 = 350 mV_{pp}			
		01 = 650 mV_{pp}			
		10 = 650 mV_{pp}			
		11 = 850 mV_{pp}			
RSASEL	Register RSA select bit 7 (MSB)	**Rate selection register A**			
–		RSASEL = 1			
–		Content of register A bits 3 to 0 is used to select the input filter BW			
–		RSASEL = 0			
RSA3	Rate select register A bit 3	Default BW of 2.4 GHz is used			
RSA2	Rate select register A bit 2				
RSA1	Rate select register A bit 1	Register RSA is used when RATE1 = 0 and RATE0 = 0			
RSA0	Rate select register A bit 0 (LSB)				
RSBSEL	Register RSB select bit 7 (MSB)	**Rate selection register B**			
–		RSBSEL = 1			
–		Content of register B bits 3 to 0 is used to select the input filter BW			
–		RSBSEL = 0			
RSB3	Rate select register B bit 3	Default BW of 7.6 GHz is used			
RSB2	Rate select register B bit 2				
RSB1	Rate select register B bit 1	Register RSB is used when RATE1 = 0 and RATE0 = 1			
RSB0	Rate select register B bit 0 (LSB)				

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Table 19. Register Functionality (continued)

SYMBOL	REGISTER BIT	FUNCTION
RSCSEL	Register RSC select bit 7 (MSB)	**Rate selection register C**
–		RSCSEL = 1
–		Content of register C bits 3 to 0 is used to select the input filter BW
–		RSCSEL = 0
RSC3	Rate select register C bit 3	Default BW of 8.4 GHz is used
RSC2	Rate select register C bit 2	
RSC1	Rate select register C bit 1	Register RSC is used when RATE1 = 1 and RATE0 = 1
RSC0	Rate select register C bit 0 (LSB)	
RSDSEL	Register RSD select bit 7 (MSB)	**Rate selection register D**
–		RSDSEL = 1
–		Content of register D bits 3 to 0 is used to select the input filter BW
–		RSDSEL = 0
RSD3	Rate select register D bit 3	Default BW of 9.0 GHz is used
RSD2	Rate select register D bit 2	
RSD1	Rate select register D bit 1	Register RSD is used when RATE1 = 1 and RATE0 = 0 or RATE1 and RATE0 are not connected
RSD0	Rate select register D bit 0 (LSB)	
LOSASEL	Register LOSA select bit 7 (MSB)	**LOS assert level register A**
LOSA6	LOS assert level register A bit 6	LOSASEL = 1
LOSA5	LOS assert level register A bit 5	Content of register A bits 6 to 0 is used to select the LOS assert level
LOSA4	LOS assert level register A bit 4	Minimum LOS assert level for 0000000
LOSA3	LOS assert level register A bit 3	Maximum LOS assert level for 1111111
LOSA2	LOS assert level register A bit 2	LOSASEL = 0
LOSA1	LOS assert level register A bit 1	Default LOS assert level of 15 mV_{pp} is used
LOSA0	LOS assert level register A bit 0 (LSB)	Register LOSA is used when RATE1 = 0 and RATE0 = 0
LOSBSEL	Register LOSB select bit 7 (MSB)	**LOS assert level register B**
LOSB6	LOS assert level register B bit 6	LOSBSEL = 1
LOSB5	LOS assert level register B bit 5	Content of register B bits 6 to 0 is used to select the LOS assert level
LOSB4	LOS assert level register B bit 4	Minimum LOS assert level for 0000000
LOSB3	LOS assert level register B bit 3	Maximum LOS assert level for 1111111
LOSB2	LOS assert level register B bit 2	LOSBSEL = 0
LOSB1	LOS assert level register B bit 1	Default LOS assert level of 18 mV_{pp} is used
LOSB0	LOS assert level register B bit 0 (LSB)	Register LOSB is used when RATE1 = 0 and RATE0 = 1
LOSCSEL	Register LOSC select bit 7 (MSB)	**LOS assert level register C**
LOSC6	LOS assert level register C bit 6	LOSCSEL = 1
LOSC5	LOS assert level register C bit 5	Content of register C bits 6 to 0 is used to select the LOS assert level
LOSC4	LOS assert level register C bit 4	Minimum LOS assert level for 0000000
LOSC3	LOS assert level register C bit 3	Maximum LOS assert level for 1111111
LOSC2	LOS assert level register C bit 2	LOSCSEL = 0
LOSC1	LOS assert level register C bit 1	Default LOS assert level of 26 mV_{pp} is used
LOSC0	LOS assert level register C bit 0 (LSB)	Register LOSC is used when RATE1 = 1 and RATE0 = 1

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Table 19. Register Functionality (continued)

SYMBOL	REGISTER BIT	FUNCTION
LOSDSEL	Register LOSD select bit 7 (MSB)	**LOS assert level register D**
LOSD6	LOS assert level register D bit 6	LOSDSEL = 1
LOSD5	LOS assert level register D bit 5	Content of register D bits 6 to 0 is used to select the LOS assert level
LOSD4	LOS assert level register D bit 4	Minimum LOS assert level for 0000000
LOSD3	LOS assert level register D bit 3	Maximum LOS assert level for 1111111
LOSD2	LOS assert level register D bit 2	LOSDSEL = 0
LOSD1	LOS assert level register D bit 1	Default LOS assert level of 26 mV_{pp} is used
LOSD0	LOS assert level register D bit 0 (LSB)	Register LOSD is used when RATE1 = 1 and RATE0 = 0
SELRATE3	Selected rate setting bit 3	**Selected rate setting (read only)**
SELRATE2	Selected rate setting bit 2	
SELRATE1	Selected rate setting bit 1	
SELRATE0	Selected rate setting bit 0	
SELLOS6	Selected LOS assert level bit 6 (MSB)	**Selected LOS assert level (read only)**
SELLOS5	Selected LOS assert level bit 5	
SELLOS4	Selected LOS assert level bit 4	
SELLOS3	Selected LOS assert level bit 3	
SELLOS2	Selected LOS assert level bit 2	
SELLOS1	Selected LOS assert level bit 1	
SELLOS0	Selected LOS assert level bit 0 (LSB)	

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

Figure 15 shows a typical application with digital control. In this case DIN+ and DIN– are connected to Transimpedance Amplifier (ROSA) and DOUT+ and DOUT– to SFP connector. SDA and SCK are connected to a microprocessor.

9.2 Typical Application

Figure 15 shows a typical application circuit using the ONET8501PB.

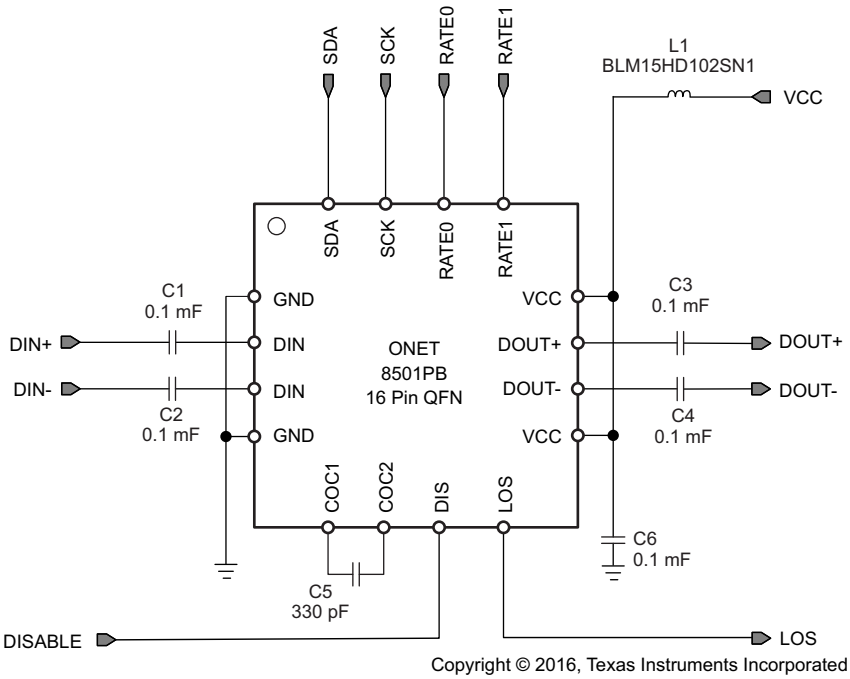

Figure 15. Typical Application Circuit

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 20 as the input parameters.

Table 20. Design Parameters

PARAMETER	EXAMPLE VALUE
Supply voltage	3.3 V
V_{IN}	20 mV_{pp} to 2000 mV_{pp}
Data rate	8.5 Gbps to 10.3 Gbps
AC capacitors	0.1 µF
COC capacitor	330 pF

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9.2.2 Detailed Design Procedure

The purpose of the series resistors is to improve the signal integrity between the VCSEL driver and the VCSEL. Because the VCSEL impedance varies depending on its type, the series resistor provides a better matching impedance for the modulation current outputs.

The output amplitude adjustments are set as: AMP0 = 1 and AMP1 = 0 (see Register 3). DIN+, DIN–, DOUT+, and DOUT– are AC-coupled with 0.1 µF.

9.2.3 Application Curves

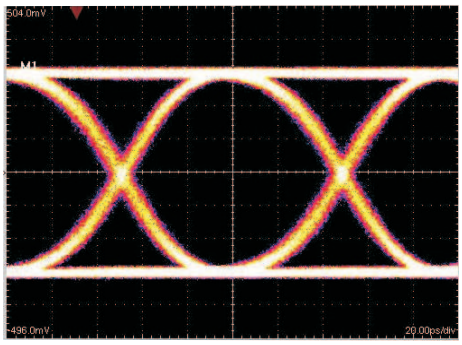

Figure 16. Output Eye-Diagram at 10.3 GBPS vs and Input Voltage (20 mV_{pp})

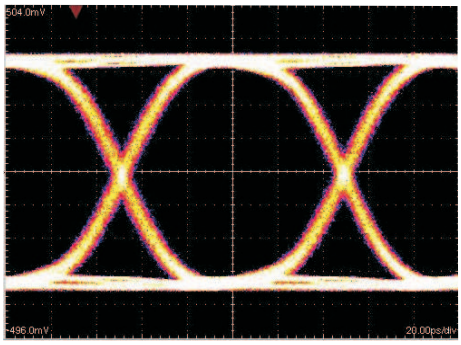

Figure 17. Output Eye-Diagram at 10.3 GBPS vs and Maximum Input Voltage (2000 mV_{pp})

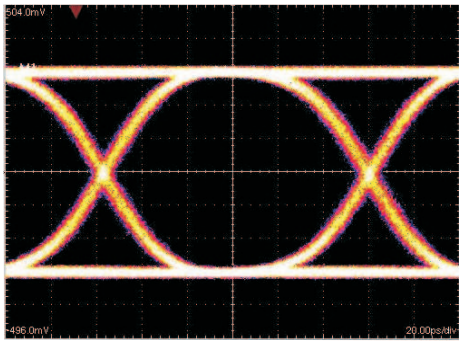

Figure 18. Output Eye-Diagram at 8.5 GBPS and Input Voltage (20 mV_{pp})

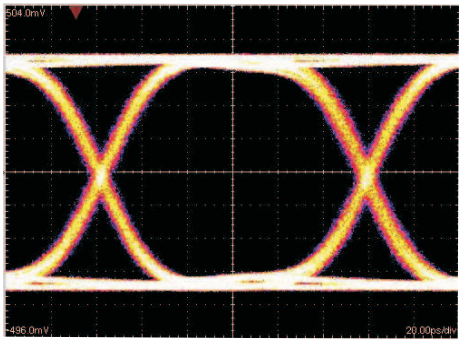

Figure 19. Output Eye-Diagram at 8.5 GBPS and Maximum Input Voltage (2000 mV_{pp})

10 Power Supply Recommendations

The ONET8401PB is designed to operate with an input supply voltage range from 2.95 V to 3.6 V.

For SFP+ modules, the ONET8501PB must be used because of its low AC common-mode voltage.

The supply current of the ONET8501PB is dependent upon the output amplitude setting.

The typical setting for an SFP+ module is the 650-mV_{pp} output voltage. The typical supply current in this case is 50 mA leading to 165 mW.

11 Layout

11.1 Layout Guidelines

For optimum performance, use 50-Ω transmission lines (100-Ω differential) for connecting the high-speed inputs and outputs. The length of transmission lines must be kept as short as possible to reduce loss and pattern-dependent jitter. TI recommends maximizing the separation of the DOUT+ and DOUT– transmission lines from the DIN+ and DIN– transmission lines to minimize transmitter to receiver crosstalk.

11.2 Layout Example

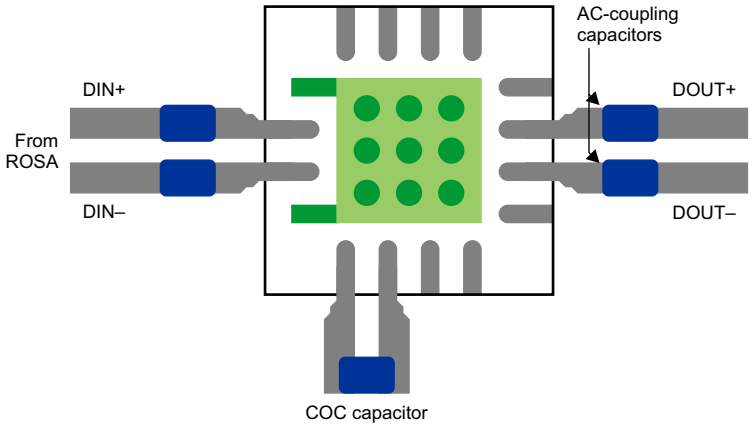

Figure 20. ONET8501PB Layout Example

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12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ONET8501PBRGTR	ACTIVE	VQFN	RGT	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 100	85PB	Samples
ONET8501PBRGTRG4	ACTIVE	VQFN	RGT	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 100	85PB	Samples
ONET8501PBRGTT	ACTIVE	VQFN	RGT	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 100	85PB	Samples
ONET8501PBRGTTG4	ACTIVE	VQFN	RGT	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 100	85PB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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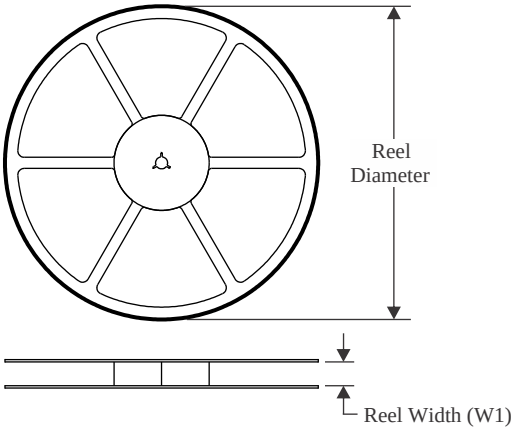
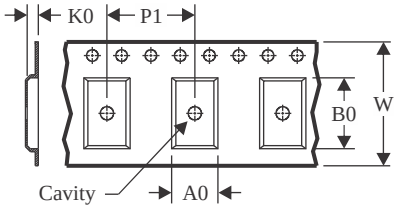
TAPE AND REEL INFORMATION

REEL DIMENSIONS

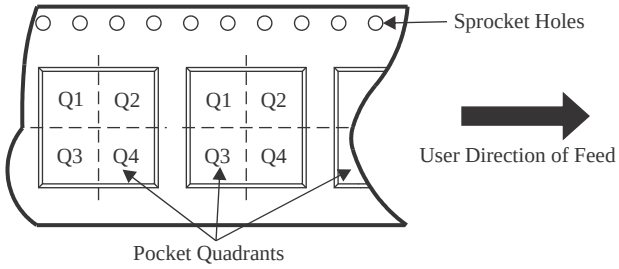


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

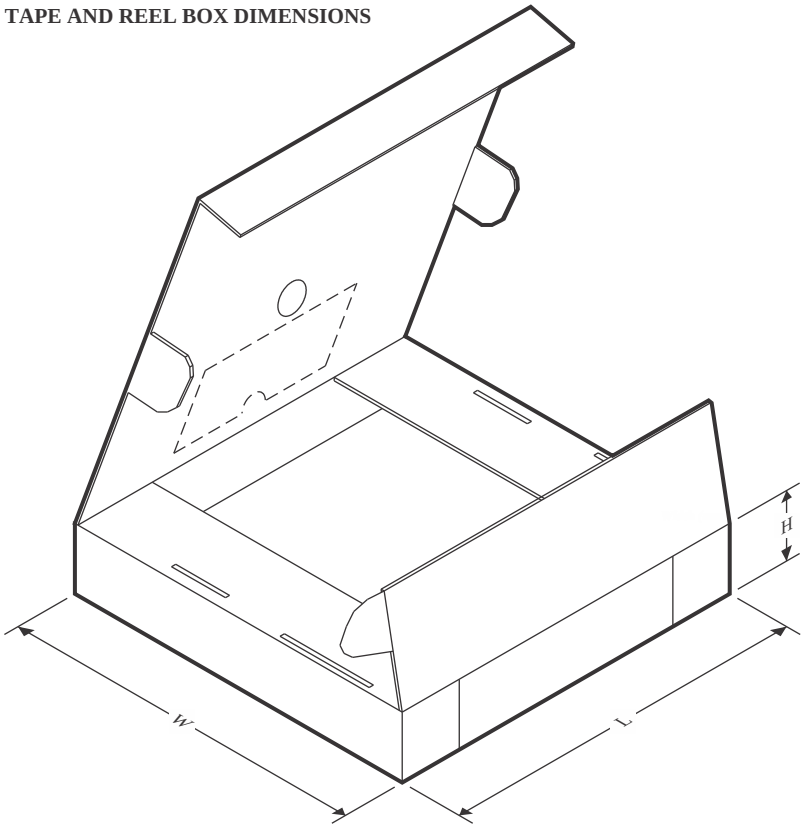
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ONET8501PBRGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ONET8501PBRGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

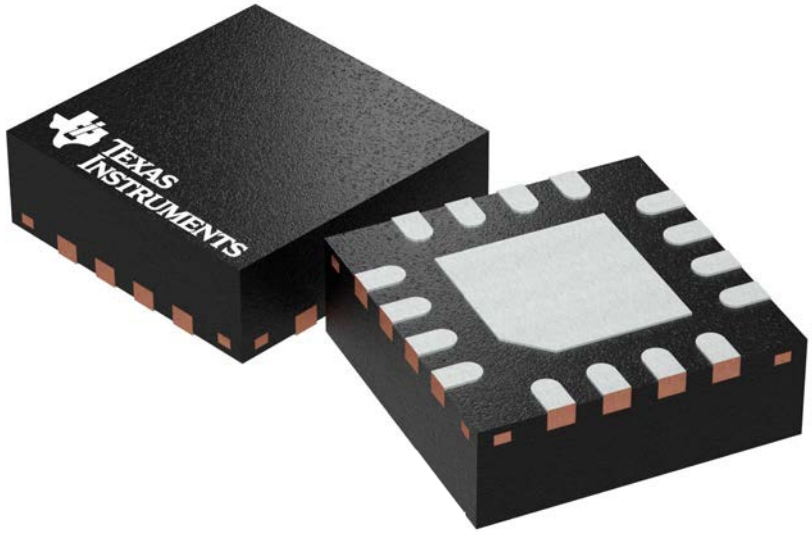
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ONET8501PBRGTR	VQFN	RGT	16	3000	346.0	346.0	33.0
ONET8501PBRGTT	VQFN	RGT	16	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

RGT 16

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

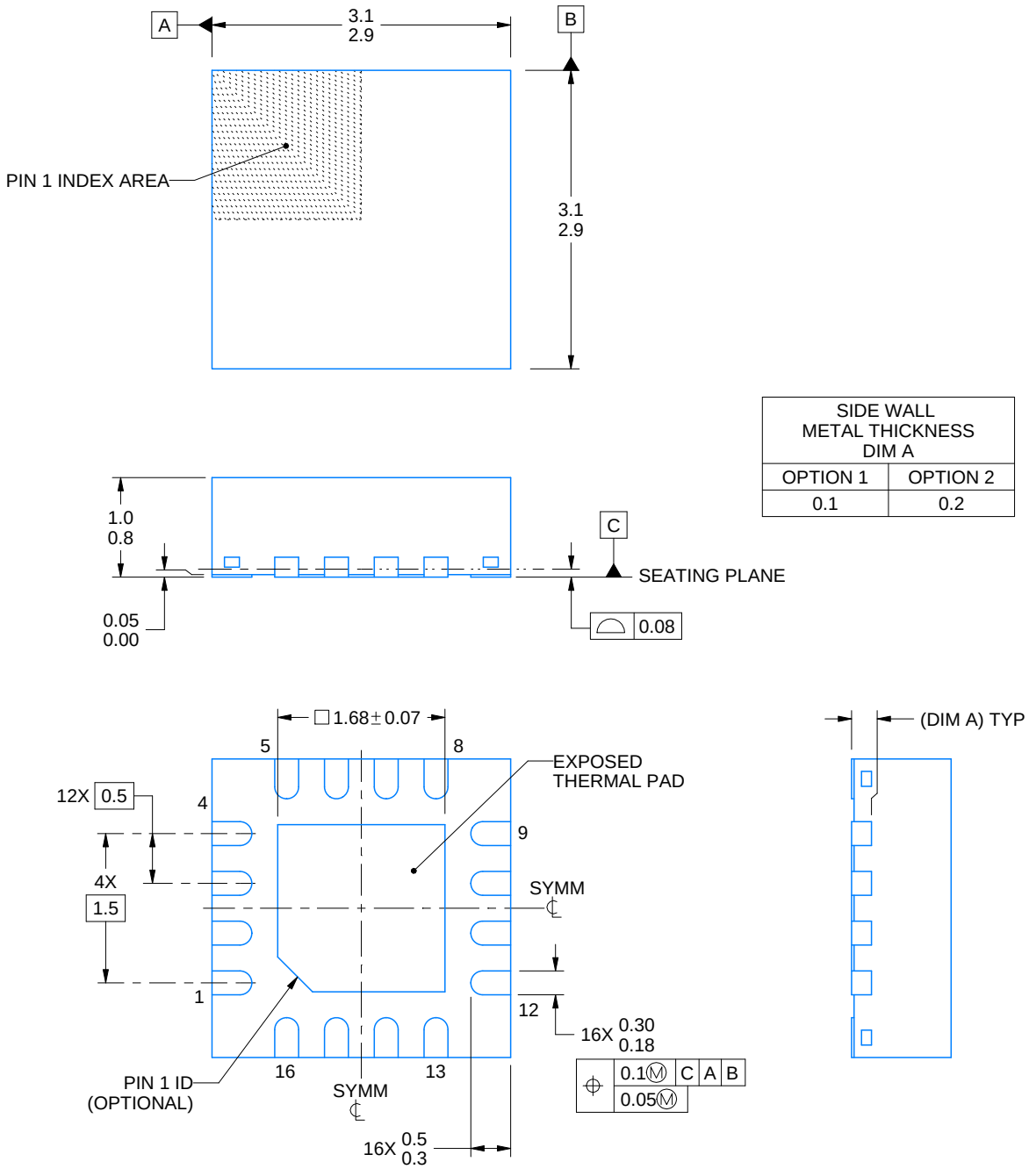
4203495/I

RGT0016C

PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



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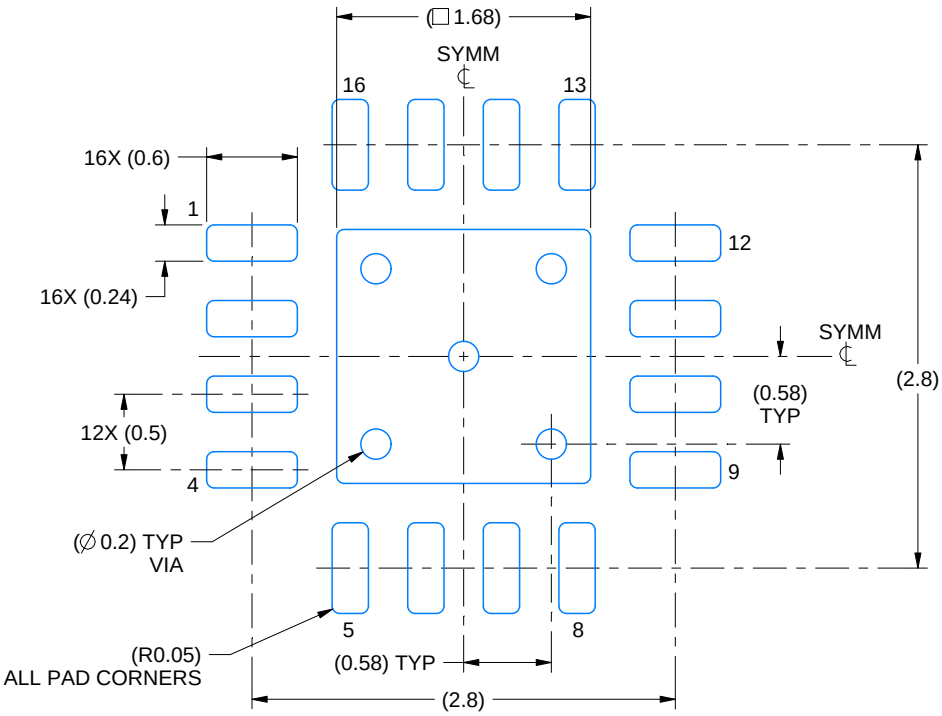
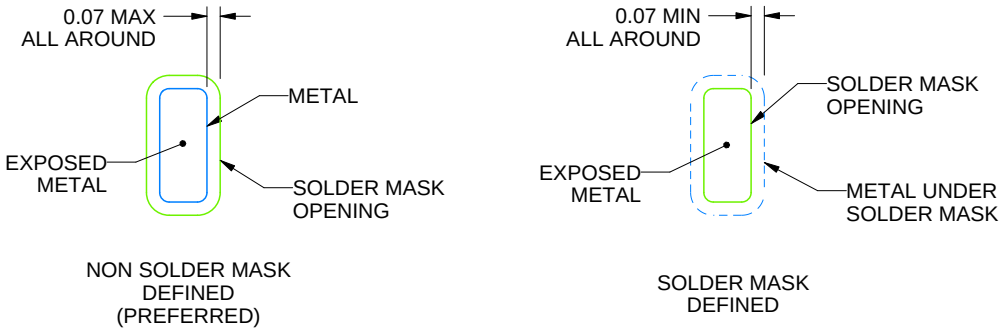
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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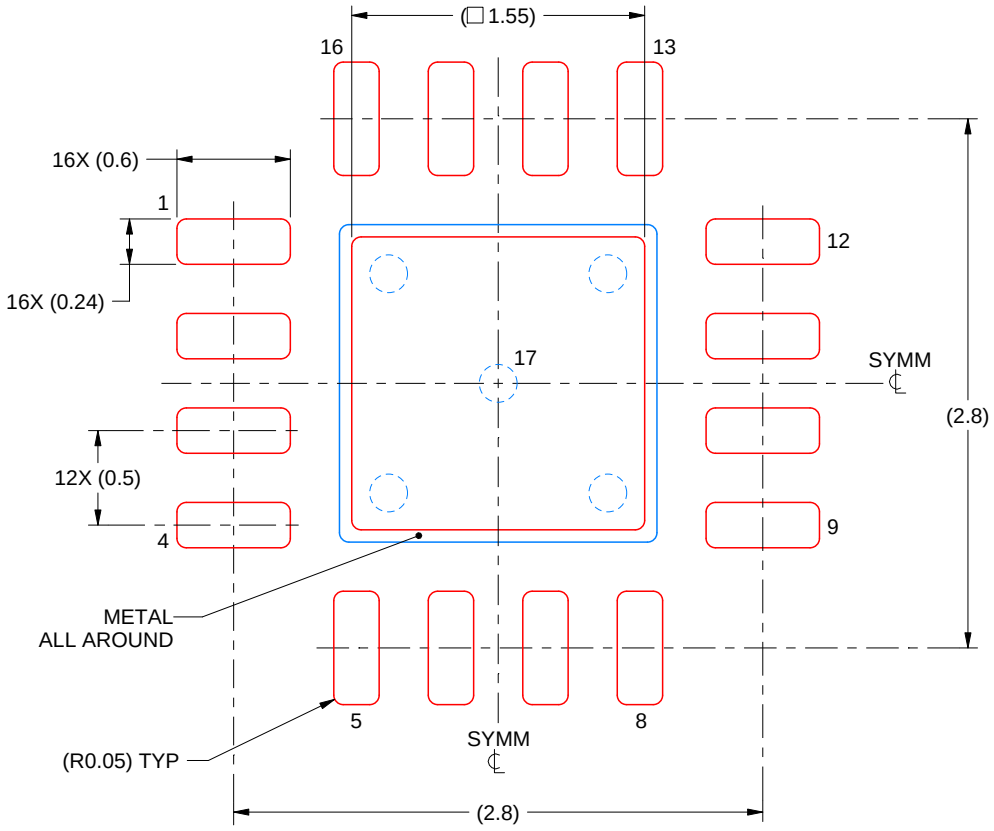
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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