DS90UB925Q-Q1 5 to 85 MHz 24-Bit Color FPD-Link III Serializer With Bidirectional Control Channel

1 Features

- Bidirectional Control Interface Channel Interface with I^2C Compatible Serial Control Bus
- Supports High Definition (720 p) Digital Video Format
- RGB888 + VS, HS, DE and I2S Audio Supported
- Supports Two 10–bit Camera Video Streams
- 5 – 85MHz PCLK Supported
- Single 3.3 V Operation with 1.8 V or 3.3 V Compatible LVCMOS I/O Interface
- AC-Coupled STP Interconnect Up to 10 Meters
- Parallel LVCMOS Video Inputs
- DC-Balanced and Scrambled Data with Embedded Clock
- Supports Repeater Application
- Internal Pattern Generation
- Low Power Modes Minimize Power Dissipation
- Automotive Grade Product: AEC-Q100 Grade 2 Qualified
- >8kV HBM and ISO 10605 ESD Rating
- Backward Compatible to FPD-Link II

2 Applications

- Automotive Display for Navigation
- Rear Seat Entertainment Systems
- Automotive Driver Assistance
- Automotive Megapixel Camera Systems

3 Description

The DS90UB925Q-Q1 serializer, in conjunction with the DS90UB926Q-Q1 deserializer, provides a complete digital interface for concurrent transmission of high-speed video, audio, and control data for automotive display and image sensing applications.

The chipset is ideally suited for automotive video-display systems with HD formats and automotive vision systems with megapixel resolutions. The DS90UB925Q-Q1 incorporates an embedded bidirectional control channel and low latency GPIO controls. This chipset translates a parallel interface into a single pair high-speed serialized interface. The serial bus scheme, FPD-Link III, supports full duplex of high-speed video data transmission and bidirectional control communication over a single differential link. Consolidation of video data and control over a single differential pair reduces the interconnect size and weight, while also eliminating skew issues and simplifying system design.

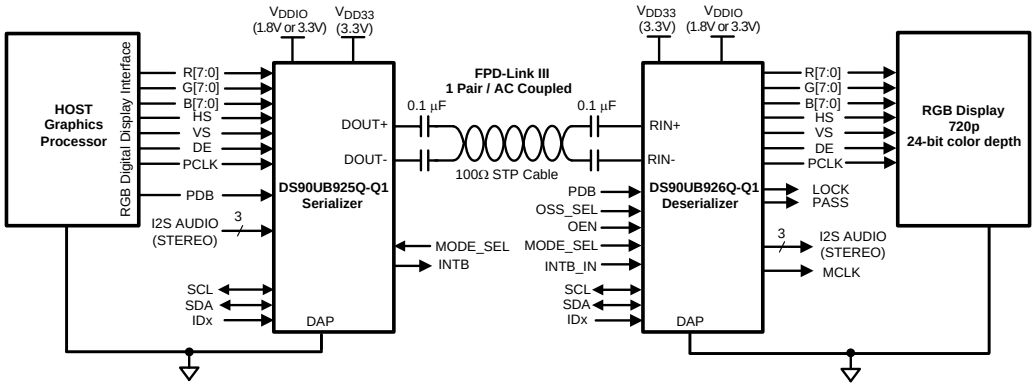
The DS90UB925Q-Q1 serializer embeds the clock, DC scrambles & balances the data payload, and level shifts the signals to high-speed low voltage differential signaling. Up to 24 data bits are serialized along the video control signals.

Serial transmission is optimized by a user selectable de-emphasis. EMI is minimized by the use of low voltage differential signaling, data scrambling and randomization and spread spectrum clocking compatibility.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DS90UB925Q-Q1	WQFN (48)	7.00 mm × 7.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (April 2013) to Revision D — **Page**

- Added data sheet flow and layout to conform with new TI standards. Added the following sections: Handling Ratings, Device Functional Modes; Programming; Power Supply Recommendations; Layout; Device and Documentation Support; Mechanical, Packaging and Ordering Information ... 1
- Added Device Information table ... 1
- Fixed typo for GPIO configuration ... 19
- Removed two MODE_SEL modes: I2S Channel B, and Backward Compatible ... 23
- Removed IDx addresses 0x22, 0x24, 0x2E, 0x30, 0x32, 0x34 ... 26
- Changed suggested resistor values for IDx addresses 0x1E, 0x20, 0x26, 0x28, 0x2A ... 26

Changes from Revision B (August 2012) to Revision C — **Page**

- Changed layout of National datasheet to TI format. ... 1

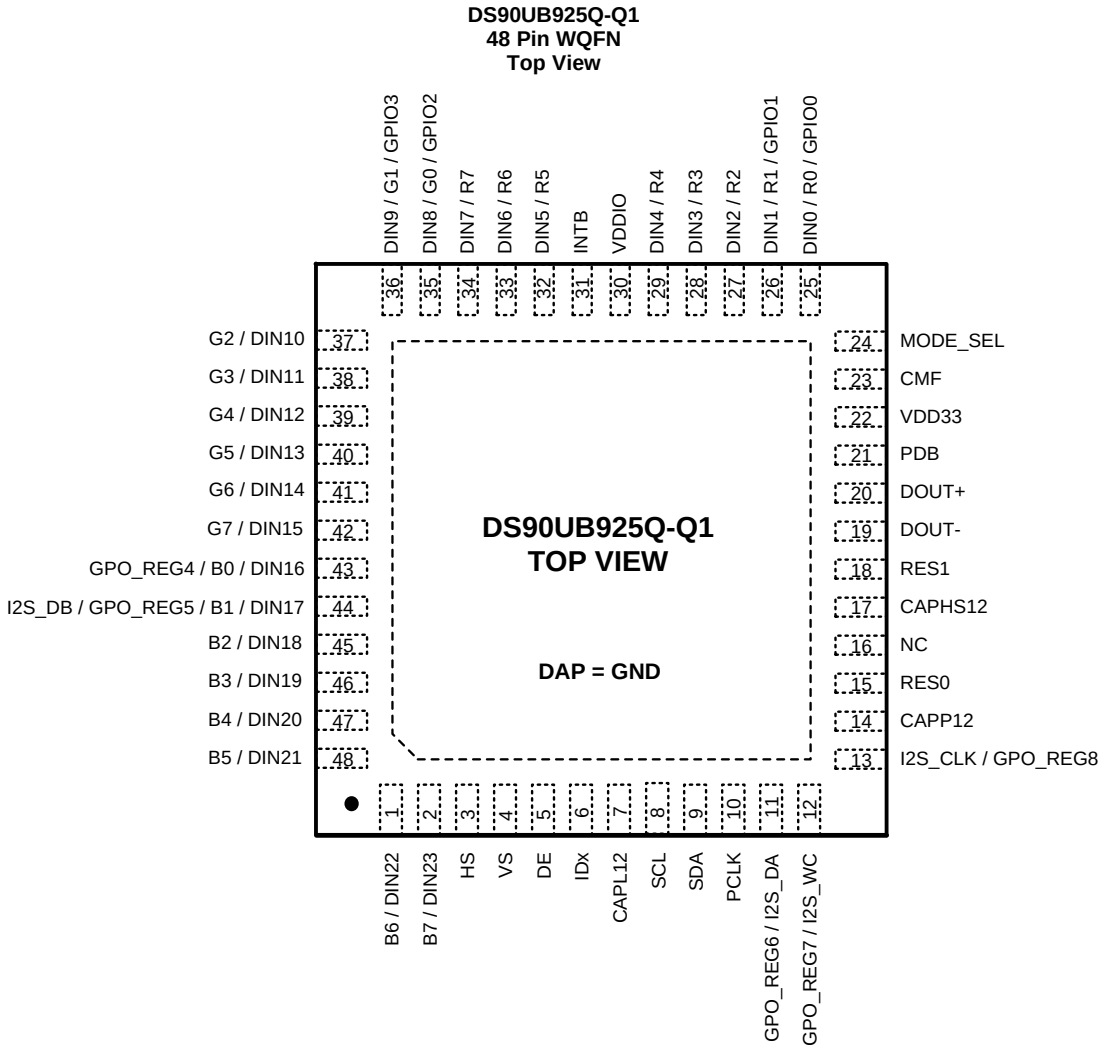
Changes from Revision A (July 2012) to Revision B — **Page**

- Added typical charateristic graphics ... 14
- Added" Note: frequency range = 15 - 65MHz when LFMODE = 0 and frequency range = 5 - <15MHz when LFMODE = 1." under Functional Description. ... 16
- Reformatted Table 2 and added clarification to notes. ... 19
- Added clarification to notes on Table 6, address 0x04[3:0] (backwards compatible and LFMODE registers). ... 27

Changes from Original (March 2012) to Revision A **Page**

- Converted to hybrid TI format. 1
- Corrected typo in SCL from pin 6 to pin 8. 4
- Corrected typo in SDA from pin 7 to pin 9. 4
- Added to Absolute Maximum Rating section, note (3): The maximum limit (V_{DDIO} +0.3V) does not apply to the PDB pin during the transition to the power down state (PDB transitioning from HIGH to LOW). 7
- Deleted derate from Maximum Power Dissipation Capacity at 25°C. 7
- Added "Note: BIST is not available in backwards compatible mode." 20
- Corrected typo in Table 4 "I2S Channel B (18-bit Mode)" from L to H 23
- Corrected typo in Table 5 Ideal V_{R2}(V) from 2.475 to 1.475. 26

5 Pin Configuration and Functions



Pin Functions

PIN NAME	PIN #	I/O, TYPE	DESCRIPTION
LVCMOS PARALLEL INTERFACE			
DIN[23:0] / R[7:0], G[7:0], B[7:0]	25, 26, 27, 28, 29, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 1, 2	I, LVCMOS w/ pull down	Parallel Interface Data Input Pins Leave open if unused DIN0 / R0 can optionally be used as GPIO0 and DIN1 / R1 can optionally be used as GPIO1 DIN8 / G0 can optionally be used as GPIO2 and DIN9 /G1 can optionally be used as GPIO3 DIN16 / B0 can optionally be used as GPIO4 and DIN17 / B1 can optionally be used as GPIO5
HS	3	I, LVCMOS w/ pull down	Horizontal Sync Input Pin Video control signal pulse width must be 3 PCLKs or longer to be transmitted when the Control Signal Filter is enabled. There is no restriction on the minimum transition pulse when the Control Signal Filter is disabled. The signal is limited to 2 transitions per 130 PCLKs. See Table 6.
VS	4	I, LVCMOS w/ pull down	Vertical Sync Input Pin Video control signal is limited to 1 transition per 130 PCLKs. Thus, the minimum pulse width is 130 PCLKs.

Pin Functions (continued)

PIN NAME	PIN #	I/O, TYPE	DESCRIPTION
DE	5	I, LVCMOS w/ pull down	Data Enable Input Pin Video control signal pulse width must be 3 PCLKs or longer to be transmitted when the Control Signal Filter is enabled. There is no restriction on the minimum transition pulse when the Control Signal Filter is disabled. The signal is limited to 2 transitions per 130 PCLKs. See Table 6.
PCLK	10	I, LVCMOS w/ pull down	Pixel Clock Input Pin. Strobe edge set by RFB configuration register. See Table 6.
I2S_CLK, I2S_WC, I2S_DA	13, 12, 11	I, LVCMOS w/ pull down	Digital Audio Interface Data Input Pins Leave open if unused I2S_CLK can optionally be used as GPO_REG8, I2S_WC can optionally be used as GPO_REG7, and I2S_DA can optionally be used as GPO_REG6.
OPTIONAL PARALLEL INTERFACE			
I2S_DB	44	I, LVCMOS w/ pull down	Second Channel Digital Audio Interface Data Input pin at 18–bit color mode and set by MODE_SEL pin or configuration register Leave open if unused I2S_DB can optionally be used as DIN17 or GPO_REG5.
GPIO[3:0]	36, 35, 26, 25	I/O, LVCMOS w/ pull down	General Purpose IOs. Available only in 18-bit color mode, and set by MODE_SEL pin or configuration register. See Table 6. Leave open if unused. Shared with DIN9, DIN8, DIN1 and DIN0
GPO_REG[8:4]	13, 12, 11, 44, 43	O, LVCMOS w/ pull down	General Purpose Outputs and set by configuration register. See Table 6. Share with I2S_CLK, I2S_WC, I2S_DA, I2S_DB or DIN17, DIN16.
CONTROL			
PDB	21	I, LVCMOS w/ pull-down	Power-down Mode Input Pin PDB = H, device is enabled (normal operation) Refer to *Power Up Requirements and PDB Pin* section. PDB = L, device is powered down. When the device is in the powered down state, the Driver Outputs are both HIGH, the PLL is shutdown, and IDD is minimized. Control Registers are **RESET**.
MODE_SEL	24	I, Analog	Device Configuration Select. See Table 4.
I^2C			
IDx	6	I, Analog	I^2C Serial Control Bus Device ID Address Select External pull-up to V_{DD33} is required under all conditions, DO NOT FLOAT. Connect to external pull-up and pull-down resistor to create a voltage divider. See Figure 19.
SCL	8	I/O, LVCMOS Open Drain	I^2C Clock Input / Output Interface Must have an external pull-up to V_{DD33}, DO NOT FLOAT. Recommended pull-up: 4.7kΩ.
SDA	9	I/O, LVCMOS Open Drain	I^2C Data Input / Output Interface Must have an external pull-up to V_{DD33}, DO NOT FLOAT. Recommended pull-up: 4.7kΩ.
STATUS			
INTB	31	O, LVCMOS Open Drain	Interrupt INTB = H, normal INTB = L, Interrupt request Recommended pull-up: 4.7kΩ to V_{DDIO}
FPD-LINK III SERIAL INTERFACE			
DOUT+	20	O, LVDS	True Output The output must be AC-coupled with a 0.1µF capacitor.
DOUT-	19	O, LVDS	Inverting Output The output must be AC-coupled with a 0.1µF capacitor.
CMF	23	Analog	Common Mode Filter. Connect 0.1µF to GND

Pin Functions (continued)

PIN NAME	PIN #	I/O, TYPE	DESCRIPTION
POWER AND GROUND (1)			
V_{DD33}	22	Power	Power to on-chip regulator **3.0 V - 3.6 V**. Requires 4.7 uF to GND
V_{DDIO}	30	Power	LVCMOS I/O Power **1.8 V ±5% OR 3.0 V - 3.6 V**. Requires 4.7 uF to GND
GND	DAP	Ground	DAP is the large metal contact at the bottom side, located at the center of the WQFN package. **Connect to the ground plane** (GND) with at least 9 vias.
REGULATOR CAPACITOR			
CAPHS12, CAPP12	17, 14	CAP	Decoupling capacitor connection for on-chip regulator. Requires a 4.7uF to GND at each CAP pin.
CAPL12	7	CAP	Decoupling capacitor connection for on-chip regulator. Requires two 4.7uF to GND at this CAP pin.
OTHERS			
NC	16	NC	Do not connect.
RES[1:0]	18, 15	GND	Reserved. Tie to Ground.

(1) The VDD (V_{DD33} and V_{DDIO}) supply ramp should be faster than 1.5 ms with a monotonic rise.

6 Specifications

6.1 Absolute Maximum Ratings (1) (2)

	MIN	MAX	UNIT
Supply Voltage – V_{DD33}	-0.3	+4.0	V
Supply Voltage – V_{DDIO}	-0.3	+4.0	V
LVCMOS I/O Voltage (3)	-0.3	V_{DDIO} + 0.3	V
Serializer Output Voltage	-0.3	+2.75	V
Junction Temperature		+150	°C

(1) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(2) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.
(3) The maximum limit (VDDIO +0.3V) does not apply to the PDB pin during the transition to the power down state (PDB transitioning from HIGH to LOW).

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		-65	+150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 (1)	±8	±8	kV
		Charged device model (CDM), per AEC Q100-011	±1.25	±1.25	
		Machine Model (MM)	±250	±250	V
ESD Rating (IEC 61000-4-2, powered-up only) R_D= 330Ω, C_S = 150pF		Air Discharge (DOUT+, DOUT-)	±15	±15	kV
		Contact Discharge (DOUT+, DOUT-)	±8	±8	
ESD Rating (ISO 10605) R_D= 330Ω, C_S = 150pF/330pF R_D= 2KΩ, C_S = 150pF/330pF		Air Discharge (DOUT+, DOUT-)	±15	±15	
		Contact Discharge (DOUT+, DOUT-)	±8	±8	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply Voltage (V_{DD33})	3.0	3.3	3.6	V
LVCMOS Supply Voltage (V_{DDIO})	3.0	3.3	3.6	V
OR				
LVCMOS Supply Voltage (V_{DDIO})	1.71	1.8	1.89	V
Operating Free Air Temperature (T_A)	−40	+25	+105	°C
PCLK Frequency	5		85	MHz
Supply Noise			100	mV_{P-P}

6.4 Thermal Information

THERMAL METRIC[1]		WQFN 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	35	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	5.2	
$R_{\theta JB}$	Junction-to-board thermal resistance	5.5	
ψ_{JT}	Junction-to-top characterization parameter	0.1	
ψ_{JB}	Junction-to-board characterization parameter	5.5	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 DC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.[1] [2] [3]

PARAMETER		TEST CONDITIONS		PIN/FREQ.	MIN	TYP	MAX	UNIT
LVCMOS I/O DC SPECIFICATIONS								
V_{IH}	High Level Input Voltage	V_{DDIO} = 3.0 to 3.6V		PDB	2.0		V_{DDIO}	V
V_{IL}	Low Level Input Voltage	V_{DDIO} = 3.0 to 3.6V			GND		0.8	V
I_{IN}	Input Current	V_{IN} = 0V or V_{DDIO} = 3.0 to 3.6V			−10	±1	+10	µA
V_{IH}	High Level Input Voltage	V_{DDIO} = 3.0 to 3.6V		DIN[23:0], HS, VS, DE, PCLK, I2S_CLK, I2S_WC, I2S_DA, I2S_DB	2.0		V_{DDIO}	V
		V_{DDIO} = 1.71 to 1.89V			0.65* V_{DDIO}		V_{DDIO}	V
V_{IL}	Low Level Input Voltage	V_{DDIO} = 3.0 to 3.6V			GND		0.8	V
		V_{DDIO} = 1.71 to 1.89V			GND		0.35* V_{DDIO}	V
I_{IN}	Input Current	V_{IN} = 0V or V_{DDIO}	V_{DDIO} = 3.0 to 3.6V		−10	±1	+10	µA
			V_{DDIO} = 1.71 to 1.89V		−10	±1	+10	µA
V_{OH}	High Level Output Voltage	I_{OH} = −4mA	V_{DDIO} = 3.0 to 3.6V	GPIO[3:0], GPO_REG[8:4]	2.4		V_{DDIO}	V
			V_{DDIO} = 1.71 to 1.89V		V_{DDIO} - 0.45		V_{DDIO}	V
V_{OL}	Low Level Output Voltage	I_{OL} = +4mA	V_{DDIO} = 3.0 to 3.6V		GND		0.4	V
			V_{DDIO} = 1.71 to 1.89V		GND		0.35	V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V				−50		mA
I_{OZ}	TRI-STATE® Output Current	V_{OUT} = 0V or V_{DDIO}, PDB = L,			−10		+10	µA

(1) The Electrical Characteristics tables list ensured specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
(2) Typical values represent most likely parametric norms at V_{DD} = 3.3 V, T_A = +25 °C, and at the *Recommended Operating Conditions* at the time of product characterization and are not ensured.
(3) Current into device pins is defined as positive. Current out of a device pin is defined as negative. Voltages are referenced to ground except V_{OD} and ΔV_{OD}, which are differential voltages.

DC Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.(1) (2) (3)

PARAMETER		TEST CONDITIONS		PIN/FREQ.	MIN	TYP	MAX	UNIT
FPD-LINK III CML DRIVER DC SPECIFICATIONS								
V_{ODp-p}	Differential Output Voltage (DOUT+) – (DOUT-)	R_L = 100Ω, See Figure 1		DOUT+, DOUT-	1160	1250	1340	mV_{p-p}
ΔV_{OD}	Output Voltage Unbalance					1	50	mV
V_{OS}	Offset Voltage – Single-ended	R_L = 100Ω, See Figure 1				2.5-0.25*V_{ODp-p} (TYP)		V
ΔV_{OS}	Offset Voltage Unbalance Single-ended					1	50	mV
I_{OS}	Output Short Circuit Current	DOUT+/- = 0V, PDB = L or H				−38		mA
R_T	Internal Termination Resistor - Single ended				40	52	62	Ω
SERIAL CONTROL BUS								
V_{IH}	Input High Level	SDA and SCL			0.7* V_{DD33}		V_{DD33}	V
V_{IL}	Input Low Level Voltage	SDA and SCL			GND		0.3* V_{DD33}	V
V_{HY}	Input Hysteresis					>50		mV
V_{OL}		SDA, I_{OL} = 1.25 mA			0		0.36	V
I_{in}		SDA or SCL, V_{IN} = V_{DD33} or GND			-10		10	µA
C_{in}	Input Capacitance	SDA or SCL				<5		pF
SUPPLY CURRENT								
I_{DD1}	Supply Current (includes load current) R_L = 100Ω, f = 85MHz	Checker Board Pattern, See Figure 2	V_{DD33}= 3.6V	V_{DD33}		148	170	mA
I_{DDIO1}			V_{DDIO} = 3.6V	V_{DDIO}		90	180	µA
			V_{DDIO} = 1.89V			1	1.6	mA
I_{DDS1}	Supply Current Remote Auto Power Down Mode	0x01[7] = 1, deserializer is powered down	V_{DD33} = 3.6V	V_{DD33}		1.2	2.4	mA
I_{DDIOS1}			V_{DDIO} = 3.6V	V_{DDIO}		65	150	µA
			V_{DDIO} = 1.89V			55	150	µA
I_{DDS2}	Supply Current Power Down	PDB = L, All LVCMOS inputs are floating or tied to GND	V_{DD33} = 3.6V	V_{DD33}		1	2	mA
I_{DDIOS2}			V_{DDIO} = 3.6V	V_{DDIO}		65	150	µA
			V_{DDIO} = 1.89V			50	150	µA

6.6 AC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (1) (2) (3)

PARAMETER		TEST CONDITIONS	PIN/FREQ.	MIN	TYP	MAX	UNIT
GPIO BIT RATE							
B_R	Forward Channel Bit Rate	See (4) (5)	f = 5 – 85 MHz GPIO[3:0]		0.25* f		Mbps
	Back Channel Bit Rate				75		kbps
RECOMMENDED TIMING FOR PCLK							
t_{TCP}	PCLK Period	See (4) (5)	PCLK	11.76	T	200	ns
t_{CIH}	PCLK Input High Time			0.4*T	0.5*T	0.6*T	ns
t_{CIL}	PCLK Input Low Time			0.4*T	0.5*T	0.6*T	ns
t_{CLKT}	PCLK Input Transition Time, See Figure 3 (4) (5)		f = 5 MHz	4.0			ns
			f = 85 MHz	0.5			ns
t_{JIT}	PCLK Input Jitter Tolerance, Bit Error Rate ≤10^{-10}	f / 40 < Jitter Freq < f / 20 (4) (6) (7)	f = 5 – 78MHz	0.4	0.6		UI

(1) The Electrical Characteristics tables list ensured specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
(2) Typical values represent most likely parametric norms at V_{DD} = 3.3 V, T_A = +25 °C, and at the *Recommended Operating Conditions* at the time of product characterization and are not ensured.
(3) Current into device pins is defined as positive. Current out of a device pin is defined as negative. Voltages are referenced to ground except V_{OD} and ΔV_{OD}, which are differential voltages.
(4) Specification is ensured by characterization and is not tested in production.
(5) Specification is ensured by design and is not tested in production.
(6) Jitter Frequency is specified in conjunction with DS90UB926 PLL bandwidth.
(7) UI – Unit Interval is equivalent to one serialized data bit width 1UI = 1 / (35*PCLK). The UI scales with PCLK frequency.

6.7 Recommended Timing for the Serial Control Bus

Over 3.3V supply and temperature ranges unless otherwise specified.

			MIN	TYP	MAX	UNIT
f_{SCL}	SCL Clock Frequency	Standard Mode	0		100	kHz
		Fast Mode	0		400	kHz
t_{LOW}	SCL Low Period	Standard Mode	4.7			µs
		Fast Mode	1.3			µs
t_{HIGH}	SCL High Period	Standard Mode	4.0			µs
		Fast Mode	0.6			µs
$t_{HD;STA}$	Hold time for a start or a repeated start condition, See Figure 8	Standard Mode	4.0			µs
		Fast Mode	0.6			µs
$t_{SU:STA}$	Set Up time for a start or a repeated start condition, See Figure 8	Standard Mode	4.7			µs
		Fast Mode	0.6			µs
$t_{HD;DAT}$	Data Hold Time, See Figure 8	Standard Mode	0	0.615	3.45	µs
		Fast Mode	0	0.615	0.9	µs
$t_{SU;DAT}$	Data Set Up Time, See Figure 8	Standard Mode	250	0.56		ns
		Fast Mode	100	0.56		ns
$t_{SU;STO}$	Set Up Time for STOP Condition, See Figure 8	Standard Mode	4.0			µs
		Fast Mode	0.6			µs
t_{BUF}	Bus Free Time Between STOP and START, See Figure 8	Standard Mode	4.7			µs
		Fast Mode	1.3			µs
t_r	SCL and SDA Rise Time, See Figure 8	Standard Mode		430	1000	ns
		Fast Mode		430	300	ns
t_f	SCL and SDA Fall Time, See Figure 8	Standard Mode		20	300	ns
		Fast mode		20	300	ns
t_{sp}	input Filter			50		ns

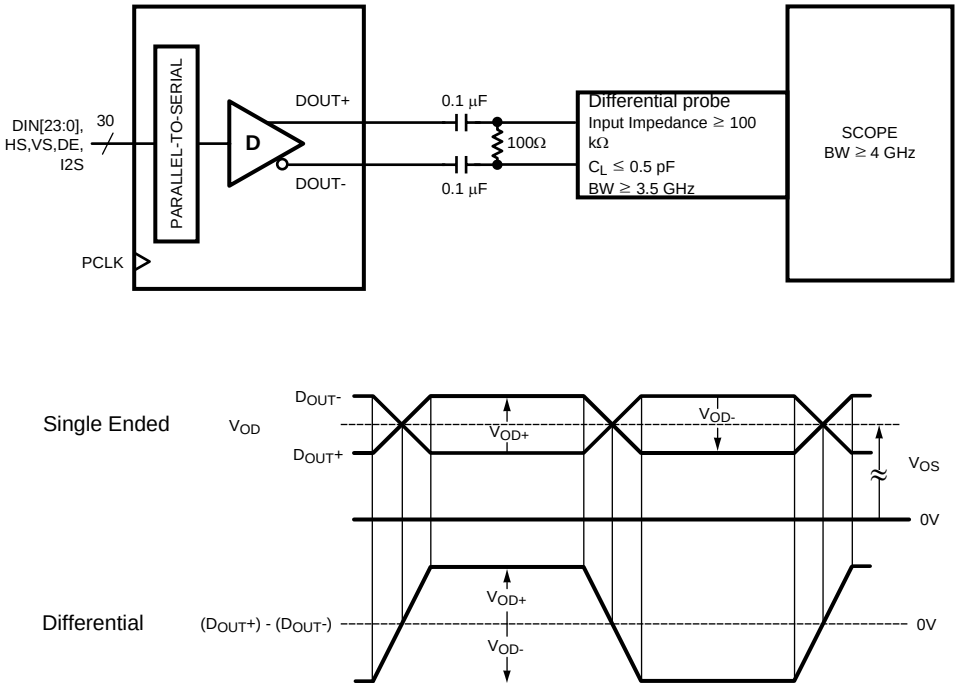


Figure 1. Serializer V_{OD} DC Output

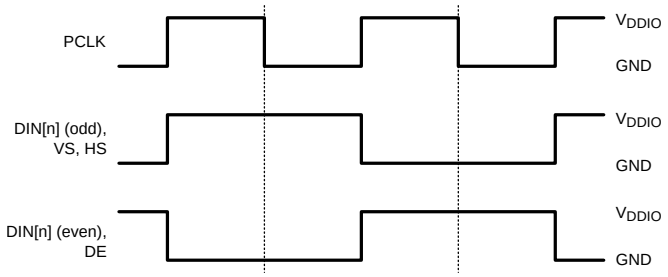


Figure 2. Checkboard Data Pattern

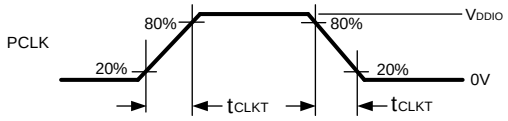


Figure 3. Serializer Input Clock Transition Time

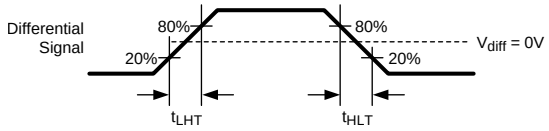


Figure 4. Serializer CML Output Load and Transition Time

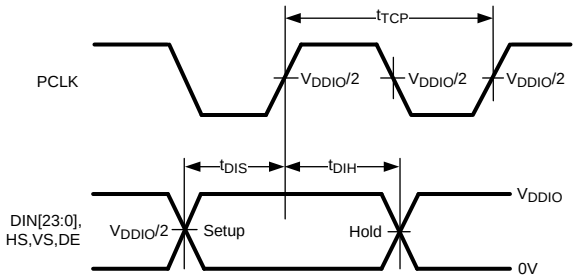


Figure 5. Serializer Setup and Hold Times

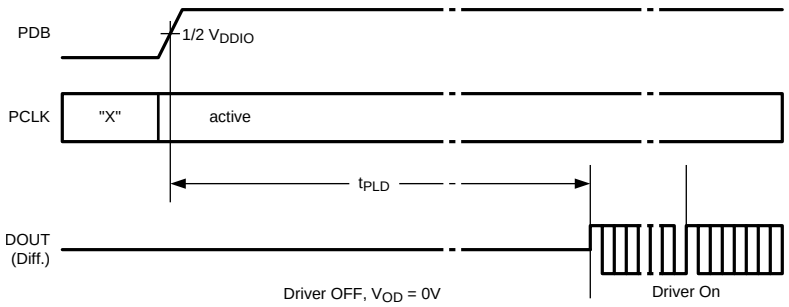


Figure 6. Serializer Lock Time

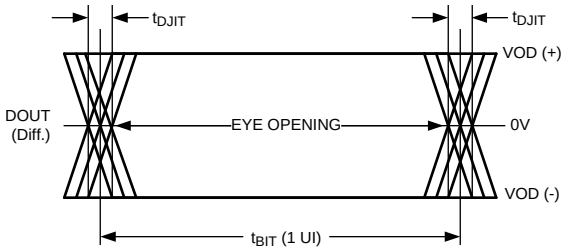


Figure 7. Serializer CML Output Jitter

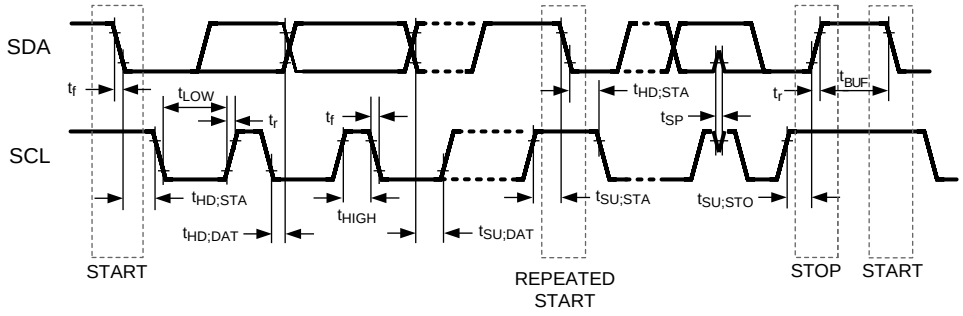


Figure 8. Serial Control Bus Timing Diagram

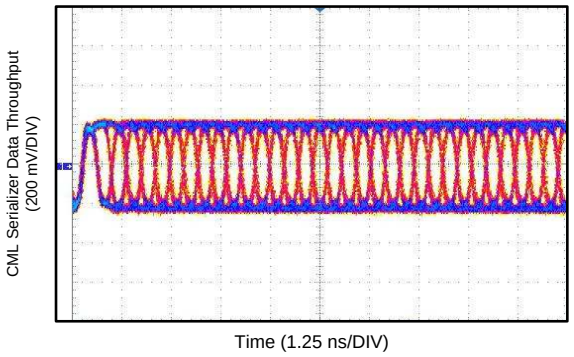
6.8 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	PIN/FREQ.	MIN	TYP	MAX	UNIT
t_{LHT}	CML Output Low-to-High Transition Time	See Figure 4	DOUT+, DOUT-		80	130	ps
t_{HLT}	CML Output High-to-Low Transition Time				80	130	ps
t_{DIS}	Data Input Setup to PCLK	See Figure 5	R[7:0], G[7:0], B[7:0], HS, VS, DE, PCLK, I2S_CLK, I2S_WC, I2S_DA	2.0			ns
t_{DIH}	Data Input Hold from PCLK			2.0			ns
t_{PLD}	Serializer PLL Lock Time	See Figure 6 (1)	f = 15 - 45MHz		131*T		ns
t_{SD}	Delay — Latency		f = 15 - 45MHz		145*T		ns
t_{TJIT}	Output Total Jitter, Bit Error Rate ≥10^{-10} Figure 7 (2) (3) (4)	R_L = 100Ω f = 45MHz	DOUT+, DOUT-		0.25	0.30	UI

(1) tPLD is the time required by the device to obtain lock when exiting power-down state with an active PCLK
(2) Specification is ensured by characterization and is not tested in production.
(3) Specification is ensured by design and is not tested in production.
(4) UI – Unit Interval is equivalent to one serialized data bit width 1UI = 1 / (35*PCLK). The UI scales with PCLK frequency.

6.9 Typical Charateristics



Note: On the rising edge of each clock period, the CML driver outputs a low Stop bit, high Start bit, and 33 DC-scrambled data bits.

Figure 9. Serializer CML Driver Output with 78 MHz TX Pixel Clock

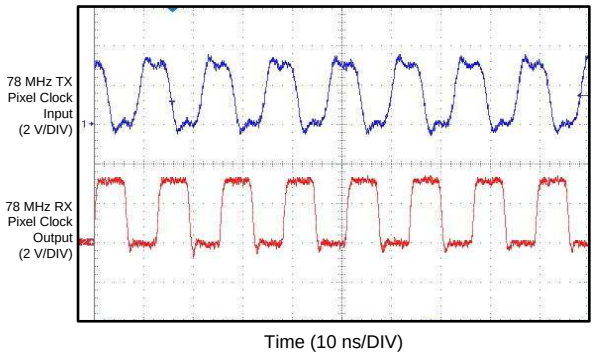


Figure 10. Comparison of Deserializer LVCMOS RX PCLK Output Locked to a 78 MHz TX PCLK

7 Detailed Description

7.1 Overview

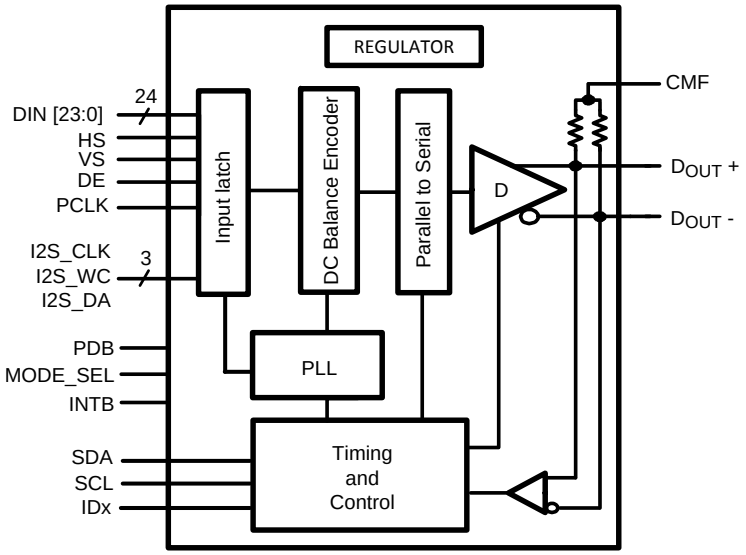
The DS90UB925Q-Q1 serializer transmits a 35-bit symbol over a single serial FPD-Link III pair operating up to 2.975 Gbps line rate. The serial stream contains an embedded clock, video control signals and DC-balanced video data and audio data which enhance signal quality to support AC coupling. The serializer is intended for use with the DS90UB926Q-Q1 deserializer, but is also backward compatible with DS90UR906Q or DS90UR908Q FPD-Link II deserializer.

The DS90UB925Q-Q1 serializer and DS90UB926Q-Q1 deserializer incorporate an I^2C compatible interface. The I^2C compatible interface allows programming of serializer or deserializer devices from a local host controller. In addition, the devices incorporate a bidirectional control channel (BCC) that allows communication between serializer/deserializer as well as remote I^2C slave devices.

The bidirectional control channel is implemented via embedded signaling in the high-speed forward channel (serializer to deserializer) as well as lower speed signaling in the reverse channel (deserializer to serializer). Through this interface, the BCC provides a mechanism to bridge I^2C transactions across the serial link from one I^2C bus to another. The implementation allows for arbitration with other I^2C compatible masters at either side of the serial link.

There are two operating modes available on DS90UB925Q-Q1, display mode and camera mode. In display mode, I^2C transactions originate from the host controller attached to the serializer and target either the deserializer or an I^2C slave attached to the deserializer. Transactions are detected by the I^2C slave in the serializer and forwarded to the I^2C master in the deserializer. Similarly, in camera mode, I^2C transactions originate from a controller attached to the deserializer and target either the serializer or an I^2C slave attached to the serializer. Transactions are detected by the I^2C slave in the deserializer and forwarded to the I^2C master in the serializer.

7.2 Functional Block Diagram



DS90UB925Q-Q1 Serializer

7.3 Feature Description

7.3.1 High Speed Forward Channel Data Transfer

The High Speed Forward Channel (HS_FC) is composed of 35 bits of data containing DIN[23:0] or RGB[7:0] or YUV data, sync signals, I^2C, and I2S audio transmitted from Serializer to Deserializer. Figure 11 illustrates the serial stream per PCLK cycle. This data payload is optimized for signal transmission over an AC coupled link. Data is randomized, balanced and scrambled.

Feature Description (continued)

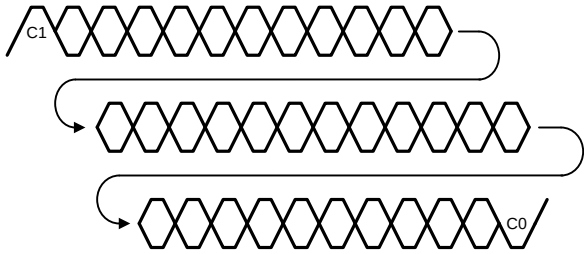


Figure 11. FPD-Link III Serial Stream

The device supports clocks in the range of 5 MHz to 85 MHz. The application payload rate is 2.975 Gbps maximum (175 Mbps minimum) with the actual line rate of 2.975 Gbps maximum and 525 Mbps Minimum.

7.3.2 Low Speed Back Channel Data Transfer

The Low-Speed Backward Channel (LS_BC) of the DS90UB925Q-Q1 provides bidirectional communication between the display and host processor. The information is carried back from the Deserializer to the Serializer per serial symbol. The back channel control data is transferred over the single serial link along with the high-speed forward data, DC balance coding and embedded clock information. This architecture provides a backward path across the serial link together with a high speed forward channel. The back channel contains the I^2C, CRC and 4 bits of standard GPIO information with 10 Mbps line rate.

7.3.3 Backward Compatible Mode

The DS90UB925Q-Q1 is also backward compatible to DS90UR906Q and DS90UR908Q FPD Link II deserializers at 5-65 MHz of PCLK. It transmits 28-bits of data over a single serial FPD-Link II pair operating at the line rate of 140 Mbps to 1.82 Gbps. The backward configuration mode can be set via MODE_SEL pin (Table 4) or the configuration register (Table 6). Note: frequency range = 15 – 65MHz when LFMODE = 0 and frequency range = 5 – <15MHz when LFMODE = 1.

7.3.4 Common Mode Filter Pin (CMF)

The serializer provides access to the center tap of the internal termination. A capacitor must be placed on this pin for additional common-mode filtering of the differential pair. This can be useful in high noise environments for additional noise rejection capability. A 0.1 µF capacitor must be connected to this pin to Ground.

7.3.5 Video Control Signal Filter

When operating the devices in Normal Mode, the Video Control Signals (DE, HS, VS) have the following restrictions:

- Normal Mode with Control Signal Filter Enabled: DE and HS — Only 2 transitions per 130 clock cycles are transmitted, the transition pulse must be 3 PCLK or longer.
- Normal Mode with Control Signal Filter Disabled: DE and HS — Only 2 transitions per 130 clock cycles are transmitted, no restriction on minimum transition pulse.
- VS — Only 1 transition per 130 clock cycles are transmitted, minimum pulse width is 130 clock cycles.

Video Control Signals are defined as low frequency signals with limited transitions. Glitches of a control signal can cause a visual display error. This feature allows for the chipset to validate and filter out any high frequency noise on the control signals. See Figure 12.

Feature Description (continued)

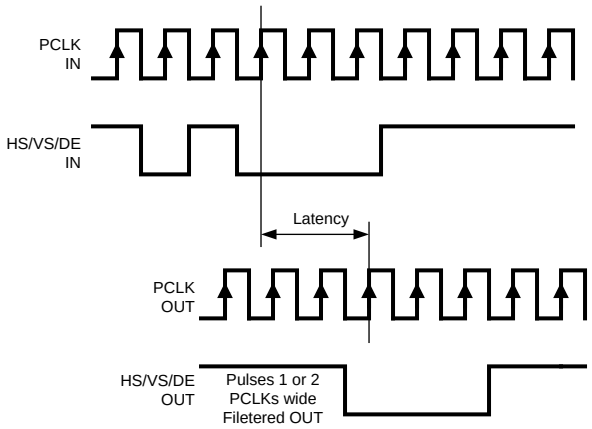


Figure 12. Video Control Signal Filter Waveform

7.3.6 EMI Reduction Features

7.3.6.1 Input SSC Tolerance (SSCT)

The DS90UB925Q-Q1 serializer is capable of tracking a triangular input spread spectrum clocking (SSC) profile up to ±2.5% amplitude deviations (center spread), up to 35 kHz modulation at 5–85 MHz, from a host source.

7.3.7 LVCMOS V_{DDIO} Option

1.8 V or 3.3 V Inputs and Outputs are powered from a separate V_{DDIO} supply to offer compatibility with external system interface signals.

NOTE

When configuring the V_{DDIO} power supplies, all the single-ended data and control input pins for device need to scale together with the same operating V_{DDIO} levels.

7.3.8 Power Down (PDB)

The Serializer has a PDB input pin to ENABLE or POWER DOWN the device. This pin can be controlled by the host or through the V_{DDIO}, where V_{DDIO} = 3.0V to 3.6V or V_{DD33}. To save power disable the link when the display is not needed (PDB = LOW). When the pin is driven by the host, make sure to release it after V_{DD33} and V_{DDIO} have reached final levels; no external components are required. In the case of driven by the V_{DDIO} = 3.0V to 3.6V or V_{DD33} directly, a 10 kohm resistor to the V_{DDIO} = 3.0V to 3.6V or V_{DD33} , and a >10uF capacitor to the ground are required (See Figure 23).

7.3.9 Remote Auto Power Down Mode

The Serializer features a remote auto power down mode. During the power down mode of the pairing deserializer, the Serializer enters the remote auto power down mode. In this mode, the power dissipation of the Serializer is reduced significantly. When the Deserializer is powered up, the Serializer enters the normal power on mode automatically. This feature is enabled through the register bit 0x01[7] Table 6.

7.3.10 Input PCLK Loss Detect

The serializer can be programmed to enter a low power SLEEP state when the input clock (PCLK) is lost. A clock loss condition is detected when PCLK drops below approximately 1MHz. When a PCLK is detected again, the serializer will then lock to the incoming PCLK. Note – when PCLK is lost, the Serial Control Bus Registers values are still RETAINED.

Feature Description (continued)

7.3.11 Serial Link Fault Detect

The serial link fault detection is able to detect any of following seven (7) conditions:

1. cable open
2. “+” to “-“ short
3. “+” short to GND
4. “-“ short to GND
5. “+” short to battery
6. “-“ short to battery
7. Cable is linked correctly

If any one of the fault conditions occurs, The Link Detect Status is 0 (cable is not detected) on bit 0 of address 0x0C Table 6.

7.3.12 Pixel Clock Edge Select (RFB)

The RFB control register bit selects which edge of the Pixel Clock is used. For the serializer, this pin determines the edge that the data is latched on. If RFB is HIGH (‘1’), data is latched on the Rising edge of the PCLK. If RFB is LOW (‘0’), data is latched on the Falling edge of the PCLK.

7.3.13 Low Frequency Optimization (LFMODE)

The LFMODE is set via register (0x04[1:0]) or MODE_SEL Pin 24 (Table 4). It controls the operating frequency of the serializer. If LFMODE is Low (default), the PCLK frequency is between 15 MHz and 85 MHz. If LFMODE is High, the PCLK frequency is between 5 MHz and <15 MHz. Please note when the device LFMODE is changed, a PDB reset is required.

7.3.14 Interrupt Pin — Functional Description And Usage (INTB)

1. On DS90UB925, set register 0xC6[5] = 1 and 0xC6[0] = 1
2. DS90UB926Q-Q1 deserializer INTB_IN (pin 16) is set LOW by some downstream device.
3. DS90UB925Q-Q1 serializer pulls INTB (pin 31) LOW. The signal is active low, so a LOW indicates an interrupt condition.
4. External controller detects INTB = LOW; to determine interrupt source, read ISR register .
5. A read to ISR will clear the interrupt at the DS90UB925, releasing INTB.
6. The external controller typically must then access the remote device to determine downstream interrupt source and clear the interrupt driving INTB_IN. This would be when the downstream device releases the INTB_IN (pin 16) on the DS90UB926Q-Q1. The system is now ready to return to step (1) at next falling edge of INTB_IN.

7.3.15 Internal Pattern Generation

The DS90UB925Q-Q1 serializer supports the internal pattern generation feature. It allows basic testing and debugging of an integrated panel through the FPD-Link III output stream. The test patterns are simple and repetitive and allow for a quick visual verification of panel operation. As long as the device is not in power down mode, the test pattern will be displayed even if no parallel input is applied. If no PCLK is received, the test pattern can be configured to use a programmed oscillator frequency. For detailed information, refer to Application Note AN-2198 (SNLA132).

7.3.16 GPIO[3:0] and GPO_REG[8:4]

In 18-bit RGB operation mode, the optional R[1:0] and G[1:0] of the DS90UB925Q-Q1 can be used as the general purpose IOs GPIO[3:0] in either forward channel (Inputs) or back channel (Outputs) application.

7.3.16.1 GPIO[3:0] Enable Sequence

See Table 1 for the GPIO enable sequencing.

Feature Description (continued)

Step 1: Enable the 18-bit mode either through the configuration register bit Table 6 on DS90UB925Q-Q1 only. DS90UB926Q-Q1 is automatically configured as in the 18-bit mode.

Step 2: To enable GPIO3 forward channel, write 0x03 to address 0x0F on DS90UB925Q-Q1, then write 0x05 to address 0x1F on DS90UB926Q-Q1.

Table 1. GPIO Enable Sequencing Table

#	DESCRIPTION	DEVICE	FORWARD CHANNEL	BACK CHANNEL
1	Enable 18-bit mode	DS90UB925Q-Q1	0x12 = 0x04	0x12 = 0x04
		DS90UB926Q-Q1	Auto Load from DS90UB925Q-Q1	Auto Load from DS90UB925Q-Q1
2	GPIO3	DS90UB925Q-Q1	0x0F = 0x03	0x0F = 0x05
		DS90UB926Q-Q1	0x1F = 0x05	0x1F = 0x03
3	GPIO2	DS90UB925Q-Q1	0x0E = 0x30	0x0E = 0x50
		DS90UB926Q-Q1	0x1E = 0x50	0x1E = 0x30
4	GPIO1	DS90UB925Q-Q1	0x0E = 0x03	0x0E = 0x05
		DS90UB926Q-Q1	0x1E = 0x05	0x1E = 0x03
5	GPIO0	DS90UB925Q-Q1	0x0D = 0x93	0x0D = 0x95
		DS90UB926Q-Q1	0x1D = 0x95	0x1D = 0x93

7.3.16.2 GPO_REG[8:4] Enable Sequence

GPO_REG[8:4] are the outputs only pins. They must be programmed through the local register bits. See Table 2 for the GPO_REG enable sequencing.

Step 1: Enable the 18-bit mode either through the configuration register bit Table 6 on DS90UB925Q-Q1 only. DS90UB926Q-Q1 is automatically configured as in the 18-bit mode.

Step 2: To enable GPO_REG8 outputs an “1”, write 0x90 to address 0x11 on DS90UB925Q.

Table 2. GPO_REG Enable Sequencing Table

#	DESCRIPTION	DEVICE	LOCAL ACCESS	LOCAL OUTPUT
1	Enable 18-bit mode	DS90UB925Q-Q1	0x12 = 0x04	
2	GPO_REG8	DS90UB925Q-Q1	0x11 = 0x90	“1”
			0x11 = 0x10	“0”
3	GPO_REG7	DS90UB925Q-Q1	0x11 = 0x09	“1”
			0x11 = 0x01	“0”
4	GPO_REG6	DS90UB925Q-Q1	0x10 = 0x90	“1”
			0x10 = 0x10	“0”
5	GPO_REG5	DS90UB925Q-Q1	0x10 = 0x09	“1”
			0x10 = 0x01	“0”
6	GPO_REG4	DS90UB925Q-Q1	0x0F = 0x90	“1”
			0x0F = 0x10	“0”

7.3.17 I2S Transmitting

In normal 24-bit RGB operation mode, the DS90UB925Q-Q1 supports 3 bits of I2S. They are I2S_CLK, I2S_WC and I2S_DA. The optionally packetized audio information can be transmitted during the video blanking (data island transport) or during active video (forward channel frame transport). Note: The bit rates of any I2S bits must maintain one fourth of the PCLK rate.

7.3.17.1 Secondary I2S Channel

In I2S Channel B operation mode, the secondary I2S data (I2S_DB) can be used as the additional I2S audio in addition to the 3–bit of I2S. The I2S_DB input must be synchronized to I2S_CLK and aligned with I2S_DA and I2S_WC at the input to the serializer. This operation mode is enabled through either the MODE_SEL pin (Table 4) or through the register bit 0x12[0] (Table 6).

Table 3 covers the range of I2S sample rates.

Table 3. Audio Interface Frequencies

SAMPLE RATE (kHz)	I2S DATA WORD SIZE (BITS)	I2S CLK (MHz)
32	16	1.024
44.1	16	1.411
48	16	1.536
96	16	3.072
192	16	6.144
32	24	1.536
44.1	24	2.117
48	24	2.304
96	24	4.608
192	24	9.216
32	32	2.048
44.1	32	2.822
48	32	3.072
96	32	6.144
192	32	12.288

7.3.18 Built In Self Test (BIST)

An optional At-Speed Built In Self Test (BIST) feature supports the testing of the high speed serial link and the low- speed back channel. This is useful in the prototype stage, equipment production, in-system test and also for system diagnostics. Note: BIST is not available in backwards compatible mode.

7.3.18.1 BIST Configuration and Status

The BIST mode is enabled at the deseralizer by the Pin select (Pin 44 BISTEN and Pin 16 BISTC) or configuration register (Table 6) through the deserializer. When LFMODE = 0, the pin based configuration defaults to external PCLK or 33 MHz internal Oscillator clock (OSC) frequency. In the absence of PCLK, the user can select the desired OSC frequency (default 33 MHz or 25MHz) through the register bit. When LFMODE = 1, the pin based configuration defaults to external PCLK or 12.5MHz MHz internal Oscillator clock (OSC) frequency.

When BISTEN of the deserializer is high, the BIST mode enable information is sent to the serializer through the Back Channel. The serializer outputs a test pattern and drives the link at speed. The deserializer detects the test pattern and monitors it for errors. The PASS output pin toggles to flag any payloads that are received with 1 to 35 bit errors.

The BIST status is monitored real time on PASS pin. The result of the test is held on the PASS output until reset (new BIST test or Power Down). A high on PASS indicates NO ERRORS were detected. A Low on PASS indicates one or more errors were detected. The duration of the test is controlled by the pulse width applied to the deserializer BISTEN pin. This BIST feature also contains a Link Error Count and a Lock Status. If the connection of the serial link is broken, then the link error count is shown in the register. When the PLL of the deserializer is locked or unlocked, the lock status can be read in the register. See Table 6.

7.3.18.1.1 Sample BIST Sequence

See Figure 13 for the BIST mode flow diagram.

Step 1: For the DS90UB925Q-Q1 and DS90UB926Q-Q1 FPD-Link III chipset, BIST Mode is enabled via the BISTEN pin of DS90UB926Q-Q1 FPD-Link III deserializer. The desired clock source is selected through BISTC pin.

Step 2: The DS90UB925Q-Q1 serializer is woken up through the back channel if it is not already on. The all zero pattern on the data pins is sent through the FPD-Link III to the deserializer. Once the serializer and the deserializer are in BIST mode and the deserializer acquires Lock, the PASS pin of the deserializer goes high and BIST starts checking the data stream. If an error in the payload (1 to 35) is detected, the PASS pin will switch low for one half of the clock period. During the BIST test, the PASS output can be monitored and counted to determine the payload error rate.

Step 3: To Stop the BIST mode, the deserializer BISTEN pin is set Low. The deserializer stops checking the data. The final test result is held on the PASS pin. If the test ran error free, the PASS output will be High. If there was one or more errors detected, the PASS output will be Low. The PASS output state is held until a new BIST is run, the device is RESET, or Powered Down. The BIST duration is user controlled by the duration of the BISTEN signal.

Step 4: The Link returns to normal operation after the deserializer BISTEN pin is low. Figure 14 shows the waveform diagram of a typical BIST test for two cases. Case 1 is error free, and Case 2 shows one with multiple errors. In most cases it is difficult to generate errors due to the robustness of the link (differential data transmission etc.), thus they may be introduced by greatly extending the cable length, faulting the interconnect, reducing signal condition enhancements (Rx Equalization).

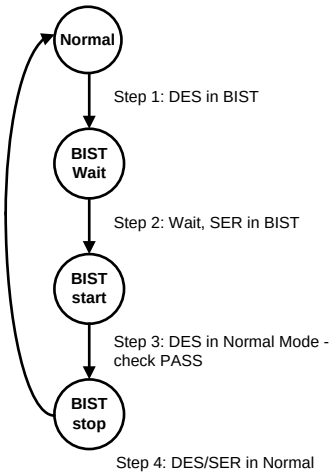


Figure 13. Bist Mode Flow Diagram

7.3.18.2 Forward Channel And Back Channel Error Checking

While in BIST mode, the serializer stops sampling RGB input pins and switches over to an internal all-zero pattern. The internal all-zeroes pattern goes through scrambler, dc-balancing etc. and goes over the serial link to the deserializer. The deserializer on locking to the serial stream compares the recovered serial stream with all-zeroes and records any errors in status registers and dynamically indicates the status on PASS pin. The deserializer then outputs a SSO pattern on the RGB output pins.

The back-channel data is checked for CRC errors once the serializer locks onto back-channel serial stream as indicated by link detect status (register bit 0x0C[0]). The CRC errors are recorded in an 8-bit register. The register is cleared when the serializer enters the BIST mode. As soon as the serializer exits BIST mode, the functional mode CRC register starts recording the CRC errors. The BIST mode CRC error register is active in BIST mode only and keeps the record of last BIST run until cleared or enters BIST mode again.

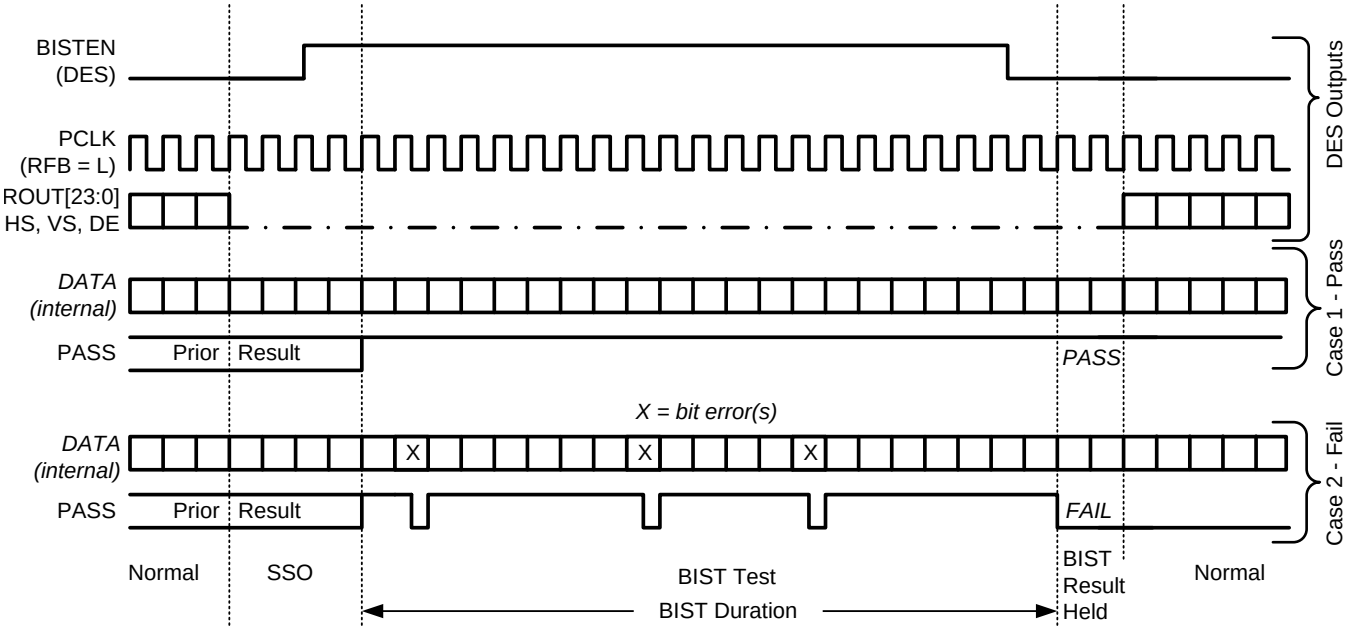


Figure 14. Bist Waveforms

7.4 Device Functional Modes

7.4.1 Configuration Select (MODE_SEL)

Configuration of the device may be done via the MODE_SEL input pin, or via the configuration register bit. A pull-up resistor and a pull-down resistor of suggested values may be used to set the voltage ratio of the MODE_SEL input (V_{R4}) and V_{DD33} to select one of the other 10 possible selected modes. See Figure 15 and Table 4.

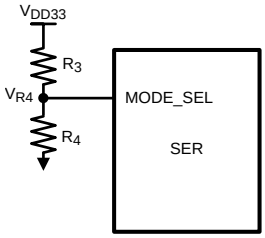


Figure 15. MODE_SEL Connection Diagram

Device Functional Modes (continued)

Table 4. Configuration Select (MODE_SEL)

#	IDEAL RATIO V_{R4}/V_{DD33}	IdeAl V_{R4} (V)	SUGGESTED RESISTOR R3 kΩ (1% tol)	SUGGESTED RESISTOR R4 kΩ (1% tol)	LFMODE	REPEATER	BACKWARD COMPATIBLE	I2S Channel B (18–bit Mode)
1	0	0	Open	40.2 or Any	L	L	L	L
2	0.164	0.541	255	49.9	L	H	L	L
3	0.221	0.729	243	69.8	L	H	L	H
4	0.285	0.941	237	95.3	H	L	L	L
5	0.359	1.185	196	110	H	L	L	H
6	0.453	1.495	169	140	H	H	L	L
7	0.539	1.779	137	158	H	H	L	H
8	0.728	2.402	90.9	243	H	L	H*	L

LFMODE:
L = frequency range is 15 – 85 MHz (Default)
H = frequency range is 5 – <15 MHz
Repeater:
L = Repeater *OFF* (Default)
H = Repeater *ON*
Backward Compatible:
L = Backward Compatible is *OFF* (Default)
H = Backward Compatible is *ON*; DES = DS90UR906Q or DS90UR916Q or DS90UR908Q
– frequency range = 15 - 65 MHz when LFMODE = 0
– frequency range = 5 - <15 MHz when LFMODE = 1
I2S Channel B:
L = I2S Channel B is *OFF*, Normal 24-bit RGB Mode (Default)
H = I2S Channel B is *ON*, 18-bit RGB Mode with I2S_DB Enabled. Note: use of GPIO(s) on unused inputs must be enabled by register.

7.4.2 Repeater Application

The DS90UB925Q-Q1 and DS90UB926Q-Q1 can be configured to extend data transmission over multiple links to multiple display devices. Setting the devices into repeater mode provides a mechanism for transmitting to all receivers in the system.

7.4.2.1 Repeater Configuration

In the repeater application, in this document, the DS90UB925Q-Q1 is referred to as the Transmitter or transmit port (TX), and the DS90UB926Q-Q1 is referred to as the Receiver (RX). Figure 16 shows the maximum configuration supported for Repeater implementations using the DS90UB925Q-Q1 (TX) and DS90UB926Q-Q1 (RX). Two levels of Repeaters are supported with a maximum of three Transmitters per Receiver.

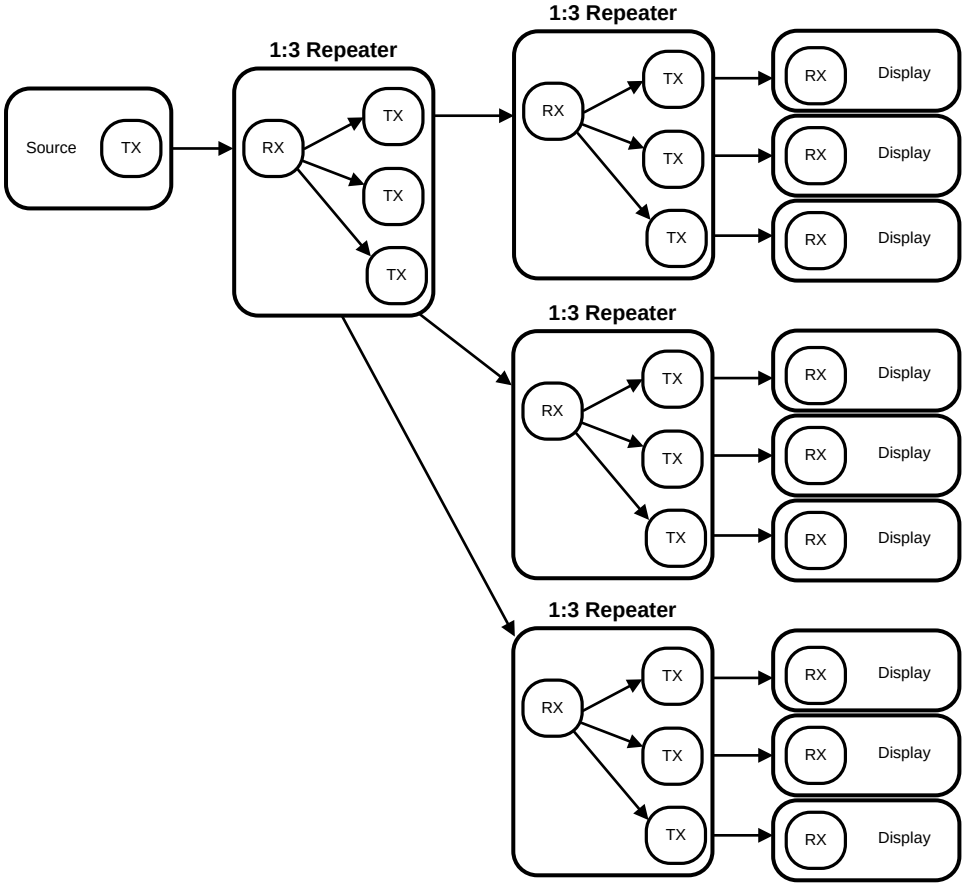


Figure 16. Maximum Repeater Application

In a repeater application, the I2C interface at each TX and RX may be configured to transparently pass I2C communications upstream or downstream to any I2C device within the system. This includes a mechanism for assigning alternate IDs (Slave Aliases) to downstream devices in the case of duplicate addresses.

At each repeater node, the parallel LVCMOS interface fans out to up to three serializer devices, providing parallel RGB video data, HS/VS/DE control signals and, optionally, packetized audio data (transported during video blanking intervals). Alternatively, the I2S audio interface may be used to transport digital audio data between receiver and transmitters in place of packetized audio. All audio and video data is transmitted at the output of the Receiver and is received by the Transmitter.

Figure 17 provides more detailed block diagram of a 1:2 repeater configuration.

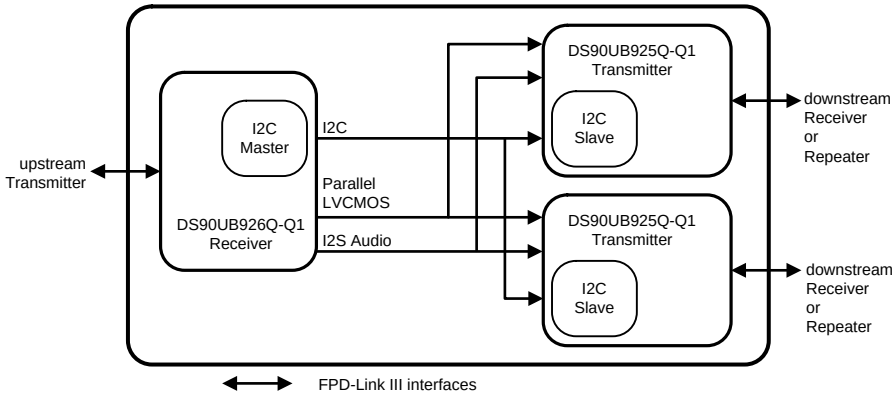


Figure 17. 1:2 Repeater Configuration

7.4.2.2 Repeater Connections

The Repeater requires the following connections between the Receiver and each Transmitter Figure 18.

1. Video Data – Connect PCLK, RGB and control signals (DE, VS, HS).
2. I2C – Connect SCL and SDA signals. Both signals should be pulled up to V_{DD33} with 4.7 kΩ resistors.
3. Audio – Connect I2S_CLK, I2S_WC, and I2S_DA signals.
4. IDx pin – Each Transmitter and Receiver must have an unique I2C address.
5. MODE_SEL pin – All Transmitter and Receiver must be set into the Repeater Mode.
6. Interrupt pin – Connect DS90UB926Q-Q1 INTB_IN pin to DS90UB925Q-Q1 INTB pin. The signal must be pulled up to V_{DDIO}.

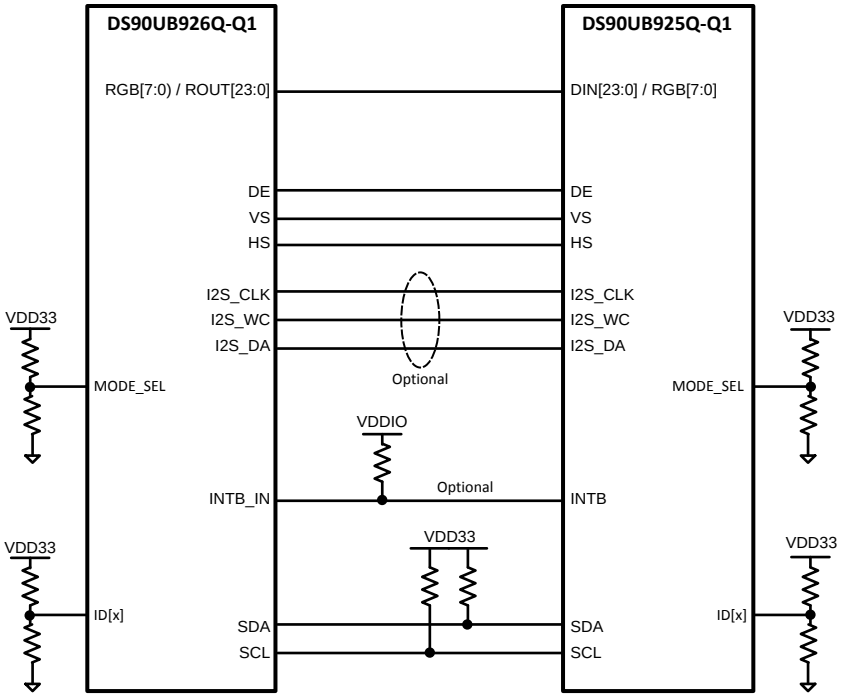


Figure 18. Repeater Connection Diagram

7.5 Programming

The DS90UB925Q-Q1 is configured by the use of a serial control bus that is I2C protocol compatible. Multiple serializer devices may share the serial control bus since 9 device addresses are supported. Device address is set via R_1 and R_2 values on IDx pin. See Figure 19.

The serial control bus consists of two signals and a configuration pin. The SCL is a Serial Bus Clock Input / Output. The SDA is the Serial Bus Data Input / Output signal. Both SCL and SDA signals require an external pull-up resistor to V_{DD33}. For most applications a 4.7 k pull-up resistor to V_{DD33} may be used. The resistor value may be adjusted for capacitive loading and data rate requirements. The signals are either pulled High, or driven Low.

Programming (continued)

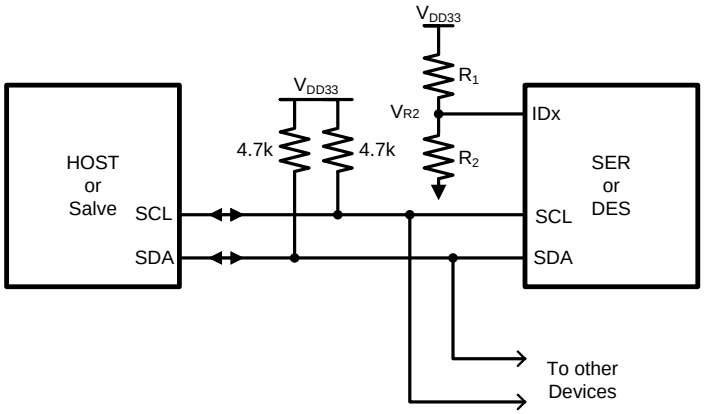


Figure 19. Serial Control Bus Connection

The configuration pin is the IDx pin. This pin sets one of 9 possible device addresses. A pull-up resistor and a pull-down resistor of suggested values may be used to set the voltage ratio of the IDx input (V_{R2}) and V_{DD33} to select one of the other 9 possible addresses. See Table 5.

Table 5. Serial Control Bus Addresses for IDx

#	IDEAL RATIO V_{R2} / V_{DD33}	IDEAL V_{R2} (V)	SUGGESTED RESISTOR R1 kΩ (1% tol)	SUGGESTED RESISTOR R2 kΩ (1% tol)	ADDRESS 7'b	ADDRESS 8'b APPENDED
1	0	0	Open	40.2 or Any	0x0C	0x18
2	0.121	0.399	294	40.2	0x0D	0x1A
3	0.152	0.502	280	49.9	0x0E	0x1C
4	0.180	0.594	137	30.1	0x0F	0x1E
5	0.208	0.685	118	30.9	0x10	0x20
6	0.303	0.999	115	49.9	0x13	0x26
7	0.345	1.137	102	53.6	0x14	0x28
8	0.389	1.284	115	73.2	0x15	0x2A
9	0.727	2.399	90.9	243	0x1B	0x36

The Serial Bus protocol is controlled by START, START-Repeated, and STOP phases. A START occurs when SCL transitions Low while SDA is High. A STOP occurs when SDA transition High while SCL is also HIGH. See Figure 20.

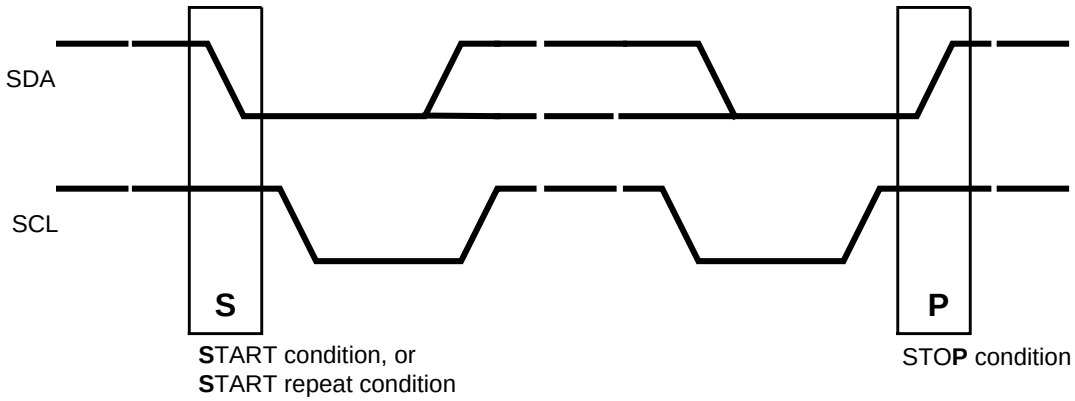


Figure 20. Start and Stop Conditions

To communicate with a remote device, the host controller (master) sends the slave address and listens for a response from the slave. This response is referred to as an acknowledge bit (ACK). If a slave on the bus is addressed correctly, it Acknowledges (ACKs) the master by driving the SDA bus low. If the address doesn't match a device's slave address, it Not-acknowledges (NACKs) the master by letting SDA be pulled High. ACKs also occur on the bus when data is being transmitted. When the master is writing data, the slave ACKs after every data byte is successfully received. When the master is reading data, the master ACKs after every data byte is received to let the slave know it wants to receive another data byte. When the master wants to stop reading, it NACKs after the last data byte and creates a stop condition on the bus. All communication on the bus begins with either a Start condition or a Repeated Start condition. All communication on the bus ends with a Stop condition. A READ is shown in Figure 21 and a WRITE is shown in Figure 22.

If the Serial Bus is not required, the three pins may be left open (NC).

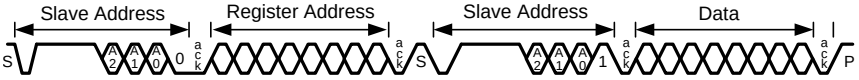


Figure 21. Serial Control Bus — Read

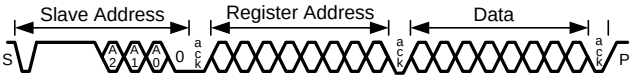


Figure 22. Serial Control Bus — Write

7.6 Register Maps

Table 6. Serial Control Bus Registers

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
0	0x00	I2C Device ID	7:1	RW		Device ID	7–bit address of Serializer
			0	RW		ID Setting	I2C ID Setting 1: Register I2C Device ID (Overrides IDx pin) 0: Device ID is from IDx pin
1	0x01	Reset	7	RW	0x00	Remote Auto Power Down	Remote Auto Power Down 1: Power down when no Bidirectional Control Channel link is detected 0: Do not power down when no Bidirectional Control Channel link is detected
			6:2				***Reserved***
			1	RW		Digital RESET1	Reset the entire digital block including registers This bit is self-clearing. 1: Reset 0: Normal operation
			0	RW		Digital RESET0	Reset the entire digital block except registers This bit is self-clearing 1: Reset 0: Normal operation

Register Maps (continued)

Table 6. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
3	0x03	Configuration [0]	7	RW	0xD2	Back channel CRC Checker Enable	Back Channel Check Enable 1: Enable 0: Disable
			6				***Reserved***
			5	RW		I2C Remote Write Auto Acknowledge	Automatically Acknowledge I2C Remote Write When enabled, I2C writes to the Deserializer (or any remote I2C Slave, if I2C PASS ALL is enabled) are immediately acknowledged without waiting for the Deserializer to acknowledge the write. This allows higher throughput on the I2C bus 1: Enable 0: Disable
			4	RW		Filter Enable	HS, VS, DE two clock filter When enabled, pulses less than two full PCLK cycles on the DE, HS, and VS inputs will be rejected 1: Filtering enable 0: Filtering disable
			3	RW		I2C Pass-through	I2C Pass-Through Mode 1: Pass-Through Enabled 0: Pass-Through Disabled
			2				***Reserved***
			1	RW		PCLK Auto	Switch over to internal OSC in the absence of PCLK 1: Enable auto-switch 0: Disable auto-switch
			0	RW		TRFB	Pixel Clock Edge Select 1: Parallel Interface Data is strobed on the Rising Clock Edge. 0: Parallel Interface Data is strobed on the Falling Clock Edge.

Register Maps (continued)

Table 6. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
4	0x04	Configuration [1]	7	RW	0x80	Failsafe State	Input Failsafe State 1: Failsafe to Low 0: Failsafe to High
			6				***Reserved***
			5	RW		CRC Error Reset	Clear back channel CRC Error Counters This bit is NOT self-clearing 1: Clear Counters 0: Normal Operation
			4			RGB DE Gate	1: Gate RGB data with DE in Backward Compatibility mode and with Non-HDCP Deserializer 0: Pass RGB data independent of DE in Backward Compatibility mode and Non-HDCP operation (default)
			3	RW		Backward Compatible select by pin or register control	Backward Compatible (BC) mode set by MODE_SEL pin or register 1: BC is set by register bit. Use register bit reg_0x04[2] to set BC Mode 0: BC is set by MODE_SEL pin.
			2	RW		Backward Compatible Mode Select	Backward compatible (BC) mode to DS90UR906Q or DS90UR908Q, if reg_0x04[3] = 1 1: Backward compatible with DS90UR906Q or DS90UR908Q 0: Backward Compatible is *OFF* (default)
			1	RW		LFMODE select by pin or register control	Frequency range is set by MODE_SEL pin or register 1: Frequency range is set by register. Use register bit reg_0x04[0] to set LFMODE 0: Frequency range is set by MODE_SEL pin.
			0	RW		LFMODE	Frequency range select 1: PCLK range = 5MHz - <15 MHz), if reg_0x04[1] = 1 0: PCLK range = 15MHz - 85MHz (default)
5	0x05	I2C Control	7:5		0x00		***Reserved***
			4:3	RW		SDA Output Delay	SDA output delay Configures output delay on the SDA output. Setting this value will increase output delay in units of 40ns. Nominal output delay values for SCL to SDA are 00: 240ns 01: 280ns 10: 320ns 11: 360ns
			2	RW		Local Write Disable	Disable remote writes to local registers Setting the bit to a 1 prevents remote writes to local device registers from across the control channel. It prevents writes to the Serializer registers from an I2C master attached to the Deserializer. Setting this bit does not affect remote access to I2C slaves at the Serializer
			1	RW		I2C Bus Timer Speedup	Speed up I2C bus watchdog timer 1: Watchdog timer expires after ~50 ms. 0: Watchdog Timer expires after ~1 s
			0	RW		I2C Bus timer Disable	Disable I2C bus watchdog timer When the I2C watchdog timer may be used to detect when the I2C bus is free or hung up following an invalid termination of a transaction. If SDA is high and no signalling occurs for ~1 s, the I2C bus assumes to be free. If SDA is low and no signaling occurs, the device attempts to clear the bus by driving 9 clocks on SCL

Register Maps (continued)

Table 6. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
6	0x06	DES ID	7:1	RW	0x00	DES Device ID	7-bit Deserializer Device ID Configures the I2C Slave ID of the remote Deserializer. A value of 0 in this field disables I2C access to the remote Deserializer. This field is automatically configured by the Bidirectional Control Channel once RX Lock has been detected. Software may overwrite this value, but should also assert the FREEZE DEVICE ID bit to prevent overwriting by the Bidirectional Control Channel.
			0	RW		Device ID Frozen	Freeze Deserializer Device ID Prevents autoloading of the Deserializer Device ID by the Bidirectional Control Channel. The ID will be frozen at the value written.
7	0x07	Slave ID	7:1	RW	0x00	Slave Device ID	7-bit Remote Slave Device ID Configures the physical I2C address of the remote I2C Slave device attached to the remote Deserializer. If an I2C transaction is addressed to the Slave Device Alias ID, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer
			0				***Reserved***
8	0x08	Slave Alias	7:1	RW	0x00	Slave Device Alias ID	7-bit Remote Slave Device Alias ID Assigns an Alias ID to an I2C Slave device attached to the remote Deserializer. The transaction will be remapped to the address specified in the Slave ID register. A value of 0 in this field disables access to the remote I2C Slave.
			0				***Reserved***
10	0x0A	CRC Errors	7:0	R	0x00	CRC Error LSB	Number of back channel CRC errors – 8 least significant bits
11	0x0B		7:0	R	0x00	CRC Error MSB	Number of back channel CRC errors – 8 most significant bits
12	0x0C	General Status	7:4		0x00		***Reserved***
			3	R		BIST CRC Error	Back channel CRC error during BIST communication with Deserializer. The bit is cleared upon loss of link, restart of BIST, or assertion of CRC ERROR RESET in register 0x04.
			2	R		PCLK Detect	PCLK Status 1: Valid PCLK detected 0: Valid PCLK not detected
			1	R		DES Error	Back channel CRC error during communication with Deserializer. The bit is cleared upon loss of link or assertion of CRC ERROR RESET in register 0x04.
			0	R		LINK Detect	LINK Status 1: Cable link detected 0: Cable link not detected (Fault Condition)

Register Maps (continued)

Table 6. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
13	0x0D	Revision ID and GPIO0 Configuration	7:4	R	0xA0	Rev-ID	Revision ID: 1010 Production Device
			3	RW		GPIO0 Output Value	Local GPIO output value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled.
			2	RW		GPIO0 Remote Enable	Remote GPIO control 1: Enable GPIO control from remote Deserializer. The GPIO pin will be an output, and the value is received from the remote Deserializer. 0: Disable GPIO control from remote Deserializer.
			1	RW		GPIO0 Direction	Local GPIO Direction 1: Input 0: Output
			0	RW		GPIO0 Enable	GPIO function enable 1: Enable GPIO operation 0: Enable normal operation
14	0x0E	GPIO2 and GPIO1 Configurations	7	RW	0x00	GPIO2 Output Value	Local GPIO output value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled.
			6	RW		GPIO2 Remote Enable	Remote GPIO control 1: Enable GPIO control from remote Deserializer. The GPIO pin will be an output, and the value is received from the remote Deserializer. 0: Disable GPIO control from remote Deserializer.
			5	RW		GPIO2 Direction	Local GPIO Direction 1: Input 0: Output
			4	RW		GPIO2 Enable	GPIO function enable 1: Enable GPIO operation 0: Enable normal operation
			3	RW		GPIO1 Output Value	Local GPIO output value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled.
			2	RW		GPIO1 Remote Enable	Remote GPIO control 1: Enable GPIO control from remote Deserializer. The GPIO pin will be an output, and the value is received from the remote Deserializer. 0: Disable GPIO control from remote Deserializer.
			1	RW		GPIO1 Direction	Local GPIO Direction 1: Input 0: Output
			0	RW		GPIO1 Enable	GPIO function enable 1: Enable GPIO operation 0: Enable normal operation

Register Maps (continued)

Table 6. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
15	0x0F	GPO_REG4 and GPIO3 Configurations	7	RW	0x00	GPO_REG 4 Output Value	Local GPO_REG4 output value This value is output on the GPO pin when the GPO function is enabled. (The local GPO direction is Output, and remote GPO control is disabled)
			6:5				***Reserved***
			4	RW		GPO_REG 4 Enable	GPO_REG4 function enable 1: Enable GPO operation 0: Enable normal operation
			3	RW		GPIO3 Output Value	Local GPIO output value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled.
			2	RW		GPIO3 Remote Enable	Remote GPIO control 1: Enable GPIO control from remote Deserializer. The GPIO pin will be an output, and the value is received from the remote Deserializer. 0: Disable GPIO control from remote Deserializer.
			1	RW		GPIO3 Direction	Local GPIO Direction 1: Input 0: Output
			0	RW		GPIO3 Enable	GPIO function enable 1: Enable GPIO operation 0: Enable normal operation
16	0x10	GPO_REG6 and GPO_REG5 Configurations	7	RW	0x00	GPO_REG 6 Output Value	Local GPO_REG6 output value This value is output on the GPO pin when the GPO function is enabled. (The local GPO direction is Output, and remote GPO control is disabled)
			6:5				***Reserved***
			4	RW		GPO_REG 6 Enable	GPO_REG6 function enable 1: Enable GPO operation 0: Enable normal operation
			3	RW		GPO_REG 5 Output Value	Local GPO_REG5 output value This value is output on the GPO pin when the GPO function is enabled, the local GPO direction is Output, and remote GPO control is disabled.
			2:1				***Reserved***
			0	RW		GPO_REG 5 Enable	GPO_REG5 function enable 1: Enable GPO operation 0: Enable normal operation

Register Maps (continued)

Table 6. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
17	0x11	GPO_REG8 and GPO_REG7 Configurations	7	RW	0x00	GPO_REG 8 Output Value	Local GPO_REG8 output value This value is output on the GPO pin when the GPO function is enabled. (The local GPO direction is Output, and remote GPO control is disabled)
			6:5				***Reserved***
			4	RW		GPO_REG 8 Enable	GPO_REG8 function enable 1: Enable GPO operation 0: Enable normal operation
			3	RW		GPO_REG 7 Output Value	Local GPO_REG7 output value This value is output on the GPO pin when the GPO function is enabled, the local GPO direction is Output, and remote GPO control is disabled.
			2:1				***Reserved***
			0	RW		GPO_REG 7 Enable	GPO_REG7 function enable 1: Enable GPO operation 0: Enable normal operation
18	0x12	Data Path Control	7:6		0x00		***Reserved***
			5	RW		DE Polarity	The bit indicates the polarity of the DE (Data Enable) signal. 1: DE is inverted (active low, idle high) 0: DE is positive (active high, idle low)
			4	RW		I2S Repeater Regen	I2S Repeater Regeneration 1: Repeater regenerate I2S from I2S pins 0: Repeater pass through I2S from video pins
			3	RW		I2S Channel B Enable Override	I2S Channel B Enable 1: Set I2S Channel B Enable from reg_12[0] 0: Set I2S Channel B Enable from MODE_SEL pin
			2	RW		18-bit Video Select	18–bit video select 1: Select 18-bit video mode Note: use of GPIO(s) on unused inputs must be enabled by register. 0: Select 24-bit video mode
			1	RW		I2S Transport Select	I2S Transport Mode Slect 1: Enable I2S Data Forward Channel Frame Transport 0: Enable I2S Data Island Transport
			0	RW		I2S Channel B Enable	I2S Channel B Enable 1: Enable I2S Channel B on B1 input 0: I2S Channel B disabled
19	0x13	Mode Status	7:5		0x10		***Reserved***
			4	R		MODE_SEL	MODE_SEL Status 1: MODE_SEL decode circuit is completed 0: MODE_SEL decode circuit is not completed
			3	R		Low Frequency Mode	Low Frequency Mode Status 1: Low frequency (5 - <15 MHz) 0: Normal frequency (15 - 85 MHz)
			2	R		Repeater Mode	Repeater Mode Status 1: Repeater mode *ON* 0: Repeater Mode *OFF*
			1	R		Backward Compatible Mode	Backward Compatible Mode Status 1: Backward compatible *ON* 0: Backward compatible *OFF*
			0	R		I2S Channel B Mode	I2S Channel B Mode Status 1: I2S Channel B *ON*, 18-bit RGB mode with I2S_DB enabled 0: I2S Channel B *OFF*; normal 24-bit RGB mode

Register Maps (continued)

Table 6. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
20	0x14	Oscillator Clock Source and BIST Status	7:3		0x00		***Reserved***
			2:1	RW		OSC Clock Source	OSC Clock Source (When LFMODE = 1, Oscillator = 12.5MHz ONLY) 00: External Pixel Clock 01: 33 MHz Oscillator 10: Reserved 11: 25 MHz Oscillator
			0	R		BIST Enable Status	BIST status 1: Enabled 0: Disabled
22	0x16	BCC Watchdog Control	7:1	RW	0xFE	Timer Value	The watchdog timer allows termination of a control channel transaction if it fails to complete within a programmed amount of time. This field sets the Bidirectional Control Channel Watchdog Timeout value in units of 2 ms. This field should not be set to 0
			0	RW		Timer Control	Disable Bidirectional Control Channel Watchdog Timer 1: Disables BCC Watchdog Timer operation 0: Enables BCC Watchdog Timer operation
23	0x17	I2C Control	7	RW	0x5E	I2C Pass All	I2C Control 1: Enable Forward Control Channel pass-through of all I2C accesses to I2C Slave IDs that do not match the Serializer I2C Slave ID. 0: Enable Forward Control Channel pass-through only of I2C accesses to I2C Slave IDs matching either the remote Deserializer Slave ID or the remote Slave ID.
			6				***Reserved***
			5:4	RW		SDA Hold Time	Internal SDA Hold Time Configures the amount of internal hold time provided for the SDA input relative to the SCL input. Units are 40 ns
			3:0	RW		I2C Filter Depth	Configures the maximum width of glitch pulses on the SCL and SDA inputs that will be rejected. Units are 5 ns
24	0x18	SCL High Time	7:0	RW	0xA1	SCL HIGH Time	I2C Master SCL High Time This field configures the high pulse width of the SCL output when the Serializer is the Master on the local I2C bus. Units are 40 ns for the nominal oscillator clock frequency. The default value is set to provide a minimum 5us SCL high time with the internal oscillator clock running at 32.5MHz rather than the nominal 25MHz.
25	0x19	SCL Low Time	7:0	RW	0xA5	SCL LOW Time	I2C SCL Low Time This field configures the low pulse width of the SCL output when the Serializer is the Master on the local I2C bus. This value is also used as the SDA setup time by the I2C Slave for providing data prior to releasing SCL during accesses over the Bidirectional Control Channel. Units are 40 ns for the nominal oscillator clock frequency. The default value is set to provide a minimum 5us SCL low time with the internal oscillator clock running at 32.5MHz rather than the nominal 25MHz.
27	0x1B	BIST BC Error	7:0	R	0x00	BIST Back Channel CRC Error Counter	BIST Mode Back Channel CRC Error Counter This error counter is active only in the BIST mode. It clears itself at the start of the BIST run.

Register Maps (continued)

Table 6. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
100	0x64	Pattern Generator Control	7:4	RW	0x10	Pattern Generator Select	Fixed Pattern Select This field selects the pattern to output when in Fixed Pattern Mode. Scaled patterns are evenly distributed across the horizontal or vertical active regions. This field is ignored when Auto-Scrolling Mode is enabled. The following table shows the color selections in non-inverted followed by inverted color mode 0000: Reserved 0001: White/Black 0010: Black/White 0011: Red/Cyan 0100: Green/Magenta 0101: Blue/Yellow 0110: Horizontally Scaled Black to White/White to Black 0111: Horizontally Scaled Black to Red/Cyan to White 1000: Horizontally Scaled Black to Green/Magenta to White 1001: Horizontally Scaled Black to Blue/Yellow to White 1010: Vertically Scaled Black to White/White to Black 1011: Vertically Scaled Black to Red/Cyan to White 1100: Vertically Scaled Black to Green/Magenta to White 1101: Vertically Scaled Black to Blue/Yellow to White 1110: Custom color (or its inversion) configured in PGRS, PGGS, PGBS registers 1111: Reserved
			3:1				***Reserved***
			0	RW		Pattern Generator Enable	Pattern Generator Enable 1: Enable Pattern Generator 0: Disable Pattern Generator

Register Maps (continued)

Table 6. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
101	0x65	Pattern Generator Configuration	7:5		0x00		***Reserved***
			4	RW		Pattern Generator 18 Bits	18-bit Mode Select 1: Enable 18-bit color pattern generation. Scaled patterns will have 64 levels of brightness and the R, G, and B outputs use the six most significant color bits. 0: Enable 24-bit pattern generation. Scaled patterns use 256 levels of brightness.
			3	RW		Pattern Generator External Clock	Select External Clock Source 1: Selects the external pixel clock when using internal timing. 0: Selects the internal divided clock when using internal timing This bit has no effect in external timing mode (PATGEN_TSEL = 0).
			2	RW		Pattern Generator Timing Select	Timing Select Control 1: The Pattern Generator creates its own video timing as configured in the Pattern Generator Total Frame Size, Active Frame Size. Horizontal Sync Width, Vertical Sync Width, Horizontal Back Porch, Vertical Back Porch, and Sync Configuration registers. 0: the Pattern Generator uses external video timing from the pixel clock, Data Enable, Horizontal Sync, and Vertical Sync signals.
			1	RW		Pattern Generator Color Invert	Enable Inverted Color Patterns 1: Invert the color output. 0: Do not invert the color output.
			0	RW		Pattern Generator Auto-Scroll Enable	Auto-Scroll Enable: 1: The Pattern Generator will automatically move to the next enabled pattern after the number of frames specified in the Pattern Generator Frame Time (PGFT) register. 0: The Pattern Generator retains the current pattern.
102	0x66	Pattern Generator Indirect Address	7:0	RW	0x00	Indirect Address	This 8-bit field sets the indirect address for accesses to indirectly-mapped registers. It should be written prior to reading or writing the Pattern Generator Indirect Data register. See AN-2198 (SNLA132).
103	0x67	Pattern Generator Indirect Data	7:0	RW	0x00	Indirect Data	When writing to indirect registers, this register contains the data to be written. When reading from indirect registers, this register contains the read back value. See AN-2198 (SNLA132)
198	0xC6	ICR	7:6				***Reserved***
			5	RW		IS_RX_INT	Interrupt on Receiver interrupt Enables interrupt on indication from the Receiver. Allows propagation of interrupts from downstream devices
			4:1				***Reserved***
			0	RW		INT Enable	Global Interrupt Enable Enables interrupt on the interrupt signal to the controller.
199	0xC7	ISR	7:6				***Reserved***
			5	R		IS RX INT	Interrupt on Receiver interrupt Receiver has indicated an interrupt request from down-stream device
			4:1				***Reserved***
			0	R		INT	Global Interrupt Set if any enabled interrupt is indicated

Register Maps (continued)

Table 6. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
240	0xF0	TX ID	7:0	R	0x5F	ID0	First byte ID code, '_'
241	0xF1		7:0	R	0x55	ID1	Second byte of ID code, 'U'
242	0xF2		7:0	R	0x48	ID2	Third byte of ID code. Value will be 'B'
243	0xF3		7:0	R	0x39	ID3	Forth byte of ID code: '9'
244	0xF4		7:0	R	0x32	ID4	Fifth byte of ID code: "2"
245	0xF5		7:0	R	0x35	ID5	Sixth byte of ID code: "5"

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DS90UB925Q-Q1, in conjunction with the DS90UB926Q-Q1, is intended for interface between a host (graphics processor) and a Display. It supports a 24-bit color depth (RGB888) and high definition (720p) digital video format. It can receive a three 8-bit RGB stream with a pixel rate up to 85 MHz together with three control bits (VS, HS and DE) and three I2S-bus audio stream with an audio sampling rate up to 192 kHz.

8.2 Typical Application

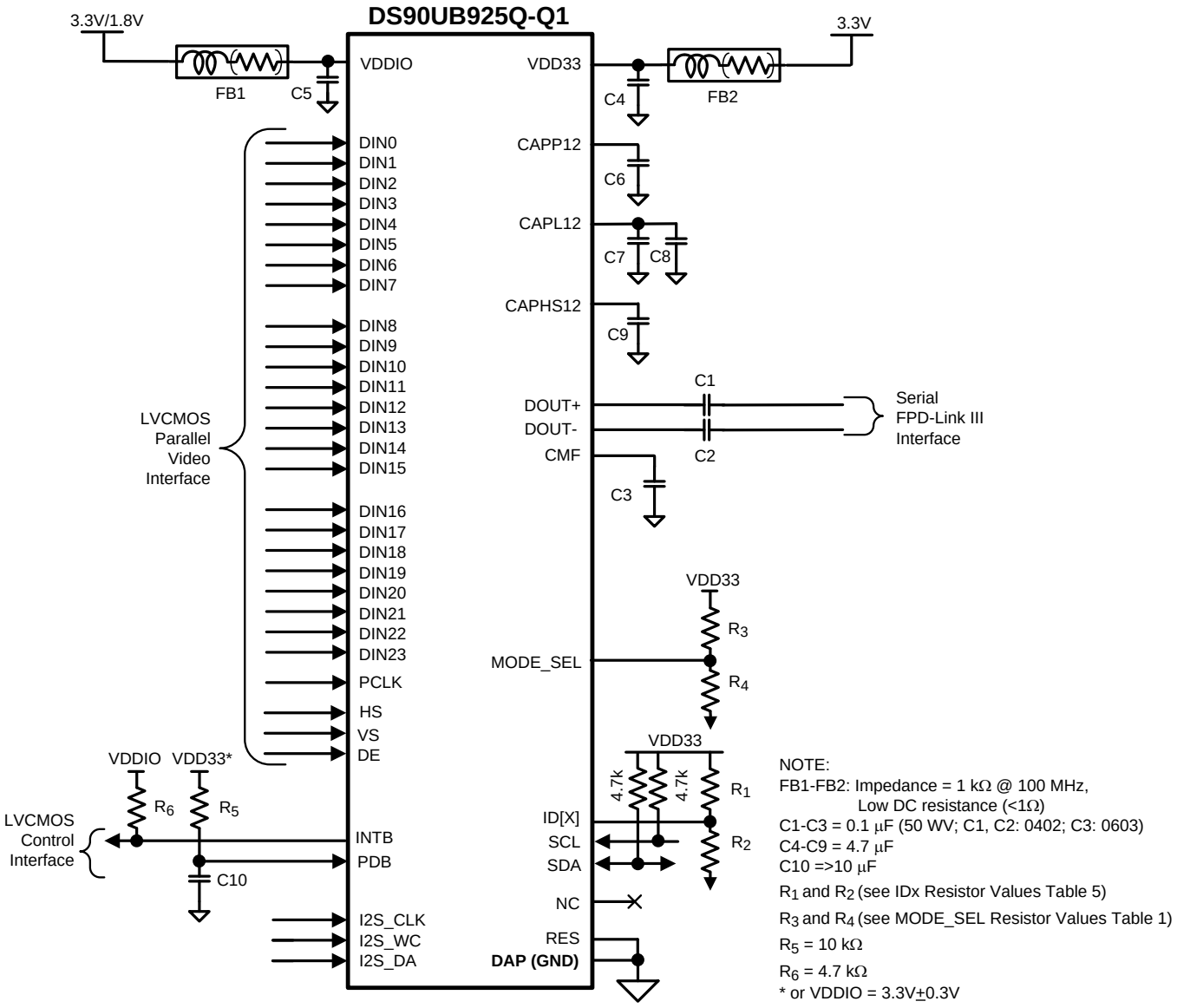


Figure 23. Typical Connection Diagram

Typical Application (continued)

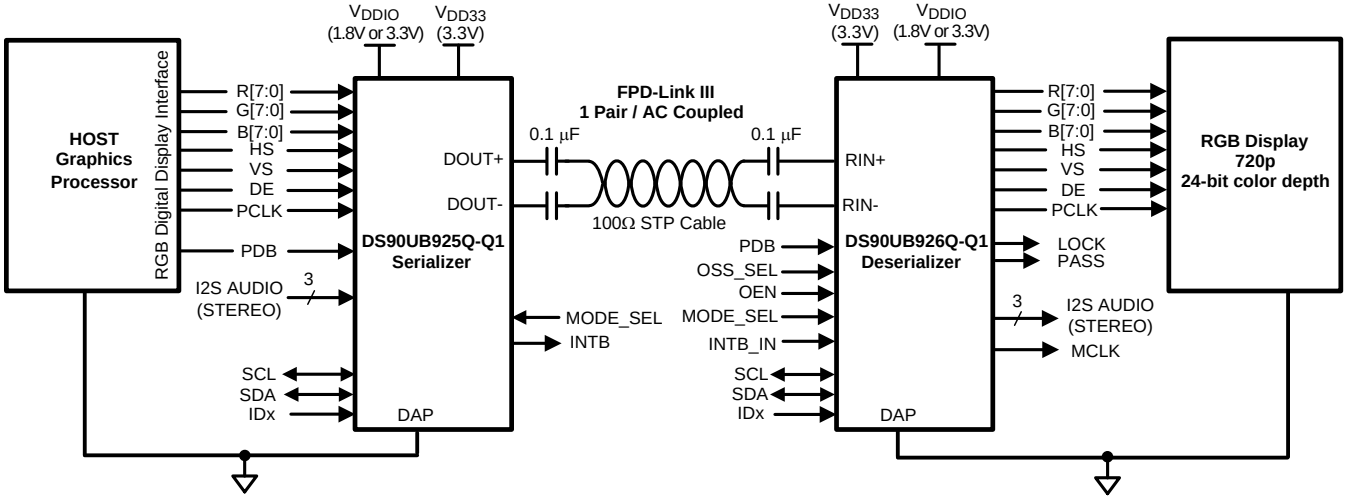


Figure 24. Typical Display System Diagram

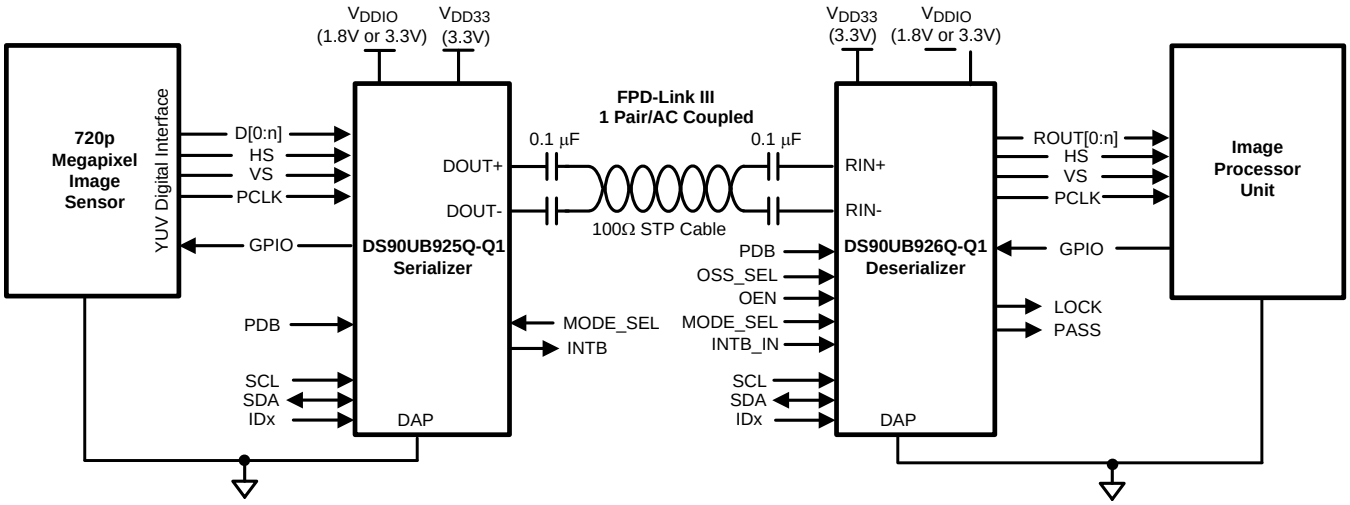


Figure 25. Typical Camera Applications Diagram

8.2.1 Design Requirements

For the typical design application, use the following as input parameters.

Table 7. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
VDDIO	1.8 V or 3.3 V
VDD33	3.3 V
AC Coupling Capacitor for DOUT±	100 nF
PCLK Frequency	85 MHz

8.2.2 Detailed Design Procedure

Figure 23 shows a typical application of the DS90UB925Q-Q1 serializer for an 85 MHz 24-bit Color Display Application. The camera application has the same recommended connections. The CML outputs must have an external 0.1 µF AC coupling capacitor on the high speed serial lines. The serializer has an internal termination. Bypass capacitors are placed near the power supply pins. At a minimum, six (6) 4.7µF capacitors and two (2) additional 1µF capacitors should be used for local device bypassing. Ferrite beads are placed on the two (2) VDDs (V_{DD33} and V_{DDIO}) for effective noise suppression. The interface to the graphics source is with 3.3V LVCMOS levels, thus the V_{DDIO} pin is connected to the 3.3 V rail. A RC delay is placed on the PDB signal to delay the enabling of the device until power is stable.

8.2.3 Application Curves

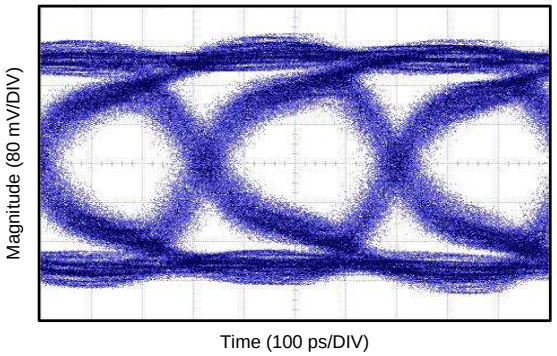


Figure 26. Serializer Eye Diagram with 78 MHz TX Pixel Clock

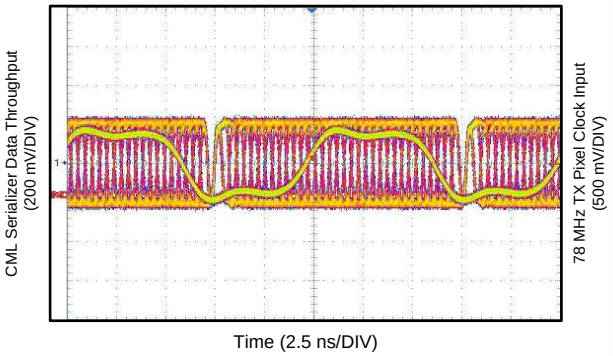


Figure 27. Serializer CML Output with 78 MHz TX Pixel Clock

9 Power Supply Recommendations

9.1 Power Up Requirements and PDB Pin

The VDDs (V_{DD33} and V_{DDIO}) supply ramp should be faster than 1.5 ms with a monotonic rise. A large capacitor on the PDB pin is needed to ensure PDB arrives after all the VDDs have settled to the recommended operating voltage. When PDB pin is pulled to V_{DDIO} = 3.0V to 3.6V or V_{DD33}, it is recommended to use a 10 kΩ pull-up and a >10 uF cap to GND to delay the PDB input signal.

All inputs must not be driven until V_{DD33} and V_{DDIO} has reached its steady state value.

This device is designed to operate from an input core voltage supply of 3.3V. Some devices provide separate power and ground terminals for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. Terminal description tables typically provide guidance on which circuit blocks are connected to which power terminal pairs. In some cases, an external filter may be used to provide clean power to sensitive circuits such as PLLs.

9.2 CML Interconnect Guidelines

See AN-1108 (SNLA008) and AN-905 (SNLA035) for full details.

- Use 100Ω coupled differential pairs
- Use the S/2S/3S rule in spacings
  - – S = space between the pair
  - – 2S = space between pairs
  - – 3S = space to LVCMOS signal
- Minimize the number of Vias
- Use differential connectors when operating above 500 Mbps line speed
- Maintain balance of the traces
- Minimize skew within the pair

Additional general guidance can be found in the LVDS Owner's Manual - available in PDF format from the Texas Instruments web site at: www.ti.com/lvds.

10 Layout

10.1 Layout Guidelines

Circuit board layout and stack-up for the FPD-Link III devices should be designed to provide low-noise power feed to the device. Good layout practice will also separate high frequency or high-level inputs and outputs to minimize unwanted stray noise pickup, feedback and interference. Power system performance may be greatly improved by using thin dielectrics (2 to 4 mils) for power / ground sandwiches. This arrangement provides plane capacitance for the PCB power system with low-inductance parasitics, which has proven especially effective at high frequencies, and makes the value and placement of external bypass capacitors less critical. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the range of 0.01 uF to 0.1 uF. Tantalum capacitors may be in the 2.2 uF to 10 uF range. Voltage rating of the tantalum capacitors should be at least 5X the power supply voltage being used.

Surface mount capacitors are recommended due to their smaller parasitics. When using multiple capacitors per supply pin, locate the smaller value closer to the pin. A large bulk capacitor is recommend at the point of power entry. This is typically in the 50uF to 100uF range and will smooth low frequency switching noise. It is recommended to connect power and ground pins directly to the power and ground planes with bypass capacitors connected to the plane with via on both ends of the capacitor. Connecting power or ground pins to an external bypass capacitor will increase the inductance of the path.

A small body size X7R chip capacitor, such as 0603 or 0402, is recommended for external bypass. Its small body size reduces the parasitic inductance of the capacitor. The user must pay attention to the resonance frequency of these external bypass capacitors, usually in the range of 20-30 MHz. To provide effective bypassing, multiple capacitors are often used to achieve low impedance between the supply rails over the frequency of interest. At high frequency, it is also a common practice to use two vias from power and ground pins to the planes, reducing the impedance at high frequency.

Some devices provide separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. Pin Description tables typically provide guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter may be used to provide clean power to sensitive circuits such as PLLs.

Use at least a four layer board with a power and ground plane. Locate LVCMOS signals away from the CML lines to prevent coupling from the LVCMOS lines to the CML lines. Closely-coupled differential lines of 100 Ohms are typically recommended for CML interconnect. The closely coupled lines help to ensure that coupled noise will appear as common-mode and thus is rejected by the receivers. The tightly coupled lines will also radiate less.

Information on the WQFN style package is provided in TI Application Note: AN-1187 (SNOA401).

10.2 Layout Example

Stencil parameters such as aperture area ratio and the fabrication process have a significant impact on paste deposition. Inspection of the stencil prior to placement of the WQFN package is highly recommended to improve board assembly yields. If the via and aperture openings are not carefully monitored, the solder may flow unevenly through the DAP. Stencil parameters for aperture opening and via locations are shown below:

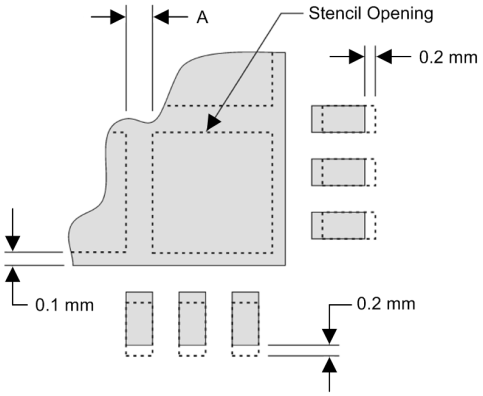


Figure 28. No Pullback WQFN, Single Row Reference Diagram

Table 8. No Pullback WQFN Stencil Aperture Summary

DEVICE	PIN COUNT	MKT Dwg	PCB I/O Pad Size (mm)	PCB PITCH (mm)	PCB DAP SIZE (mm)	STENCIL I/O APERTURE (mm)	STENCIL DAP Aperture (mm)	NUMBER of DAP APERTURE OPENINGS	GAP BETWEEN DAP APERTURE (Dim A mm)
DS90UB925Q-Q1	48	SQA48A	0.25 x 0.6	0.5	5.1 x 5.1	0.25 x 0.7	1.1 x 1.1	16	0.2

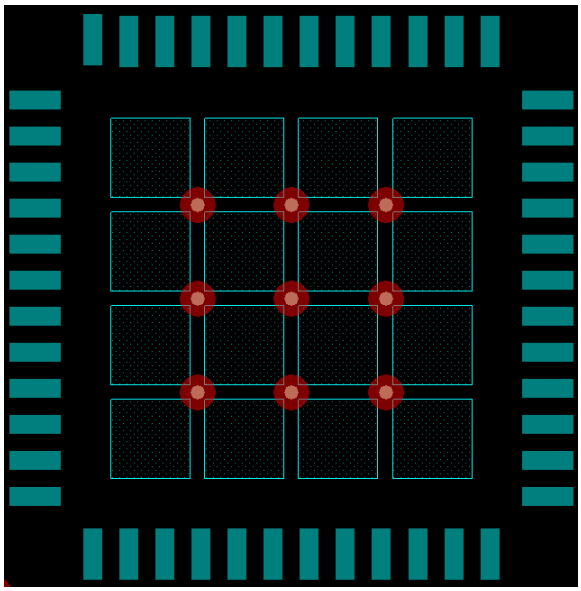


Figure 29. 48-Pin WQFN Stencil Example of Via and Opening Placement

Figure 30 PCB layout example is derived from the layout design of the DS90UB925QSEVB Evaluation Board. The graphic and layout description are used to determine both proper routing and proper solder techniques when designing the Serializer board.

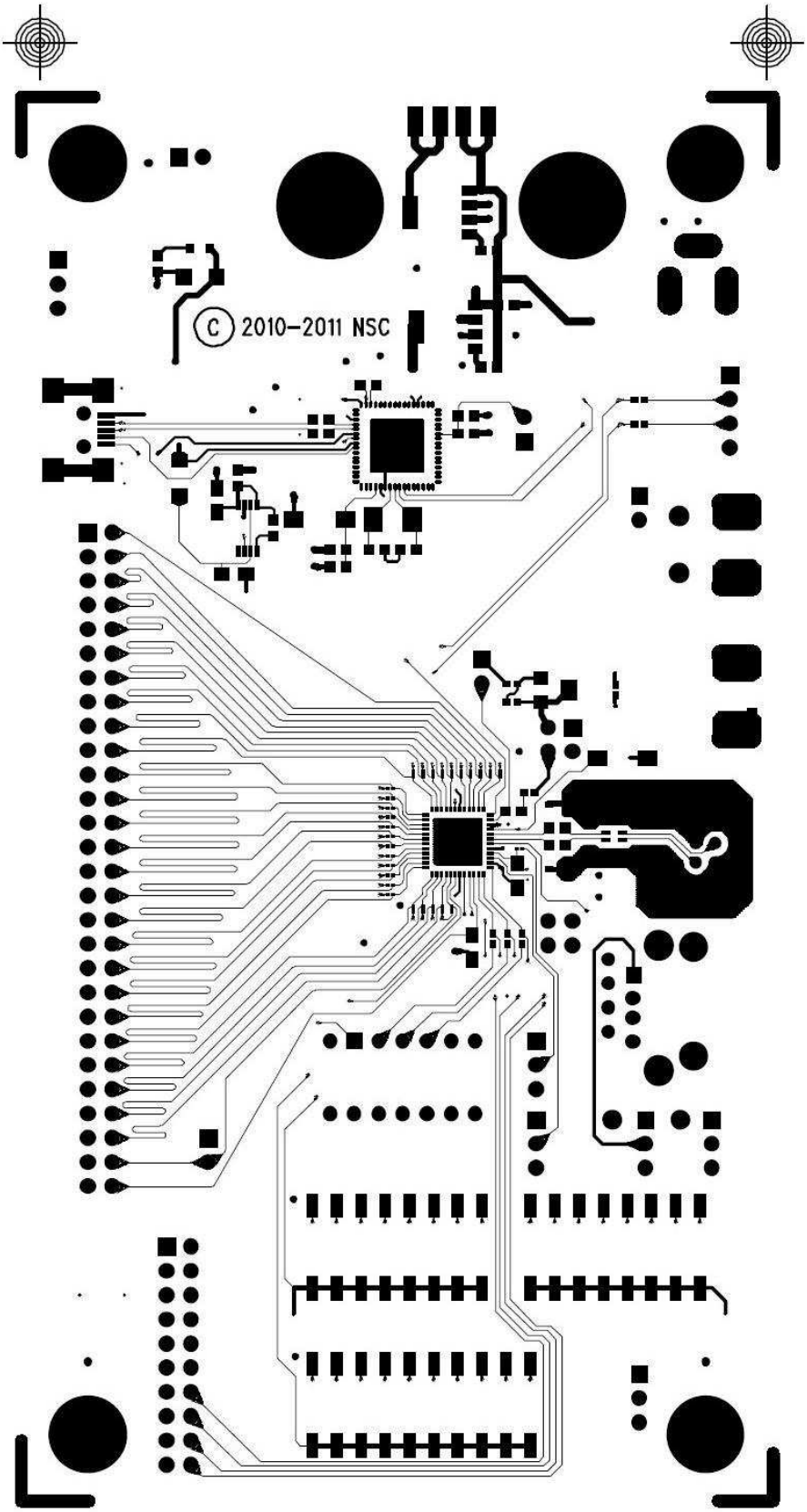


Figure 30. DS90UB925Q-Q1 Serializer Example Layout

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

- AN-2198 Exploring the Internal Test Pattern Generation SNLA132
- AN-1108 Channel-Link PCB and Interconnect Design-In Guidelines SNLA008
- SCAN18245T Non-Inverting Transceiver with TRI-STATE Outputs SNLA035
- TI Interface Website www.ti.com/lvds
- AN-1187 Leadless Leadframe Package (LLP) SNOA401
- Semiconductor and IC Package Thermal Metrics SPRA953

11.2 Trademarks

All trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS90UB925QSQ/NOPB	ACTIVE	WQFN	RHS	48	1000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 105	UB925QSQ	Samples
DS90UB925QSQE/NOPB	ACTIVE	WQFN	RHS	48	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 105	UB925QSQ	Samples
DS90UB925QSQX/NOPB	ACTIVE	WQFN	RHS	48	2500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 105	UB925QSQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

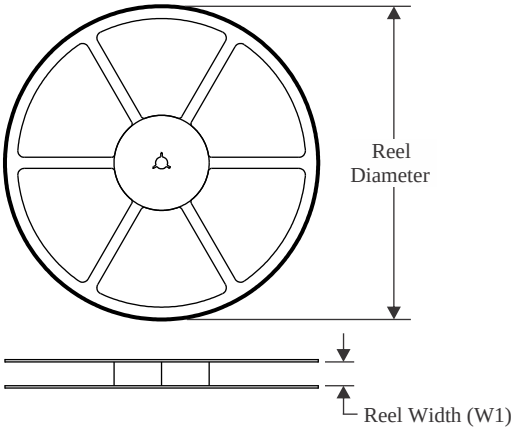
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

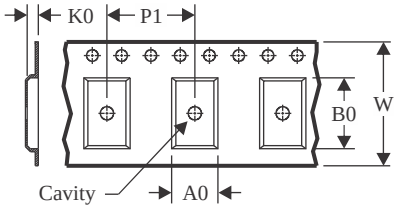
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

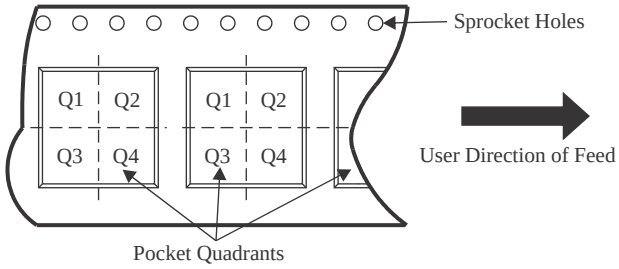


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

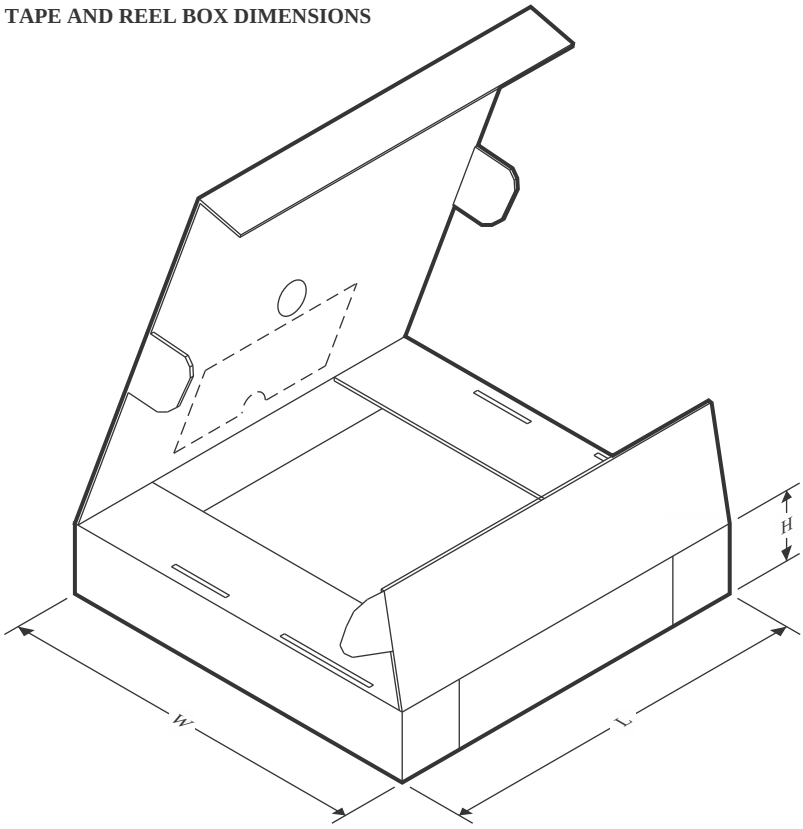
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90UB925QSQ/NOPB	WQFN	RHS	48	1000	330.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1
DS90UB925QSQE/NOPB	WQFN	RHS	48	250	178.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1
DS90UB925QSQX/NOPB	WQFN	RHS	48	2500	330.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90UB925QSQ/NOPB	WQFN	RHS	48	1000	356.0	356.0	35.0
DS90UB925QSQE/NOPB	WQFN	RHS	48	250	208.0	191.0	35.0
DS90UB925QSQX/NOPB	WQFN	RHS	48	2500	356.0	356.0	35.0

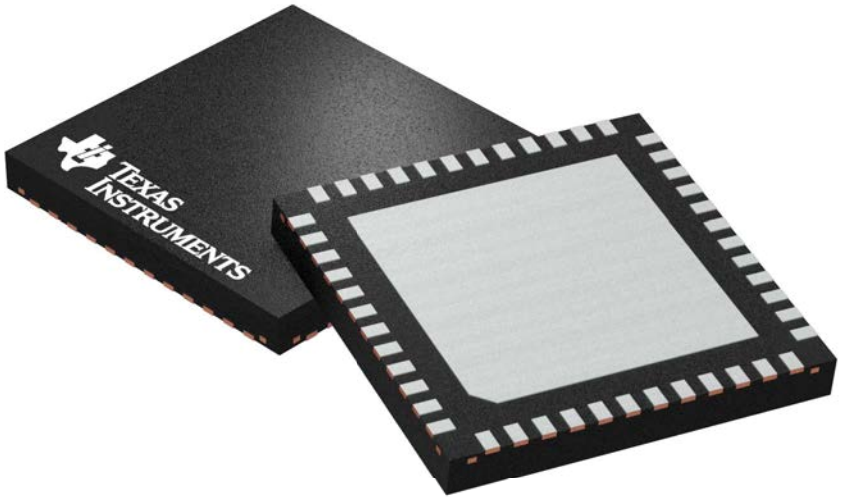
GENERIC PACKAGE VIEW

RHS 48

WQFN - 0.8 mm max height

7 x 7 mm, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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