ONET1130EC 11.7 Gbps Transceiver with Dual CDRs and Modulator Driver

1 Features

- Dual CDR with 9.80-11.7 Gbps Reference-Free Operation
- 2-Wire Digital Interface with Integrated DACs and ADC for Control and Diagnostic Management
- Output Polarity Select for TX and RX
- Programmable Jitter Transfer Bandwidth
- Electrical and Optical Loopback.
- CDR Bypass Mode for Low Data Rate Operation
- Integrated Modulator Driver with Output Amplitude up to 2 V_{PP} Single-ended and Bias Current up to 150 mA Source.
- Automatic Power Control (APC) Loop with Selectable Monitor PD Range
- Programmable TX Input Equalizer
- TX Cross-Point Adjust and De-Emphasis
- Includes Laser Safety Features
- Integrated Limiting Amplifier with Programmable LOS Threshold
- Adjustable RX Equalization and Input Threshold
- Programmable RX Output Voltage and De-emphasis.
- Power Supply Monitor and Temperature Sensor
- Single 2.5-V Supply
- –40°C to 100°C Operation
- Surface Mount 4 mm x 4 mm 32-Pin QFN Package with 0.4 mm Pitch

2 Applications

- XFP and SFP+ 10 Gbps SONET OC-192 Optical Transceivers
- XFP and SFP+ 10 GBASE-ER/ZR Optical Transceivers

3 Description

The ONET1130EC is a 2.5 V integrated modulator driver and limiting amplifier with transmit and receive clock and data recovery (CDR) designed to operate between 9.80 Gbps and 11.7 Gbps without the need for a reference clock. Optical and electrical loopback are included. CDR bypass mode can be used for operation at lower data rates and a two-wire serial interface allows digital control of the features.

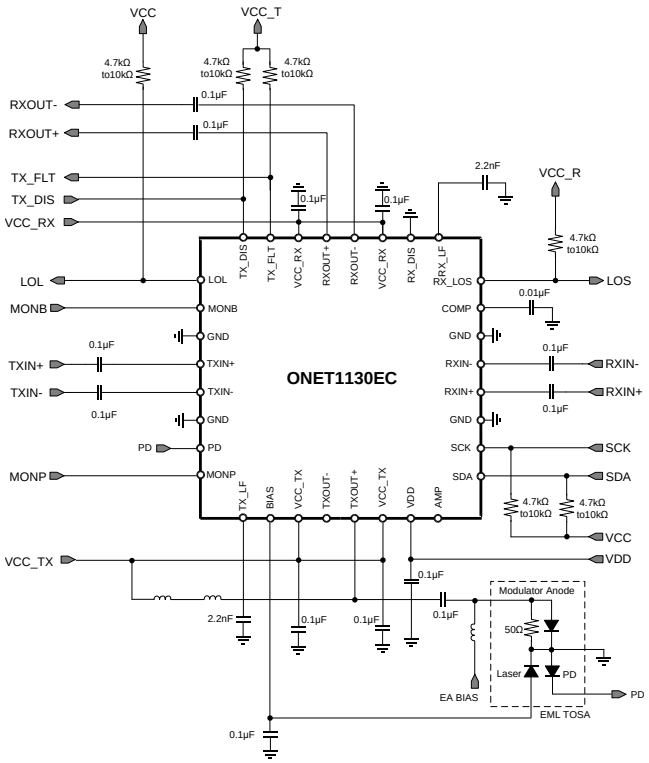
The transmit path consists of an adjustable input equalizer for equalization of up to 300 mm (12 inches) of microstrip or stripline transmission line of FR4 printed circuit boards, a multi-rate CDR and an output modulator driver. Output waveform control, in the form of cross-point adjustment and de-emphasis are available to improve the optical eye mask margin. Bias current for the laser is provided and an integrated automatic power control (APC) loop to compensate for variations in average optical power over voltage, temperature and time is included.

The receive path consists of a limiting amplifier with programmable equalization and threshold adjustment, a multi-rate CDR and output de-emphasis to compensate for frequency dependent loss of connectors, microstrips or striplines connected to the output of the device, The receiver output amplitude and loss of signal assert level can be adjusted.

Device Information

ORDER NUMBER	PACKAGE (PIN)	BODY SIZE
ONET1130EC	VQFN (32)	4.00 mm x 4.00 mm

Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (June 2015) to Revision A	Page
• Changed From: Product Preview To Production	1

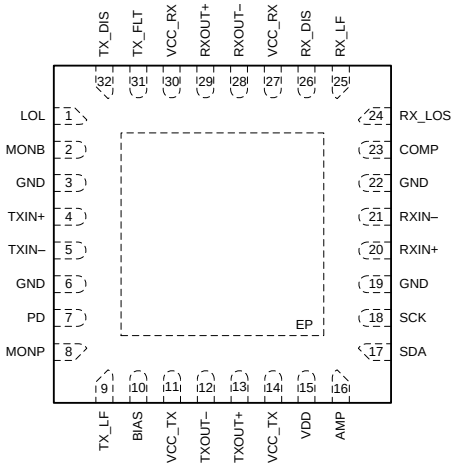
5 Description (continued)

The ONET1130EC contains internal analog to digital and digital to analog converters to support transceiver management and eliminate the need for special purpose microcontrollers.

The transceiver is characterized for operation from –40°C to 100°C case temperatures and is available in a small footprint 4mm × 4mm, 32 pin RoHS compliant VQFN package.

6 Pin Configuration and Function

RSM PACKAGE
32 PIN VQFN
(TOP VIEW)



Pin Functions

NUMBER	NAME	Type	DESCRIPTION
AMP	16	Analog-in	Output amplitude control. Output amplitude can be adjusted by applying a voltage of 0 to 2 V to this pin. Leave open when not used.
BIAS	10	Analog	Sinks or sources the bias current for the laser in both APC and open loop modes.
COMP	23	Analog	Compensation pin used to control the bandwidth of the APC loop. Connect a 0.01-µF capacitor to ground.
GND	3, 6, 19, 22	Supply	Circuit ground.
LOL	1	Digital-out	Transmitter and receiver loss of lock indicator. High level indicates the transmitter or the receiver is out of lock. Open drain output. Requires an external 4.7 kΩ to 10 kΩ pull-up resistor to VCC for proper operation. This pin is 3.3 V tolerant.
MONB	2	Analog-out	Bias current monitor.
MONP	8	Analog-out	Photodiode current monitor.
PD	7	Analog	Photodiode input. Pin can source or sink current dependent on register setting.
RX_DIS	26	Digital-in	Disables the receiver output buffer when set to a high level. Includes a 250-kΩ pull-up resistor to VCC. Ground the pin to enable the output. This is an ORed function with the RXOUT_DIS bit (bit 6 in *register 4*). This pin is 3.3-V tolerant.
RX_LF	25	Analog-in	Receiver loop filter capacitor.
RX_LOS	24	Digital-out	Receiver loss of signal. High level indicates that the receiver input signal amplitude is below the programmed threshold level. Open drain output. Requires an external 4.7-kΩ to 10-kΩ pull-up resistor to VCC for proper operation. This pin is 3.3-V tolerant.
RXIN+	20	Analog-in	Non-inverted receiver data input. On-chip differentially 100 Ω terminated to RXIN–. Must be AC coupled.
RXIN-	21	Analog-in	Inverted receiver data input. On-chip differentially 100 Ω terminated to RXIN+. Must be AC coupled.
RXOUT–	28	CML-out	Inverted receiver data output. 45 Ω back-terminated to VCC.
RXOUT+	29	CML-out	Non-inverted data output. 45 Ω back-terminated to VCC.

Pin Functions (continued)

NUMBER	NAME	Type	DESCRIPTION
SDA	17	Digital-in/out	2-wire interface serial data input. Requires an external 4.7-kΩ to10-kΩ pull-up resistor to VCC. This pin is 3.3-V tolerant.
SCK	18	Digital-in	2-wire interface serial clock input. Requires an external 4.7-kΩ to10-kΩ pull-up resistor to VCC. This pin is 3.3-V tolerant.
TX_DIS	32	Digital-in	Disables both bias and modulation currents when set to high state. Includes a 250-kΩ pull-up resistor to VCC. Requires an external 4.7 kΩ to 10 kΩ pull-up resistor to VCC for proper operation Toggle to reset a fault condition. This is an ORed function with the TXBIASEN bit (bit 2 in *register 1*). This pin is 3.3-V tolerant.
TXIN+	4	Analog-in	Non-inverted transmitter data input. On-chip differentially 100 Ω terminated to TXIN–. Must be AC coupled.
TXIN–	5	Analog-in	Inverted transmitter data input. On-chip differentially 100 Ω terminated to TXIN+. Must be AC coupled.
TX_LF	9	Analog-in	Transmitter loop filter capacitor.
TX_FLT	31	Digital-out	Transmitter fault detection flag. High level indicates that a fault has occurred. Open drain output. Requires an external 4.7 kΩ to 10 kΩ pull-up resistor to VCC for proper operation. This pin is 3.3-V tolerant.
TXOUT–	12	CML-out	Inverted transmitter data output. Internally terminated in single-ended operation mode.
TXOUT+	13	CML-out	Non-Inverted transmitter data output.
VCC_RX	27, 30	Supply	2.5 V ± 5% supply for the receiver.
VCC_TX	11, 14	Supply	2.5 V ± 5% supply for the transmitter.
VDD	15	Supply	2.5 V ± 5% supply for the digital circuitry.
Exposed Pad	EP		Exposed die pad. Solder to the PCB.

7 Specifications

7.1 Absolute Maximum Ratings (1)(2)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage	at VCC_TX, VCC_RX, VDD	–0.5	3	V
Voltage	at 3.3-V tolerant pins LOL, SDA, SCK, RX_LOS, RX_DIS, TX_FLT, TX_DIS	–0.5	3.6	V
	at all other pins MONB, TXIN+, TXIN–, PD, MONP, TX_LF, BIAS, TXOUT–, TXOUT+, AMP, RXIN+, RXIN–, COMP, RX_LF, RXOUT–, RXOUT+,	–0.5	3	V
Maximum current at transmitter input pins	TXIN+, TXIN–		10	mA
Maximum current at transmitter output pins	TXOUT+, TXOUT–		125	mA
Maximum current at receiver input pins	RXIN+, RXIN–		10	mA
Maximum current at receiver output pins	RXOUT+, RXOUT–		30	mA
Maximum junction temperature, T_J			125	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage		2.37	2.5	2.63	V
V_{IH}	Digital input high voltage	TX_DIS, RX_DIS, SCK, SDA, 3.3-V tolerant IOs	2			V
V_{IL}	Digital input low voltage				0.8	V
	Photodiode current range	Control bit TXPDRNG = 1x, step size = 3 µA		3080		µA
		Control bit TXPDRNG = 01, step size = 1.5 µA		1540		
		Control bit TXPDRNG = 00, step size = 0.75 µA		770		
	Serial Data rate	TXCDR_DIS = 0 and RXCDR_DIS = 0	9.8		11.7	Gbps
		TXCDR_DIS = 1 and RXCDR_DIS = 1	1		11.7	
V_{AMP}	Amplitude control input voltage range		0		2	V
t_{R-IN}	Input rise time	20%–80%		30	45	ps
t_{F-IN}	Input fall time	20%–80%		30	45	ps
T_C	Temperature at thermal pad		–40		100	°C

7.4 Thermal Information

THERMAL METRIC(1)		RSM (VQFN) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	37.2	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	30.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	7.6	°C/W
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	2.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 DC Electrical Characteristics

Over recommended operating conditions, open loop operation, V_{OUT} = 2 V_{PP} single-ended, $I_{(BIAS)}$ = 80 mA, unless otherwise noted. Typical operating condition is at V_{CC} = 2.5 V and T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		2.37	2.5	2.63	V
I_{VCC}	Supply current in single-ended TX mode with CDRs enabled	TXMODE = 1, TXCDR_DIS = 0, TX V_{OUT} = 2 V_{PP} single-ended, $I_{(BIAS)}$ = 0 mA; RXCDR_DIS = 0, 600 mV_{PP} differential RX output		225	266	mA
	Power dissipation in single-ended TX mode with CDRs enabled			563	699	mW
	Supply current in differential TX mode with CDRs enabled	TXMODE = 0, TXCDR_DIS = 0, TX V_{OUT} = 1.8 V_{PP} single-ended, $I_{(BIAS)}$ = 0 mA; RXCDR_DIS = 0, 600 mV_{PP} differential RX output		270	310	mA
	Power dissipation in differential TX mode with CDRs enabled			675	815	mW
	Supply current in single-ended TX mode with CDRs disabled	TXMODE = 1, TXCDR_DIS = 1, TX V_{OUT} = 2 V_{PP} single-ended, $I_{(BIAS)}$ = 0 mA; RXCDR_DIS = 1, 600 mV_{PP} differential RX output		161	185	mA
	Power dissipation in single-ended TX mode with CDRs disabled			403	487	mW
	Supply current in differential TX mode with CDRs disabled	TXMODE = 0, TXCDR_DIS = 1, TX V_{OUT} = 1.8 V_{PP} single-ended, $I_{(BIAS)}$ = 0 mA; RXCDR_DIS = 1, 600 mV_{PP} differential RX output		206	242	mA
	Power dissipation in differential TX mode with CDRs disabled			515	636	mW
$R_{(TXIN)}$	Transmitter data input resistance	Differential between TXIN+ / TXIN–		100		Ω
	Transmitter data input termination mismatch				5%	
$R_{(RXIN)}$	Receiver data input resistance	Differential between RXIN+ / RXIN–		100		Ω
$R_{(OUT)}$	Transmitter output resistance	Single-ended at TXOUT+ or TXOUT–		60		Ω
$R_{(RXOUT)}$	Receiver data output resistance	Differential between RXOUT+ or RXOUT–		90		Ω
	Receiver data output termination mismatch				5%	
	Digital input current	TX_DIS, RX_DIS pull up to VCC	–20		20	µA
V_{OH}	Digital output high voltage	LOL, TX_FLT, RX_LOS, pull-up to V_{CC}, I_{SOURCE} = 37.5 µA	2.1			V
V_{OL}	Digital output low voltage	LOL, TX_FLT, RX_LOS, pull-up to V_{CC}, I_{SINK} = 350 µA			0.4	V
$I_{(BIAS-MIN)}$	Minimum bias current	See (1)			5	mA
$I_{(BIAS-MAX)}$	Maximum bias current	Source. BIASPOL = 0, DAC set to maximum, open and closed loop	145	150		mA
		Sink. BIASPOL = 1, DAC set to maximum, open and closed loop	95	100		
$I_{(BIAS-DIS)}$	Bias current during disable				100	µA
	Average power stability	APC loop enabled		±0.5		dB
	Bias pin compliance voltage	Source. TXBIASPOL = 0			V_{CC}-0.45	V
		Sink. TXBIASPOL = 1	0.45			
	Temperature sensor accuracy	With 1-point external mid-scale calibration		±3		°C

(1) The bias current can be set below the specified minimum according to the corresponding register setting; however, in closed loop operation settings below the specified value may trigger a fault.

DC Electrical Characteristics (continued)

Over recommended operating conditions, open loop operation, V_{OUT} = 2 V_{PP} single-ended, $I_{(BIAS)}$ = 80 mA, unless otherwise noted. Typical operating condition is at V_{CC} = 2.5 V and T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(PD)}$	Photodiode reverse bias voltage	APC active, $I_{(PD)}$ = 1500 µA	1.3	2.3		V
	Photodiode fault current level	Percent of target $I_{(PD)}$ (2)		150%		
	Photodiode current monitor ratio	$I_{(MONP)}$ / $I_{(PD)}$ with control bit PDRNG = 1X	10%	12.5%	15%	
		$I_{(MONP)}$ / $I_{(PD)}$ with control bit PDRNG = 01	20%	25%	30%	
		$I_{(MONP)}$ / $I_{(PD)}$ with control bit TXPDRNG = 00	40%	50%	60%	
	Monitor diode DMI accuracy	With external mid-scale calibration		±10%		
	Bias current monitor ratio	$I_{(MONB)}$ / $I_{(BIAS)}$ (nominal 1/100 = 1%), $V_{(MONB)}$ < 1.5V	0.9%	1%	1.1%	
	Bias current DMI accuracy	$I_{(BIAS)}$ ≥ 20 mA	–15%		15%	
	Power supply monitor accuracy	With external mid-scale calibration	–2%		2%	
$V_{(CC-RST)}$	V_{CC} reset threshold voltage	V_{CC} voltage level which triggers power-on reset		1.8	2.1	V
$V_{(CC-RSTHYS)}$	V_{CC} reset threshold voltage hysteresis			100		mV
$V_{(MONB-FLT)}$	Fault voltage at MONB	TXFLTEN = 1, TXDMONB = 0, Fault occurs if voltage at MONB exceeds this value	1.15	1.2	1.25	V
$V_{(MONP-FLT)}$	Fault voltage at MONP	TXFLTEN = 1, TXMONPFLT = 1, TXDMONP = 0, Fault occurs if voltage at MONP exceeds this value	1.15	1.2	1.25	V

(2) Assured by design over process, supply and temperature variation

7.6 Transmitter AC Electrical Characteristics

Over recommended operating conditions, open loop operation, V_{OUT} = 2 V_{PP} single-ended, $I_{(BIAS)}$ = 80 mA unless otherwise noted. Typical operating condition is at V_{CC} = 2.5 V and T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TX INPUT SPECIFICATIONS						
	CDR lock range	CPRI, Ethernet, SONET, Fibre Channel	9.80		11.7	Gbps
	Differential input return loss	0.05 GHz < f ≤ 0.1 GHz	20			dB
		0.1 GHz < f ≤ 5.5 GHz	12	15		
		5.5 GHz < f < 12 GHz	8			
	Differential to common mode conversion	0.1 GHz < f < 12 GHz	10	15		dB
	Common mode input return loss	0.1 GHz < f < 12 GHz	3			dB
	Input AC common mode voltage tolerance		15			mV
	Total Non-DDJ	Total jitter less ISI			0.45	UI_{PP}
$T_{(J\_TX)}$	Total Jitter				0.65	UI_{PP}
$S_{(J\_TX)}$	Sinusoidal Jitter Tolerance	With addition of input jitter, See Figure 1				UI_{PP}
V_{IN}	Differential input voltage swing		100		1000	mV_{PP}
$EQ_{(boost)}$	EQ high freq boost	Maximum setting; 7 GHz	6	9		dB
TX OUTPUT SPECIFICATIONS						
	Differential output return loss	0.01 GHz < f < 12 GHz		12		dB
$V_{O(MIN)}$	Minimum output amplitude	AC Coupled Outputs, 50-Ω single-ended load			0.5	V_{PP}
TX OUTPUT SPECIFICATIONS in SINGLE-ENDED MODE of OPERATION (TXMODE = 1)						
$V_{O(MAX)}$	Maximum output amplitude	AC Coupled Outputs, 50-Ω load, single-ended	2			V_{PP}
	Output amplitude stability	AC Coupled Outputs, 50-Ω load, single-ended		230		mV_{PP}
	High Cross Point Control Range	50-Ω load, single-ended	70%	75%		
	Low Cross Point Control Range	50-Ω load, single-ended		35%	40%	
	Cross Point Stability	50-Ω load, single-ended	-5		5	pp
	Output de-emphasis	TXDEADJ[0..3] = 1111, TXPKSEL = 0		5		dB
		TXDEADJ[0..3] = 1111, TXPKSEL = 1		6		
TX OUTPUT SPECIFICATIONS in DIFFERENTIAL MODE of OPERATION (TXMODE = 0)						
$V_{O(MAX)}$	Maximum output amplitude	AC Coupled Outputs, 100-Ω differential load	3.6			V_{PP}
	Output amplitude stability	AC Coupled Outputs, 100-Ω differential load		230		mV_{PP}
	High Cross Point Control Range	100-Ω differential load	65%	75%		
	Low Cross Point Control Range	100-Ω differential load		35%	40%	
	Cross Point Stability	100-Ω differential load	–5		5	pp
	Output de-emphasis	TXDEADJ[0..3] = 1111, TXPKSEL = 0		5		dB
		TXDEADJ[0..3] = 1111, TXPKSEL = 1		6		
TX CDR SPECIFICATIONS						
$BW_{(TX)}$	Jitter Transfer Bandwidth	9.95 Gbps, PRBS31			8	MHz
$J_{(P\_TX)}$	Jitter Peaking	> 120 kHz			1	dB
$J_{GEN(rms)}$	Random RMS jitter generation	Clock pattern, 50 kHz to 80 MHz			6	mUI_{rms}
$J_{GEN(PP)}$	Total jitter generation	Clock pattern, 50 kHz to 80 MHz, BER = 10^{-12}			60	mUI_{PP}

7.7 Receiver AC Electrical Characteristics

Over recommended operating conditions, outputs connected to a 50-Ω load, V_{OD} = 600 mVpp differential unless otherwise noted. Typical operating condition is at V_{CC} = 2.5 V and T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RX INPUT SPECIFICATIONS						
	CDR lock range	CPRI, Ethernet, SONET, Fibre Channel	9.8		11.7	Gbps
	Differential input return loss	0.01 GHz < f ≤ 5 GHz		15		dB
		5 GHz < f < 12 GHz		8		
	Differential to common mode conversion	0.1 GHz < f < 12 GHz		15		dB
$V_{I(RX,MIN)}$	Data input sensitivity	TXOUT_DIS = 1, PRBS31 pattern at 11.7Gbps, BER < 10^{-12}		6	9	mV_{PP}
$V_{I(RX,MAX)}$	Data input overload		800			mV_{PP}
$J_{(T\_RX)}$	Sinusoidal jitter tolerance	9.95 Gbps, BER = 10^{-12}, f = 400kHz	1.5			UI_{PP}
		9.95 Gbps, BER = 10^{-12}, f = 4MHz	0.4			
		9.95 Gbps, BER = 10^{-12}, f = 80MHz	0.4			
RX OUTPUT SPECIFICATIONS						
	Differential output return loss	0.05 GHz < f ≤ 0.1 GHz	20			dB
		0.1 GHz < f < 5.5 GHz	8	15		
		5.5 GHz < f < 12 GHz	8			
	Common mode input return loss	0.1 GHz < f < 12 GHz	3			dB
$CMOV_{(RX)}$	Output AC common mode voltage	PRBS31 pattern, RXAMP[0..3] = 0001			7	mV_{rms}
f_{3dB-L}	Low frequency –3dB bandwidth			20	50	kHz
$D_{(J\_RX)}$	Deterministic output jitter				0.1	UI_{PP}
$T_{(J\_RX)}$	Total output jitter				0.2	UI_{PP}
V_{OD}	Differential data output voltage	V_{IN} > 25 mV_{PP}, RX_DIS = 0, RXAMP[0..3] = 0000		300		mV_{PP}
		V_{IN} > 25 mV_{PP}, RX_DIS = 0, RXAMP[0..3] = 1111		900		mV_{PP}
		RX_DIS = 1			5	mV_{rms}
	Output De-emphasis	RXDADJ[0..1] = 11		1		dB
RX LOS SPECIFICATIONS						
V_{TH}	LOW LOS assert threshold range min	PRBS7 pattern at 11.3Gbps, RXLOSRNG = 1		10		mV_{PP}
	LOW LOS assert threshold range max	PRBS7 pattern at 11.3Gbps, RXLOSRNG = 1		50		
V_{TH}	HIGH LOS assert threshold range min	PRBS7 pattern at 11.3Gbps, RXLOSRNG = 0		40		mV_{PP}
	HIGH LOS assert threshold range max	PRBS7 pattern at 11.3Gbps, RXLOSRNG = 0		130		
	LOS hysteresis (electrical)		2	4	6	dB
	LOS threshold variation	Versus temperature		1.5		dB
		Versus supply voltage		1		
		Versus data rate		1.5		
RX CDR SPECIFICATIONS						
$BW_{(RX)}$	Jitter Transfer Bandwidth	9.95 Gbps, PRBS31			8	MHz
$J_{(P\_TX)}$	Jitter Peaking	> 50 kHz			1	dB

7.8 Timing Requirements

Over recommended operating conditions, open loop operation, TXOUT+ = 2 V_{PP} singled-ended, $I_{(BIAS)}$ = 80 mA, V_{OD} = 600 mV_{PP} differential (unless otherwise noted). Typical operating condition is at V_{CC} = 2.5 V and T_A = 25°C

			MIN	TYP	MAX	UNIT
$t_{(APC)}$	APC time constant	C_{APC} 0.01 µF, I_{PD} = 500 µA, PD coupling ratio CR = 150, PDRNG = 01		50		µs
$t_{(INIT1)}$	Power-on to initialize	Power-on to registers ready to be loaded		0.2	1	ms
$t_{(INIT2)}$	Initialize to transmit	Register load STOP command to part ready to transmit valid data			2	ms
$t_{(OFF)}$	Transmitter disable time	Rising edge of TX_DIS to $I_{(BIAS)} \le 0.1 \times I_{(BIAS\text{-}NOMINAL)}$		1	5	µs
$t_{(ON)}$	Disable negate time	Falling edge of TX_DIS to $I_{(BIAS)} \ge 0.9 \times I_{(BIAS\text{-}NOMINAL)}$			1	ms
$t_{(RESET)}$	TX_DIS pulse width	Time TX_DIS must held high to reset part	100			ns
$t_{(FAULT)}$	Fault assert time	Time from fault condition to FLT high			50	µs
TX OUTPUT SPECIFICATIONS in SINGLE-ENDED MODE of OPERATION (TXMODE = 1)						
$t_{R(OUTTX)}$	Output rise time	20% - 80%, AC Coupled Outputs, 50-Ω load, single-ended		30	42	ps
$t_{F(OUTTX)}$	Output fall time	20% - 80%, AC Coupled Outputs, 50-Ω load, single-ended		30	42	ps
$ISI_{(TX)}$	Intersymbol interference	TXEQ_DIS = 1, 11.3 Gbps, PRBS9 pattern, 150-mVpp, 600-mVpp, 1200-mVpp differential input voltage		4	12	ps
		TXEQ_DIS = 0, 11.3 Gbps, PRBS9 pattern, 150-mVpp, 600-mVpp, 1200-mVpp differential input voltage, maximum equalization with 18-inch transmission line at the input.		7		
$R_{(J\_TX)}$	Serial data output random jitter			0.4	0.7.5	ps_{RMS}
	Output de-emphasis width	TXPKSEL = 0		28		ps
		TXPKSEL = 1		35		
TX OUTPUT SPECIFICATIONS in DIFFERENTIAL MODE of OPERATION (TXMODE = 0)						
$t_{R(OUTTX)}$	Output rise time	20%–80%, AC Coupled Outputs, 100-Ω differential load		30	42	ps
$t_{F(OUTTX)}$	Output fall time	20%–80%, AC Coupled Outputs, 100-Ω differential load		30	42	ps
$ISI_{(TX)}$	Intersymbol interference	TXEQ_DIS = 1, 11.3 Gbps, PRBS9 pattern, 150-mVpp, 600-mVpp, 1200-mVpp differential input voltage		4	10	ps
		TXEQ_DIS = 0, 11.3 Gbps, PRBS9 pattern, 150-mVpp, 600-mVpp, 1200-mVpp differential input voltage, maximum equalization with 18-inch transmission line at the input.		7		
$R_{(J\_TX)}$	Serial data output random jitter			0.4	0.75	ps_{RMS}
	Output Peaking Width	TXPKSEL = 0		28		ps
		TXPKSEL = 1		35		
TX CDR SPECIFICATIONS						
$t_{(Lock,TX)}$	CDR Acquisition time				2	ms
	LOL assert time				500	µs
RX OUTPUT SPECIFICATIONS						
$t_{R(OUTRX)}$	Output rise time	20%–80%, 100-Ω differential load, adjustable		30	40	ps
$t_{F(OUTRX)}$	Output fall time	20%–80%, 100-Ω differential load, adjustable		30	40	ps
	Serial data output deterministic jitter	PRBS9 pattern 11.3 Gbps, V_{IN} = 15 mVpp to 900 mVpp		3	10	ps
RX LOS SPECIFICATIONS						
$t_{(LOS\_AST)}$	LOS assert time		2.5	10	50	µs
$t_{(LOS,\ DEA)}$	LOS deassert time		2.5	10	50	µs
RX CDR SPECIFICATIONS						
$t_{(Lock,RX)}$	CDR Acquisition time				2	ms
	LOL assert time				500	µs

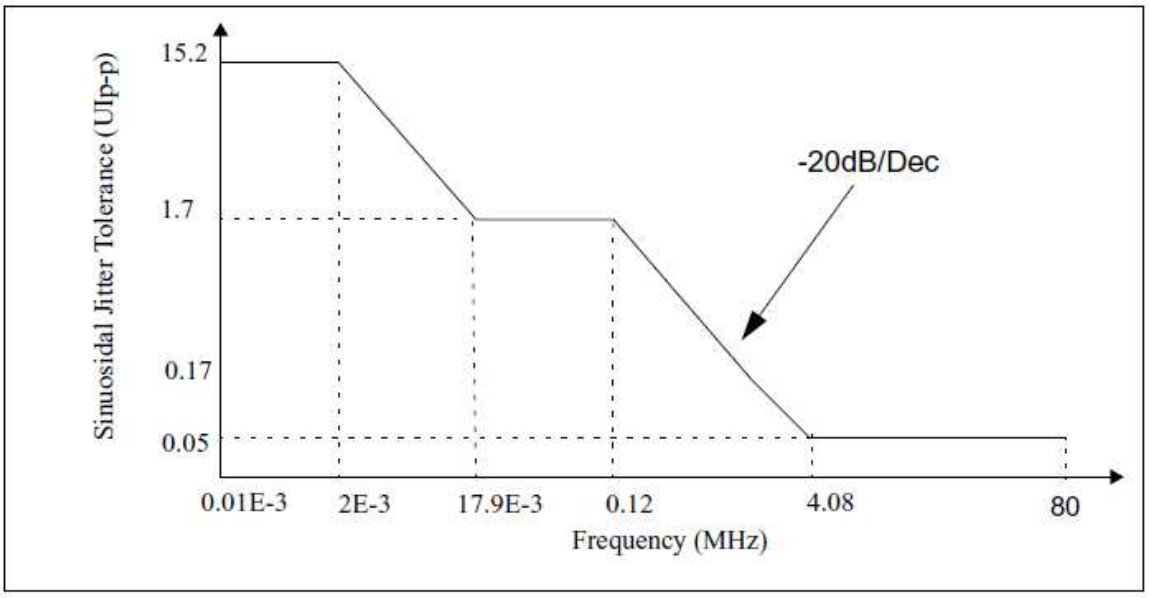


Figure 1. Transmitter Input Sinusoidal Jitter Tolerance (INF-8077i Rev. 4.5 XFP MSA)

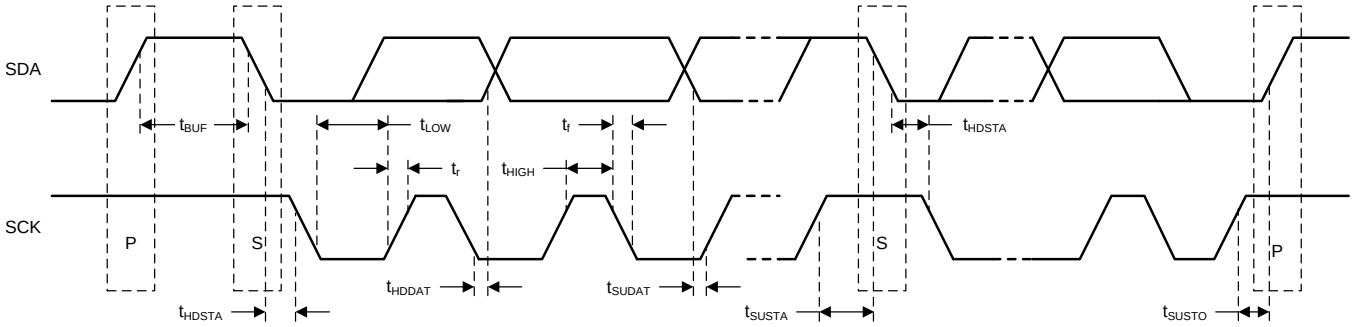


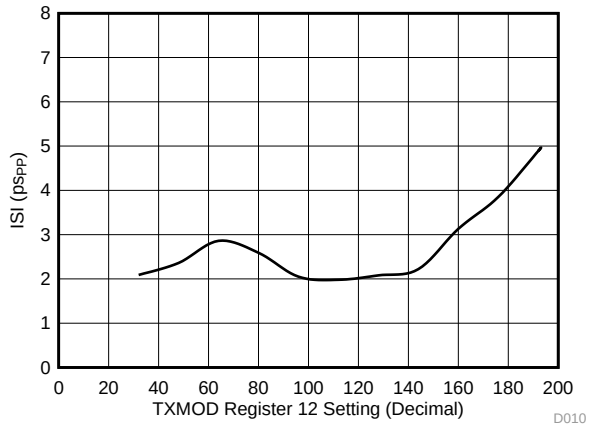
Figure 2. 2-Wire Interface Diagram

Table 1. Timing Diagram Definitions

Symbol	Description	Min	Max	Unit
f_{SCK}	SCK clock frequency		400	kHz
t_{BUF}	Bus free time between START and STOP conditions	1.3		µs
t_{HDSTA}	Hold time after repeated START condition. After this period, the first clock pulse is generated	0.6		µs
t_{LOW}	Low period of the SCK clock	1.3		µs
t_{HIGH}	High period of the SCK clock	0.6		µs
t_{SUSTA}	Setup time for a repeated START condition	0.6		µs
t_{HDDAT}	Data HOLD time	0		µs
t_{SUDAT}	Data setup time	100		ns
t_R	Rise time of both SDA and SCK signals		300	ns
t_F	Fall time of both SDA and SCK signals		300	ns
t_{SUSTO}	Setup time for STOP condition	0.6		µs

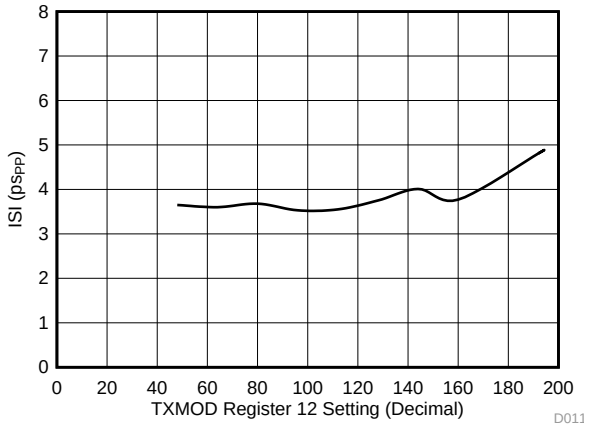
7.9 Typical Characteristics

Typical operating condition is at V_{CC} = 2.5 V, T_A = 25°C, TXOUT+ = 2 V_{PP} Single-ended, RXOUT = 600 mV_{PP} differential, TXIN = 600 mV_{PP} differential, TX and RX CDRs enabled (unless otherwise noted).



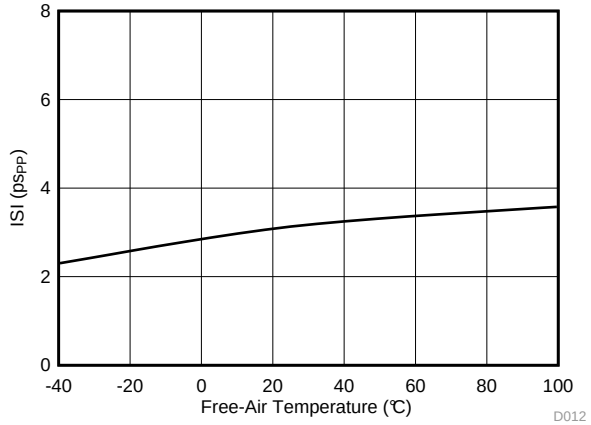
TXMODE = 0

Figure 3. TX Deterministic Jitter vs Modulation Current



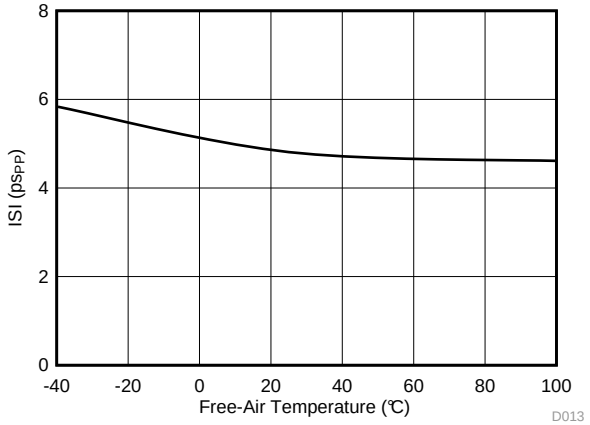
TXMODE = 1

Figure 4. TX Deterministic Jitter vs Modulation Current



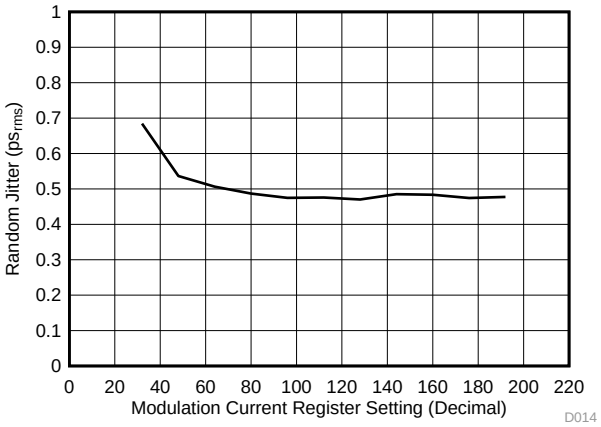
TXMODE = 0

Figure 5. TX Deterministic Jitter vs Temperature



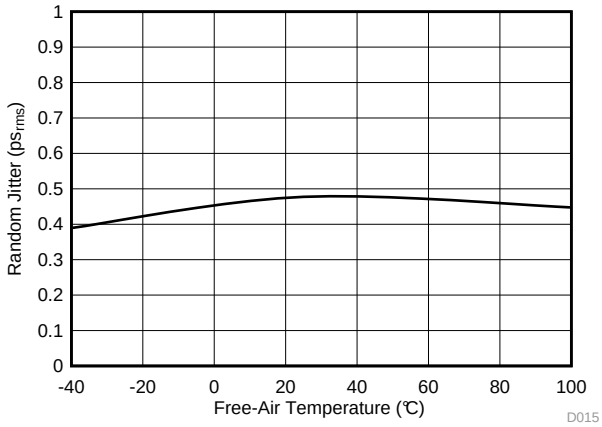
TXMODE = 1

Figure 6. TX Deterministic Jitter vs Temperature



TXMODE = 1

Figure 7. TX Random Jitter vs Modulation Current

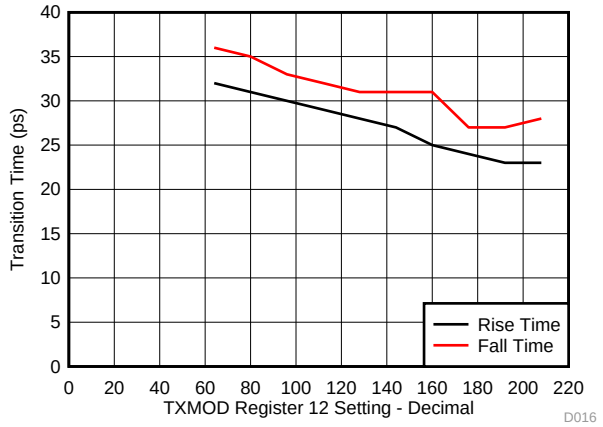


TXMODE = 1

Figure 8. TX Random Jitter vs Temperature

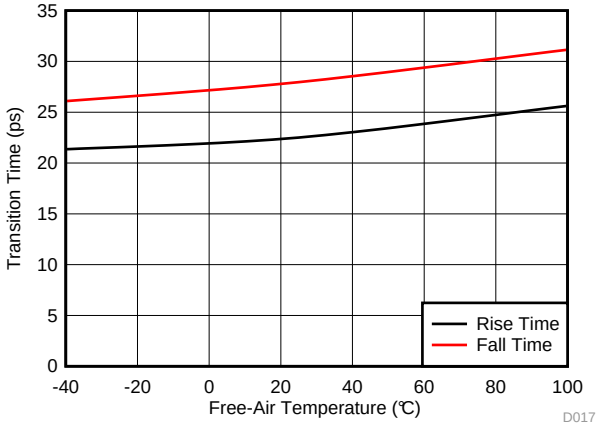
Typical Characteristics (continued)

Typical operating condition is at V_{CC} = 2.5 V, T_A = 25°C, TXOUT+ = 2 V_{PP} Single-ended, RXOUT = 600 mV_{PP} differential, TXIN = 600 mV_{PP} differential, TX and RX CDRs enabled (unless otherwise noted).



TXMODE = 1

Figure 9. TX Rise-Time and Fall-Time vs Modulation Current



TXMODE = 1

Figure 10. TX Rise-Time and Fall-Time vs Temperature

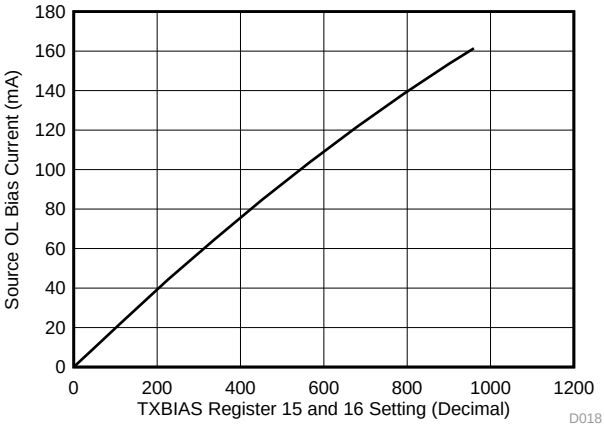


Figure 11. Source Bias Current in Open Loop Mode vs Bias Register Setting

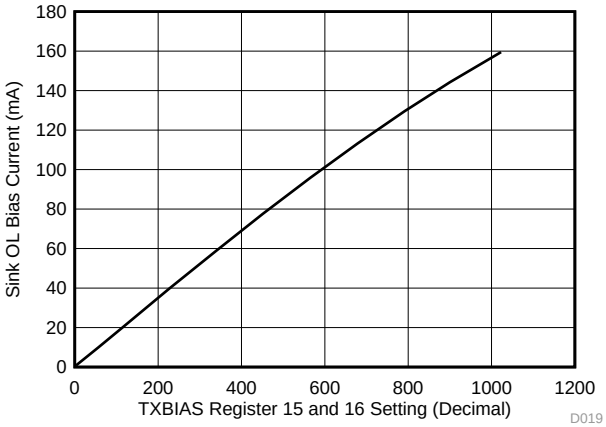


Figure 12. Sink Bias Current in Open Loop Mode vs Bias Register Setting

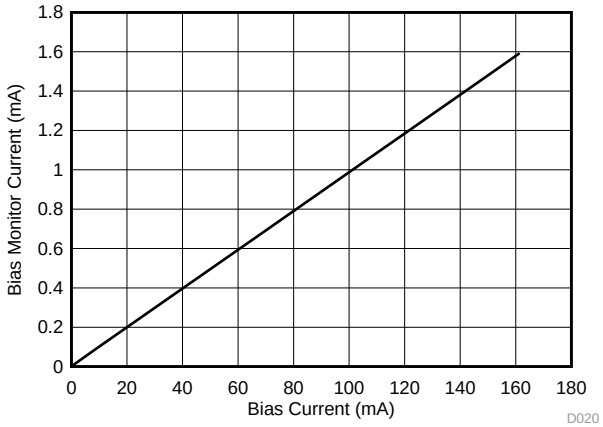
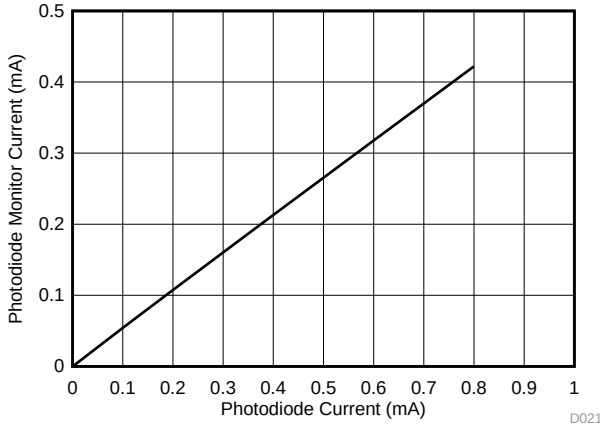


Figure 13. Bias-Monitor Current $I_{(MONB)}$ vs Bias Current

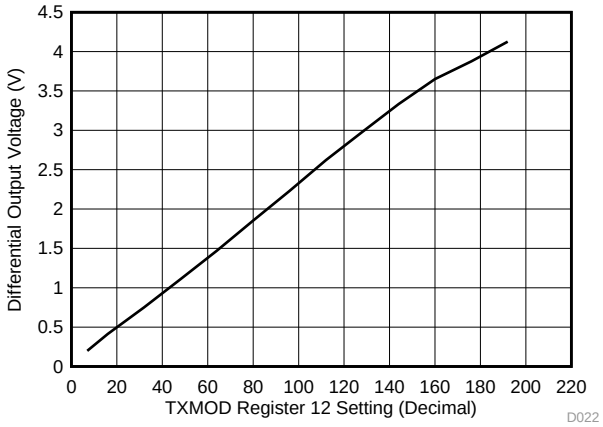


TXPDRNG[0..1] = 00

Figure 14. Photodiode-Monitor Current $I_{(MONP)}$ vs PD Current

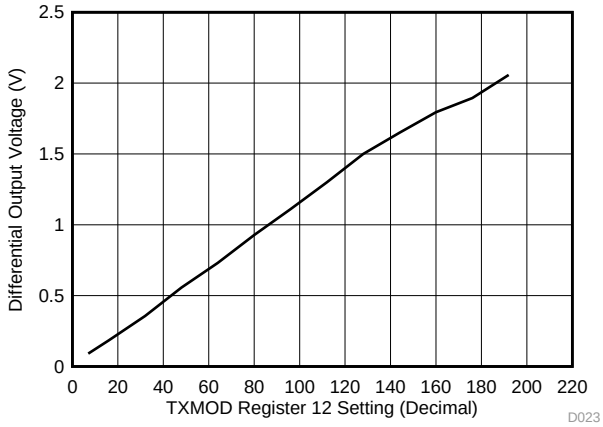
Typical Characteristics (continued)

Typical operating condition is at V_{CC} = 2.5 V, T_A = 25°C, TXOUT+ = 2 V_{PP} Single-ended, RXOUT = 600 mV_{PP} differential, TXIN = 600 mV_{PP} differential, TX and RX CDRs enabled (unless otherwise noted).



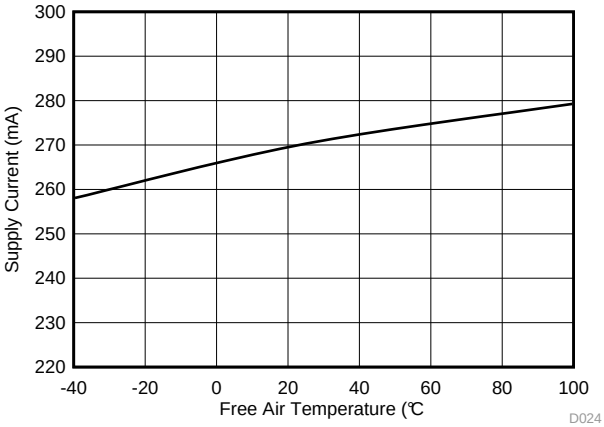
TXMODE = 0

Figure 15. Output Voltage vs Modulation Current



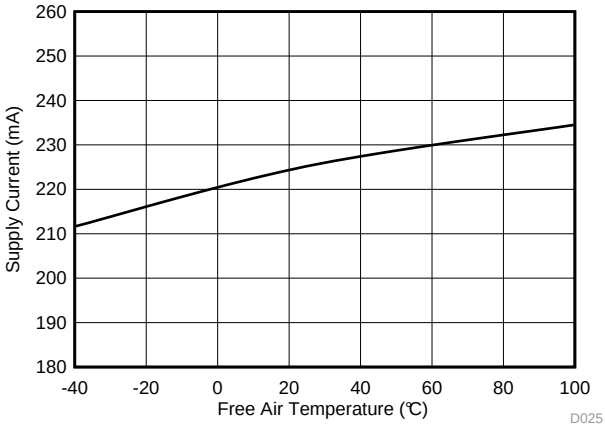
TXMODE = 1

Figure 16. Output Voltage vs Modulation Current



TXMODE = 0 Bias Current = 0

Figure 17. Supply Current vs Temperature



TXMODE = 1 Bias Current = 0

Figure 18. Supply Current vs Temperature

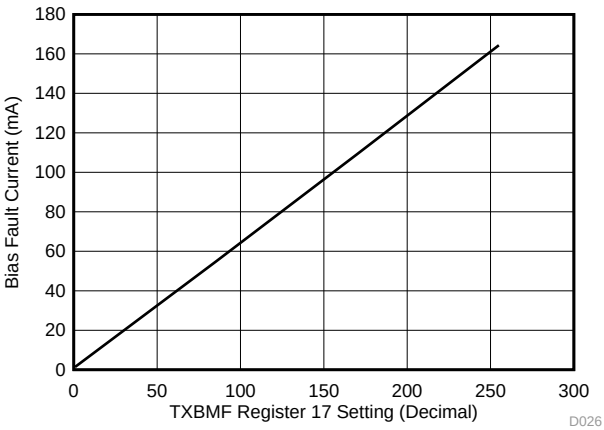


Figure 19. Bias Current Monitor Fault vs TXBMF Register Setting

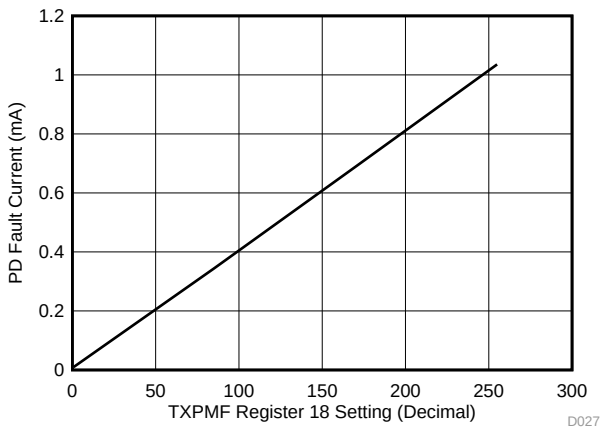
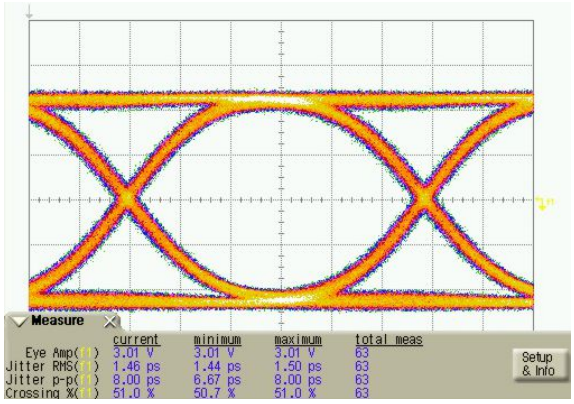


Figure 20. Photodiode Current Monitor Fault vs TXPMF Register Setting

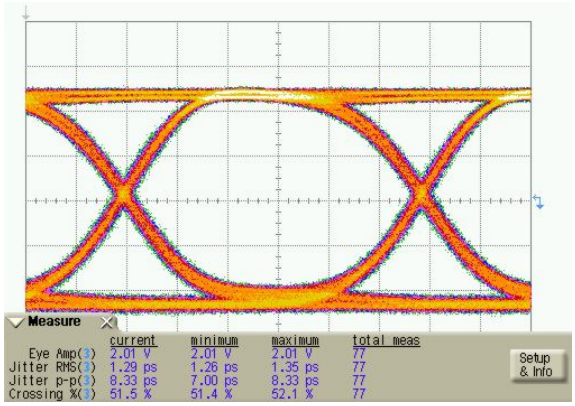
Typical Characteristics (continued)

Typical operating condition is at V_{CC} = 2.5 V, T_A = 25°C, TXOUT+ = 2 V_{PP} Single-ended, RXOUT = 600 mV_{PP} differential, TXIN = 600 mV_{PP} differential, TX and RX CDRs enabled (unless otherwise noted).



TXMODE = 0 15 ps/Div

Figure 21. TX Eye-Diagram at 11.3 Gbps



TXMODE = 1 15 ps/Div

Figure 22. TX Eye-Diagram at 11.3 Gbps

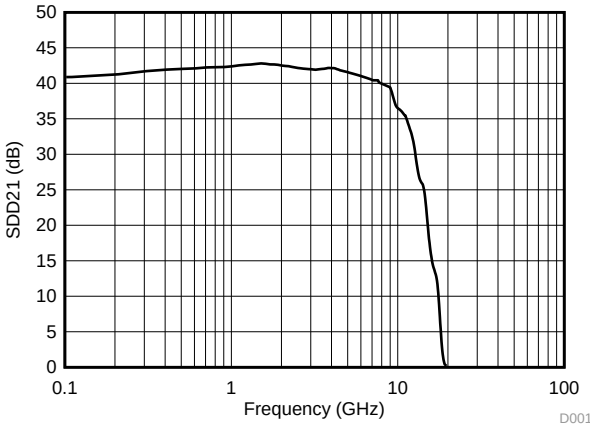


Figure 23. RX Frequency Response (CDR Disabled)

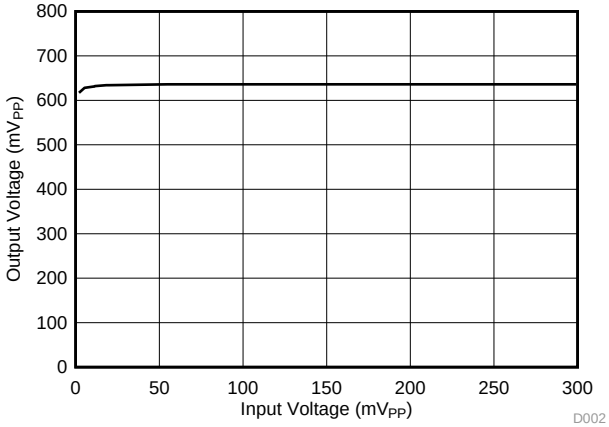


Figure 24. RX Transfer Function

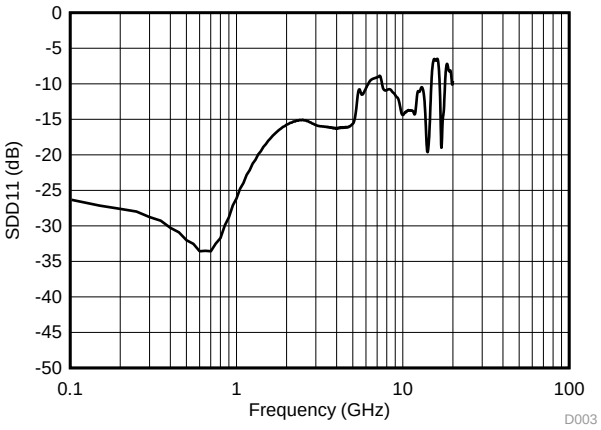


Figure 25. RX Differential Input Return Gain vs Frequency

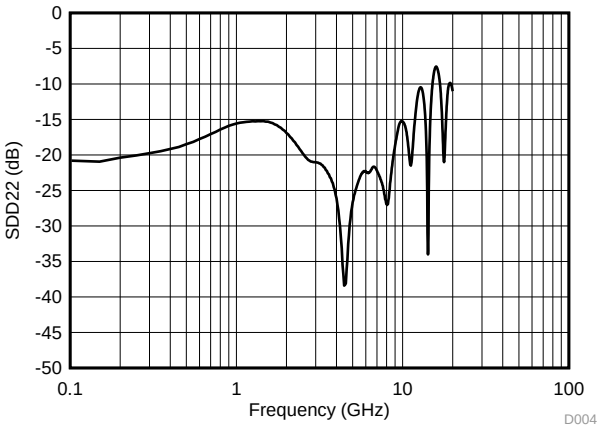


Figure 26. RX Differential Output Return Gain vs Frequency

Typical Characteristics (continued)

Typical operating condition is at V_{CC} = 2.5 V, T_A = 25°C, TXOUT+ = 2 V_{PP} Single-ended, RXOUT = 600 mV_{PP} differential, TXIN = 600 mV_{PP} differential, TX and RX CDRs enabled (unless otherwise noted).

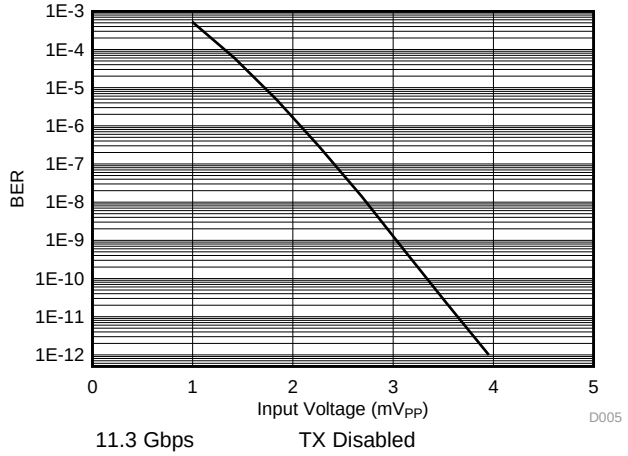


Figure 27. RX Bit-Error Ratio vs Input Amplitude

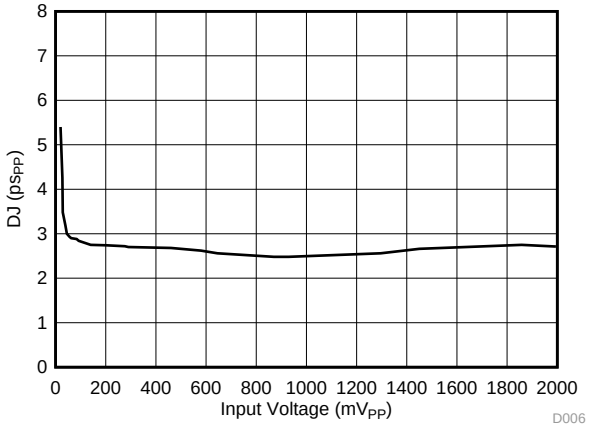


Figure 28. RX Deterministic Jitter vs Input Amplitude

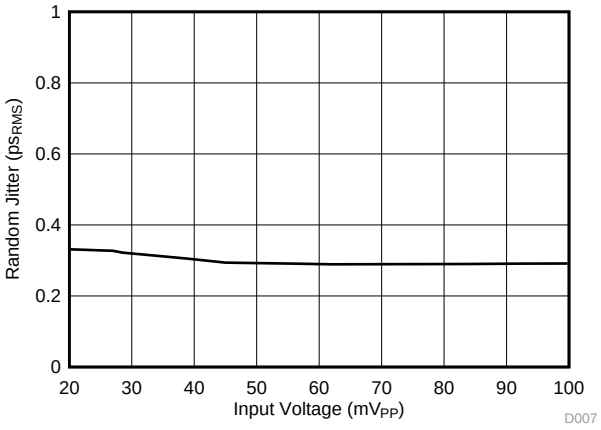


Figure 29. RX Random Jitter vs Input Amplitude

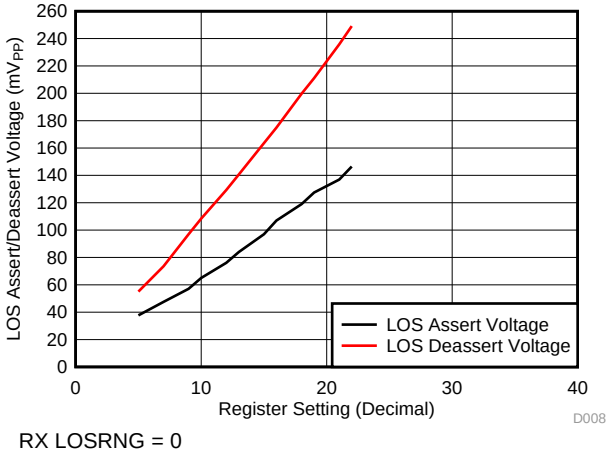


Figure 30. LOS Assert / Deassert Voltage vs Register 7 Setting

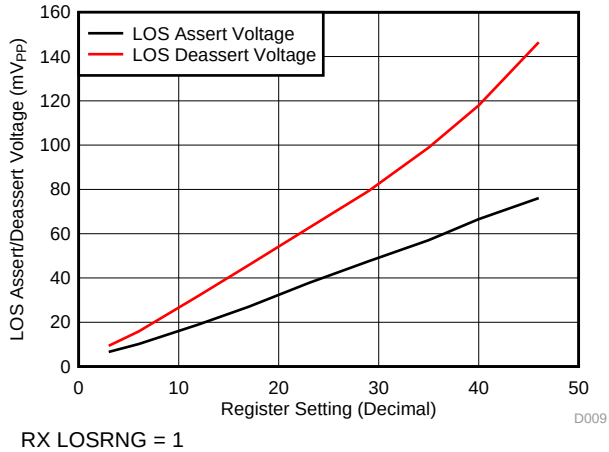


Figure 31. LOS Assert / Deassert Voltage vs Register 7 Setting

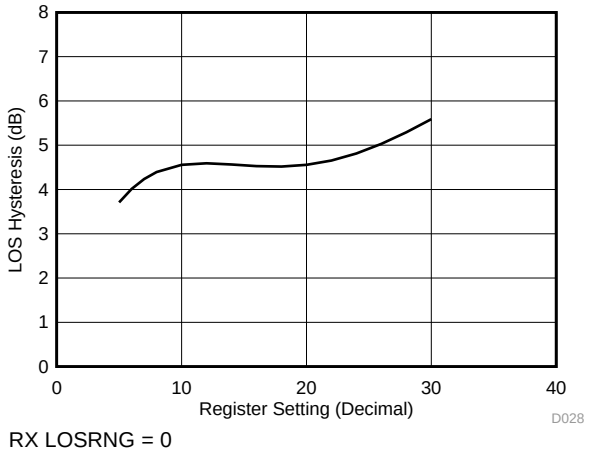
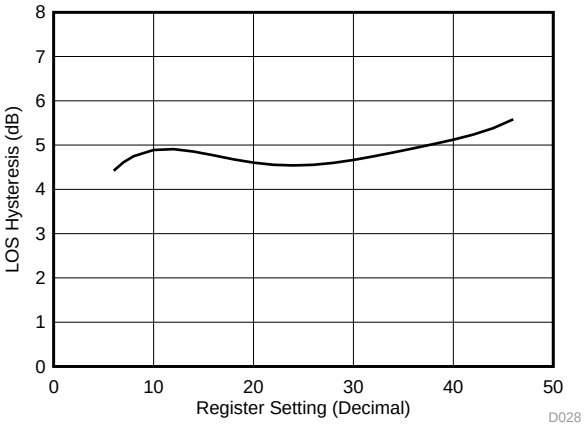


Figure 32. LOS Hysteresis vs Register 7 Setting

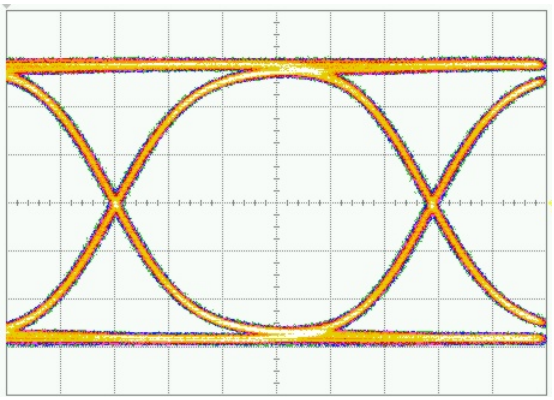
Typical Characteristics (continued)

Typical operating condition is at V_{CC} = 2.5 V, T_A = 25°C, TXOUT+ = 2 V_{PP} Single-ended, RXOUT = 600 mV_{PP} differential, TXIN = 600 mV_{PP} differential, TX and RX CDRs enabled (unless otherwise noted).



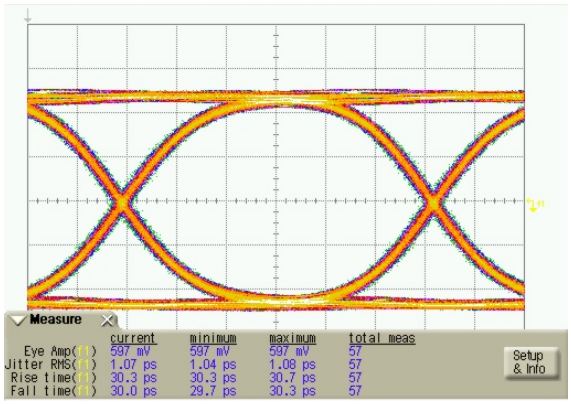
RX LOSRNG = 1

Figure 33. LOS Hysteresis vs Register Setting



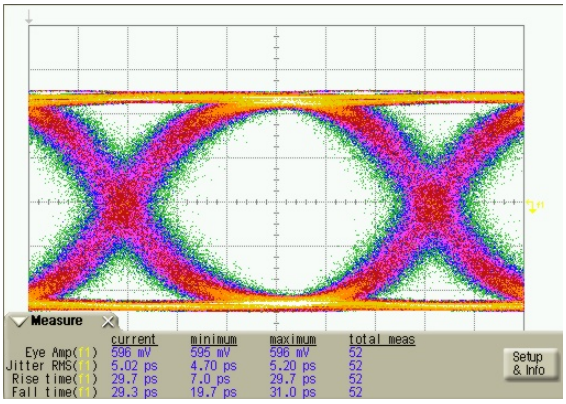
V_I = 20 mV_{PP}

Figure 34. RX Output Eye-Diagram at 11.3 Gbps



Pin = –20 dBm CDR Enabled

Figure 35. RX Output Eye-diagram at 10.71 Gbps



Pin = –20 dBm CDR Disabled

Figure 36. RX Output Eye-diagram at 10.71 Gbps

8 Detailed Description

8.1 Overview

A simplified block diagram of the ONET1130EC is shown in *Functional Block Diagram*.

The ONET1130EC consists of a transmitter path, a receiver path, an analog reference block, an analog to digital converter and a 2-wire serial interface and control logic block with power-on reset.

The transmit path consists of an adjustable input equalizer, a multi-rate CDR and an output modulator driver. The output driver provides a differential output voltage but can be operated in a single-ended mode to reduce the power consumption. Output waveform control, in the form of cross-point adjustment and de-emphasis are available to improve the optical eye mask margin. Bias current for the laser is provided and an integrated automatic power control (APC) loop to compensate for variations in average optical power over voltage, temperature and time is included.

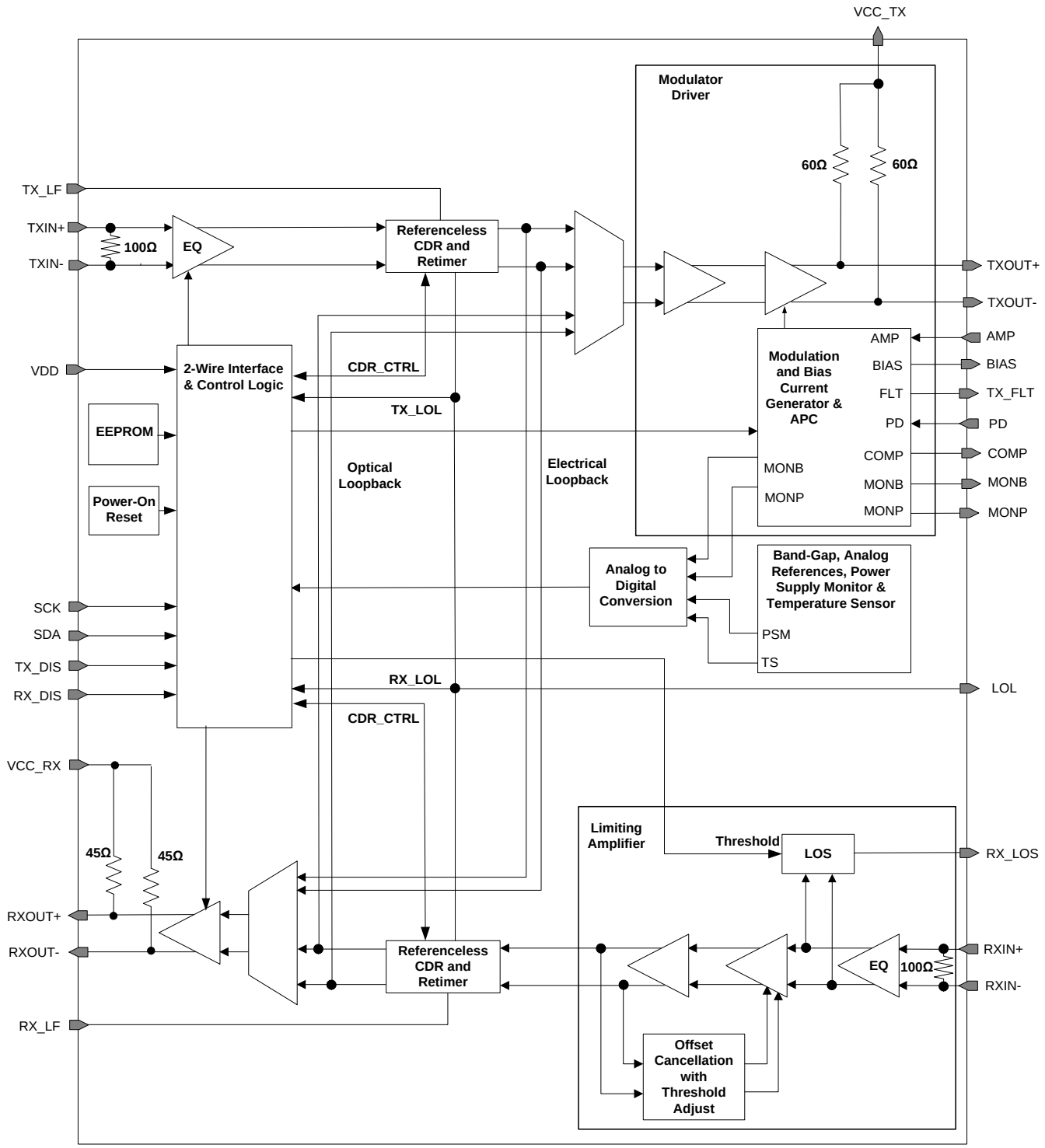
The receive path consists of a limiting amplifier with programmable equalization and threshold adjustment, a multi-rate CDR and an output driver with de-emphasis to compensate for frequency dependent loss of connectors and transmission lines. The receiver output amplitude, de-emphasis and loss of signal assert level can be adjusted.

The ONET1130EC contains an analog to digital converter to support transceiver digital diagnostics and can report the supply voltage, laser bias current, laser photodiode current and internal temperature.

The 2-wire serial interface is used to control the operation of the device and read the status of the control registers.

The device contains internal EEPROM for trimming purposes only.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Transmitter

8.3.1.1 Equalizer

The data signal is applied to an input equalizer by means of the input signal pins TXIN+ / TXIN–, which provide on-chip differential 100-Ω line termination. The equalizer is enabled by default and can be disabled by setting the transmitter equalizer disable bit TXEQ_DIS = 1 (bit 1 of *register 10*). Equalization of up to 300 mm (12 inches) of microstrip or stripline transmission line on FR4 printed circuit boards can be achieved. The amount of equalization is set through register settings TXCTLE [0..3] (*register 11*). The device can accept input amplitude levels from 100 mVpp up to 1000 mVpp.

8.3.1.2 CDR

The clock and data recovery function consists of a Phase-Locked Loop (PLL) and retimer. The CDR can be operated without a reference clock and the Voltage Controlled Oscillator (VCO) can cover 9.8 Gbps to 11.7 Gbps data rates. The PLL is phase locked to the incoming data stream and attenuates the high frequency jitter on the data, producing a recovered clean clock with substantially reduced jitter. An external capacitor for the PLL loop filter is connected to the TX_LF pin. A value of 2.2 nF is recommended. The clean clock is used to retime the incoming data, producing an output signal with reduced jitter, and in effect, resetting the jitter budget for the transmitter.

The CDR is enabled by default. The CDR can be disabled and bypassed by setting the transmitter CDR disable bit TXCDR_DIS = 1 (bit 4 of *register 10*). Alternatively, the CDR can be left powered on but bypassed by setting the transmitter CDR bypass bit TX_CDRBP = 1 (bit 3 of *register 10*); however, this function only works if the receiver CDR bypass bit RX_CDRBP (bit 3 of *register 4*) is also set to 1.

The CDR is designed to meet the XFP Datacom requirements and Telecom requirements for a maximum of 1-dB jitter peaking at a frequency greater than 120 kHz. The CDR is not designed to meet the Telecom regenerator requirements of jitter peaking less than 0.03 dB at a frequency less than 120 kHz. The default CDR bandwidth is typically 4.5 MHz and can be adjusted using the SEL_RES[0..2] bits (bits 5 to 7 of *register 51*). Adjusting these bits changes the bandwidth of both the transmitter and receiver CDRs.

For the majority of applications, the default settings in *register 19* for the transmitter CDR can be used. However, for some applications or for test purposes, some modes of operation may be useful. The frequency detector for the PLL is set to an automatic mode of operation by default. When a signal is applied to the transmitter input the frequency detector search algorithm will be initiated to determine the frequency of the data. The default algorithm ensures a fast CDR lock time of less than 2 ms. The fast lock can be disabled by setting the transmitter CDR fast lock disable bit TXFL_DIS = 1 (bit 3 of *register 19*). Once the frequency has been detected then the frequency detector will be disabled and the supply current will decrease by approximately 10mA. In some applications, such as when there are long periods of idle data, it may be advantageous to keep the frequency detector permanently enabled by setting the transmitter frequency detector enable bit TXFD_EN = 1 (bit 5 of *register 19*). For test purposes, the frequency detector can be permanently disabled by setting the transmitter frequency detector disable bit TXFD_DIS = 1 (bit 4 of *register 19*). For fast lock times the frequency detector can be set to one of two preselected data rates using the transmitter frequency detection mode selection bits TXFD_MOD[0..1] (bits 6 and 7 of *register 19*). If it is desired to use the retimer at lower data rates than the standard 9.8 to 11.7Gbps then the transmitter divider ratio should be adjusted accordingly through TXDIV[0..2] (bits 0 to 2 of *register 19*). For example, for re-timed operation at 2.5 Gbps the divider should be set to divide by 4.

8.3.1.3 Modulator Driver

The modulation current is sunk from the common emitter node of the limiting output driver differential pair by means of a modulation current generator, which is digitally controlled by the 2-wire serial interface.

The collector nodes of the output stages are connected to the transmitter output pins TXOUT+ and TXOUT–. The collectors have internal 50Ω back termination resistors to VCC_TX. The outputs are optimized to drive a 50 Ω single-ended load and to obtain the maximum single-ended output voltage of 2.0Vpp, AC coupling and inductive pull-ups to VCC are required. For reduced power consumption the DC resistance of the inductive pull-ups should be minimized to provide sufficient headroom on the TXOUT+ and TXOUT– pins.

Feature Description (continued)

The polarity of the output pins can be inverted by setting the transmitter output polarity switch bit, TXOUTPOL (bit 5 of *register 10*) to 1. In addition, the output driver can be disabled by setting the transmitter output driver disable bit TXOUT_DIS = 1 (bit 6 of *register 10*).

The output driver is set to differential output by default. In order to reduce the power consumption for single-ended applications driving an electroabsorptive modulated laser (EML) the output drive *register 13* should be set to single-ended mode. The single-ended output signal is enabled by setting the transmitter mode select bit TXMODE = 1 (bit 6 of *register 13*). The positive output is active by default. To enable the negative output and disable the positive output set TXOUTSEL = 1 (bit 7 of *register 13*).

Output de-emphasis can be applied to the signal by adjusting the transmitter de-emphasis bits TXDEADJ[0..3] (bits 0 to 3 of *register 13*). In addition, the width of the applied de-emphasis can be increased by setting the transmitter output peaking width TXPKSEL = 1 (bit 6 of *register 11*). The wide peaking width would typically be useful for a more capacitive transmitter load. How de-emphasis is applied is controlled through the TXSTEP bit (bit 5 of *register 13*). Setting TXSTEP = 1 delays the time of the applied de-emphasis and has more of an impact on the falling edge. A graphical representation of the two de-emphasis modes is shown in Figure 37. Using de-emphasis can help to optimize the transmitted output signal; however, it will add to the power consumption.

The output edge speed can be set to slow mode of operation through the TXSLOW bit (bit 4 of *register 13*). For transmitter modulation output settings (TXMOD - *register 12*) below 0xC0 it is recommended to set TXSLOW = 1 to reduce the output jitter.

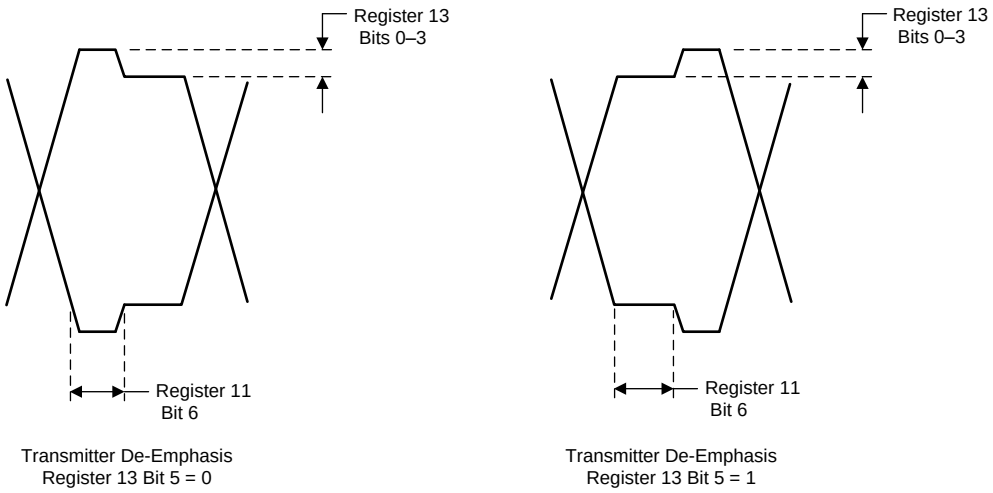


Figure 37. Transmitter De-Emphasis Modes

8.3.1.4 Modulation Current Generator

The modulation current generator provides the current for the high speed output driver described above. The circuit can be digitally controlled through the 2-wire interface block or controlled by applying an analog voltage in the range of 0 to 2V to the AMP pin. The default method of control is through the 2-wire interface. To use the AMP pin set the transmitter amplitude control bit TXAMPCTRL = 1 (bit 0 of *register 10*).

An 8-bit wide control bus, TXMOD[0..7] (*register 12*), is used to set the desired modulation current and the output voltage.

The entire transmitter signal path, including CDR, can be disabled and powered down by setting TX_DIS = 1 (bit 7 of *register 10*).

Feature Description (continued)

8.3.1.5 DC Offset Cancellation and Cross Point Control

The ONET1130EC transmitter has DC offset cancellation to compensate for internal offset voltages. The offset cancellation can be disabled by setting TXOC_DIS = 1 (bit 2 of *register 10*).

The crossing point can be moved toward the one level by setting TXCPSGN = 1 (bit 7 of *register 14*) and it can be moved toward the zero level by setting TXCPSGN = 0. The percentage of shift depends upon the register settings of the transmitter cross-point adjustment bits TXCPADJ[0..6] (*register 14*).

8.3.1.6 Transmitter Loopback (Electrical Loopback)

The signal input to the TXIN+ and TXIN– pins can be looped back to the receiver output after the retimer as shown in Figure 38 by setting TX_LBMUX = 1 (bit 0 of *register 2*). Loopback from the receiver input to the transmitter output (optical loopback) can be enabled at the same time.

If it is desired to loopback the signal input to the TXIN+ and TXIN– pins to the receiver output with the CDR disabled then the transmit CDR must be disabled and bypassed by setting TXCDR_DIS = 1 (bit 4 of *register 10*) and the receiver CDR must also be disabled and bypassed by setting RXCDR_DIS =1 (bit 4 of *register 4*).

Feature Description (continued)

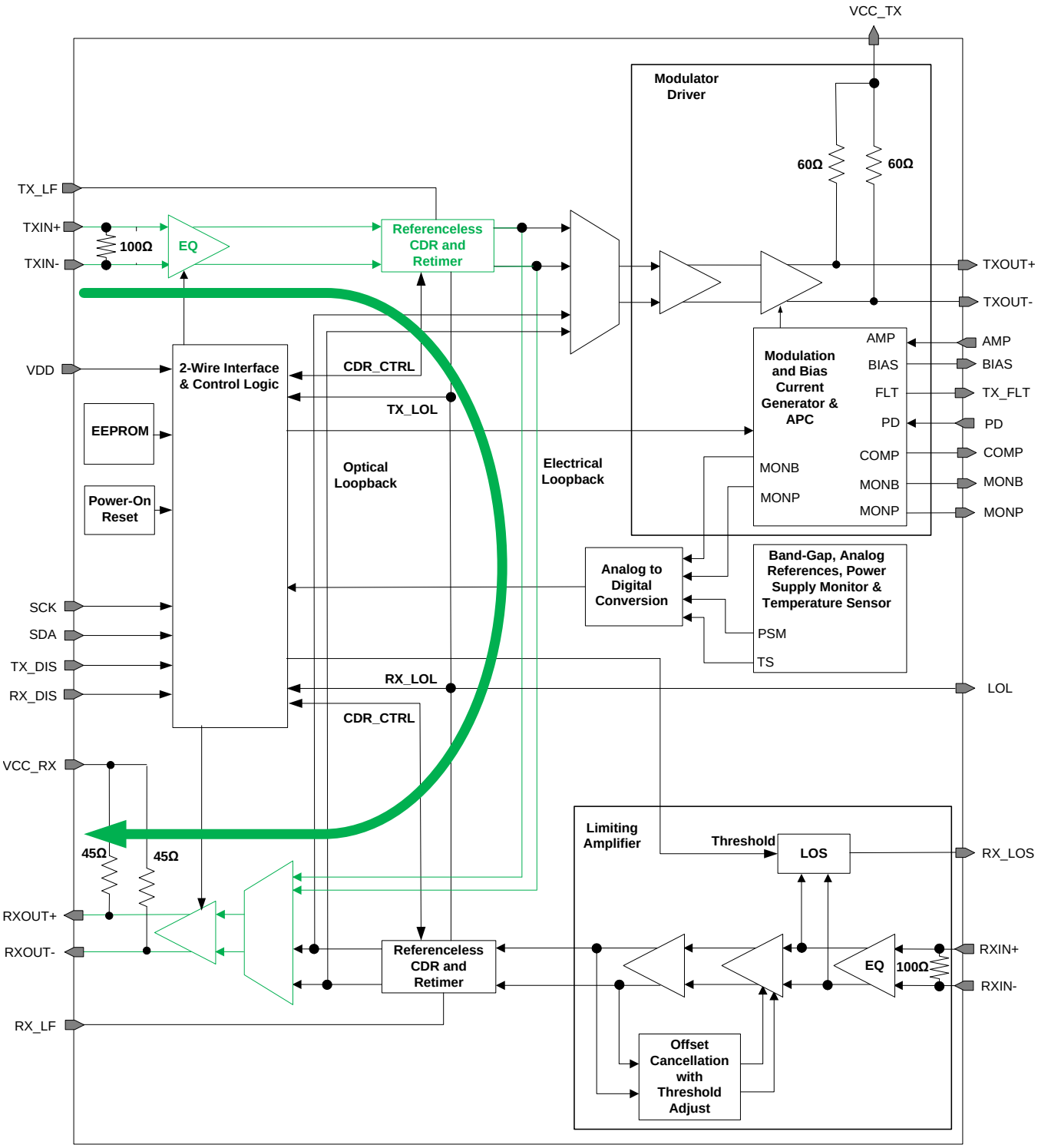


Figure 38. Electrical Loopback

Feature Description (continued)

8.3.1.7 Bias Current Generation and APC Loop

The bias current for the laser is turned off by default and has to be enabled by setting the laser bias current enable bit TXBIASEN = 1 (bit 2 of *register 1*). In open loop operation, selected by setting TXOLENA = 1 (bit 4 of *register 1*), the bias current is set directly by the 10-bit wide control word TXBIAS[0..9] (*register 15* and *register 16*). In Automatic Power Control (APC) mode, selected by setting TXOLENA = 0, the bias current depends on the register settings TXBIAS[0..9] and the coupling ratio (CR) between the laser bias current and the photodiode current. CR = I_{BIAS}/I_{PD}. If the photodiode cathode is connected to VCC and the anode is connected to the PD pin (PD pin is sinking current) set TXPDPOL = 1 (bit 0 of *register 1*). If the photodiode anode is connected to ground and the cathode is connected to the PD pin (PD pin is sourcing current), set TXPDPOL = 0.

Three photodiode current ranges can be selected by means of the photodiode current range bits TXPDRNG[0..1] (bits 5 and 6 of *register 1*). The photodiode range should be chosen to keep the laser bias control DAC, TXBIAS[0..9], close to the center of its range. This keeps the laser bias current set point resolution high. For details regarding the bias current setting in open-loop mode as well as in closed-loop mode, see the *Register Mapping* table.

The ONET1130EC has the ability to source or sink the bias current. The default condition is for the BIAS pin to source the current (TXBIASPOL = 0). To act as a sink, set TXBIASPOL = 1 (bit 1 of *register 1*).

The bias current is monitored using a current mirror with a gain equal to 1/100. By connecting a resistor between MONB and GND, the bias current can be monitored as a voltage across the resistor. A low temperature coefficient precision resistor should be used. The bias current can also be monitored as a 10 bit unsigned digital word by setting the transmitter bias current digital monitor selection bit TXDMONB = 1 (bit 5 of *register 16*) and removing the resistor from MONB to ground.

The photodiode current is monitored using a current mirror with various gains that are dependent upon the photodiode current range being used. By connecting a resistor between MONP and GND, the photodiode current can be monitored as a voltage across the resistor. A low temperature coefficient precision resistor should be used. The photodiode current can also be monitored as a 10 bit unsigned digital word by setting the transmitter photodiode current digital monitor selection bit TXDMONP = 1 (bit 6 of *register 16*) and removing the resistor from MONP to ground.

8.3.1.8 Laser Safety Features and Fault Recovery Procedure

The ONET1130EC provides built in laser safety features. The following fault conditions are detected if the transmitter fault detection enable bit TXFLTEN = 1 (bit 3 of *register 1*):

1. Voltage at MONB exceeds the bandgap voltage (1.2 V) or, alternately, if TXDMONB = 1 and the bias current exceeds the bias current monitor fault threshold set by TXBMF[0..7] (*register 17*). When using the digital monitor, the resistor from the MONB pin to ground must be removed.
2. Voltage at MONP exceeds the bandgap voltage (1.2 V) and the analog photodiode current monitor fault trigger bit, TXMONPFLT (bit 7 of *register 1*), is set to 1. Alternately, a fault can be triggered if TXDMONP = 1 and the photodiode current exceeds the photodiode current monitor fault threshold set by TXPMF[0..7] (*register 18*). When using the digital monitor, the resistor from the MONP pin to ground must be removed.
3. Photodiode current exceeds 150% of its set value,
4. Bias control DAC drops in value by more than 50% in one step.

If the fault detection is being used then to avoid a fault from occurring at start-up it is recommended to set up the required bias current and APC loop conditions first and enable the laser bias current (TXBIASEN = 1) as the last step in the sequence of commands.

If one or more fault conditions occur and the transmitter fault enable bit TXFLTEN is set to 1, the ONET1130EC responds by:

1. Setting the bias current to zero.
2. Asserting and latching the TX_FLT pin.
3. Setting the TX_FLT bit (bit 5 of *register 43*) to 1.

Fault recovery is performed by the following procedure:

1. The transmitter disable pin TX_DIS and/or the transmitter bias current enable bit TXBIASEN are toggled for at least the fault latch reset time.

Feature Description (continued)

2. The TX_FLT pin de-asserts while the transmitter disable pin TX_DIS is asserted or the transmitter bias current enable bit TXBIASEN is de-asserted.
3. If the fault condition is no longer present, the part will return to normal operation with its prior output settings after the disable negate time.
4. If the fault condition is still present, TX_FLT re-asserts once TX_DIS is set to a low level and/or TXBIASEN is set to 0 and the part will not return to normal operation.

8.3.2 Receiver

8.3.2.1 Equalizer

The data signal is applied to an input equalizer by means of the input signal pins RXIN+ / RXIN–, which provide on-chip differential 100 Ω line-termination. The equalizer is enabled by default and can be disabled by setting the receiver equalizer disable bit RXEQ_DIS = 1 (bit 1 of *register 4*). Equalization is provided for bandwidth compensation of the optical receiver. The amount of equalization is set through the register settings RXCTLE [0..2] (*register 5*). The device can accept input amplitude levels from 6 mVpp up to 800 mVpp.

8.3.2.2 DC Offset Cancellation and Cross Point Control

Receiver offset cancellation compensates for internal offset voltages and thus ensures proper operation even for very small input data signals. The offset cancellation is enabled by default and the input threshold voltage can be adjusted using register settings RXTHADJ[0..3] (*register 6*) to optimize the bit error rate or change the eye crossing point to compensate for input signal pulse width distortion. The offset cancellation can be disabled by setting RXOC_DIS = 1 (bit 2 of *register 4*) and this also disables the cross point adjustment.

8.3.2.3 CDR

The receiver clock and data recovery function consists of a Phase-Locked Loop (PLL) and retimer. The CDR can be operated without a reference clock and the Voltage Controlled Oscillator (VCO) can cover 9.8Gbps to 11.7 Gbps data rates. The PLL is phase locked to the incoming data stream and attenuates the high frequency jitter on the data, producing a recovered clean clock with substantially reduced jitter. An external capacitor for the PLL loop filter is connected to the RX_LF pin. A value of 2.2 nF is recommended. The clean clock is used to retime the incoming data, producing an output signal with reduced jitter, and in effect, resetting the jitter budget for the receiver.

The CDR is enabled by default. The CDR can be disabled and bypassed by setting the receiver CDR disable bit RXCDR_DIS = 1 (bit 4 of *register 4*). Alternatively, the CDR can be left powered on but bypassed by setting the receiver CDR bypass bit RX_CDRBP = 1 (bit 3 of *register 4*); however, this only works if the transmitter CDR bypass bit TX_CDRBP (bit 3 of *register 10*) is also set to 1.

The CDR is designed to meet the XFP Datacom requirements and Telecom requirements for a maximum of 1 dB jitter peaking at a frequency greater than 120 kHz. The CDR is not designed to meet the Telecom regenerator requirements of jitter peaking less than 0.03 dB at a frequency less than 120 kHz.The default CDR bandwidth is typically 4.5 MHz and can be adjusted using the SEL_RES[0..2] bits (bits 5 to 7 of *register 51*). Adjusting these bits changes the bandwidth of both the receiver and transmitter CDRs.

For the majority of applications the default settings in *register 9* for the receiver CDR can be used. However, for some applications or for test purposes, some modes of operation may be useful. The frequency detector for the PLL is set to an automatic mode of operation by default. When a signal is applied to the receiver input the frequency detector search algorithm will be initiated to determine the frequency of the data. The default algorithm ensures a fast CDR lock time of less than 2 ms. The fast lock can be disabled by setting the receiver CDR fast lock disable bit RXFL_DIS = 1 (bit 3 of *register 9*). Once the frequency has been detected then the frequency detector will be disabled and the supply current will decrease by approximately 10 mA. In some applications, such as when there are long periods of idle data, it may be advantageous to keep the frequency detector permanently enabled by setting the receiver frequency detector enable bit RXFD_EN = 1 (bit 5 of *register 9*). For test purposes, the frequency detector can be permanently disabled by setting the receiver frequency detector

Feature Description (continued)

disable bit RXFD_DIS = 1 (bit 4 of *register 9*). For fast lock times the frequency detector can be set to one of two preselected data rates using the receiver frequency detection mode selection bits RXFD_MOD[0..1] (bits 6 and 7 of *register 9*). If it is desired to use the retimer at lower data rates than the standard 9.8 to 11.7 Gbps then the receiver divider ratio should be adjusted accordingly through RXDIV[0..2] (bits 0 to 2 of *register 9*). For example, for retimed operation at 2.5 Gbps the divider should be set to divide by 4.

8.3.2.4 Output Driver

The output amplitude of the driver can be varied from 300 mVpp to 900 mVpp using the register settings RXAMP[0..3] (*register 8*). The default amplitude setting is 300 mVpp. To compensate for frequency dependent losses of transmission lines connected to the output, adjustable de-emphasis is provided. The de-emphasis can be adjusted using RXDADJ[0..2] (*register 8*). The polarity of the output pins can be inverted by setting the receiver output polarity switch bit RXOUTPOL = 1 (bit 5 of *register 4*).

In addition, the output driver can be disabled by setting the receiver output driver disable bit RXOUT_DIS = 1 (bit 6 of *register 4*) or the receiver signal path can be disabled and powered down by setting RX_DIS = 1 (bit 7 of *register 4*).

8.3.2.5 Receiver Loopback (Optical Loopback)

The signal input to the RXIN+ and RXIN– pins can be looped back to the transmitter output after the retimer as shown in Figure 39 by setting RX_LBMUX = 1 (bit 1 of *register 2*). Loopback from the transmitter input to the receiver output (electrical loopback) can be enabled at the same time.

If it is desired to loopback the signal input to the RXIN+ and RXIN– pins to the transmitter output with the CDR disabled then the receive CDR must be disabled and bypassed by setting RXCDR_DIS = 1 (bit 4 of *register 4*) and the transmit CDR must also be disabled and bypassed by setting TXCDR_DIS =1 (bit 4 of *register 10*).

Feature Description (continued)

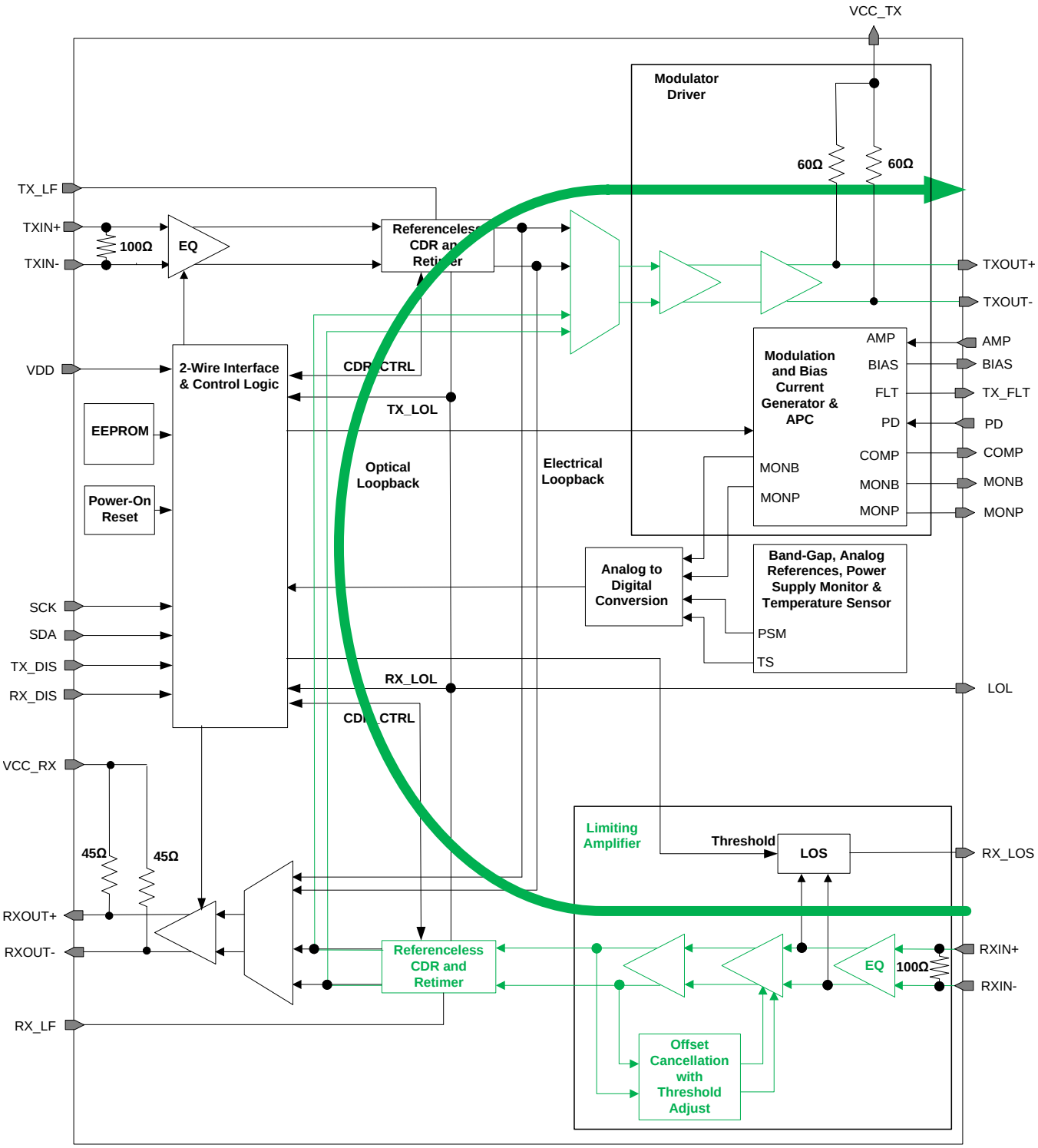


Figure 39. Optical Loopback

Feature Description (continued)

8.3.2.6 Loss of Signal Detection

The loss of signal (LOS) detection is done by 2 separate level detectors to cover a wide dynamic range. The peak values of the input signal are monitored by a peak detector and compared to a pre-defined loss of signal threshold voltage inside the loss of signal detection block. As a result of the comparison, the LOS signal, which indicates that the input signal amplitude is below the defined threshold level, is generated. There are 2 LOS ranges settable with the RXLOSRNG bit (bit 0 of *register 4*). With RXLOSRNG = 0 the high range of the LOS assert values are used (40 mV_{PP} to 130 mV_{PP}) and by setting RXLOSRNG = 1 the low range of the LOS assert values are used (10 mV_{PP} to 50 mV_{PP}). There are 64 possible internal LOS settings set with RXLOSA[0..5] (*register 7*) for each LOS range to adjust the LOS assert level.

The typical LOS hysteresis, as defined by 20log(LOS de-assert voltage/LOS assert voltage) is 4 dB. This can be reduced by approximately 2 dB by setting receiver hysteresis RXHYS = 1 (bit 7 of *register 6*). In addition, the LOS detection time can be reduced by setting the receiver fast LOS bit RXFLOS = 1 (bit 3 of *register 5*); however, this may result in chatter (LOS bounce).

8.3.3 Analog Block

8.3.3.1 Analog Reference and Temperature Sensor

The ONET1130EC is supplied by a single 2.5 V ±5% supply voltage connected to the VCC_TX, VCC_RX and VDD pins. This voltage is referred to ground (GND) and can be monitored as a 10 bit unsigned digital word through the 2-wire interface.

On-chip bandgap voltage circuitry generates a reference voltage, independent of the supply voltage, from which all other internally required voltages and bias currents are derived.

In order to minimize the module component count, the ONET1130ECprovides an on-chip temperature sensor. The temperature can be monitored as a 10 bit unsigned digital word through the 2-wire interface.

8.3.3.2 Power-On Reset

The ONET1130EC has power on reset circuitry which ensures that all registers are reset to default values during startup. After the power-on to initialize time (t_{INIT1}), the internal registers are ready to be loaded. The part is ready to transmit data after the initialize to transmit time (t_{INIT2}), assuming that the enable chip bit EN_CHIP = 1 (bit 0 of *register 0*). In addition, the transmitter disable pin TX_DIS and receiver disable pin RX_DIS must be set to zero.

The ONET1130EC bias current can be disabled by setting the TX_DIS pin high. The internal registers are not reset. After the transmitter disable pin TX_DIS is set low the part returns to its prior output settings.

8.3.3.3 Analog to Digital Converter

The ONET1130EC has an internal 10 bit analog to digital converter (ADC) that converts the analog monitors for temperature, power supply voltage, bias current and photodiode current into a 10 bit unsigned digital word. The first 8 most significant bits (MSBs) are available in *register 40* and the 2 least significant bits (LSBs) are available in *register 41*. Depending on the accuracy required, 8 bits or 10 bits can be read. However, due to the architecture of the 2-wire interface, in order to read the 2 registers, 2 separate read commands have to be sent.

The ADC is enabled by default so to monitor a particular parameter, select the parameter with ADCSEL[0..2] (bits 0 to 2 of *register 3*). Table 2 shows the ADCSEL bits and the parameter that is monitored.

Table 2. ADC Selection Bits and the Monitored Parameter

ADCSEL2	ADCSEL1	ADCSEL0	MONITORED PARAMETER
0	0	0	Temperature
0	0	1	Supply voltage
0	1	0	Bias current
0	1	1	Photodiode current

To digitally monitor the photodiode current, ensure that TXDMONP = 1 (bit 6 of *register 16*) and that a resistor is not connected to the MONP pin. To digitally monitor the bias current, ensure that TXDMONB = 1 (bit 5 of *register 16*) and that a resistor is not connected to the MONB pin. The ADC is disabled by default. To enable the ADC, set the ADC oscillator enable bit OSCEN = 1 (bit 6 of *register 3*) and set the ADC enable bit ADCEN = 1 (bit 7 of *register 3*).

The digital word read from the ADC can be converted to its analog equivalent through the following formulas.

$$\text{Temperature (°C)} = (0.5475 \times \text{ADCx}) - 273 \quad (1)$$

$$\text{Power supply voltage (V)} = (1.36\text{m} \times \text{ADCx}) + 1.76 \quad (2)$$

$$\text{IPD}(\mu\text{A}) = 2 \times [\,(0.62 \times \text{ADCx}) - 16] \text{ for TXPDRNG00} \quad (3)$$

$$\text{IPD}(\mu\text{A}) = 4 \times [\,(0.62 \times \text{ADCx}) - 16] \text{ for TXPDRNG01} \quad (4)$$

$$\text{IPD}(\mu\text{A}) = 8 \times [\,(0.62 \times \text{ADCx}) - 16] \text{ for TXPDRNG1x} \quad (5)$$

$$\text{IBIAS (mA)} = (0.2 \times \text{ADCx}) - 4.5 \quad (6)$$

Where: ADCx = the decimal value read from the ADC

8.3.3.4 2-Wire Interface and Control Logic

The ONET1130EC uses a 2-wire serial interface for digital control. The two circuit inputs, SDA and SCK, are driven, respectively, by the serial data and serial clock from a microprocessor, for example. The SDA and SCK pins require external 4.7-kΩ to 10-kΩ pull-up resistor to VCC for proper operation.

The 2-wire interface allows write access to the internal memory map to modify control registers and read access to read out the control signals. The ONET1130EC is a slave device only which means that it cannot initiate a transmission itself; it always relies on the availability of the SCK signal for the duration of the transmission. The master device provides the clock signal as well as the START and STOP commands. The protocol for a data transmission is as follows:

1. START command
2. Seven (7) bit slave address (0001000) followed by an eighth bit which is the data direction bit (R/W). A zero indicates a WRITE and a 1 indicates a READ.
3. 8 bit register address
4. 8 bit register data word
5. STOP command

Regarding timing, the ONET1130EC is I^2C compatible. The typical timing is shown in Figure 2 and a complete data transfer is shown in Figure 40. Parameters for Figure 2 are defined in Table 1.

8.3.3.5 Bus Idle

Both SDA and SCK lines remain HIGH

8.3.3.6 Start Data Transfer

A change in the state of the SDA line, from HIGH to LOW, while the SCK line is HIGH, defines a START condition (S). Each data transfer is initiated with a START condition.

8.3.3.7 Stop Data Transfer

A change in the state of the SDA line from LOW to HIGH while the SCK line is HIGH defines a STOP condition (P). Each data transfer is terminated with a STOP condition; however, if the master still wishes to communicate on the bus, it can generate a repeated START condition and address another slave without first generating a STOP condition.

8.3.3.8 Data Transfer

Only one data byte can be transferred between a START and a STOP condition. The receiver acknowledges the transfer of data.

8.3.4 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge bit. The transmitter releases the SDA line and a device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge clock pulse. Setup and hold times must be taken into account. When a slave-receiver doesn't acknowledge the slave address, the data line must be left HIGH by the slave. The master can then generate a STOP condition to abort the transfer. If the slave-receiver does acknowledge the slave address but some time later in the transfer cannot receive any more data bytes, the master must abort the transfer. This is indicated by the slave generating the not acknowledge on the first byte to follow. The slave leaves the data line HIGH and the master generates the STOP condition, see Figure 2.

8.4 Device Functional Modes

The ONET1130EC has two main functional modes of operation: differential transmitter output and single-ended transmitter output.

8.4.1 Differential Transmitter Output

Operation with differential output is the default mode of operation. This mode is intended for externally modulated lasers requiring differential drive such as Mach Zehnder modulators.

8.4.2 Single-Ended Transmitter Output

In order to reduce the power consumption for single-ended EML applications the output driver should be set to single-ended mode. The single-ended output signal can be enabled by setting the transmitter mode select bit TXMODE = 1 (bit 6 of *register 13*). The positive output is active by default. To enable the negative output and disable the positive output set TXOUTSEL = 1 (bit 7 of *register 13*).

8.5 Programming

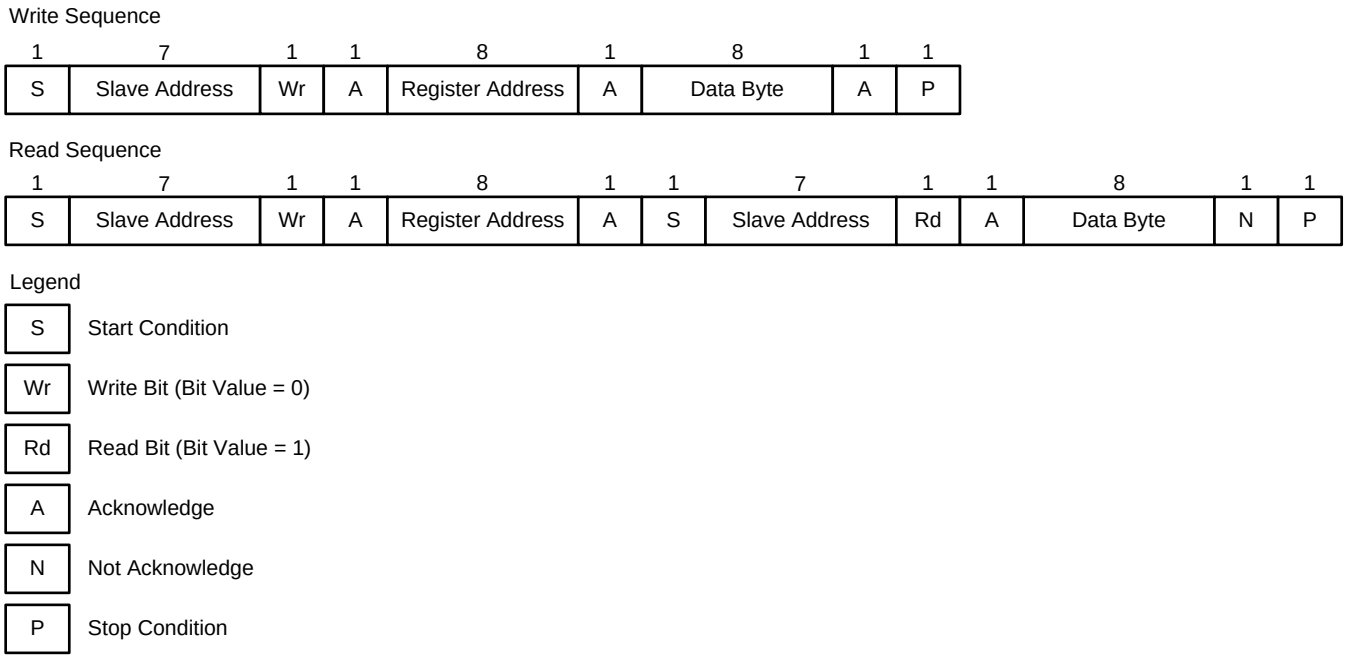


Figure 40. Programming Sequence

8.6 Register Mapping

8.6.1 R/W Control Registers

8.6.1.1 Core Level Register 0 (offset = 0100 0001 [reset = 41h]

Figure 41. Core Level Register 0

7	6	5	4	3	2	1	0
0	Reserved					0	1
RWSC	RW	–	–	–	RWSC	RWSC	RW

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset. RWSC = Read/Write self clearing (always reads back to zero)

Table 3. Core Level Register 0 Field Descriptions

Bit	Field	Type	Reset	Description
7	GLOBAL SW_PIN RESET	RWSC	0h	**Global Reset SW** 1 = reset, resets all I2C and EEPROM modules to default 0 = normal operation (self-clearing, always reads back '0')
6 :2	–	R/W	4h	Reserved
1	I2C RESET	RWSC	0h	**Chip reset bit** 1 = resets all I2C registers to default 0 = normal operation (self-clearing, always reads back '0')
0	EN_CHIP	R/W	1h	**Enable chip bit** 1 = Chip enabled

8.6.1.2 Core Level Register 1 (offset = 0000 0000) [reset = 0h]

Figure 42. Core Level Register 1

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 4. Core Level Register 1 Field Descriptions

Bit	Field	Type	Reset	Description
7	TXMONPFLT	R/W	0	Analog photodiode current monitor fault trigger bit 1 = Fault trigger on MONP pin is enabled 0 = Fault trigger on MONP pin is disabled
6 5	TXPDRNG1 TXPDRNG0	R/W	0	**Photodiode current range bits** 1X: up to 3080µA / 3µA resolution 01: up to 1540µA / 1.5µA resolution 00: up to 770µA / 0.75µA resolution
4	TXOLENA	R/W	0	**Open loop enable bit** 1 = Open loop bias current control 0 = Closed loop bias current control
3	TXFLTEN	R/W	0	**Fault detection enable bit** 1 = Fault detection on 0 = Fault detection off
2	TXBIASEN	R/W	0	**Laser Bias current enable bit** 1 = Bias current enabled. Toggle to 0 to reset a fault condition. 0 = Bias current disabled
1	TXBIASPOL	R/W	0	**Laser Bias current polarity bit** 1 = Bias pin sinks current 0 = Bias pin sources current

Table 4. Core Level Register 1 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	TXPDPOL	R/W	0	**Photodiode polarity bit** 1 = Photodiode cathode connected to VCC 0 = Photodiode anode connected to GND

8.6.1.3 Core Level Register 2 (offset = 0000 0000) [reset = 0h]

Figure 43. Core Level Register 2

7	6	5	4	3	2	1	0
Reserved						0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 5. Core Level Register 2 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	–	R/W	0h	Reserved
3	–	R/W	0h	Reserved
2	–	R/W	0h	Reserved
1	RX_LBMUX	R/W	0h	**RX-Loopback MUX Setting (optical LB)** 1 = Loopback from TX-CDR output selected. 0 = Normal operation: RX-CDR output selected
0	TX_LBMUX	R/W	0h	**TX-Loopback MUX Setting (electrical LB)** 1 = Loopback from RX-CDR output selected. 0 = Normal operation: TX-CDR output selected

8.6.1.4 Core Level Register 3 (offset = 0000 0000) [reset = 0h]

Figure 44. Core Level Register 3

7	6	5	4	3	2	1	0
0	0	–	0	–	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6. Core Level Register 3 Field Descriptions

Bit	Field	Type	Reset	Description
7	ADCEN	R/W	0h	**ADC enabled bit** 1 = ADC enabled 0 = ADC disabled
6	OSCEN	R/W	0h	**ADC oscillator bit** 1 = Oscillator enabled 0 = Oscillator disabled
5	–	R/W	0h	Reserved
4	ADCRST	R/W	0h	**ADC reset** 1 = ADC reset 0 = ADC no reset
3	–	R/W	0h	Reserved
2	ADCSEL2	R/W	0h	**ADC input selection bits <2:0>** 000 selects the temperature sensor 001 selects the power supply monitor 010 selects IMONB 011 selects IMONP 1XX are reserved
1	ADCSEL1	R/W	0h	
0	ADCSEL0	R/W	0h	

8.6.2 RX Registers

8.6.2.1 RX Register 4 (offset = 0000 0000) [reset = 0h]

Figure 45. RX Register 4

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7. RX Register 4 Field Descriptions

Bit	Field	Type	Reset	Description
7	RX_DIS	R/W	0h	**RX disable bit** 1 = RX disabled (power-down) 0 = RX enabled
6	RXOUT_DIS	R/W	0h	**RX Output Driver disable bit** 1 = output driver is disabled 0 = output driver is enabled
5	RXOUTPOL	R/W	0h	**RX Output polarity switch bit** 1 = inverted polarity 0 = normal polarity
4	RXCDR_DIS	R/W	0h	**RX CDR disable bit** 1 = RX CDR is disabled and bypassed 0 = RX CDR is enabled
3	RX_CDRBP	R/W	0h	**RX CDR bypass bit** 1 = RX-CDR bypassed. TX_CDRBP must be set to 1 for this function to operate. 0 = RX-CDR not bypassed
2	RXOC_DIS	R/W	0h	**RX Offset cancellation disable bit** 1 = offset cancellation and threshold adjust is disabled 0 = offset cancellation and threshold adjust is enabled
1	RXEQ_DIS	R/W	0h	**RX Equalizer disable bit** 1 = RX Equalizer is disabled and bypassed 0 = RX Equalizer is enabled
0	RXLOSRNG	R/W	0h	**LOS range bit** 1 = low LOS assert voltage range 0 = high LOS assert voltage range

8.6.2.2 RX Register 5 (offset = 0000 0000) [reset = 0h]

Figure 46. RX Register 5

7	6	5	4	3	2	1	0
Reserved				0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 8. RX Register 5 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	–	R/W	0h	Reserved
3	RXFLOS	R/W	0h	**Receiver fast LOS bit** 1 = Fast LOS 0 = normal operation
2	RXCTLE2	R/W	0h	**RX input CTLE setting** 000 = minimum 111 = maximum
1	RXCTLE1	R/W	0h	
0	RXCTLE0	R/W	0h	

8.6.2.3 RX Register 6 (offset = 0000 0000) [reset = 0h]

Figure 47. RX Register 6

7	6	5	4	3	2	1	0
0	Reserved		0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9. RX Register 6 Field Descriptions

Bit	Field	Type	Reset	Description
7	RXHYS	R/W	0h	**Receiver Hysteresis** 1 = Reduce hysteresis level by approximately 2dB 0 = default level of hysteresis (approximately 4dB)
6:5	–	R/W	0h	Reserved
4	RXTHSGN	R/W	0h	**RX Eye cross-point adjustment setting** RXTHSGN = 1 (positive shift) Maximum shift for 1111 Minimum shift for 0000 RXTHSGN = 0 (negative shift) Maximum shift for 1111 Minimum shift for 0000
3	RXTHADJ3	R/W	0h	
2	RXTHADJ2	R/W	0h	
1	RXTHADJ1	R/W	0h	
0	RXTHADJ0	R/W	0h	

8.6.2.4 RX Register 7 (offset = 0000 0000) [reset = 0h]

Figure 48. RX Register 7

7	6	5	4	3	2	1	0
Reserved		0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 10. RX Register 7 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	–	R/W	0h	Reserved
5	RXLOSA5	R/W	0h	**LOS assert level** Minimum LOS assert level for 000000 Maximum LOS assert level for 111111
4	RXLOSA4	R/W	0h	
3	RXLOSA3	R/W	0h	
2	RXLOSA2	R/W	0h	
1	RXLOSA1	R/W	0h	
0	RXLOSA0	R/W	0h	

8.6.2.5 RX Register 8 (offset = 0000 0000) [reset = 0h]

Figure 49. RX Register 8

7	6	5	4	3	2	1	0
Reserved	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 11. RX Register 8 Field Descriptions

Bit	Field	Type	Reset	Description
7	–	R/W	0h	Reserved
6	RXDADJ1	R/W	0h	**RX output de-emphasis setting** 00 = minimum de-emphasis 11 = maximum de-emphasis
5	RXDADJ0	R/W	0h	
4	RXDRVSC	R/W	0h	**RX driver short circuit protection** 1 = short circuit protection enabled 0 = normal operation
3	RXAMP3	R/W	0h	**RX output amplitude adjustment** 0000 = minimum amplitude 1111 = maximum amplitude
2	RXAMP2	R/W	0h	
1	RXAMP1	R/W	0h	
0	RXAMP0	R/W	0h	

8.6.2.6 RX Register 9 (offset = 0000 0000) [reset = 0h]

Figure 50. RX Register 9

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 12. RX Register 9 Field Descriptions

Bit	Field	Type	Reset	Description
7	RXFD_MOD1	R/W	0h	**RX frequency detection mode selection** 00 = auto selection enabled 01 = Pre-selected to 10.3Gbps 10 = Pre-select to 11.1Gbps 11 = test mode (do not use)
6	RXFD_MOD0	R/W	0h	
5	RXFD_EN	R/W	0h	**RX frequency detector enable bit** 1 = RX frequency detector is always enabled 0 = RX frequency detector in automatic mode
4	RXFD_DIS	R/W	0h	**RX frequency detector disable bit** 1 = RX frequency detector is always disabled 0 = RX frequency detector is in automatic mode
3	RXFL_DIS	R/W	0h	**RX CDR fast lock disable bit** 1 = RX CDR fast lock disabled 0 = RX CDR in fast lock mode
2	RXDIV2	R/W	0h	**RX Divider Ratio** 000: Full-Rate, 001: Divide by 2 010: Divide by 4 011: Divide by 8 100: Divide by 16 101: Divide by 32
1	RXDIV1	R/W	0h	
0	RXDIV0	R/W	0h	

8.6.3 TX Registers

8.6.3.1 TX Register 10 (offset = 0000 0000) [reset = 0h]

Figure 51. TX Register 10

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 13. TX Register 10 Field Descriptions

Bit	Field	Type	Reset	Description
7	TX_DIS	R/W	0h	**TX disable bit** 1 = TX disabled (power-down) 0 = TX enabled
6	TXOUT_DIS	R/W	0h	**TX Output Driver disable bit** 1 = output disabled 0 = output enabled
5	TXOUTPOL	R/W	0h	**TX Output polarity switch bit** 1 = inverted polarity 0 = normal polarity
4	TXCDR_DIS	R/W	0h	**TX CDR disable bit** 1 = TX CDR is disabled and bypassed 0 = TX CDR is enabled
3	TX_CDRBP	R/W	0h	**TX CDR bypass bit** 1 = TX-CDR bypassed. RX_CDRBP must be set to 1 for this function to operate. 0 = TX-CDR not bypassed
2	TXOC_DIS	R/W	0h	**TX OC disable bit** 1 = TX Offset Cancellation disabled 0 = TX Offset Cancellation enabled
1	TXEQ_DIS	R/W	0h	**TX Equalizer disable bit** 1 = TX Equalizer is disabled and bypassed 0 = TX Equalizer is enabled
0	TXAMPCTRL	R/W	0h	**TX AMP Ctrl** 1 = TX AMP Control is enabled (analog amplitude control) 0 = TX AMP Control is disabled (digital amplitude control)

8.6.3.2 TX Register 11 (offset = 0000 0000) [reset = 0h]

Figure 52. TX Register 11

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 14. TX Register 11 Field Descriptions

Bit	Field	Type	Reset	Description
7	TXAMPRNG	R/W	0h	**TX output AMP range** 1 = Half TX output amplitude range 0 = Full TX output amplitude range
6	TXPKSEL	R/W	0h	**TX output peaking width** 1 = wide peaking width 0 = narrow peaking width
5	TXTCSEL1	R/W	0h	TXOUT temperature compensation select bit 1
4	TXTCSEL0	R/W	0h	TXOUT temperature compensation select bit 0
3	TXCTLE3	R/W	0h	**TX input CTLE setting** 0000 = minimum 1111 = maximum
2	TXCTLE2	R/W	0h	
1	TXCTLE1	R/W	0h	
0	TXCTLE0	R/W	0h	

8.6.3.3 TX Register 12 (offset = 0000 0000) [reset = 0h]

Figure 53. TX Register 12

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 15. TX Register 12 Field Descriptions

Bit	Field	Type	Reset	Description
7	TXMOD7	R/W	0h	**TX Modulation current setting: sets the output voltage** Output Voltage: 2.4 Vpp / 9.5 mVpp steps
6	TXMOD6	R/W	0h	
5	TXMOD5	R/W	0h	
4	TXMOD4	R/W	0h	
3	TXMOD3	R/W	0h	
2	TXMOD2	R/W	0h	
1	TXMOD1	R/W	0h	
0	TXMOD0	R/W	0h	

8.6.3.4 TX Register 13 (offset = 0h) [reset = 0]

Figure 54. TX Register 13

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 16. TX Register 13 Field Descriptions

Bit	Field	Type	Reset	Description
7	TXOUTSEL	R/W	0h	**TX output selection bit** 1 = The negative output TXOUT– is active if TXMODE = 1 0 = The positive output TXOUT+ is active if TXMODE = 1
6	TXMODE	R/W	0h	**TX output mode selection bit** 1 = Single-ended mode 0 = Differential mode
5	TXSTEP	R/W	0h	**TX output de-emphasis mode selection bit** 1 = Delayed de-emphasis 0 = Normal de-emphasis
4	TXSLOW	R/W	0h	**TX edge speed selection bit** 1 = Slow edge speed 0 = Normal operation
3	TXDEADJ3	R/W	0h	**TX de-emphasis setting** 0000 = minimum 1111 = maximum
2	TXDEADJ2	R/W	0h	
1	TXDEADJ1	R/W	0h	
0	TXDEADJ0	R/W	0h	

8.6.3.5 TX Register 14 (offset = 0000 0000) [reset = 0h]

Figure 55. TX Register 14

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 17. TX Register 14 Field Descriptions

Bit	Field	Type	Reset	Description
7	TXCPSGN	R/W	0h	**TX Eye cross-point adjustment setting** TXCPSGN = 1 (positive shift) Maximum shift for 1111111 Minimum shift for 0000000 TXCPSGN = 0 (negative shift) Maximum shift for 1111111 Minimum shift for 0000000
6	TXCPADJ6	R/W	0h	
5	TXCPADJ5	R/W	0h	
4	TXCPADJ4	R/W	0h	
3	TXCPADJ3	R/W	0h	
2	TXCPADJ2	R/W	0h	
1	TXCPADJ1	R/W	0h	
0	TXCPADJ0	R/W	0h	

8.6.3.6 TX Register 15 (offset = 0000 0000) [reset = 0h]

Figure 56. TX Register 15

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 18. TX Register 15 Field Descriptions

Bit	Field	Type	Reset	Description
7	TXBIAS9	R/W	0h	**Bias current settings (8MSB; 2LSBs are in register 16)** **Closed loop (APC):** Coupling ratio CR = I_{BIAS} / I_{PD}, TXBIAS = 0..1023, I_{BIAS} ≤ 150mA: TXPDRNG = 00; I_{BIAS} = 0.75µA x CR x TXBIAS TXPDRNG = 01; I_{BIAS} = 1.5µA x CR x TXBIAS TXPDRNG = 1X; I_{BIAS} = 3µA x CR x TXBIAS **Open Loop:** I_{BIAS} ~ 156µA x TXBIAS in source mode I_{BIAS} ~ 156µA x TXBIAS in sink mode
6	TXBIAS8	R/W	0h	
5	TXBIAS7	R/W	0 h	
4	TXBIAS6	R/W	0h	
3	TXBIAS5	R/W	0h	
2	TXBIAS4	R/W	0h	
1	TXBIAS3	R/W	0h	
0	TXBIAS2	R/W	0h	

8.6.3.7 TX Register 16 (offset = 0000 0000) [reset = 0h]

Figure 57. TX Register 16

7	6	5	4	3	2	1	0
Reserved	0	0	Reserved			0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 19. TX Register 16 Field Descriptions

Bit	Field	Type	Reset	Description
7	–	R/W	0h	Reserved
6	TXDMONP	R/W	0h	**Digital photodiode current monitor selection bit (MONP)** 1 = Digital photodiode monitor is active (no external resistor is needed) 0 = Analog photodiode monitor is active (external resistor is required)
5	TXDMONB	R/W	0h	**Digital bias current monitor selection bit (MONB)** 1 = Digital bias current monitor is active (no external resistor is needed) 0 = Analog bias current monitor is active (external resistor is required)
4:2	–	R/W	0h	Reserved
1	TXBIAS1	R/W	0h	**Bias current setting (2 LSBs)**
0	TXBIAS0	R/W	0h	

8.6.3.8 TX Register 17 (offset = 0000 0000) [reset = 0h]

Figure 58. TX Register 17

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 20. TX Register 17 Field Descriptions

Bit	Field	Type	Reset	Description
7	TXBMF7	R/W	0h	**Bias current monitor fault threshold** With TXDMONB = 1 Register sets the value of the bias current that will trigger a fault. The external resistor on the MONB pin must be removed to use this feature.
6	TXBMF6	R/W	0h	
5	TXBMF5	R/W	0h	
4	TXBMF4	R/W	0h	
3	TXBMF3	R/W	0h	
2	TXBMF2	R/W	0h	
1	TXBMF1	R/W	0h	
0	TXBMF0	R/W	0h	

8.6.3.9 TX Register 18 (offset = 0000 0000) [reset = 0h]

Figure 59. TX Register 18

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 21. TX Register 18 Field Descriptions

Bit	Field	Type	Reset	Description
7	TXPMF7	R/W	0h	**Power monitor fault threshold** With TXDMONP = 1 Register sets the value of the photodiode current that will trigger a fault. The external resistor on the MONP pin must be removed to use this feature.
6	TXPMF6	R/W	0h	
5	TXPMF5	R/W	0h	
4	TXPMF4	R/W	0h	
3	TXPMF3	R/W	0h	
2	TXPMF2	R/W	0h	
1	TXPMF1	R/W	0h	
0	TXPMF0	R/W	0h	

8.6.3.10 TX Register 19 (offset = 0000 0000) [reset = 0h]

Figure 60. TX Register 19

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 22. TX Register 19 Field Descriptions

Bit	Field	Type	Reset	Description
7	TXFD_MOD1	R/W	0	**TX frequency detection mode selection** 00 = auto selection enabled 01 = Pre-selected to 10.3Gbps 10 = Pre-select to 11.1Gbps 11 = test mode (do not use)
6	TXFD_MOD0	R/W	0	
5	TXFD_EN	R/W	0	**TX frequency detector enable bit** 1 =TX frequency detector is always enabled 0 = TX frequency detector in automatic mode
4	TXFD_DIS	R/W	0	**TX frequency detector disable bit** 1 = TX frequency detector is always disabled 0 = TX frequency detector is in automatic mode
3	TXFL_DIS	R/W	0	**TX CDR fast lock disable bit** 1 = TX CDR fast lock disabled 0 = TX CDR in fast lock mode
2	TXDIV2	R/W	0	**TX Divider Ratio** 000: Full-Rate, 001: Divide by 2 010: Divide by 4 011: Divide by 8 100: Divide by 16 101: Divide by 32
1	TXDIV1	R/W	0	
0	TXDIV0	R/W	0	

8.6.4 Reserved Registers

8.6.4.1 Reserved Registers 20-39

Figure 61. Reserved Registers 20-39

7	6	5	4	3	2	1	0
Reserved							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 23. Reserved Registers 20-39 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	–	–	–	Reserved

8.6.5 Read Only Registers

8.6.5.1 Core Level Register 40 (offset = 0000 0000) [reset = 0h]

Figure 62. Core Level Register 40

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 24. Core Level Register 40 Field Descriptions

Bit	Field	Type	Reset	Description
7	ADC9 (MSB)	R	0h	**Digital representation of the ADC input source (read only)**
6	ADC8	R	0h	
5	ADC7	R	0h	
4	ADC6	R	0h	
3	ADC5	R	0h	
2	ADC4	R	0h	
1	ADC3	R	0h	
0	ADC2	R	0h	

8.6.5.2 Core Level Register 41 (offset = 0000 0000) [reset = 0h]

Figure 63. Core Level Register 41

7	6	5	4	3	2	1	0
Reserved						0	0
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 25. Core Level Register 41 Field Descriptions

Bit	Field	Type	Reset	Description
7:2	–	R	0h	Reserved
1	ADC1	R	0h	**Digital representation of the ADC input source (read only)**
0	ADC0 (LSB)	R	0h	

8.6.5.3 RX Registers 42 (offset = 0000 0000) [reset = 0h]

Figure 64. RX Registers 42

7	6	5	4	3	2	1	0
0	0	0	0	Reserved			
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset; RCLR = Read clear

Table 26. RX Registers 42 Field Descriptions

Bit	Field	Type	Reset	Description
7	RXCDRLock	R	0	**RX CDR lock status bit** 1 = RX CDR is not locked 0 = RX CDR is locked
6	RXCDRlock (latched LOW)	RCLR	0	Latched low status of bit 7. Cleared when read. Latched low bit set to 0 when raw status goes low and keep it low even if raw status goes high.
5	RXLOS	R	0	**RX LOS status bit** 1 = RX LOS asserted 0 = RX LOS de-asserted
4	RX_LOS (latched high)	RCLR	0	Latched high status of RXLOS(bit5). Cleared when read. Latched high status set to 1 when raw status goes high and keep it high even if raw status goes low.
3:0	–	R	0	Reserved

8.6.5.4 TX Register 43 (offset = 0000 0000) [reset = 0h]

Figure 65. Core Level Register 43

7	6	5	4	3	2	1	0
0	0	0	0	Reserved			
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset; RCLR = Read clear

Table 27. TX Registers 43 Field Descriptions

Bit	Field	Type	Reset	Description
7	TXCDRLock	R	0	**TX CDR lock status bit** 1 = TX CDR is not locked 0 = TX CDR is locked
6	TXCDRLock (latched Low)	RCLR	0	Latched low status of bit 7. Cleared when read. Latched low bit set to 0 when raw status goes low and keep it low even if raw status goes high.
5	TX_FLT	R	0	**TX fault status bit** 1 = TX fault detected 0 = TX fault not detected
4	TX_DRVDIS	R	0	**TX driver disable status bit** 1 = TX fault logic disables the driver 0 = TX fault logic does not disable the driver
3:0	–	R	0	Reserved

8.6.6 Adjustment Registers

8.6.6.1 Adjustment Registers 44-50

Figure 66. Adjustment Registers 44-50

7	6	5	4	3	2	1	0
Reserved							
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 28. Adjustment Registers 44-50 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	–	–	–	Reserved

8.6.6.2 Adjustment Register 51 (offset = 0100 0000) [reset = 40h]

Figure 67. Adjustment Register 51

7	6	5	4	3	2	1	0
0	1	0	Reserved				
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 29. Adjustment Register 51 Field Descriptions

Bit	Field	Type	Reset	Description
7	SEL_RES_2	R/W	0	**TX and RX CDR Loop Filter Resistor** 000: 75, 001: 150 010: 225 011: 300 100: 375 101: 450 110: 525 111: 600 Default = 225
6	SEL_RES_1	R/W	1	
5	SEL_RES_0	R/W	0	
4:0	–	R/W	0	Reserved

9 Application Information and Implementations

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The ONET1130EC is designed to be used in conjunction with a Transmitter Optical Sub-Assembly (TOSA) and a Receiver Optical Sub-Assembly (ROSA). The ONET1130EC, TOSA, ROSA, microcontroller and power management circuitry will typically be used in an XFP or SFP+ 10 Gbps optical transceiver. Figure 68 shows the ONET1130EC in differential mode of operation modulating a differentially driven Mach Zehnder (MZ) modulator TOSA and Figure 70 and Figure 71 show the device in single-ended output mode with an Electroabsorptive Modulated Laser (EML) TOSA. Figure 70 has the photodiode cathode available and Figure 71 has the photodiode anode available.

9.2 Typical Application, Transmitter Differential Mode

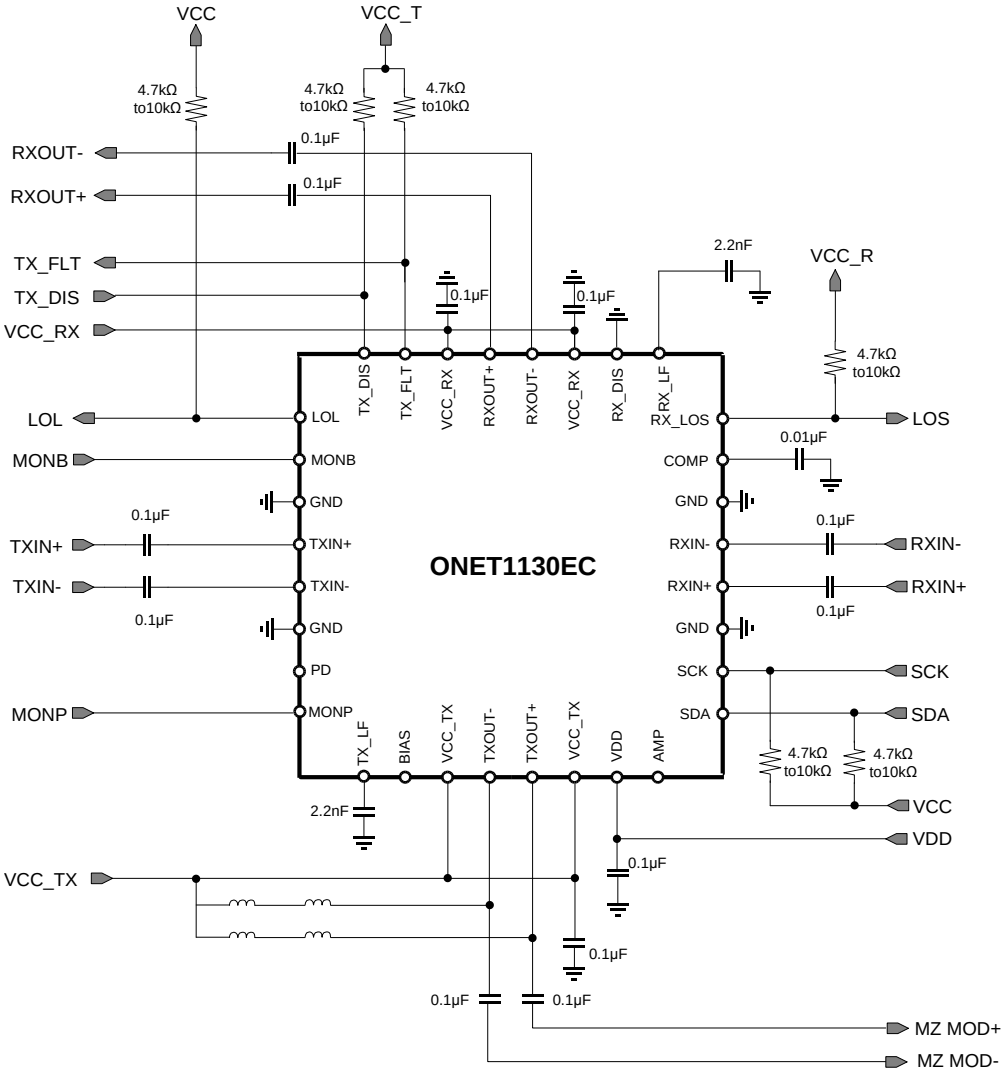


Figure 68. Typical Application Circuit in Differential Mode

Typical Application, Transmitter Differential Mode (continued)

9.2.1 Design Requirements

Table 30. Design Parameters

PARAMETER	VALUE
Supply voltage	2.5 V
Transmitter input voltage	100 mVpp to 1000 mVpp differential
Transmitter output voltage	1 Vpp to 3.6 Vpp differential
Receiver input voltage	6 mVpp to 800 mVpp differential
Receiver output voltage	300 mVpp to 900 mVpp differential

9.2.2 Detailed Design Procedure

In the transmitter differential mode of operation, the output driver is intended to be used with a differentially driven Mach Zehnder (MZ) modulator TOSA. On the input side, the TXIN+ and TXIN- pins are required to be AC coupled to the signal from the host system and the input voltage should be between 100 mVpp and 1000 mVpp differential. On the output side, the TXOUT+ pin is AC coupled to the modulator positive input and the TXOUT– pin is AC coupled to the modulator negative input. A bias-T from VCC to both the TXOUT+ and TXOUT– pins is required to supply sufficient headroom voltage for the output driver transistors. It is recommended that the inductance in the bias-T have low DC resistance to limit the DC voltage drop and maximize the voltage supplied to the TXOUT+ and TXOUT– pins. If the voltage on these pins drops below approximately 2.1V then the output rise and fall times can be adversely affected.

The receiver inputs, RXIN+ and RXIN–, are AC coupled to the output of ROSA and the input voltage should be between 6 mVpp and 800 mVpp differential. The receiver outputs, RXOUT+ and RXOUT–, are AC coupled to the receiver input of the host system.

9.2.3 Application Curve

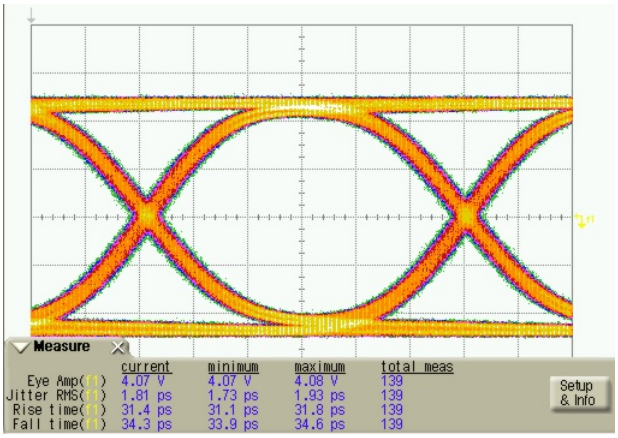


Figure 69. Differential Mode Transmitter Output Eye Diagram

9.2.4 Typical Application, Transmitter Single-Ended Mode

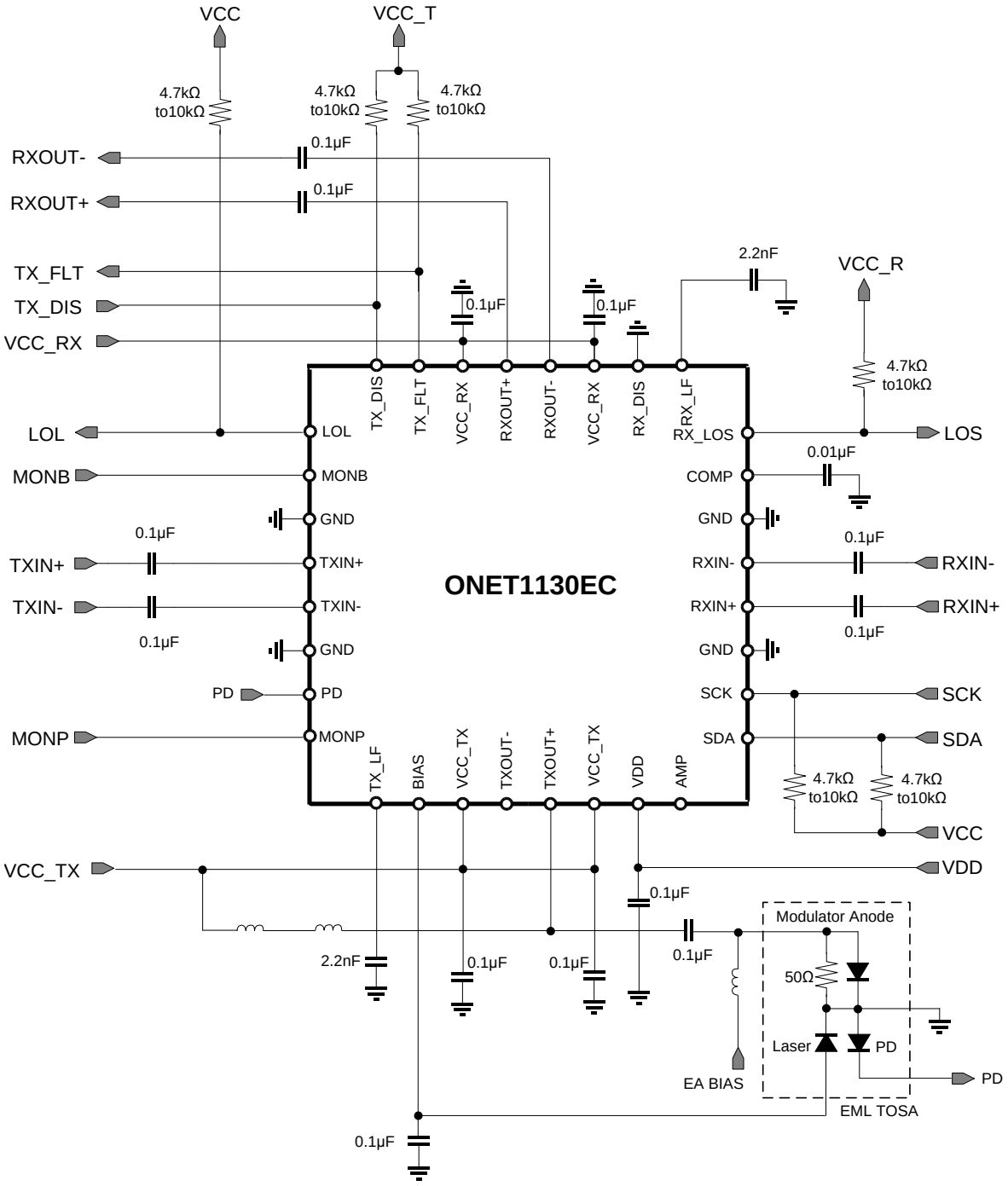


Figure 70. Typical Application Circuit in Single-Ended Mode with an EML and the PD Monitor Cathode Available

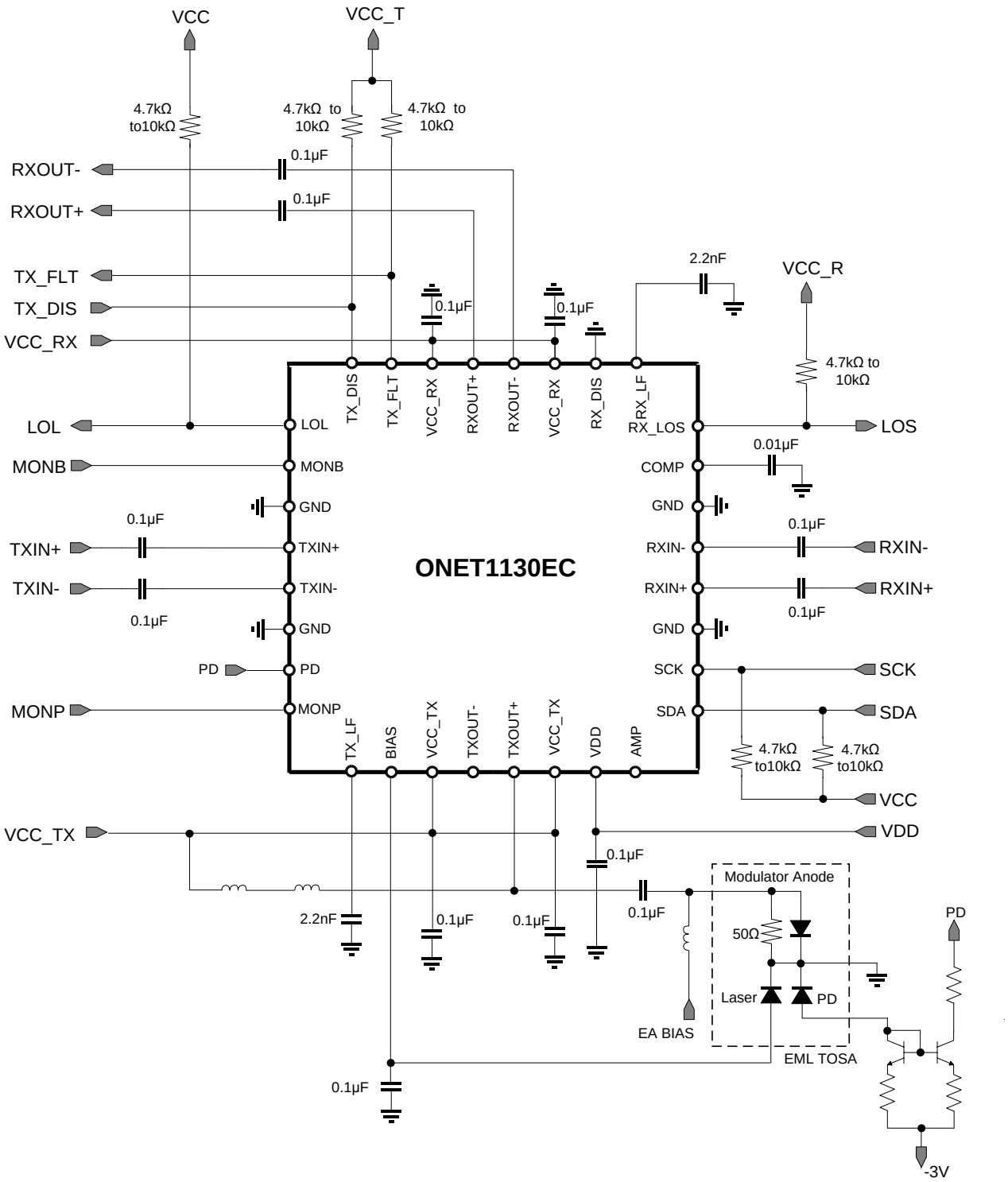


Figure 71. Typical Application Circuit in Single-Ended Mode with an EML and the PD Monitor Anode Available

9.2.4.1 Design Requirements

Table 31. Design Parameters

PARAMETER	VALUE
Supply voltage	2.5 V
Transmitter input voltage	100 mVpp to 1000 mVpp differential
Transmitter output voltage	0.5 Vpp to 2 Vpp single-ended
Receiver input voltage	6 mVpp to 800 mVpp differential
Receiver output voltage	300 mVpp to 900 mVpp differential

9.2.4.2 Detailed Design Procedure

In the transmitter single-ended mode of operation, the output driver is intended to be used with a single-ended driven Electroabsorptive Modulated Laser (EML) TOSA. On the input side, the TXIN+ and TXIN– pins are required to be AC coupled to the signal from the host system and the input voltage should be between 100mVpp and 1000mVpp differential. On the output side, it is recommended that the TXOUT+ pin is AC coupled to the modulator input and the TXOUT– pin can be left unterminated or terminated to VCC through a 50Ω resistor. A bias-T from VCC to the TXOUT+ pin is required to supply sufficient headroom voltage for the output driver transistors. It is recommended that the inductance in the bias-T have low DC resistance to limit the DC voltage drop and maximize the voltage supplied to the TXOUT+ pin. If the voltage on this pins drops below approximately 2.1V then the output rise and fall times can be adversely affected.

The receiver inputs, RXIN+ and RXIN–, are AC coupled to the output of ROSA and the input voltage should be between 6mVpp and 800mVpp differential. The receiver outputs, RXOUT+ and RXOUT–, are AC coupled to the receiver input of the host system.

9.2.4.3 Application Curves

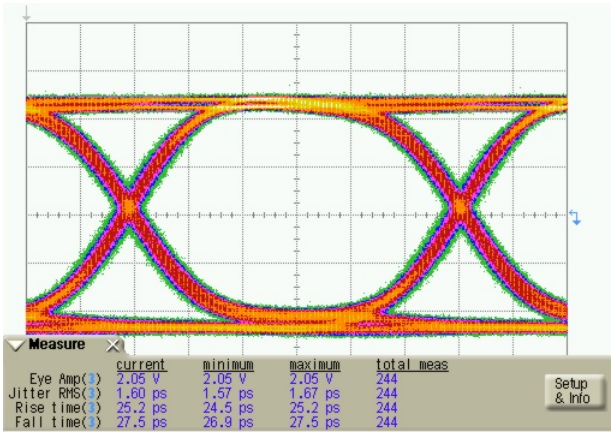


Figure 72. Single-Ended Mode Transmitter Output Eye Diagram

10 Power Supply Recommendations

The ONET1130EC is designed to operate from an input supply voltage range between 2.37 V and 2.63 V. To reduce transmitter and receiver power supply coupling, as well as digital coupling into the analog circuitry, there are separate supplies for the transmitter, receiver and digital circuitry. VCC_TX is used to supply power to the transmitter, VCC_RX is used to supply power to the receiver and VDD is used to supply power to the digital block. Power supply decoupling capacitors should be placed as close as possibly to the respective power supply pins.

11 Layout

11.1 Layout Guidelines

For optimum performance, use 50-Ω transmission lines (100-Ω differential) for connecting the high speed inputs and outputs. The length of transmission lines should be kept as short as possible to reduce loss and pattern-dependent jitter. It is recommended to maximize the separation of the TXOUT+ and TXOUT- transmission lines from the RXIN+ and RXIN- transmission lines to minimize transmitter to receiver crosstalk.

If the single-ended mode of operation is being used (TXMODE = 1) then it is recommended to terminate the unused output with a 50-Ω resistor to VCC. Figure 73 shows a typical layout for the high speed inputs and outputs.

11.2 Layout Example

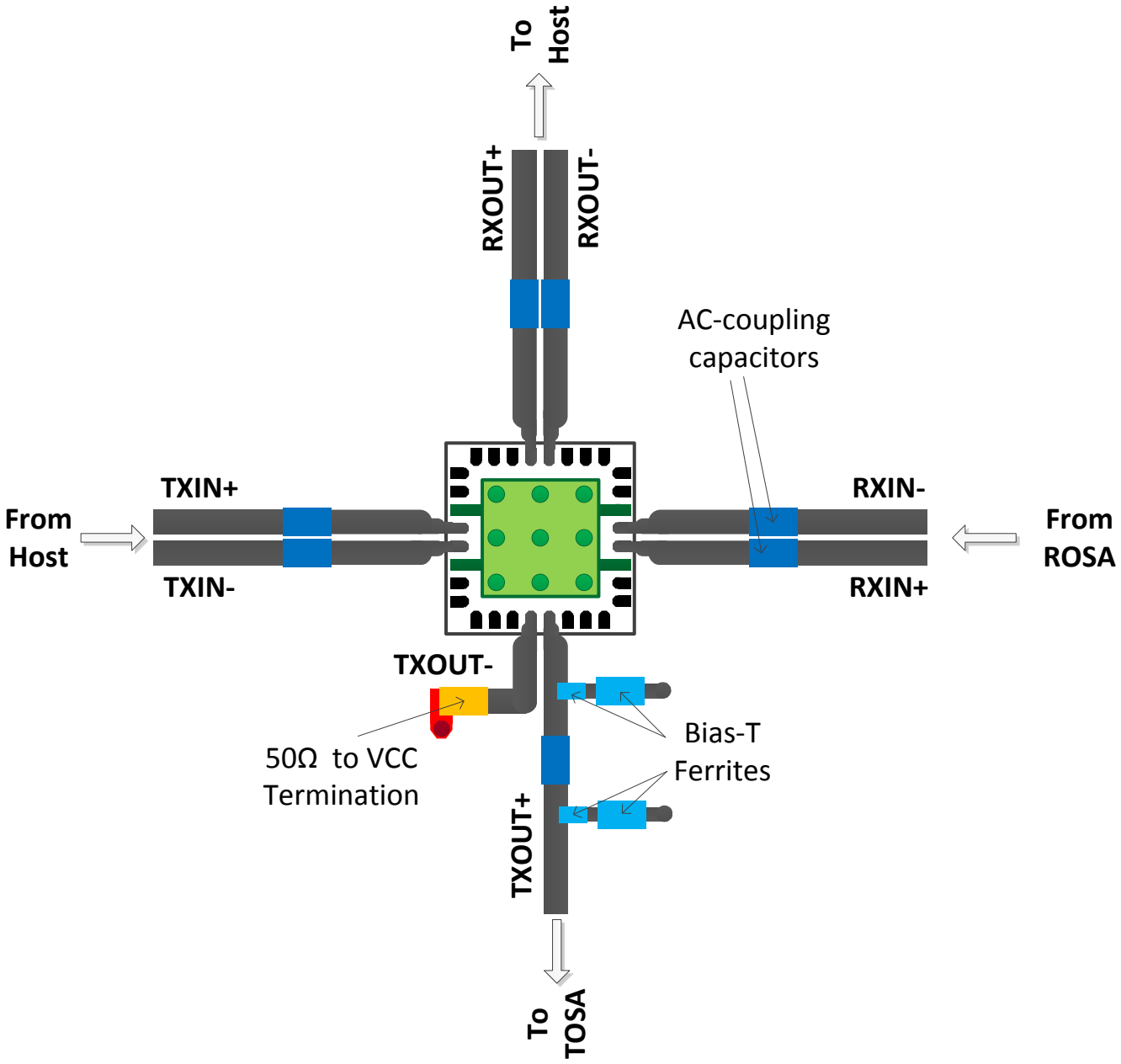


Figure 73. Board Layout

12 Device and Documentation Support

12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ONET1130ECRSMR	ACTIVE	VQFN	RSM	32	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 100	ONET 1130EC	Samples
ONET1130ECRSMT	ACTIVE	VQFN	RSM	32	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 100	ONET 1130EC	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

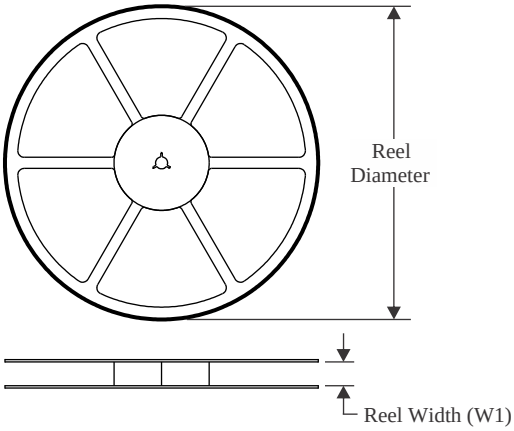
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

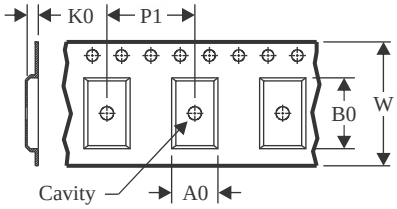
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

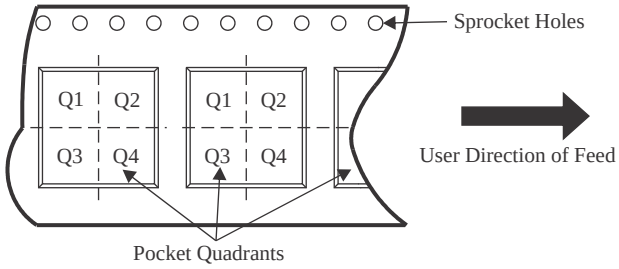


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

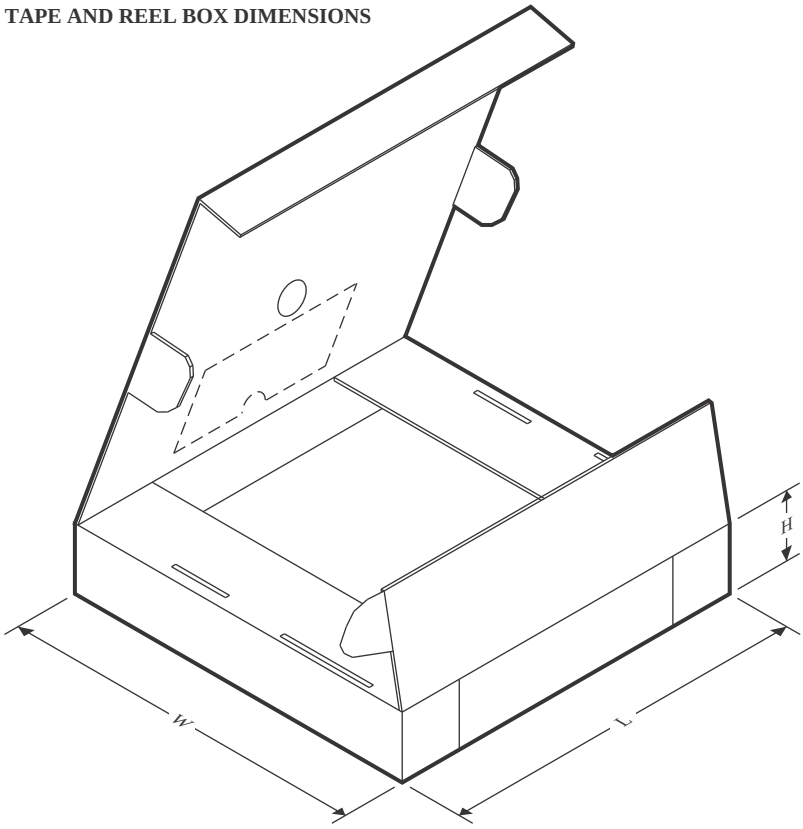
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ONET1130ECRSMT	VQFN	RSM	32	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ONET1130ECRSMT	VQFN	RSM	32	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

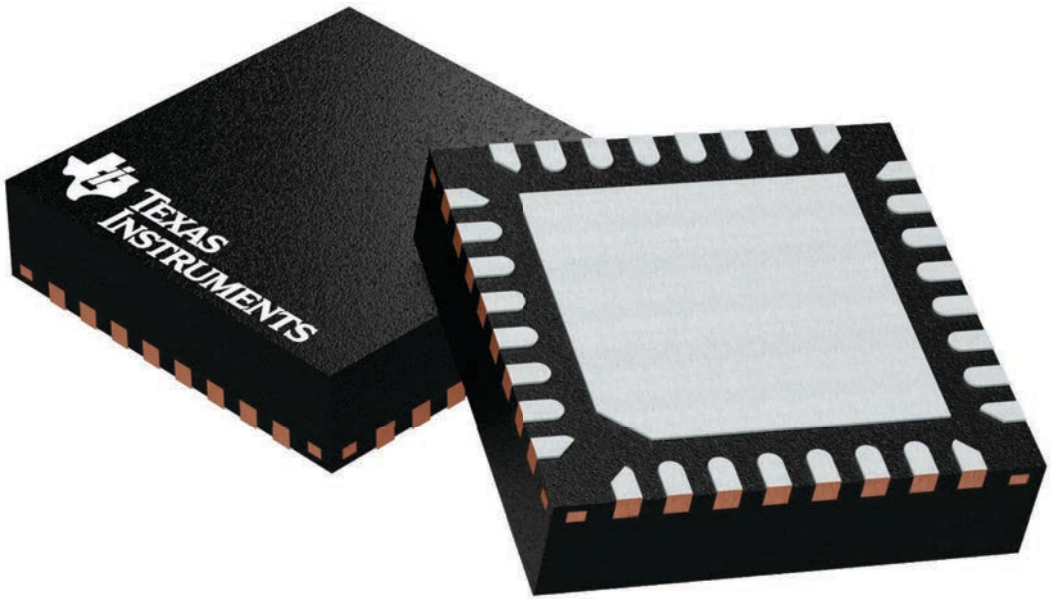
RSM 32

VQFN - 1 mm max height

4 x 4, 0.4 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



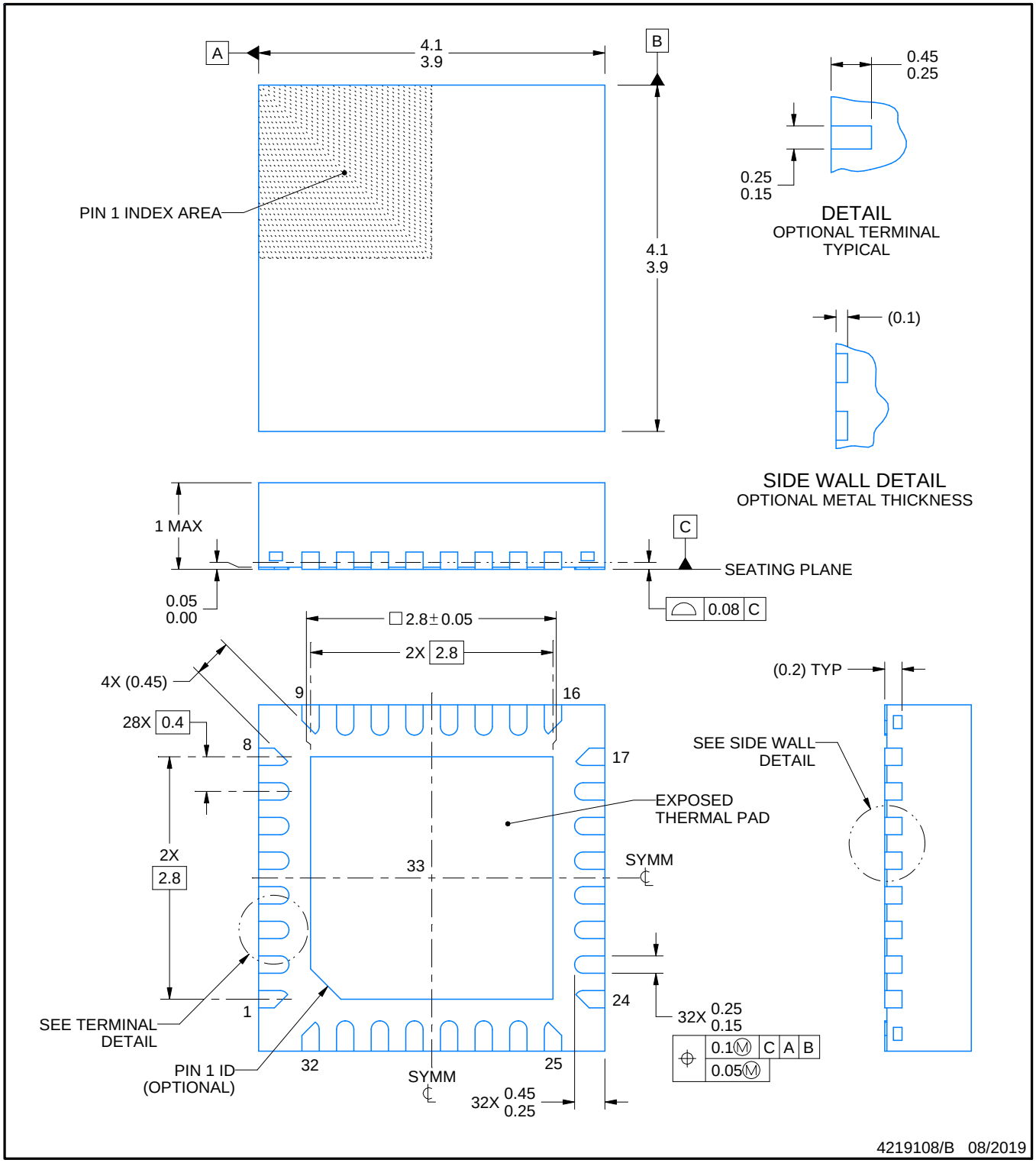
4224982/A

PACKAGE OUTLINE

RSM0032B

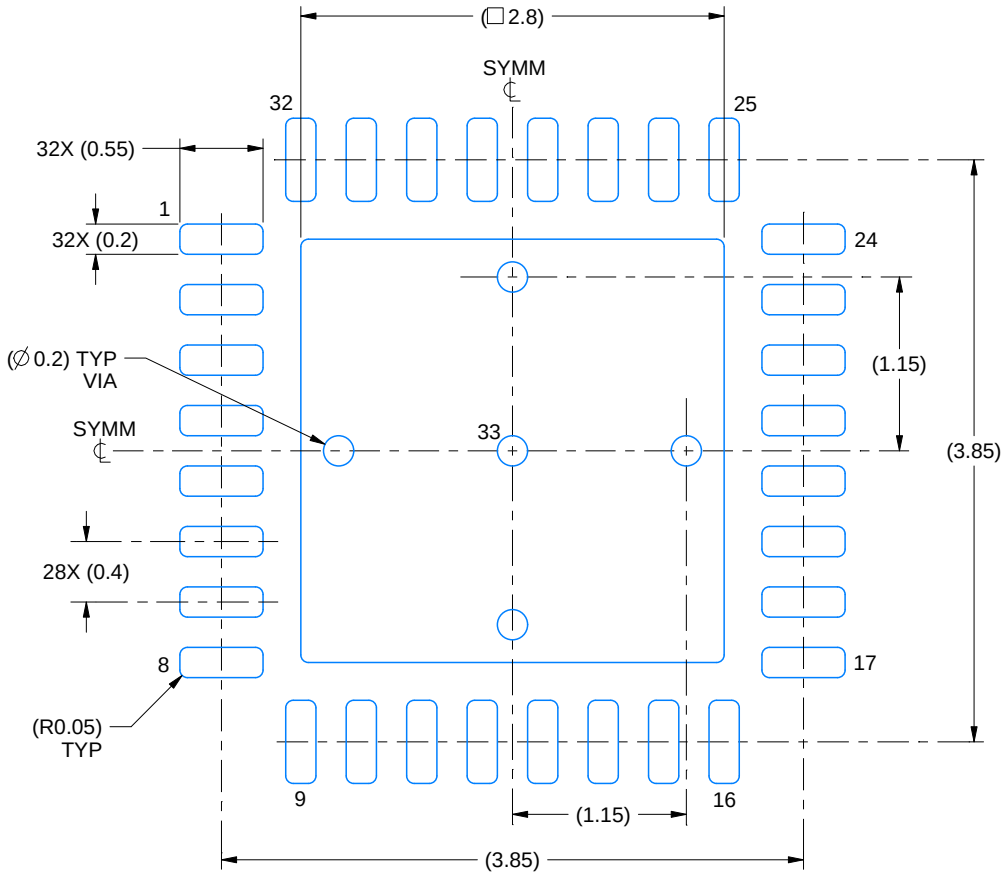
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

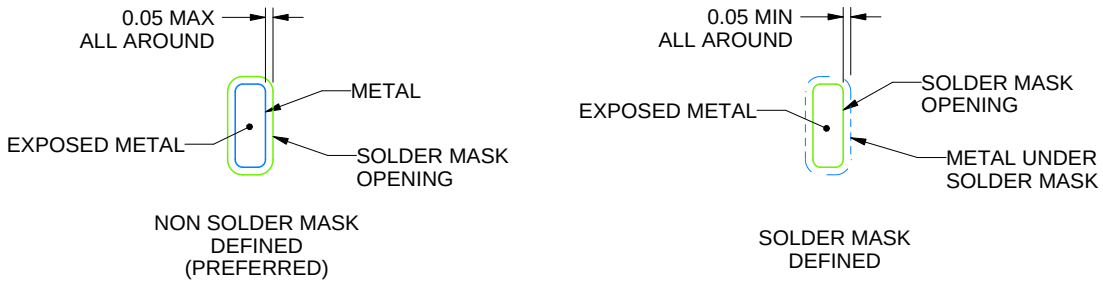


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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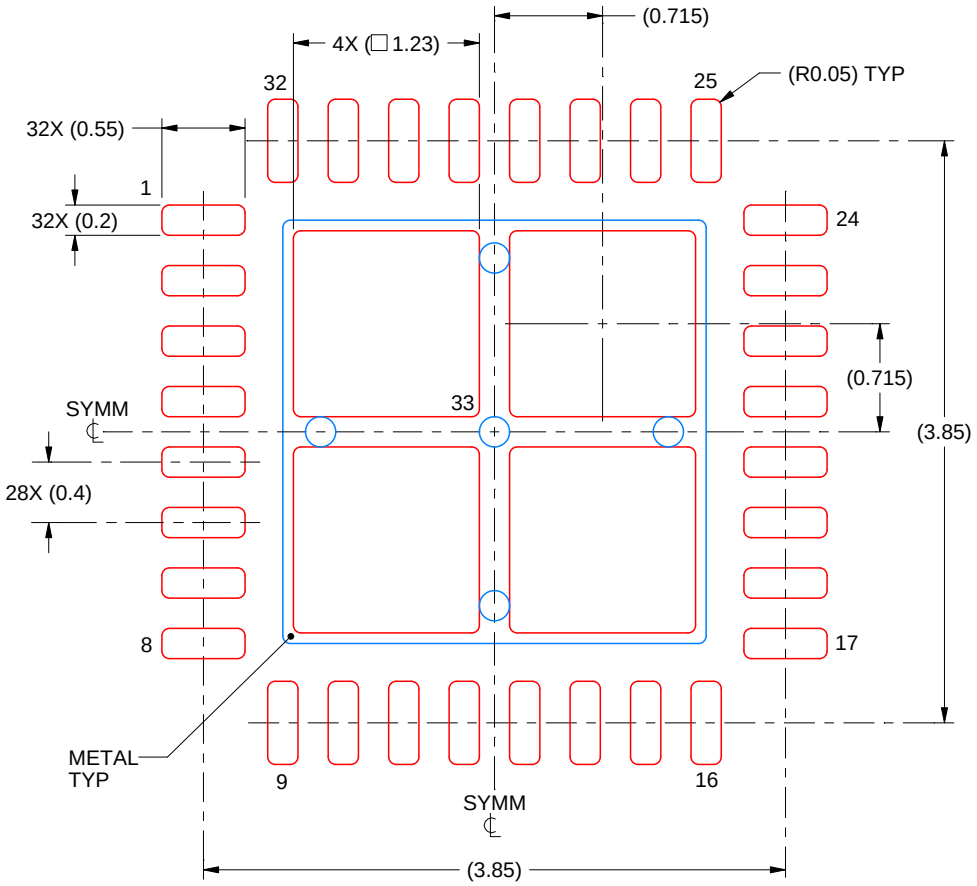
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 33:
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4219108/B 08/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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