DS160PT801 PCIe® 4.0, 16 Gbps, 8-Lane (16-Channel) Retimer

1 Features

- 8-lane (16-channel) protocol-aware PCI-express retimer supporting 16.0, 8.0, 5.0, and 2.5 GT/s interfaces
- Inter-chip communication (ICC) enable dual chip link width scaling to form 16-lane Gen-4 retimer
- Supports common clock, separate reference clock with no spread spectrum clocking (SSC), and separate reference clock with SSC
- Supports 2x4 bifurcation
- Adaptive receive CTLE and DFE supporting maximum PCIe Gen-4 channel loss
- Supports equalization training
- Low-latency architecture
- On-chip eye opening monitor (EOM) and PCIe receive margining capability
- Small 8.50-mm × 13.40-mm BGA package
- Flow-through pinout enables signal breakout in two signal layers
- Compatible with standard 1.00-mm BGA PCB manufacturing
- Dual power supply: 1.17 V and 1.8 V
- I2C configuration (up to 1 MHz) through the external EEPROM or I2C controller
- Industrial temperature range: −40°C to 85°C

2 Applications

- Rack server
- Microserver and tower server
- High performance computing
- Hardware accelerator

3 Description

The DS160PT801 is a high-performance eight-lane (16-channel) PCI-Express protocol-aware retimer supporting all standard PCIe data rates up to 16 GT/s. It is used to extend the reach and robustness of high-speed PCIe serial links, from chip-to-chip motherboard links to more complex multi-connector system topologies.

The DS160PT801 supports both common-clock and independent reference clock architectures, with and without spread-spectrum clocking. This allows for maximum flexibility in defining the system clock architecture.

The eight lanes in the DS160PT801 can be bifurcated into two x4 links to support different system topologies.

A compact yet easy-to-manufacture BGA package provides excellent thermal performance while enabling optimal placement in space-constrained applications like 1RU riser cards. This feature reduces overall solution size, PCB routing complexity, and BOM cost.

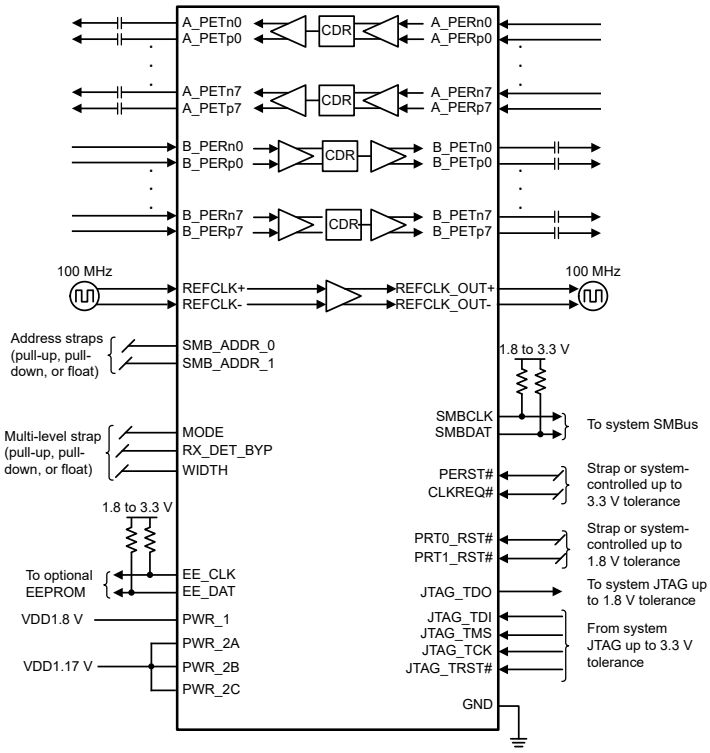
Diagnostic capabilities include in-band receiver margining, out-of-band non-destructive horizontal or vertical eye margin monitor, receiver loopback, encoding error detection, and on die temperature sensor. These features help gauge link margin and can be used to monitor system health over time.

The DS160PT801 is configurable through SMBus interface. The Initial configuration can be automatically loaded from external EEPROM.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DS160PT801	FCCSP (332)	8.50 mm × 13.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2020) to Revision A (June 2022)	Page
• Changed the status of the data sheet from: *Advanced Information* to: *Production Data*	1

5 Device Comparison

PART NUMBER	LINK WIDTH	PCIe GEN	DEVICE TYPE
DS160PT801	x8	4, 3, 2, 1	Retimer

6 Device and Documentation Support

6.1 Device Support

6.1.1 Development Support

- **IBIS-AMI model.** Simulate the DS160PT801's high-speed receiver and transmitter in tools which support IBIS-AMI simulations. Contact your local Texas Instruments sales representative for the latest status of available models.

6.1.2 12.1.2 Device Nomenclature

- **x2 –** Two-lane PCI-Express Link, also referred to as by-2.
- **x4 –** Four-lane PCI-Express Link, also referred to as by-4.
- **x8 –** Eight-lane PCI-Express Link, also referred to as by-8.
- **x16 –** Sixteen-lane PCI-Express Link, also referred to as by-16.
- **Bifurcation –** Dividing a by-M PCI-Express Link (for example, x8) into two or more separate by-N Links (for example, two x4), where N < M.
- **Stacking –** Combining multiple by-N devices (for example, two x8) to form a by-M interface (for example, x16), where M > N.

6.2 Documentation Support

6.2.1 Related Documentation

For related documentation, see the following:

- Texas Instrument, *DS160PT801 Evaluation Board* reference design

6.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

6.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
PCIe® is a registered trademark of PCI-SIG.
All trademarks are the property of their respective owners.

6.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

6.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS160PT801ACBR	ACTIVE	FCCSP	ACB	332	2000	RoHS & Green	Call TI | SNAGCU	Level-3-260C-168 HR	-40 to 85	D160PT801	Samples
DS160PT801ACBT	ACTIVE	FCCSP	ACB	332	250	RoHS & Green	Call TI | SNAGCU	Level-3-260C-168 HR	-40 to 85	D160PT801	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

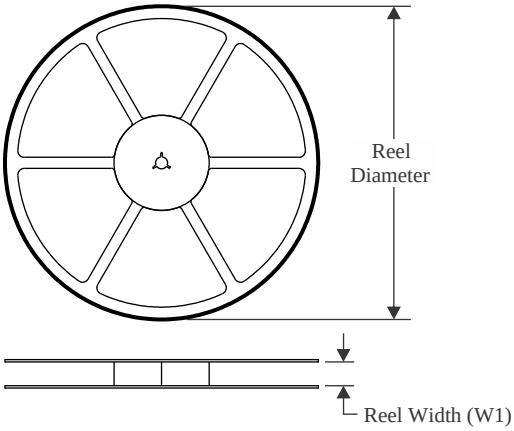
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

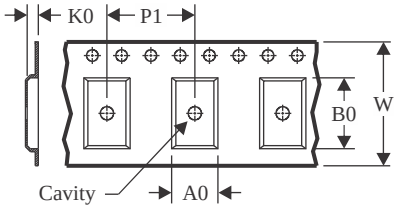
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

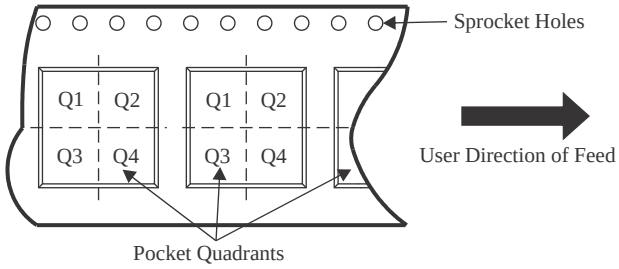


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

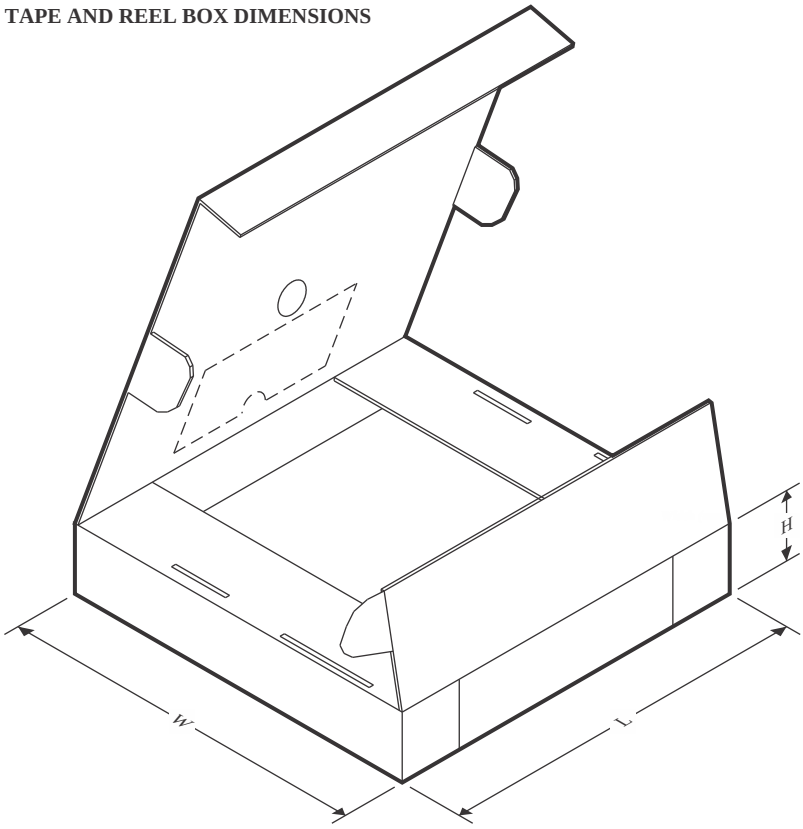
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS160PT801ACBT	FCCSP	ACB	332	250	330.0	24.4	9.3	14.3	1.3	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

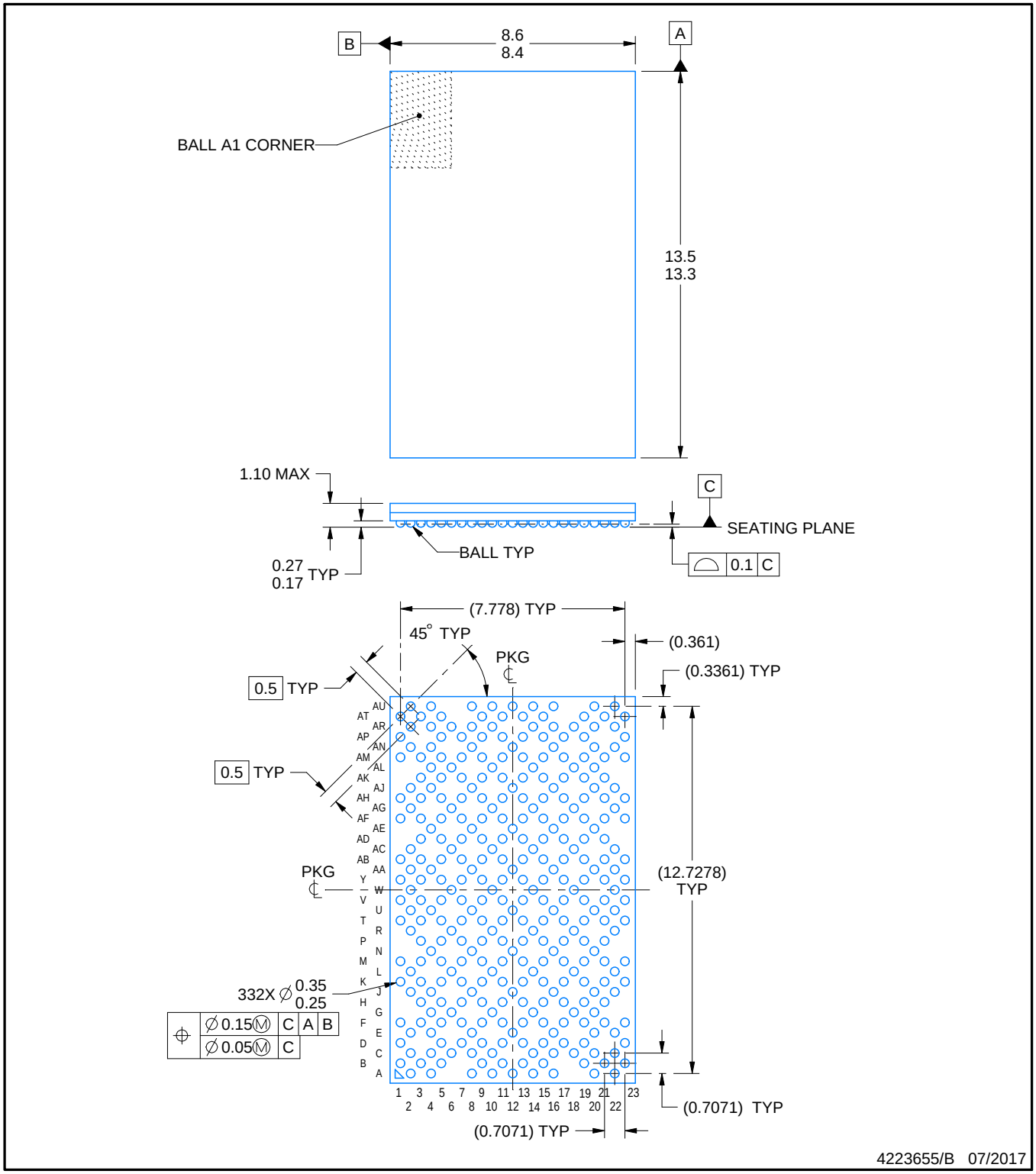
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS160PT801ACBT	FCCSP	ACB	332	250	336.6	336.6	41.3

PACKAGE OUTLINE

ACB0332A

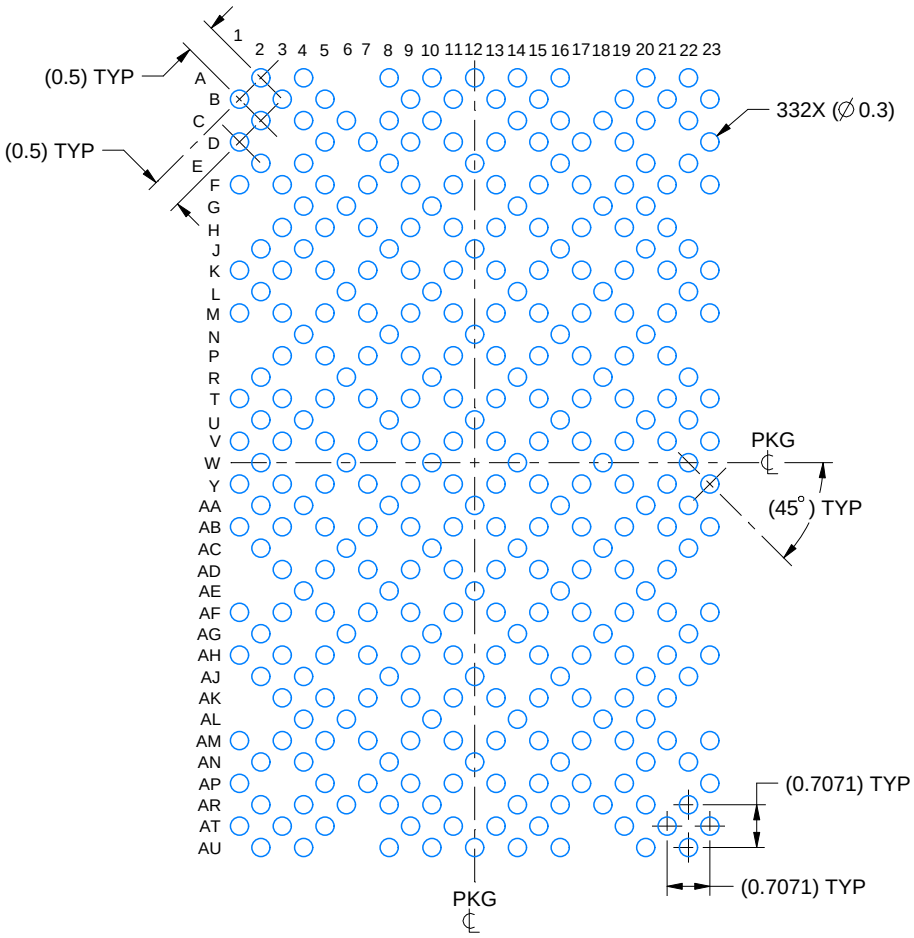
FCBGA - 1.10 mm max height

BALL GRID ARRAY

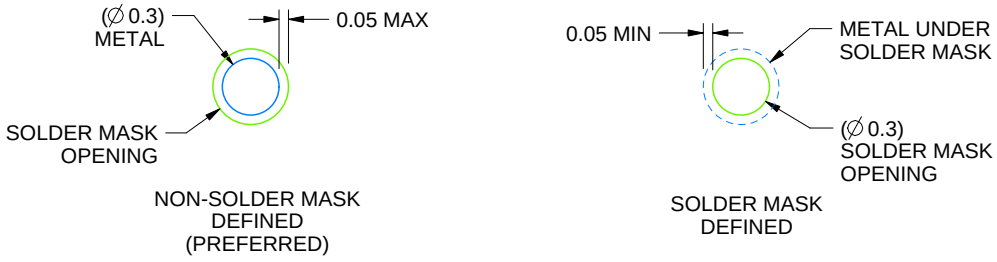


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS
NOT TO SCALE

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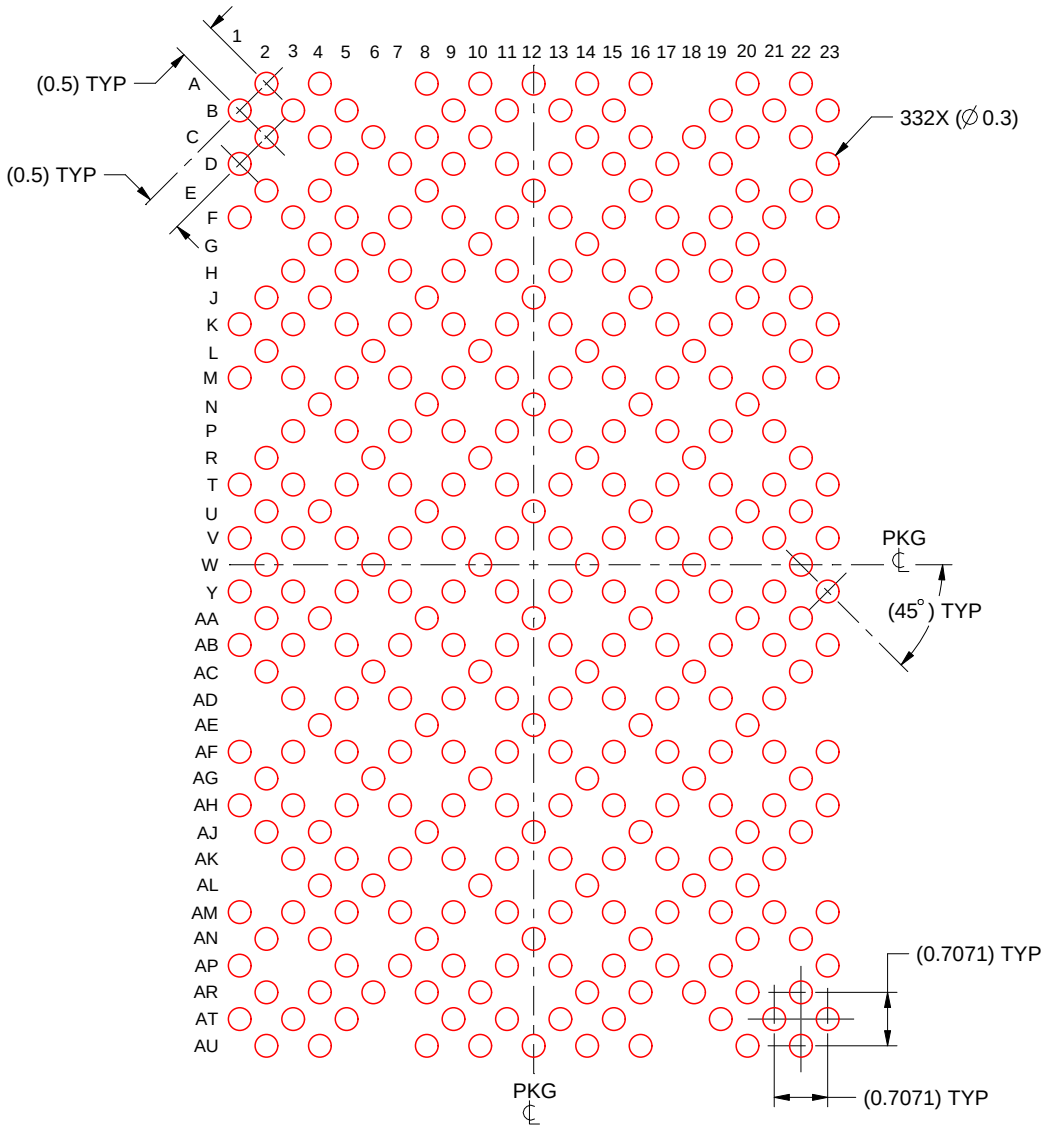
NOTES: (continued)

5. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SPRU811 (www.ti.com/lit/spru811).



SOLDER PASTE EXAMPLE
BASED ON 0.15 mm THICK STENCIL
SCALE:10X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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