LMK1D120x Low Additive Jitter LVDS Buffer

1 Features

- High-performance LVDS clock buffer family with 2 inputs and 4 (2:4) or 8 (2:8) outputs.
- Output frequency up to 2 GHz.
- Supply voltage: 1.71 V to 3.465 V
- Low additive jitter: < maximum 60 fs RMS in 12-kHz to 20-MHz at 156.25 MHz
  - Very low phase noise floor: –164 dBc/Hz (typical)
- Very low propagation delay: < 575 ps maximum
- Output skew: 20 ps maximum
- Universal inputs accept LVDS, LVPECL, LVCMOS, LP-HCSL, HCSL and CML inputs
- LVDS reference voltage, V_{AC_REF}, available for capacitive-coupled inputs
- Industrial temperature range: –40°C to 105°C
- Packages available:
  - LMK1D1204: 3-mm × 3-mm, 16-pin VQFN (RGT)
  - LMK1D1208: 5-mm × 5-mm, 28-pin VQFN (RHD)

2 Applications

- Telecommunications and networking
- Medical imaging
- Test and measurement
- Wireless infrastructure
- Pro audio, video and signage

3 Description

The LMK1D120x clock buffer distributes one of two selectable clock inputs (IN0 and IN1) to 4 or 8 pairs of differential LVDS clock outputs (OUT0 through OUT7) with minimum skew for clock distribution. The LMK1D12x family can accept two clock sources into an input multiplexer. The inputs can either be LVDS, LVPECL, LP-HCSL, HCSL, CML or LVCMOS.

The LMK1D12x is specifically designed for driving 50-Ω transmission lines. In case of driving the inputs in single-ended mode, the appropriate bias voltage as shown in Figure 8-6 must be applied to the unused negative input pin.

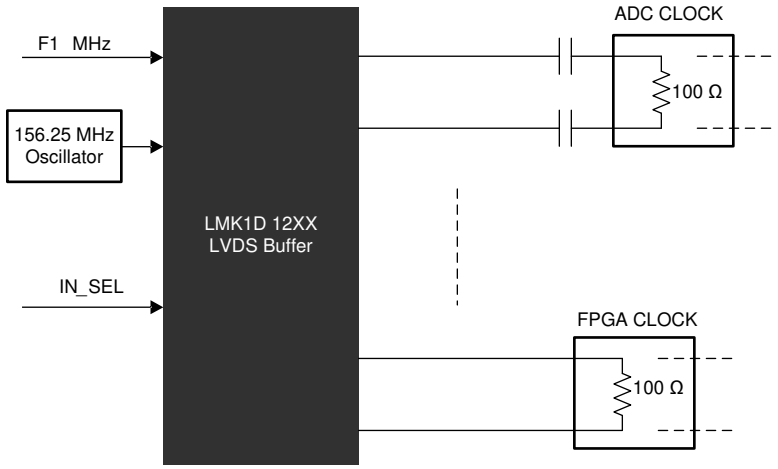
The IN_SEL pin selects the input which is routed to the outputs. If this pin is left open, it disables the outputs (logic low). The part supports a fail-safe function. The device further incorporates an input hysteresis which prevents random oscillation of the outputs in the absence of an input signal.

The device operates in 1.8-V or 2.5-V or 3.3-V supply environment and is characterized from –40°C to 105°C (ambient temperature). The LMK1D12x package variant is shown in the table below:

Device Information

PART NUMBER(1)	PACKAGE	BODY SIZE (NOM)
LMK1D1204	VQFN (16)	3.00 mm × 3.00 mm
LMK1D1208	VQFN (28)	5.00 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Application Example

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2020) to Revision A (August 2021)	Page
• First public release	1

5 Pin Configuration and Functions

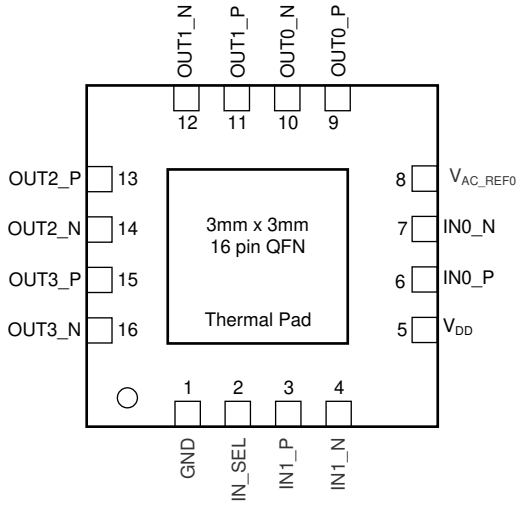


Figure 5-1. LMK1D1204: RGT Package 16-Pin VQFN Top View

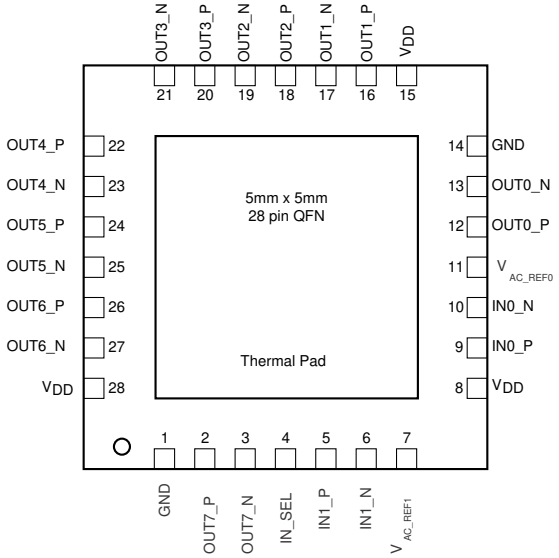


Figure 5-2. LMK1D1208: RHD Package 28-Pin VQFN Top View

Table 5-1. Pin Functions

PIN			TYPE[1]	DESCRIPTION
NAME	LMK1D1204	LMK1D1208		
DIFFERENTIAL/SINGLE-ENDED CLOCK INPUT				
IN0_P	6	9	I	Primary: Differential input pair or single-ended input
IN0_N	7	10		
IN1_P	3	5	I	Secondary: Differential input pair or single-ended input. Note that INP0, INN0 are used indistinguishably with IN0_P, IN0_N.
IN1_N	4	6		
INPUT SELECT				
IN_SEL	2	4	I	Input Selection with an internal 500-kΩ pullup and 320-kΩ pulldown resistor, selects input port; (See Table 8-1)
BIAS VOLTAGE OUTPUT				

Table 5-1. Pin Functions (continued)

PIN			TYPE(1)	DESCRIPTION
NAME	LMK1D1204	LMK1D1208		
V_{AC_REF0}	8	11	O	Bias voltage output for capacitive coupled inputs. If used, TI recommends using a 0.1-µF capacitor to GND on this pin.
V_{AC_REF1}	—	7		
DIFFERENTIAL CLOCK OUTPUT				
OUT0_P	9	12	O	Differential LVDS output pair number 0
OUT0_N	10	13		
OUT1_P	11	16	O	Differential LVDS output pair number 1
OUT1_N	12	17		
OUT2_P	13	18	O	Differential LVDS output pair number 2
OUT2_N	14	19		
OUT3_P	15	20	O	Differential LVDS output pair number 3
OUT3_N	16	21		
OUT4_P	—	22	O	Differential LVDS output pair number 4
OUT4_N		23		
OUT5_P	—	24	O	Differential LVDS output pair number 5
OUT5_N		25		
OUT6_P	—	26	O	Differential LVDS output pair number 6
OUT6_N		27		
OUT7_P	—	2	O	Differential LVDS output pair number 7
OUT7_N		3		
SUPPLY VOLTAGE				
V_{DD}	5	8	P	Device Power Supply (1.8V or 2.5V or 3.3V)
		15		
		28		
GROUND				
GND	1	1	G	Ground
	—	14		
MISC				
DAP	DAP	DAP	GND	Die Attach Pad. Connect to the PCB ground plane for heat dissipation.
NC	—	—	NC	No Connection

(1) G = Ground, I = Input, O = Output, P = Power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{DD}	Supply voltage	–0.3	3.6	V
V_{IN}	Input voltage	–0.3	3.6	V
V_O	Output voltage	–0.3	V_{DD} + 0.3	V
I_{IN}	Input current	–20	20	mA
I_O	Continuous output current	–50	50	mA
T_J	Junction temperature		135	°C
T_{stg}	Storage temperature (2)	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Device unpowered

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±3000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{DD}	Core supply voltage	3.3-V supply	3.135	3.3	3.465	V
		2.5-V supply	2.375	2.5	2.625	
		1.8-V supply	1.71	1.8	1.89	
Supply Ramp	Supply voltage ramp	Requires monotonic ramp (10-90% of V_{DD})	0.1		20	ms
T_A	Operating free-air temperature		–40		105	°C
T_J	Operating junction temperature		–40		135	°C

6.4 Thermal Information

THERMAL METRIC(1)		LMK1D1204 VQFN 16 PINS	LMK1D1208 VQFN 28 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	48.7	38.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.4	32.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	23.6	18.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.6	1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	23.6	18.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	8.6	8.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

VDD = 1.8 V ± 5 %, –40 °C ≤T_A ≤ 105 °C. Typical values are at VDD = 1.8 V, 25 °C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY CHARACTERISTICS						
IDD_{STAT}	LMK1D1204	All-outputs enabled and unterminated, f = 0 Hz		50		mA
IDD_{STAT}	LMK1D1208	All-outputs enabled and unterminated, f = 0 Hz		55		mA
IDD_{100M}	LMK1D1204	All-outputs enabled, R_L = 100 Ω, f =100 MHz		60	72	mA
IDD_{100M}	LMK1D1208	All-outputs enabled, R_L = 100 Ω, f =100 MHz		78	95	mA
IN_SEL CONTROL INPUT CHARACTERISTICS (Applies to V_{DD} = 1.8 V ± 5%, 2.5 V ± 5% and 3.3 V ± 5%)						
Vd_{I3}	3-state input	Open		0.4*V_{CC}		V
V_{IH}	Input high voltage	Minimun input voltage for a logical "1" state in table 1	0.7*V_{CC}		V_{CC} + 0.3	V
V_{IL}	Input low voltage	Maximum input voltage for a logical "0" state in table 1	–0.3		0.3*V_{CC}	V
I_{IH}	Input high current	V_{DD} can be 1.8V/2.5V/3.3V with V_{IH} = V_{DD}			30	uA
I_{IL}	Input low current	V_{DD} can be 1.8V/2.5V/3.3V with V_{IH} = V_{DD}	–30			uA
$R_{pull-up(IN\_SEL)}$	Input pullup resistor			500		kΩ
$R_{pull-down(IN\_SEL)}$	Input pulldown resistor			320		kΩ
SINGLE-ENDED LVCMOS/LVTTL CLOCK INPUT (Applies to V_{DD} = 1.8 V ± 5%, 2.5 V ± 5% and 3.3 V ± 5%)						
f_{IN}	Input frequency	Clock input	DC		250	MHz
V_{IN_S-E}	Single-ended Input Voltage Swing	Assumes a square wave input with two levels	0.4		3.465	V
dVIN/dt	Input Slew Rate (20% to 80% of the amplitude)		0.05			V/ns
I_{IH}	Input high current	V_{DD} = 3.465 V, V_{IH} = 3.465 V			50	uA
I_{IL}	Input low current	V_{DD} = 3.465 V, V_{IL} = 0 V	-30			uA
C_{IN_SE}	Input capacitance	at 25°C		3.5		pF
DIFFERENTIAL CLOCK INPUT (Applies to V_{DD} = 1.8 V ± 5%, 2.5 V ± 5% and 3.3 V ± 5%)						
f_{IN}	Input frequency	Clock input			2	GHz

VDD = 1.8 V ± 5 %, –40 °C ≤T_A ≤ 105 °C. Typical values are at VDD = 1.8 V, 25 °C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IN,DIFF(p-p)}$	Differential input voltage peak-to-peak {2*(V_{INP}-V_{INN})}	V_{ICM} = 1 V (V_{DD} = 1.8 V)	0.3		2.4	V_{PP}
		V_{ICM} = 1.25 V (V_{DD} = 2.5 V/3.3 V)	0.3		2.4	
V_{ICM}	Input common mode voltage	$V_{IN,DIFF(P-P)}$ > 0.4 V (V_{DD} = 1.8 V/2.5/3.3 V)	0.25		2.3	V
I_{IH}	Input high current	V_{DD} = 3.465 V, V_{INP} = 2.4 V, V_{INN} = 1.2 V			30	uA
I_{IL}	Input low current	V_{DD} = 3.465 V, V_{INP} = 0 V, V_{INN} = 1.2 V	–30			uA
C_{IN_S-E}	Input capacitance (Single-ended)	at 25°C		3.5		pF
LVDS DC OUTPUT CHARACTERISTICS						
|VOD|	Differential output voltage magnitude | V_{OUTP} - V_{OUTN}|	$V_{IN,DIFF(P-P)}$ = 0.3 V, R_{LOAD} = 100 Ω	250	350	450	mV
ΔVOD	Change in differential output voltage magnitude. Per output, defined as the difference between VOD in logic hi/lo states.	$V_{IN,DIFF(P-P)}$ = 0.3 V, R_{LOAD} = 100 Ω	–15		15	mV
$V_{OC(SS)}$	Steady-state common mode output voltage	$V_{IN,DIFF(P-P)}$ = 0.3 V, R_{LOAD} = 100 Ω (V_{DD} = 1.8 V)	1		1.2	V
		$V_{IN,DIFF(P-P)}$ = 0.3 V, R_{LOAD} = 100 Ω (V_{DD} = 2.5 V/3.3 V)	1.1		1.375	
$\Delta_{VOC(SS)}$	Change in steady-state common mode output voltage. Per output, defined as the difference in VOC in logic hi/lo states.	$V_{IN,DIFF(P-P)}$ = 0.3 V, R_{LOAD} = 100 Ω	–15		15	mV
LVDS AC OUTPUT CHARACTERISTICS						
V_{ring}	Output overshoot and undershoot	$V_{IN,DIFF(P-P)}$ = 0.3 V, R_{LOAD} = 100 Ω, f_{OUT} = 491.52 MHz	–0.1		0.1	V_{OD}
V_{OS}	Output AC common mode	$V_{IN,DIFF(P-P)}$ = 0.3 V, R_{LOAD} = 100 Ω		50	100	mV_{pp}
I_{OS}	Short-circuit output current (differential)	V_{OUTP} = V_{OUTN}	–12		12	mA
$I_{OS(cm)}$	Short-circuit output current (common-mode)	V_{OUTP} = V_{OUTN} = 0	–24		24	mA
t_{PD}	Propagation delay	$V_{IN,DIFF(P-P)}$ = 0.3 V, R_{LOAD} = 100 Ω (1)	0.3		0.575	ns
$t_{SK,\ O}$	Output skew	skew between outputs with the same load conditions (4 and 8 channel) (2)			20	ps
$t_{SK,\ PP}$	Part-to-part skew	Skew between outputs on different parts subjected to the same operating conditions with the same input and output loading.			250	ps
$t_{SK,\ P}$	Pulse skew	50% duty cycle input, crossing point-to-crossing-point distortion (3)	–20		20	ps
$t_{RJIT(ADD)}$	Random additive Jitter (rms)	f_{IN} = 156.25 MHz with 50% duty-cycle, Input slew rate = 1.5V/ns, Integration range = 12kHz - 20MHz, with output load R_{LOAD} = 100 Ω		50	60	fs, RMS
Phase noise	Phase Noise for a carrier frequency of 156.25 MHz with 50% duty-cycle, Input slew rate = 1.5V/ns with output load R_{LOAD} = 100 Ω	PN_{1kHz}		–143		dBc/Hz
		PN_{10kHz}		-152		
		PN_{100kHz}		-157		
		PN_{1MHz}		-160		
		PN_{floor}		–164		

VDD = 1.8 V ± 5 %, –40 °C ≤T_A ≤ 105 °C. Typical values are at VDD = 1.8 V, 25 °C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
MUX_{ISO}	Mux Isolation	f_{IN} = 156.25 MHz. The difference in power level @ f_{IN} when the selected clock is active and the unselected clock is static versus when the selected clock is inactive and the unselected clock is active.		80		dB
ODC	Output duty cycle	With 50% duty cycle input	45		55	%
t_R/t_F	Output rise and fall time	20% to 80% with R_{LOAD} = 100 Ω			300	ps
V_{AC_REF}	Reference output voltage	VDD = 2.5 V, I_{LOAD} = 100 uA	0.9	1.25	1.375	V
POWER SUPPLY NOISE REJECTION (PSNR) V_{DD} = 2.5 V/ 3.3 V						
PSNR	Power Supply Noise Rejection ($f_{carrier}$ = 156.25 MHz)	10 kHz, 100 mVpp ripple injected on V_{DD}		–70		dBc
		1 MHz, 100 mVpp ripple injected on V_{DD}		–50		

(1) Measured between single-ended/differential input crossing point to the differential output crossing point.
(2) For the dual bank devices, the inputs are phase aligned and have 50% duty cycle.
(3) Defined as the magnitude of the time difference between the high-to-low and low-to-high propagation delay times at an output.

6.6 Typical Characteristics

The Figure 6-1 captures the variation of the LMK1D1208 current consumption with input frequency and supply voltage. The LMK1D1204 follows a similar trend. Figure 6-2 shows the variation of the differential output voltage (VOD) swept across frequency. This result is applicable to LMK1D1204 as well.

It is important to note that Figure 6-1 and Figure 6-2 serve as a guidance to the users on what to expect for the range of operating frequency supported by LMK1D120x. It is crucial to note that these graphs were plotted for a limited number of frequencies and load conditions which may not represent the customer system.

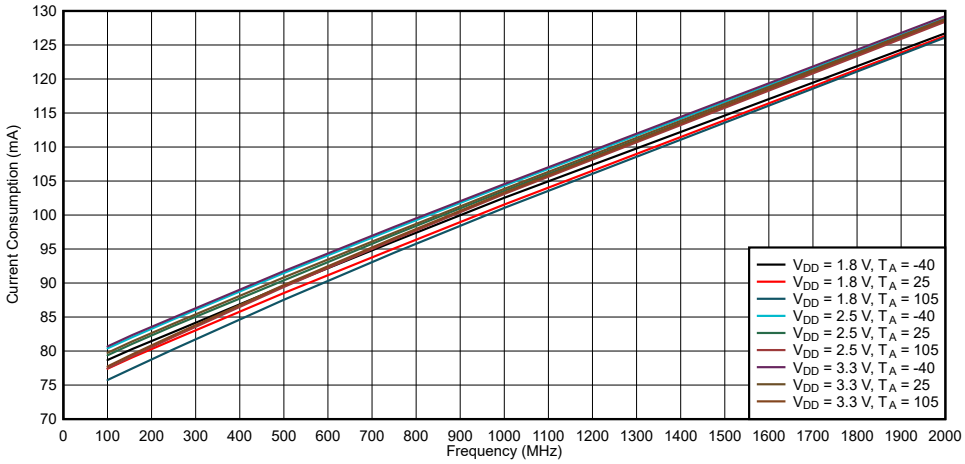


Figure 6-1. LMK1D1208 Current Consumption vs. Frequency

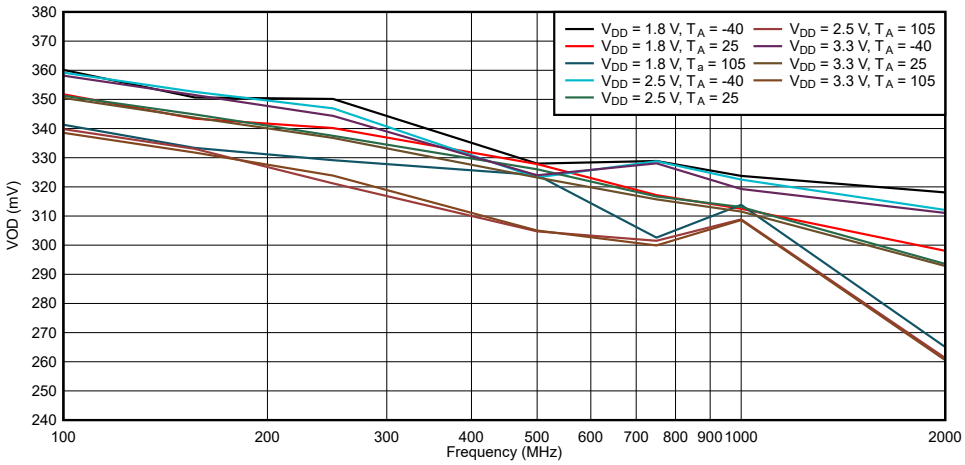


Figure 6-2. LMK1D1208 VOD vs. Frequency

7 Parameter Measurement Information

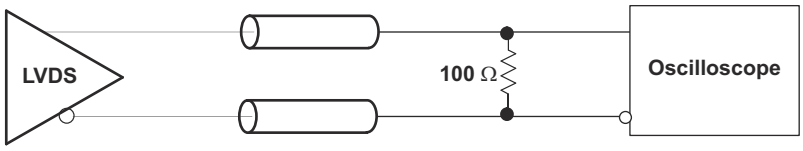


Figure 7-1. LVDS Output DC Configuration During Device Test

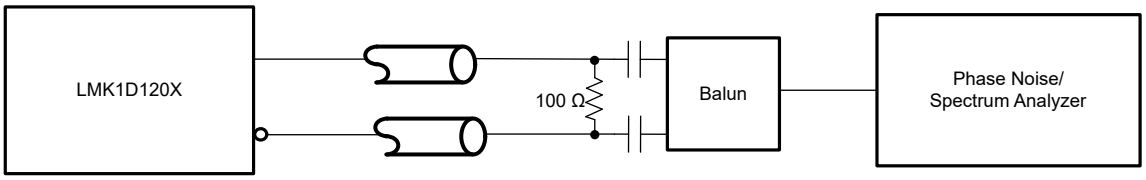


Figure 7-2. LVDS Output AC Configuration During Device Test

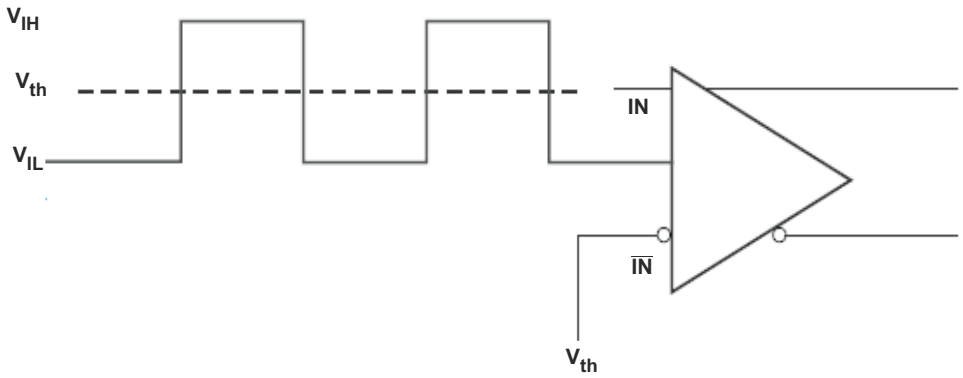


Figure 7-3. DC-Coupled LVCMOS Input During Device Test

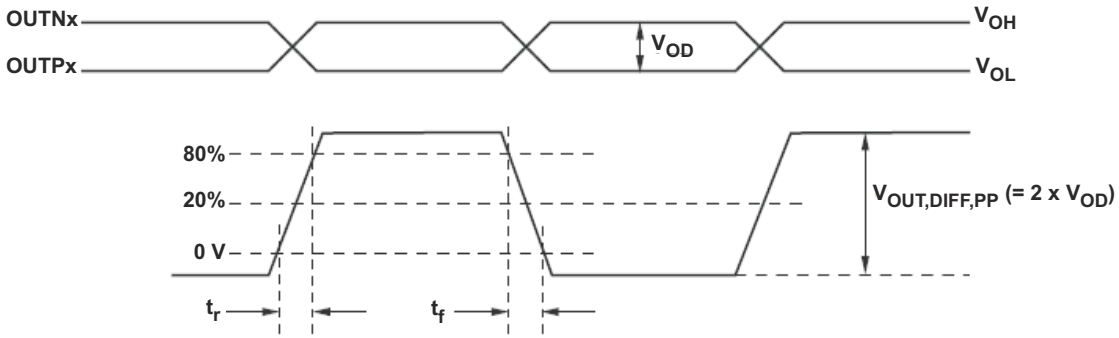
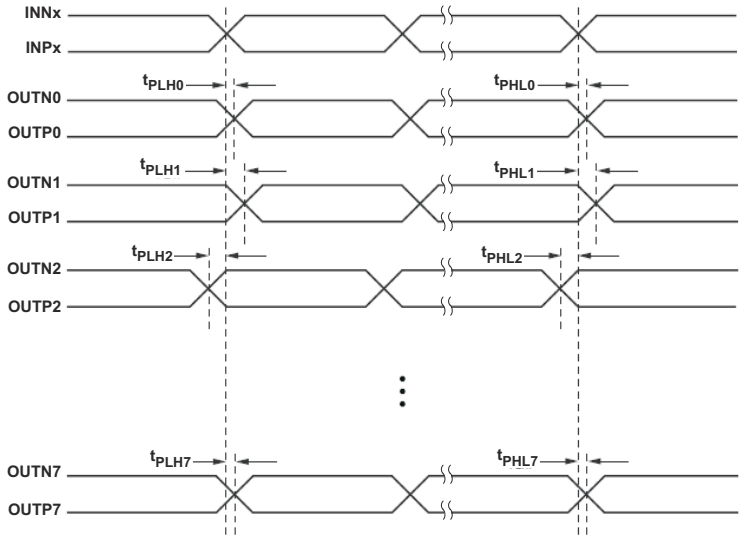


Figure 7-4. Output Voltage and Rise/Fall Time



A. Output skew is calculated as the greater of the following: the difference between the fastest and the slowest t_{PLHn} or the difference between the fastest and the slowest t_{PHLn} (n = 0, 1, 2, ..7)

B. Part to part skew is calculated as the greater of the following: the difference between the fastest and the slowest t_{PLHn} or the difference between the fastest and the slowest t_{PHLn} across multiple devices (n = 0, 1, 2, ..7)

Figure 7-5. Output Skew and Part-to-Part Skew

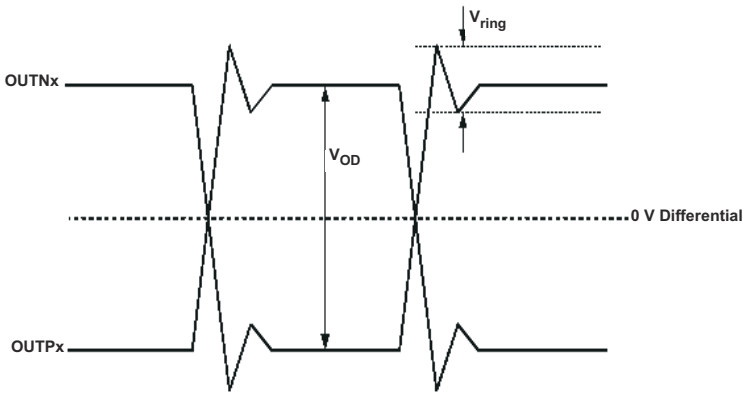


Figure 7-6. Output Overshoot and Undershoot

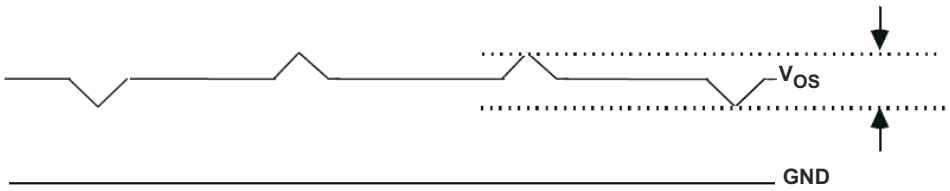


Figure 7-7. Output AC Common Mode

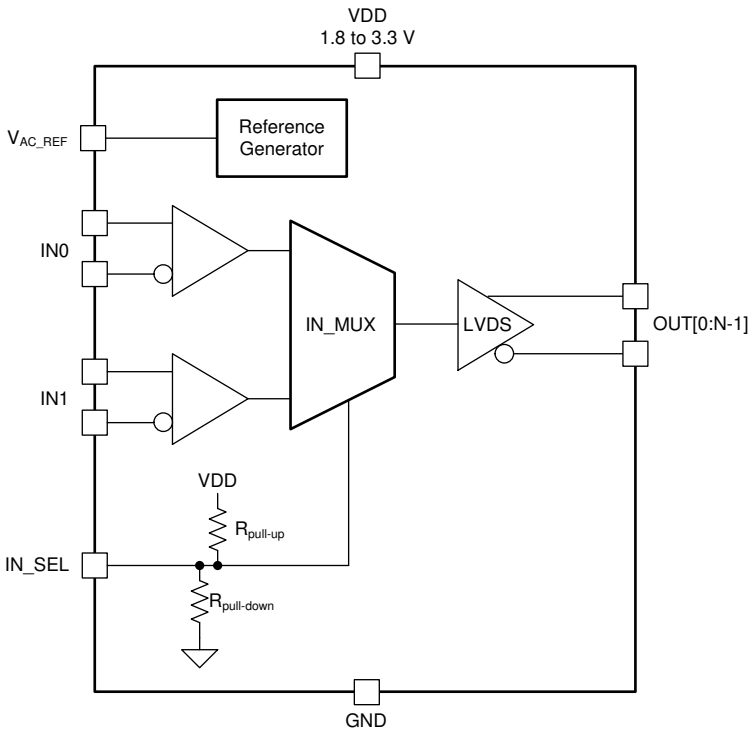
8 Detailed Description

8.1 Overview

The LMK1D120x LVDS drivers use CMOS transistors to control the output current. Therefore, proper biasing and termination are required to ensure correct operation of the device and to maximize signal integrity.

The proper LVDS termination for signal integrity over two 50-Ω lines is 100 Ω between the outputs on the receiver end. Either DC-coupled termination or AC-coupled termination can be used for LVDS outputs. TI recommends placing a termination resistor close to the receiver. If the receiver is internally biased to a voltage different than the output common-mode voltage of the LMK1D12XX, AC-coupling must be used. If the LVDS receiver has internal 100-Ω termination, external termination must be omitted.

8.2 Functional Block Diagram



8.3 Feature Description

The LMK1D120x is a low additive jitter LVDS fan-out buffer that can generate up to eight copies of two selectable LVPECL, LVDS, LP-HCSL, HCSL or LVCMOS inputs. The LMK1D120x can accept reference clock frequencies up to 2 GHz while providing low output skew.

8.3.1 Fail-Safe Input and Hysteresis

The LMK1D120x family of devices is designed to support fail-safe input operation feature. This feature allows the user to drive the device inputs before V_{DD} is applied without damaging the device. Refer to *Specifications* for more information on the maximum input supported by the device. User should note that incorporating the fail-safe inputs also results in a slight increase in clock input pin capacitance.

The device also incorporates an input hysteresis which prevents random oscillation in absence of an input signal. Furthermore, this feature allows the input pins to be left open.

8.3.2 Input Mux

The LMK1D120x family of devices has a 2:1 input mux. This feature allows the user to select between the two clock inputs (using the IN_SEL pin) to the device and fan it out to the outputs. More information on the input selection is provided in the next section.

8.4 Device Functional Modes

The two inputs of the LMK1D120x are internally muxed together and can be selected through the control pin (see Table 8-1). Unused input can be left floating thus reducing the need for additional components. Both AC- and DC-coupling schemes can be used with the LMK1D120x to provide greater system flexibility.

Table 8-1. Input Selection Table

IN_SEL	ACTIVE CLOCK INPUT
0	IN0_P, IN0_N
1	IN1_P, IN1_N
Open	None (1)

(1) The input buffers are disabled and the outputs are static logic low.

8.4.1 LVDS Output Termination

TI recommends unused outputs to be terminated differentially with a 100-Ω resistor for optimum performance, although unterminated outputs are also okay but will result in slight degradation in performance (Output AC common-mode V_{OS}) in the outputs being used.

The LMK1D120x can be connected to LVDS receiver inputs with DC- and AC-coupling as shown in Figure 8-1 and Figure 8-2 (respectively).

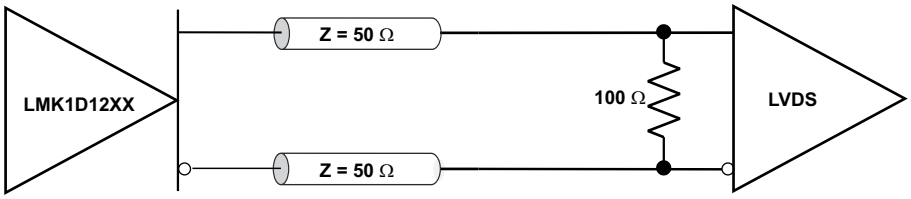


Figure 8-1. Output DC Termination

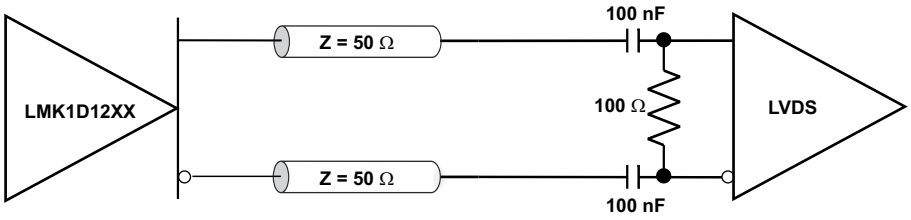


Figure 8-2. Output AC Termination (With the Receiver Internally Biased)

8.4.2 Input Termination

The LMK1D120x input stage is designed with flexibility in mind to allow the user to drive the device with a wide variety of signal types. This device can be interfaced with LVDS, LVPECL, LP-HCSL, HCSL, CML or LVCMOS drivers. Please refer to *Electrical Characteristics* for more details.

LVDS drivers can be connected to LMK1D120x inputs with DC- and AC-coupling as shown Figure 8-3 and Figure 8-4 (respectively).

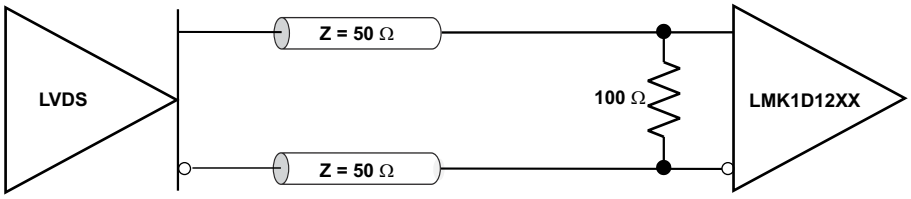


Figure 8-3. LVDS Clock Driver Connected to LMK1D120x Input (DC-Coupled)

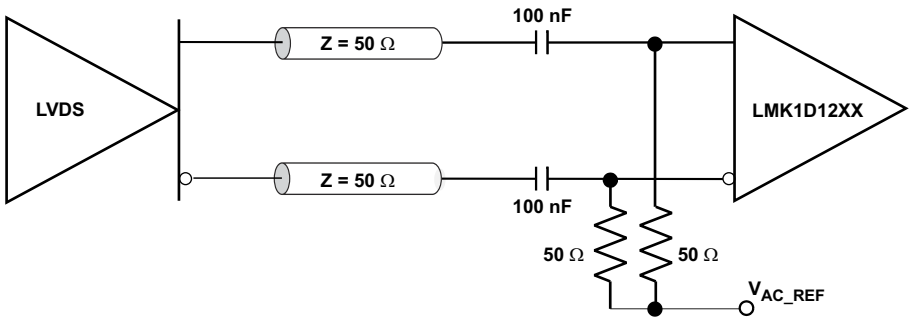


Figure 8-4. LVDS Clock Driver Connected to LMK1D120x Input (AC-Coupled)

Figure 8-5 shows how to connect LVPECL inputs to the LMK1D120x. The series resistors are required to reduce the LVPECL signal swing if the signal swing is >1.6 V_{PP}.

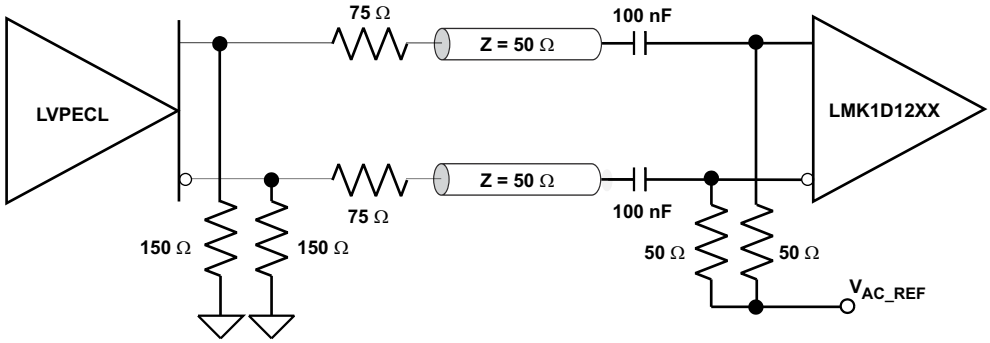


Figure 8-5. LVPECL Clock Driver Connected to LMK1D120x Input

Figure 8-6 illustrates how to couple a LVCMOS clock input to the LMK1D120x directly.

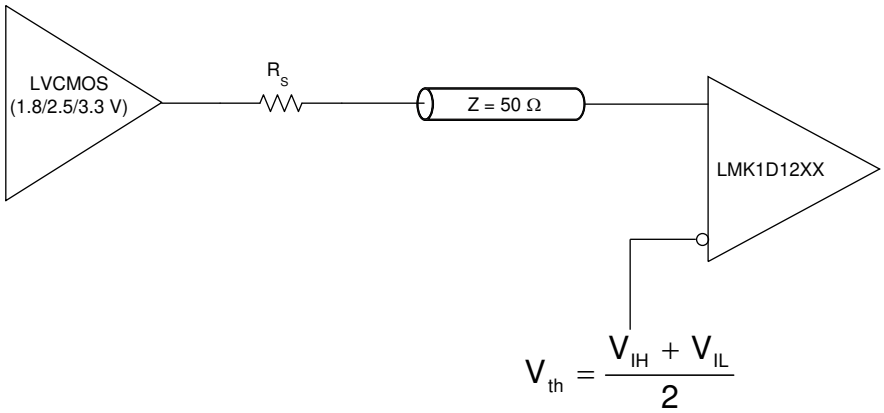


Figure 8-6. 1.8-V/2.5-V/3.3-V LVCMOS Clock Driver Connected to LMK1D120x Input

For unused input, TI recommends grounding both input pins (INP, INN) using 1-kΩ resistors.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The LMK1D120x is a low additive jitter universal to LVDS fan-out buffer with 2 selectable inputs. The small package, low output skew, and low additive jitter make for a flexible device in demanding applications.

9.2 Typical Application

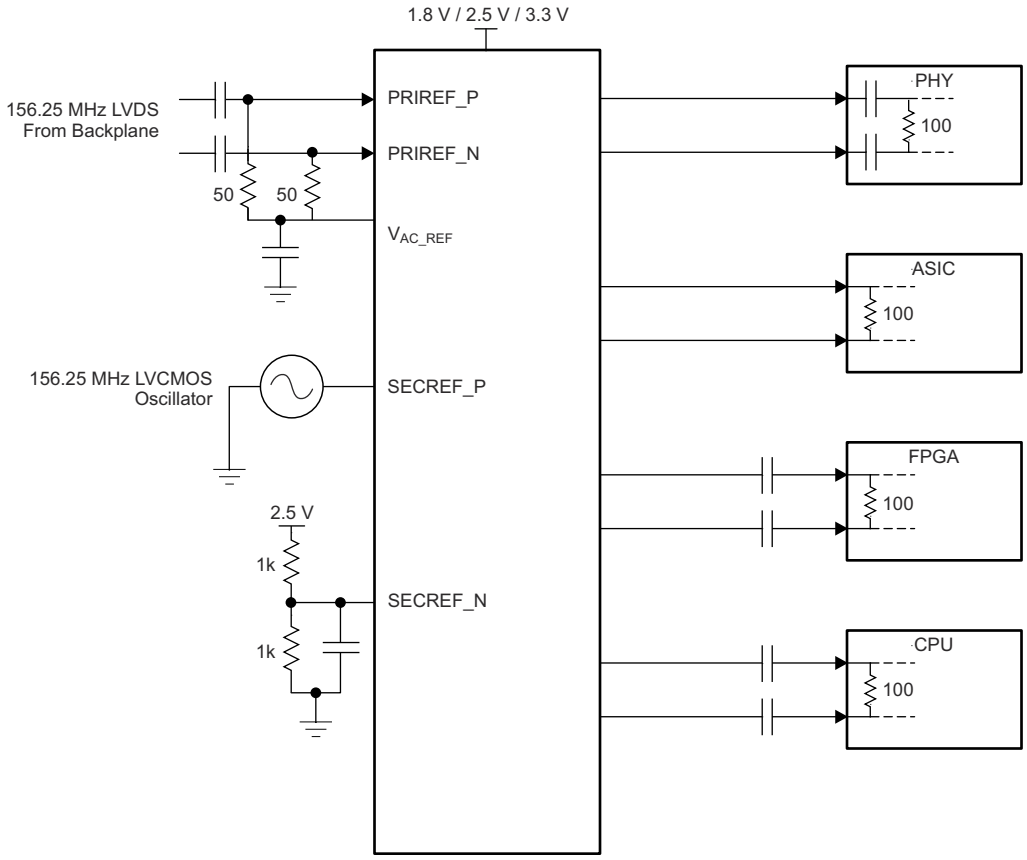


Figure 9-1. Fan-Out Buffer for Line Card Application

9.2.1 Design Requirements

The LMK1D120x shown in Figure 9-1 is configured to select two inputs: a 156.25-MHz LVDS clock from the backplane, or a secondary 156.25-MHz LVCMOS 2.5-V oscillator. The LVDS clock is AC-coupled and biased using the integrated reference voltage generator. A resistor divider is used to set the threshold voltage correctly for the LVCMOS clock. 0.1-µF capacitors are used to reduce noise on both V_{AC_REF} and SECREF_N. Either input signal can be then fanned out to desired devices, as shown. The configuration example is driving 4 LVDS receivers in a line card application with the following properties:

- The PHY device is capable of DC-coupling with an LVDS driver such as the LMK1D120x. This PHY device features internal termination so no additional components are required for proper operation.
- The ASIC LVDS receiver features internal termination and operates at the same common-mode voltage as the LMK1D120x. Again, no additional components are required.
- The FPGA requires external AC-coupling, but has internal termination. 0.1-µF capacitors are placed to provide AC-coupling. Similarly, the CPU is internally terminated, and requires only external AC-coupling capacitors.
- Unused outputs of the LMK1D device are terminated differentially with a 100-Ω resistor for optimum performance.

9.2.2 Detailed Design Procedure

See *Input Termination* for proper input terminations, dependent on single-ended or differential inputs.

See *LVDS Output Termination* for output termination schemes depending on the receiver application.

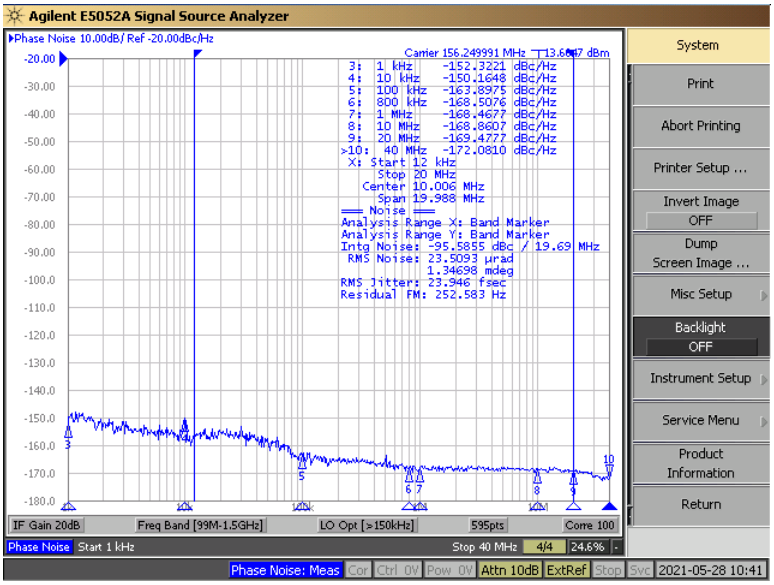
TI recommends unused outputs to be terminated differentially with a 100-Ω resistor for optimum performance, although unterminated outputs are also okay but will result in slight degradation in performance (Output AC common-mode V_{OS}) in the outputs being used.

In this example, the PHY, ASIC, and FPGA or CPU require different schemes. Power-supply filtering and bypassing is critical for low-noise applications.

See *Power Supply Recommendations* for recommended filtering techniques. A reference layout is provided in *Low-Additive Jitter, Four LVDS Outputs Clock Buffer Evaluation Board* (SCAU043).

9.2.3 Application Curves

The LMK1D1208's low additive noise is shown below. The low noise 156.25-MHz source with 24-fs RMS jitter shown in Figure 9-2 drives the LMK1D1208, resulting in 46.4-fs RMS when integrated from 12 kHz to 20 MHz (Figure 9-3). The resultant additive jitter is a low 39.7-fs RMS for this configuration. Note that this result applies to the LMK1D1204 device as well.



A. Reference signal is low-noise Rohde and Schwarz SMA100B

Figure 9-2. LMK1D208 Reference Phase Noise, 156.25 MHz, 24-fs RMS (12 kHz to 20 MHz)

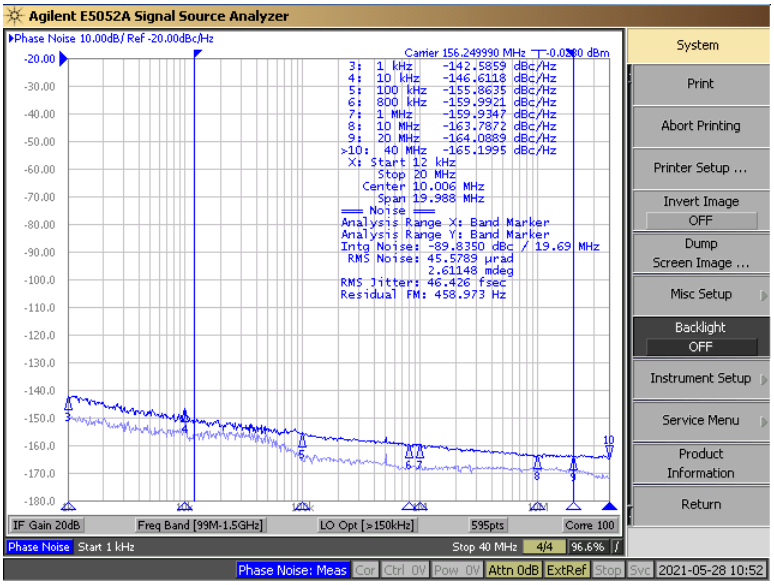


Figure 9-3. LMK1D1208 Output Phase Noise, 156.25 MHz, 46.4-fs RMS (12 kHz to 20 MHz)

The Figure 9-4 captures the low close-in phase noise of the LMK1D1208 device. The LMK1D1204 and LMK1D1208 have excellent flicker noise as a result of superior process technology and design. This enables their use for clock distribution in radar systems, medical imaging systems etc which require ultra-low close-in phase noise clocks.

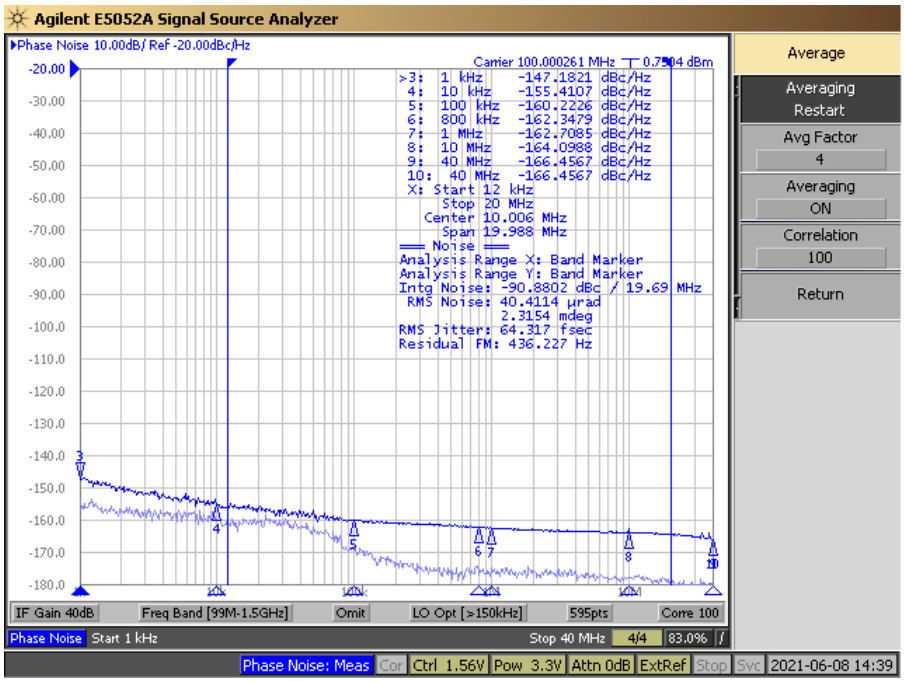


Figure 9-4. LMK1D1208 Output Phase Noise, 100 MHz, 1 kHz offset: -147 dBc/Hz

10 Power Supply Recommendations

High-performance clock buffers are sensitive to noise on the power supply, which can dramatically increase the additive jitter of the buffer. Thus, it is essential to reduce noise from the system power supply, especially when jitter or phase noise is critical to applications.

Filter capacitors are used to eliminate the low-frequency noise from the power supply, where the bypass capacitors provide the low impedance path for high-frequency noise and guard the power-supply system against the induced fluctuations. These bypass capacitors also provide instantaneous current surges as required by the device and must have low equivalent series resistance (ESR). To properly use the bypass capacitors, they must be placed close to the power-supply pins and laid out with short loops to minimize inductance. TI recommends adding as many high-frequency (for example, 0.1-µF) bypass capacitors as there are supply pins in the package. TI recommends, but does not require, inserting a ferrite bead between the board power supply and the chip power supply that isolates the high-frequency switching noises generated by the clock driver; these beads prevent the switching noise from leaking into the board supply. Choose an appropriate ferrite bead with low DC-resistance because it is imperative to provide adequate isolation between the board supply and the chip supply, as well as to maintain a voltage at the supply pins that is greater than the minimum voltage required for proper operation.

Figure 10-1 shows this recommended power-supply decoupling method.

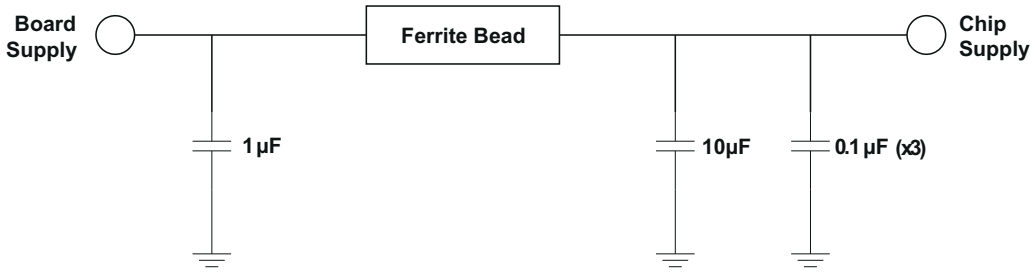


Figure 10-1. Power Supply Decoupling

11 Layout

11.1 Layout Guidelines

For reliability and performance reasons, the die temperature must be limited to a maximum of 135°C.

The device package has an exposed pad that provides the primary heat removal path to the printed circuit board (PCB). To maximize the heat dissipation from the package, a thermal landing pattern including multiple vias to a ground plane must be incorporated into the PCB within the footprint of the package. The thermal pad must be soldered down to ensure adequate heat conduction to of the package. Figure 11-1 shows a recommended land and via pattern for LMK1D1208.

11.2 Layout Example

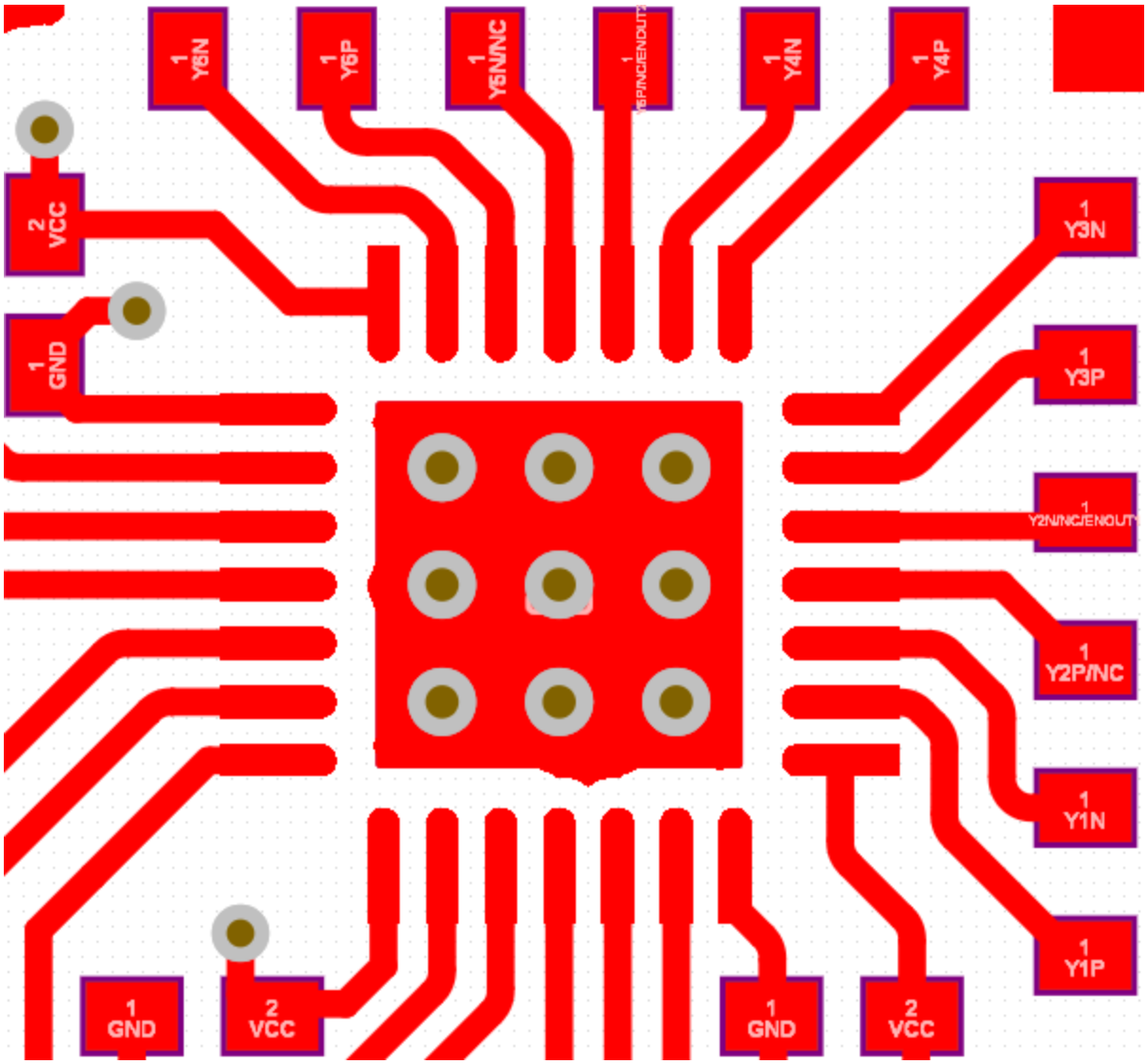


Figure 11-1. Recommended PCB Layout, Top Layer

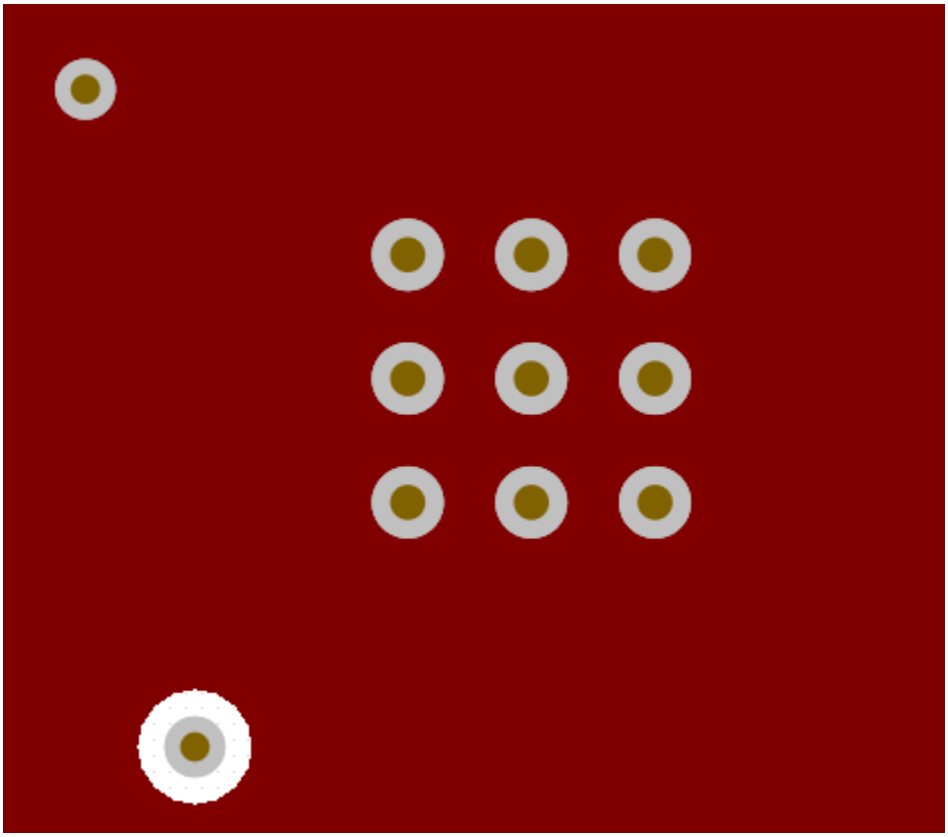


Figure 11-2. PCB Layout, GND Layer

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- *Low-Additive Jitter, Four LVDS Outputs Clock Buffer Evaluation Board* (SCAU043)
- *Power Consumption of LVPECL and LVDS* (SLYT127)
- *Semiconductor and IC Package Thermal Metrics* (SPRA953)
- *Using Thermal Calculation Tools for Analog Components* (SLUA556)

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

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12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMK1D1204RGTR	ACTIVE	VQFN	RGT	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	LD1204	Samples
LMK1D1204RGTT	ACTIVE	VQFN	RGT	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	LD1204	Samples
LMK1D1208RHDR	ACTIVE	VQFN	RHD	28	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	LMK1D 1208	Samples
LMK1D1208RHDT	ACTIVE	VQFN	RHD	28	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	LMK1D 1208	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

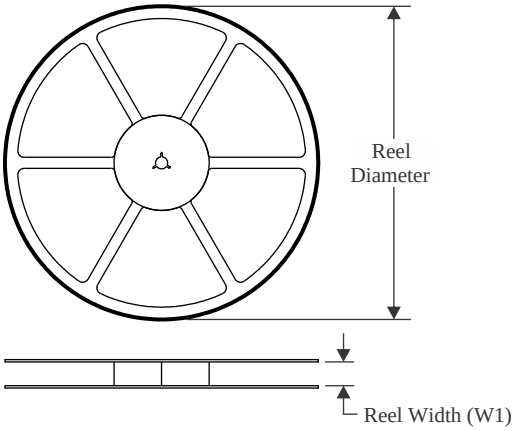
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

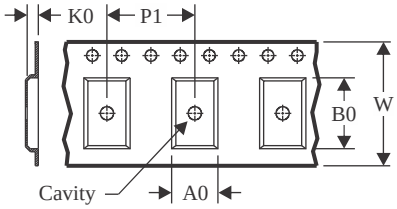
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

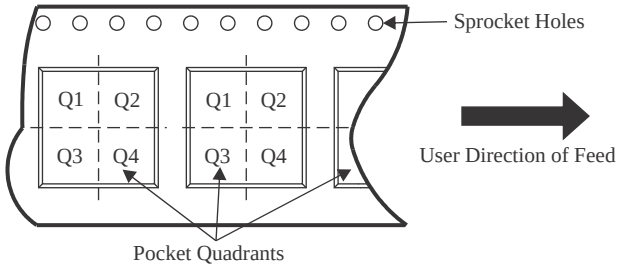


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

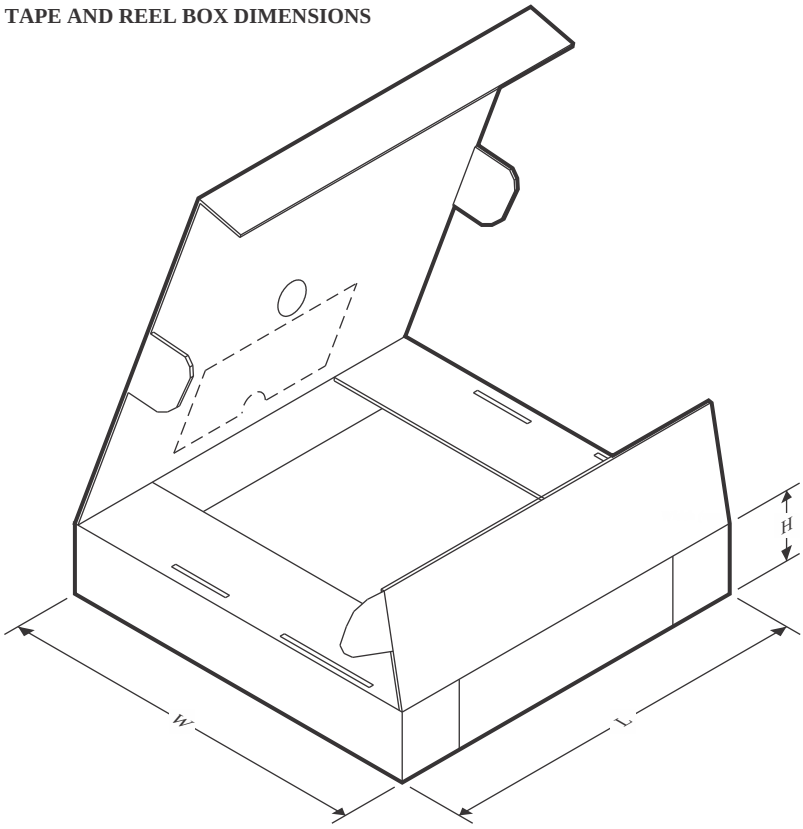
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMK1D1204RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
LMK1D1204RGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
LMK1D1208RHDR	VQFN	RHD	28	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
LMK1D1208RHDT	VQFN	RHD	28	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMK1D1204RGTR	VQFN	RGT	16	3000	367.0	367.0	35.0
LMK1D1204RGTT	VQFN	RGT	16	250	210.0	185.0	35.0
LMK1D1208RHDR	VQFN	RHD	28	3000	367.0	367.0	35.0
LMK1D1208RHDT	VQFN	RHD	28	250	210.0	185.0	35.0

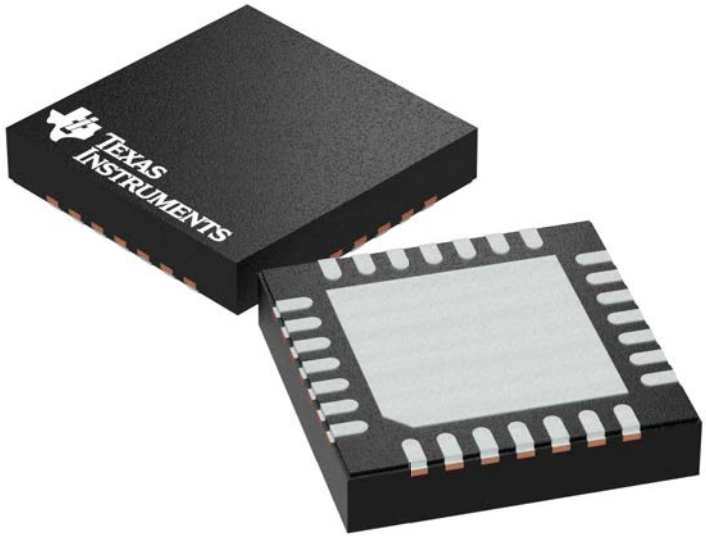
GENERIC PACKAGE VIEW

RHD 28

VQFN - 1 mm max height

5 x 5 mm, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

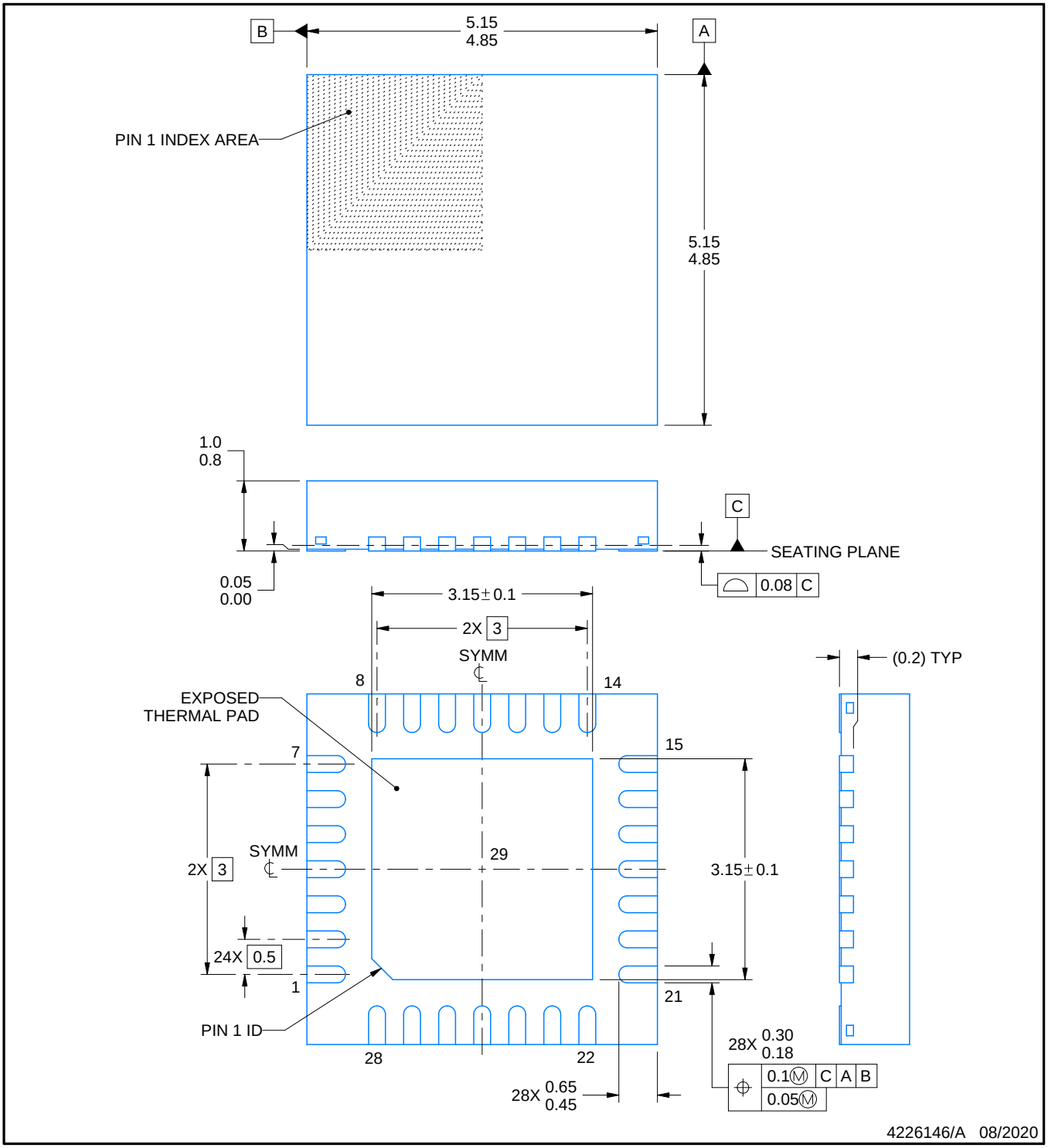
4204400/G

RHD0028B

PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

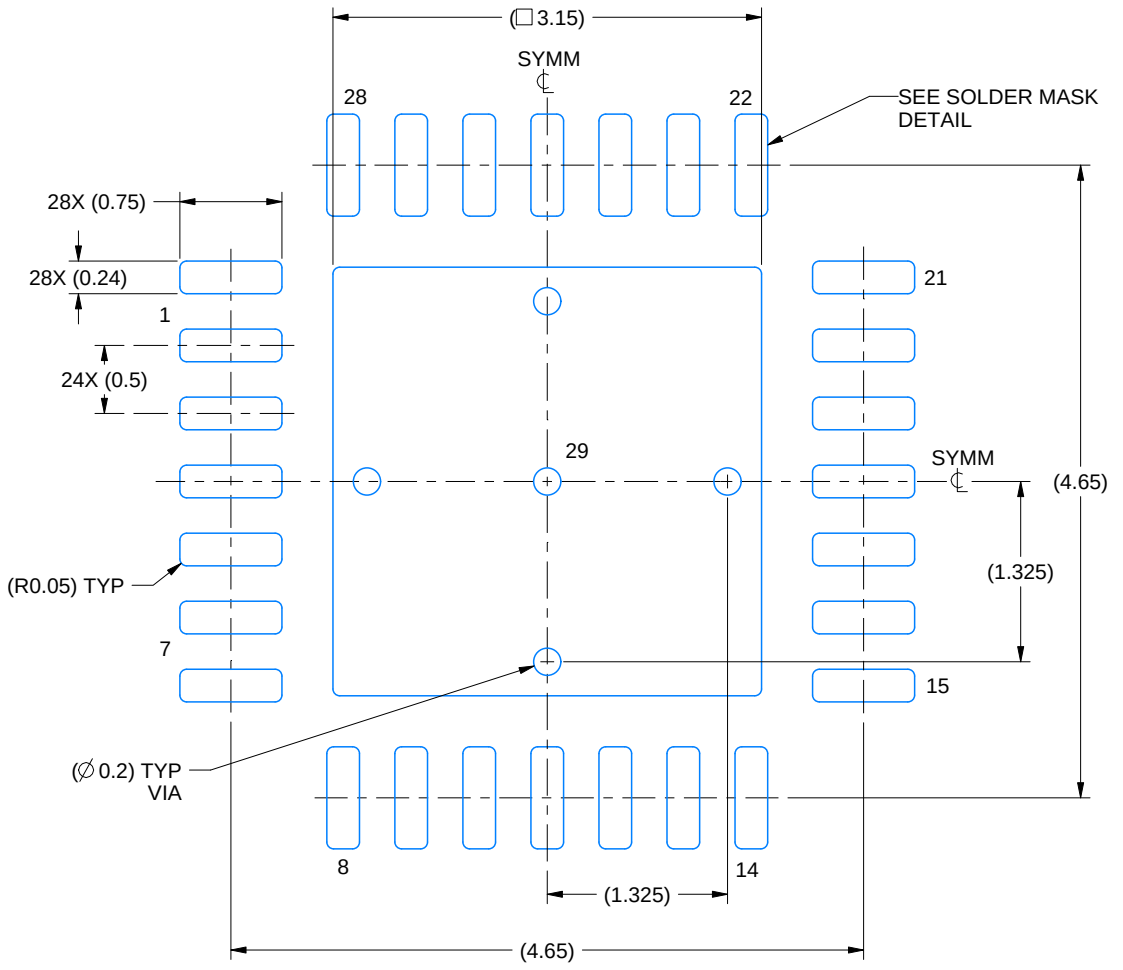
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

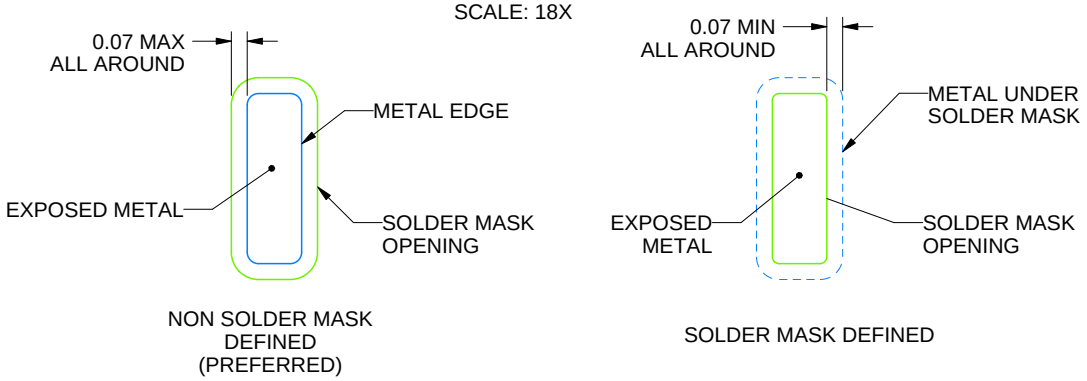
RHD0028B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 18X

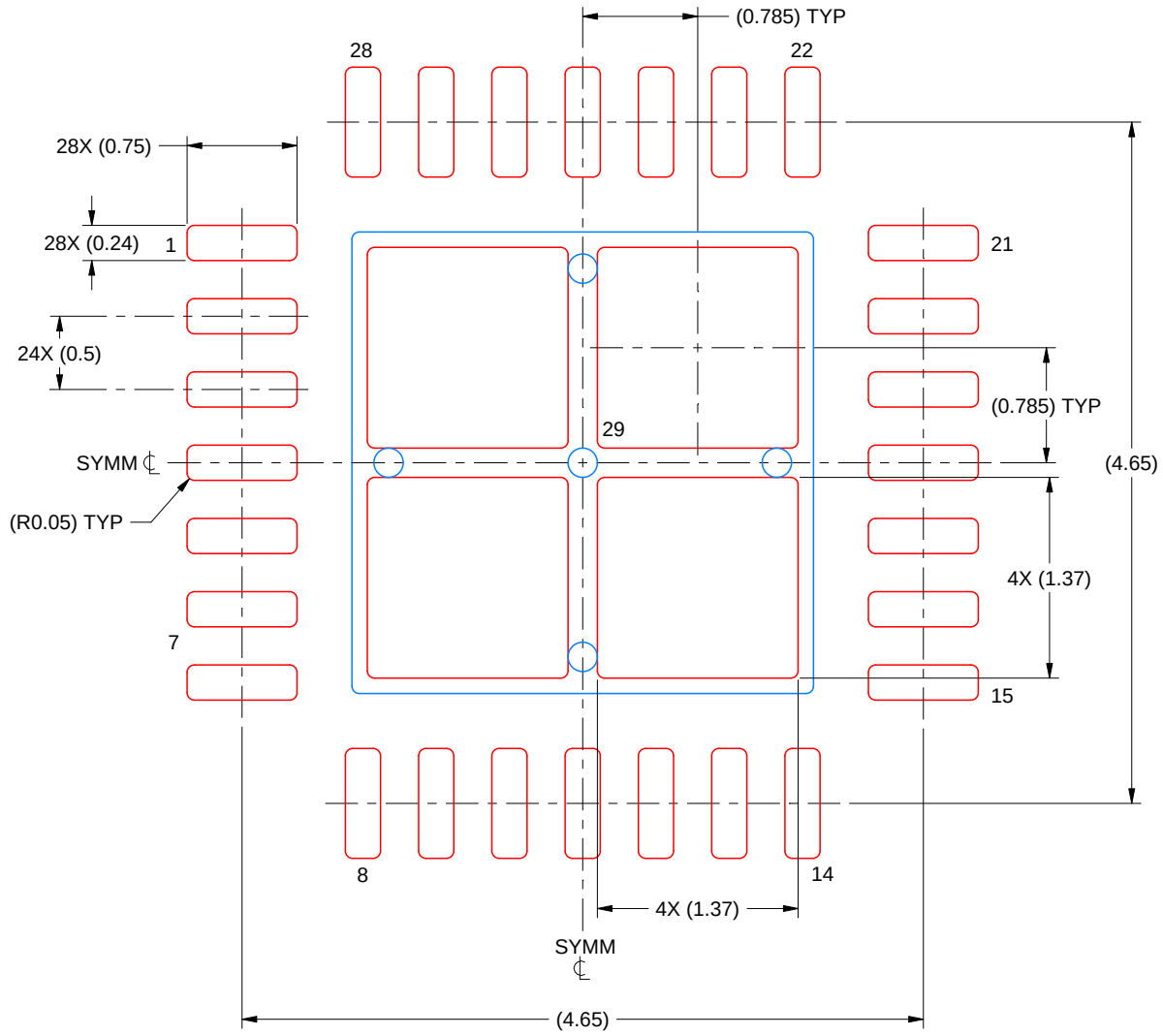


SOLDER MASK DETAILS

4226146/A 08/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 29
76% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

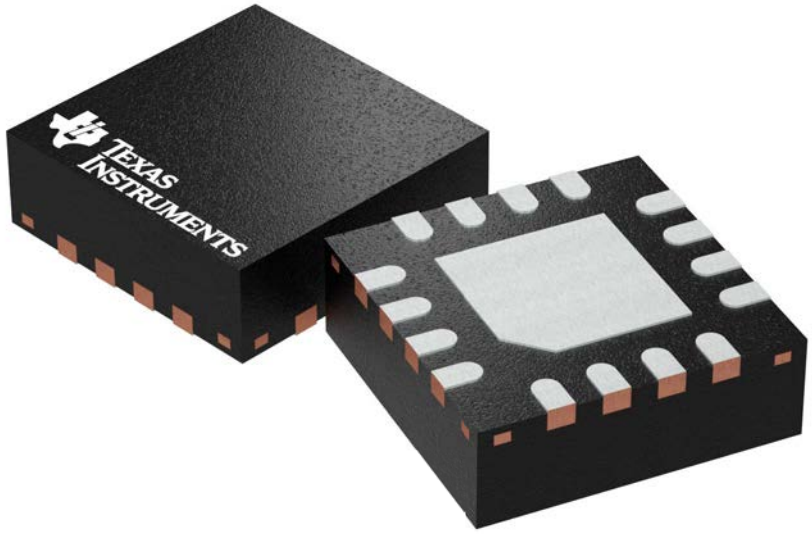
4226146/A 08/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

RGT 16 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



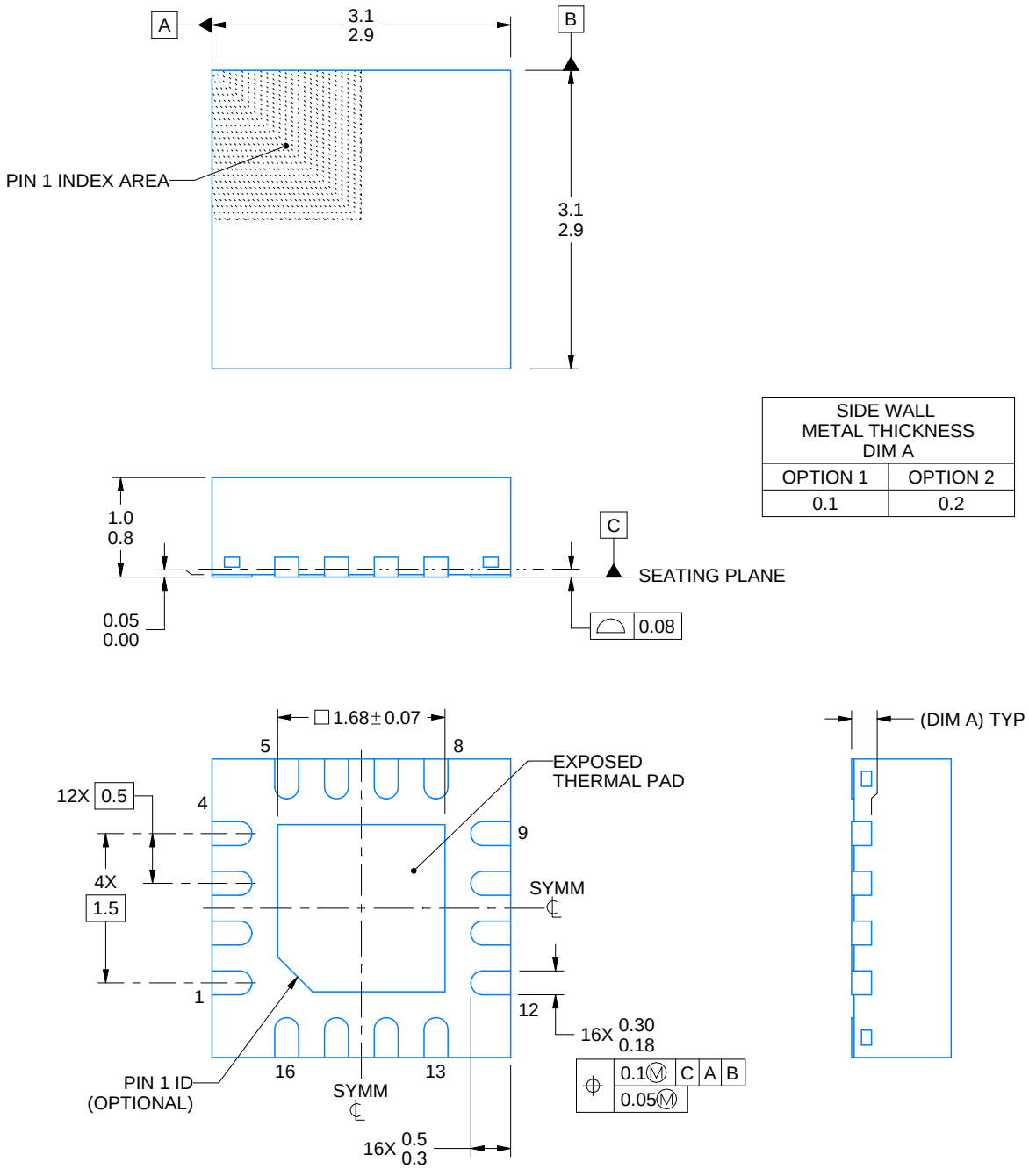
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

RGT0016C

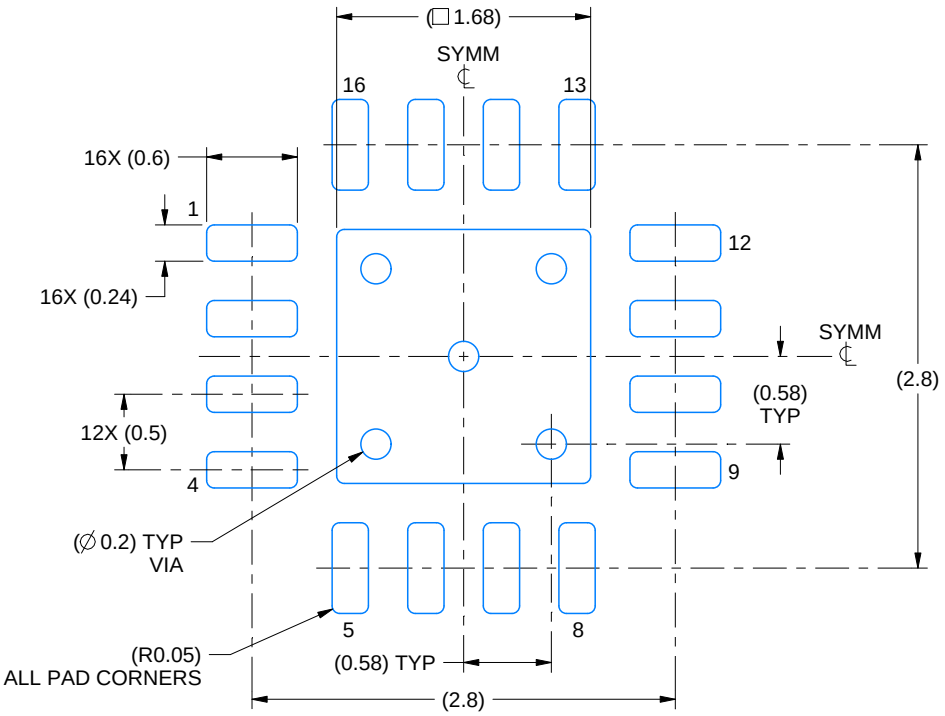
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

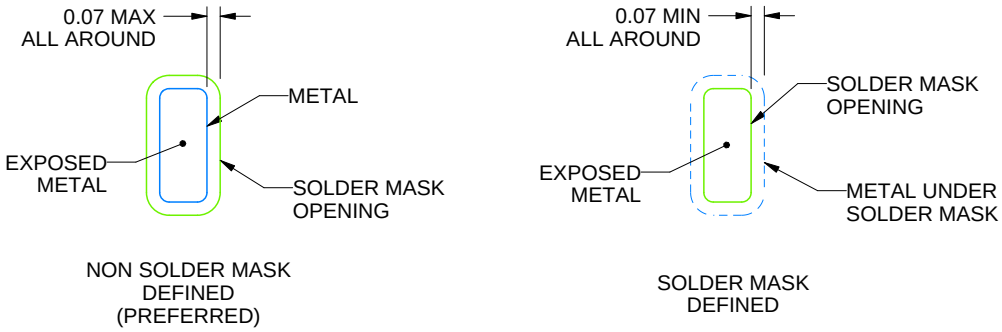


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

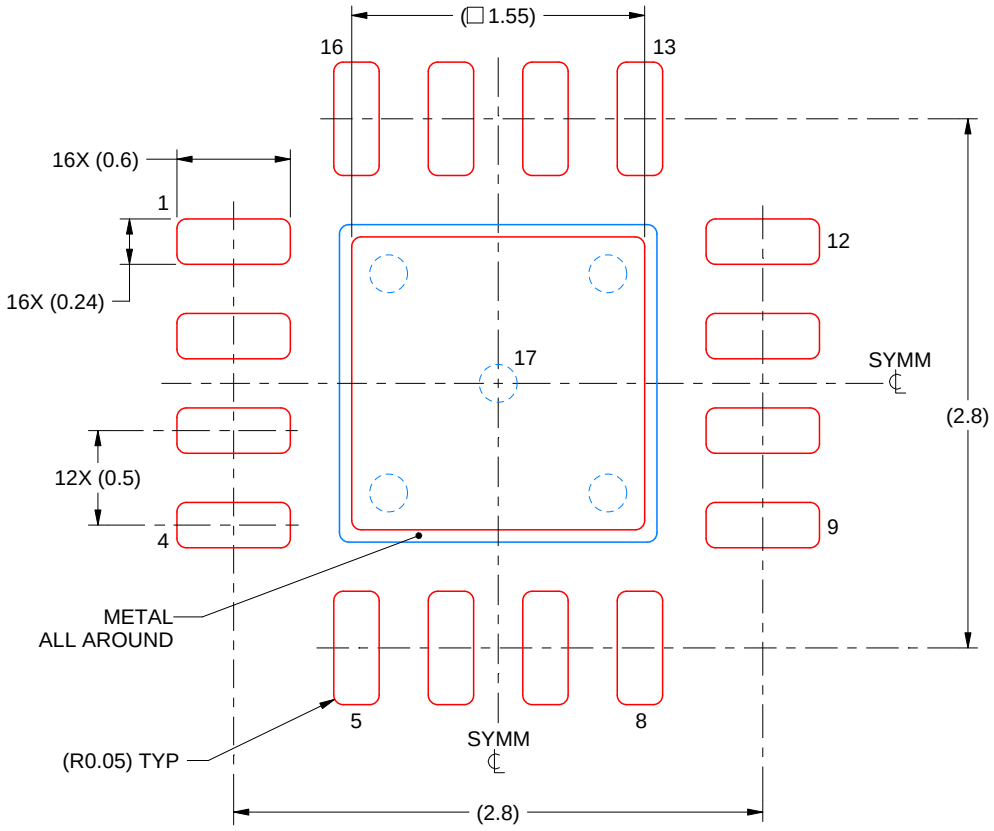


SOLDER MASK DETAILS

4222419/D 04/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4222419/D 04/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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