LMH1980 Auto-Detecting SD/HD/PC Video Sync Separator

Check for Samples: LMH1980

FEATURES

- **Analog Video Sync Separation for NTSC, PAL, 480I/P, 576I/P, 720P, 1080I/P/PsF, and Many VESA-Compatible Timing Formats**
- **Composite Video (CVBS), S-Video (Y/C), and Component Video (YP_BP_R/GBR) and PC Graphics (RGsB) Interfaces**
- **SD/PC Bi-Level Sync & HD Tri-Level Sync Compatible**
- **Composite, Horizontal, and Vertical Sync Outputs**
- **Burst/Back Porch Timing, Odd/Even Field, and HD Detect Flag outputs**
- **Automatic Video Format Detection**
- **Fixed-Level Sync Slicing for Video Inputs from 0.5 to 2 V_{PP}**
- **3.3V to 5V Supply Operation**

APPLICATIONS

- **Consumer, Professional, Automotive & Industrial Video**
- **Video Capture, Editing, and Processing**
- **Genlock Circuits**
- **Surveillance & Security Video Systems**
- **Set-Top Boxes (STB) & Digital Video Recorders (DVR)**
- **LCD / Plasma Displays and Video Projectors**
- **Machine Vision and Inspection Systems**
- **Video Trigger Oscilloscopes and Waveform Monitors**

DESCRIPTION

The LMH1980 is an auto-detecting SD/HD/PC video sync separator ideal for use in a wide range of video applications, such as automotive LCD monitors, video capture & editing devices, surveillance & security equipment, and machine vision and inspection systems.

The LMH1980 accepts an analog video input signal with either bi-level or tri-level sync and automatically detects the video format, eliminating the need for external R_{SET} resistor adjustment required by other sync separators (e.g.: LM1881). The outputs provide timing signals in CMOS logic, including Composite, Horizontal, and Vertical Syncs, Burst/Back Porch Timing, and Odd/Even Field outputs. The $\overline{HD}$ flag output (pin 5) provides a logic low signal only when a valid $\overline{HD}$ video input with tri-level sync is detected. The $\overline{HD}$ flag can be used to disable an external switch-controlled SD chroma filter when HD video is detected, or enable it when SD video is detected. For non-standard video with bi-level sync and without vertical serration pulses, a default vertical sync pulse will be output and no horizontal sync pulses will be output during the vertical sync interval.

The LMH1980 is available in a space-saving 10-lead Mini-SO Package (VSSOP) and operates over a temperature range of −40°C to +85°C.

Connection Diagram

Top View

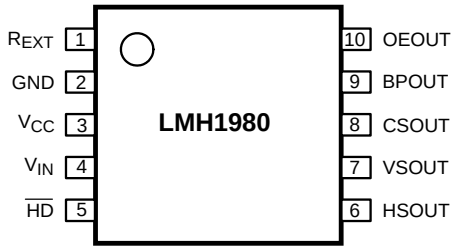


Figure 1. 10-Lead VSSOP Package
See Package Number DGS0010A

Pin Descriptions

Pin No.	Pin Name	Pin Description
1	R_{EXT}	Bias Current External Resistor
2	GND	Ground
3	V_{CC}	Supply Voltage
4	V_{IN}	Analog Video Input
5	$\overline{HD}$	HD Detect Flag Output
6	HSOUT	Horizontal Sync Output
7	VSOUT	Vertical Sync Output
8	CSOUT	Composite Sync Output
9	BPOUT	Burst/Back Porch Timing Output
10	OEOUT	Odd/Even Field Output

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

ESD Tolerance (3)	Human Body Model	3.5 kV
	Machine Model	350V
Supply Voltage, V_{CC}		0V to 5.5V
Video Input, V_{IN}		−0.3V to V_{CC} + 0.3V
Storage Temperature Range		−65°C to +150°C
Lead Temperature (soldering 10 sec.)		300°C
Junction Temperature, T_{JMAX} (4)		+150°C
Thermal Resistance, θ_{JA} (no airflow)		120°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics Tables.
(2) All voltages are measured with respect to GND, unless otherwise specified.
(3) Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC)Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).
(4) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

Operating Ratings (1)

Temperature Range (2)	−40°C to +85°C
V_{CC}	3.3V −10% to 5V +10%
Input Amplitude, $V_{IN-AMPL}$	140 mV to V_{CC}–$V_{IN-CLAMP}$

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics Tables.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

Electrical Characteristics (1)

Unless otherwise specified, all limits are specified for T_A = 25°C, V_{CC} = 3.3V, R_{EXT} = 10 kΩ 1%, R_L = 10 kΩ, C_L < 10 pF.**Boldface** limits apply at the temperature extremes. See Figure 2 for Test Circuit.

Parameter		Test Conditions		Min (2)	Typ (3)	Max (2)	Units
I_{CC}	Supply Current	No input signal	V_{CC} = 3.3V		10.5	12.5	mA
			V_{CC} = 5V		12.0	14.0	
Video Input Specifications							
$V_{IN-SYNC}$	Input Sync Amplitude	Amplitude from negative sync tip to video blanking level for SD/EDTV bi-level sync (4) (5)		0.14	0.30	0.60	V_{PP}
		Amplitude from negative to positive sync tips for HDTV tri-level sync (4) (6)		0.30	0.60	1.20	
$V_{IN-CLAMP}$	Input Sync Tip Clamp Level (7)				0.7		V
$V_{IN-SLICE}$	Input Sync Slice Level	Slicing level above $V_{IN-CLAMP}$			70		mV
Logic Output Specifications (8)							
V_{OL}	Output Logic 0	See output load conditions above	V_{CC} = 3.3V			0.3	V
			V_{CC} = 5V			0.5	
V_{OH}	Output Logic 1	See output load conditions above	V_{CC} = 3.3V	3.0			V
			V_{CC} = 5V	4.5			
$T_{SYNC-LOCK}$	Sync Lock Time	Time for the output signals to be correct after the video signal settles at V_{IN} following a significant input change. See START-UP TIME for more information			2		V periods
T_{VSOUT}	Vertical Sync Output Pulse Width	Serration Pulses in the Vertical Interval. See Figure 3, Figure 4, Figure 5, Figure 6, Figure 7, and Figure 8 for SDTV, EDTV & HDTV Vertical Interval Timing			3		H periods

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. Parametric performance indicated in the electrical tables is not ensured under conditions of internal self-heating where $T_J > T_A$.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using the Statistical Quality Control (SQC) method.
(3) Typical values represent the most likely parametric norm at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.
(4) $V_{IN-AMPL}$ plus $V_{IN-CLAMP}$ should not exceed V_{CC}.
(5) Tested with 480I signal.
(6) Tested with 1080P signal.
(7) Maximum voltage offset (DC bounce) between 2 consecutive input sync tips must be less than 25 mV_{PP}; otherwise, this may cause incorrect output signals to occur.
(8) Outputs are negative-polarity logic signals, except for Odd/Even Field.

LMH1980 Test Circuit

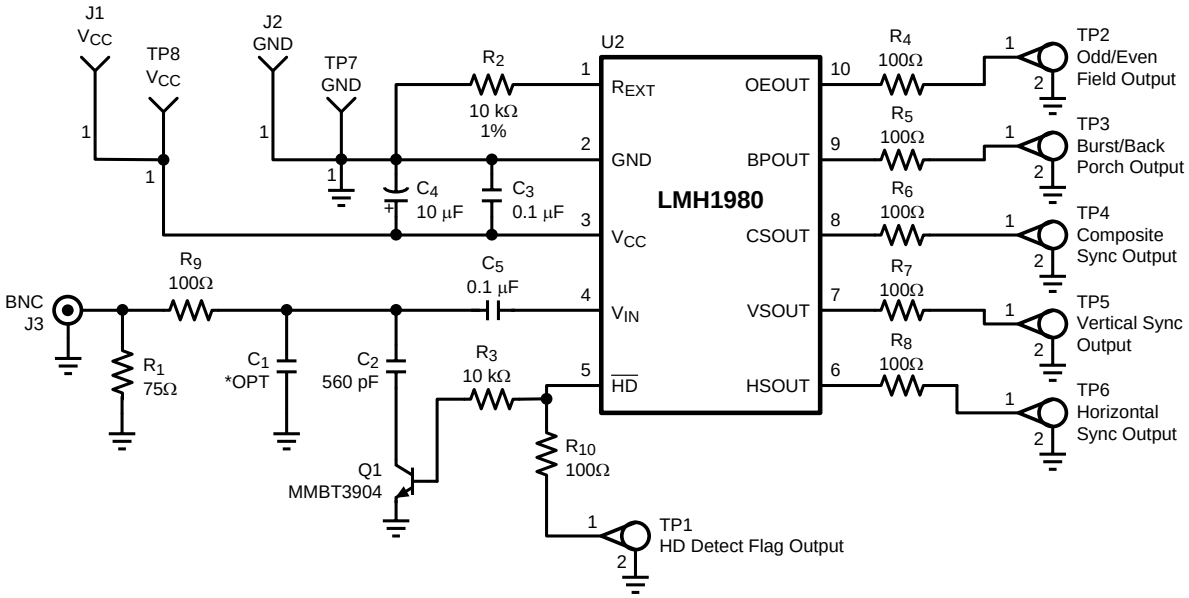


Figure 2. Test Circuit

The LMH1980 test circuit is shown in Figure 2. The video generator should provide a clean, low-noise video input signal with minimal sync pulse overshoot over 75Ω coaxial cable, which should be impedance-matched with a 75Ω load termination resistor to prevent unwanted signal distortion. The output waveforms should be monitored using a low-capacitance probe on an oscilloscope with at least 500 MHz bandwidth. See PCB LAYOUT CONSIDERATIONS for more information about signal and supply trace routing and component placement. Also, refer to the "LMH1980 Evaluation Board Instruction Manual" Application Note (AN-1618 [SNLA096]).

SDTV Vertical Interval Timing Diagrams (NTSC, PAL, 480I, 576I)

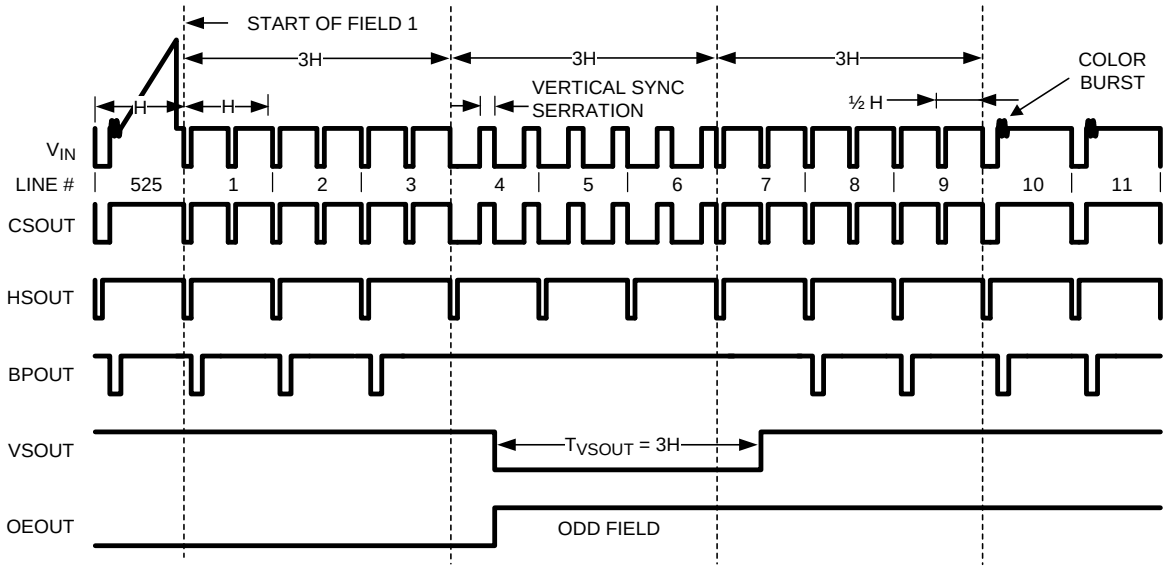


Figure 3. NTSC Odd Field Vertical Interval

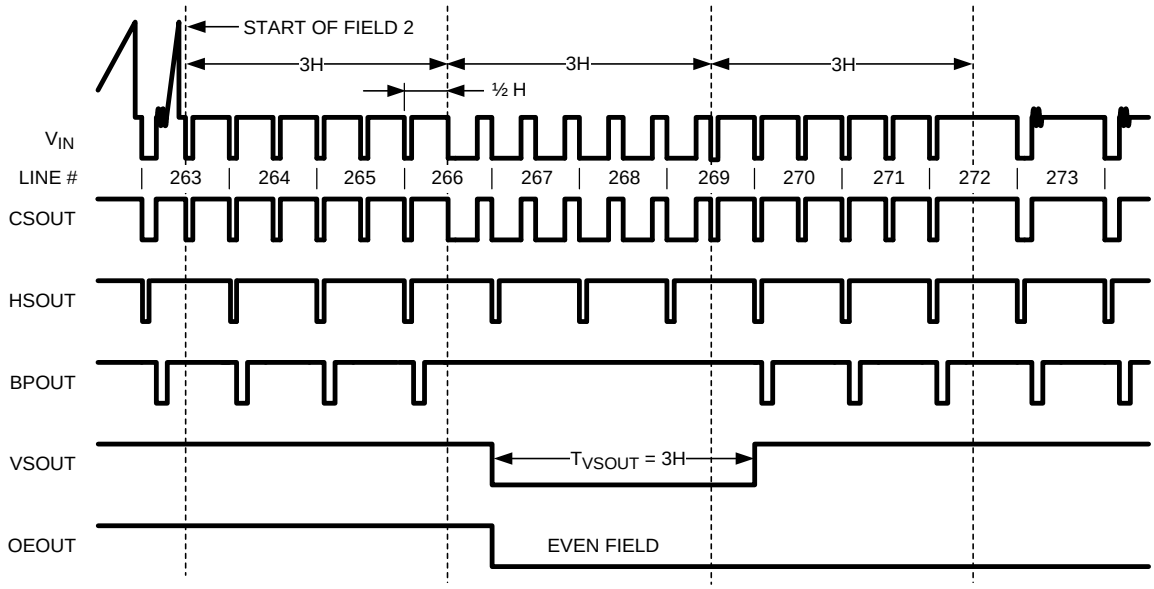


Figure 4. NTSC Even Field Vertical Interval

EDTV Vertical Interval Timing Diagram (480P, 576P)

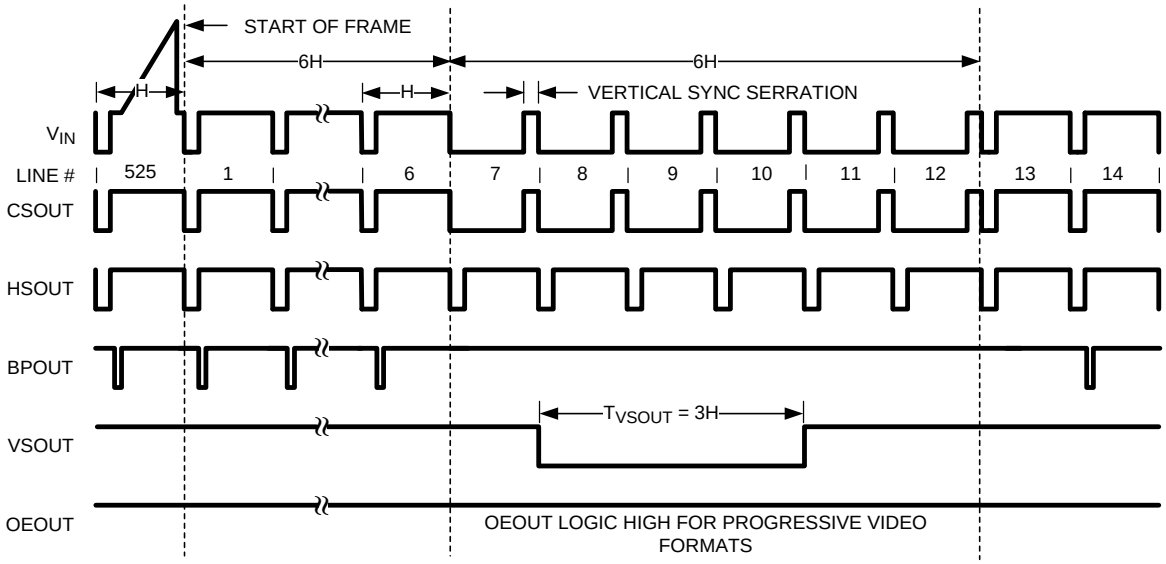


Figure 5. 480P Vertical Interval

HDTV Vertical Interval Timing Diagram (720P, 1080P)

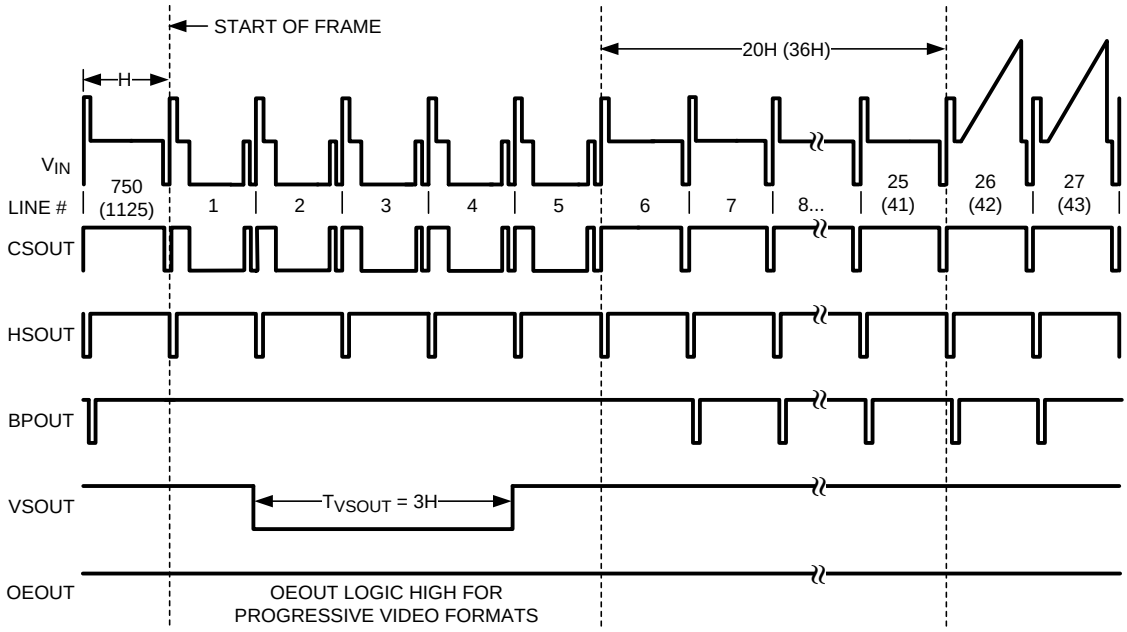


Figure 6. 720P (1080P) Vertical Interval

HDTV Vertical Interval Timing Diagrams (1080I)

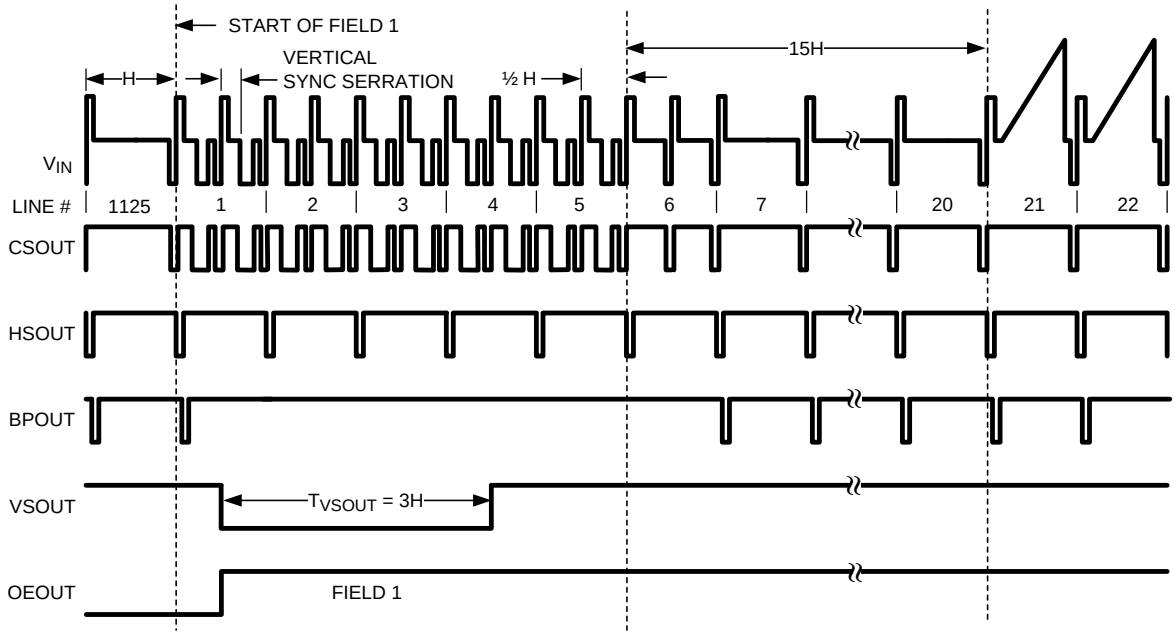


Figure 7. 1080I Field 1 Vertical Interval

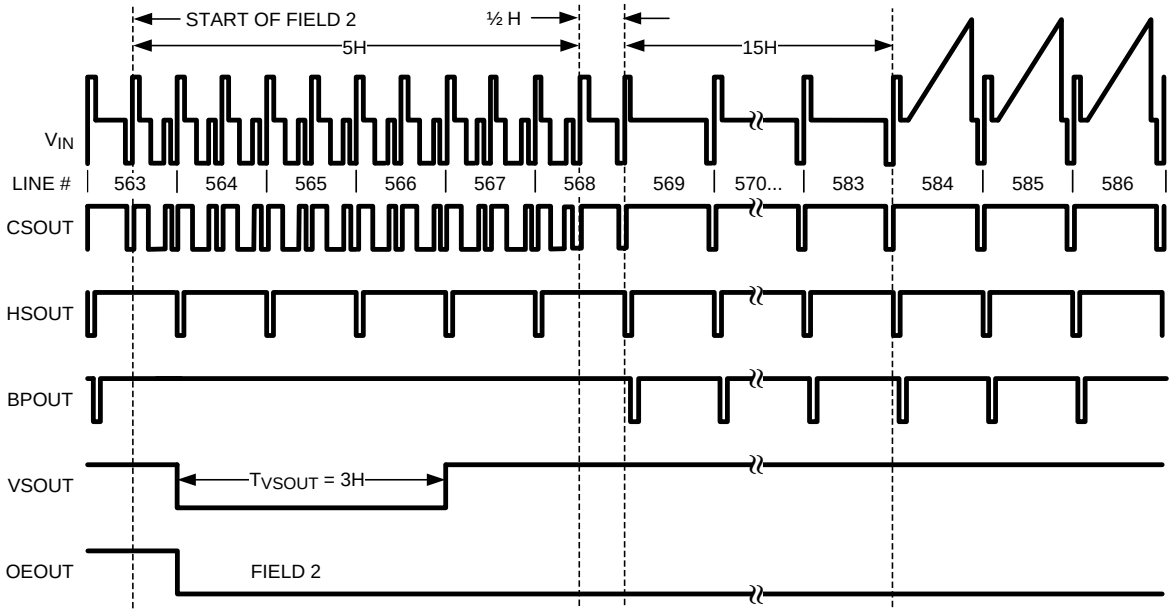


Figure 8. 1080I Field 2 Vertical Interval

SD/EDTV Horizontal Interval Timing Diagram

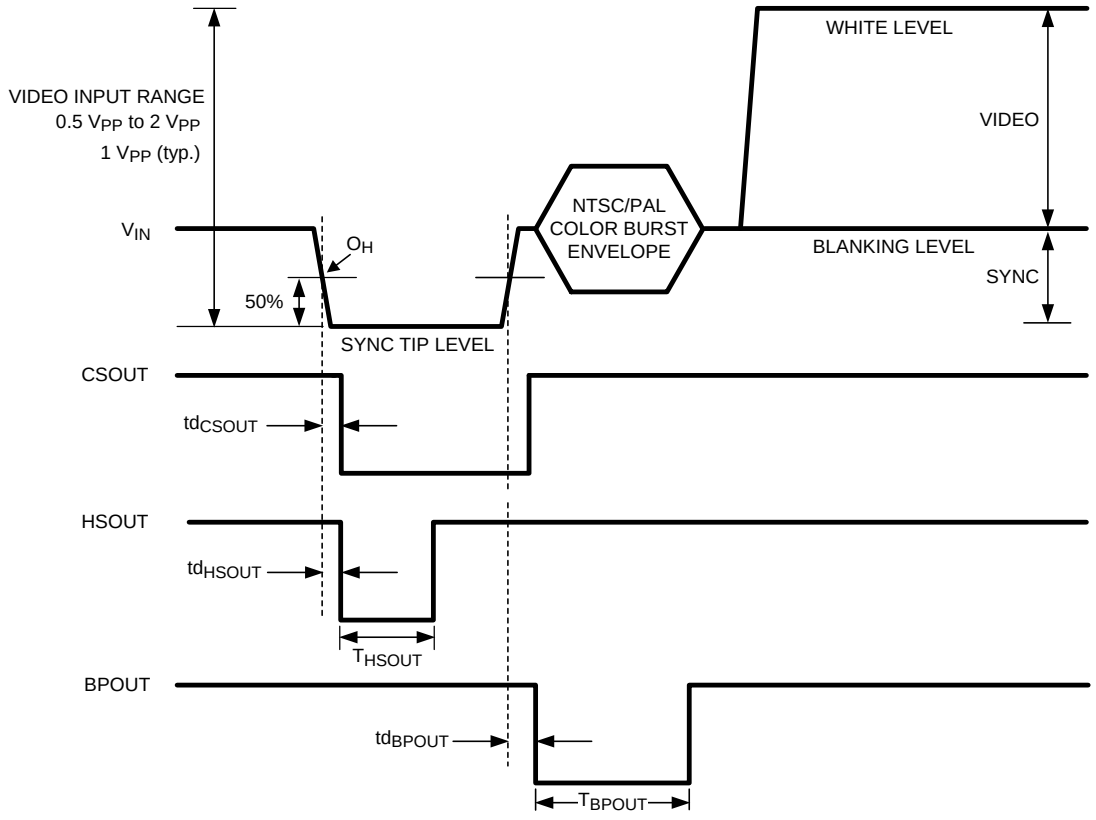


Figure 9. SD/EDTV Horizontal Interval with Bi-level Sync

Table 1. SDTV Horizontal Interval Timing Characteristics(1)

Parameter		Test Conditions	Typ	Units
td_{CSOUT}	Composite Sync Output Propagation Delay from Input Sync Reference (O_H)	See Figure 9	525	ns
td_{HSOUT}	Horizontal Sync Output Propagation Delay from Input Sync Reference (O_H)	See Figure 9	530	ns
td_{BPOUT}	Burst/Back Porch Timing Output Propagation Delay from Input Sync Trailing Edge	See Figure 9	400	ns
T_{HSOUT}	Horizontal Sync Output Pulse Width	See Figure 9	2.5	µs
T_{BPOUT}	Burst/Back Porch Timing Output Pulse Width	See Figure 9	3.0	µs

(1) V_{CC} = 3.3V , T_A = 25°C, No Input Filter, PAL Video Input from Tek TG700 Generator with AVG7 SD video module

Table 2. EDTV Horizontal Interval Timing Characteristics(1)

Parameter		Test Conditions	Typ	Units
td_{CSOUT}	Composite Sync Output Propagation Delay from Input Sync Reference (O_H)	See Figure 9	170	ns
td_{HSOUT}	Horizontal Sync Output Propagation Delay from Input Sync Reference (O_H)	See Figure 9	175	ns
td_{BPOUT}	Burst/Back Porch Timing Output Propagation Delay from Input Sync Trailing Edge	See Figure 9	485	ns
T_{HSOUT}	Horizontal Sync Output Pulse Width	See Figure 9	2.3	µs
T_{BPOUT}	Burst/Back Porch Timing Output Pulse Width	See Figure 9	350	ns

(1) V_{CC} = 3.3V , T_A = 25°C, No Input Filter, 576P Video Input from Tek TG700 Generator with AVG7 SD module

HDTV Horizontal Interval Timing Diagram

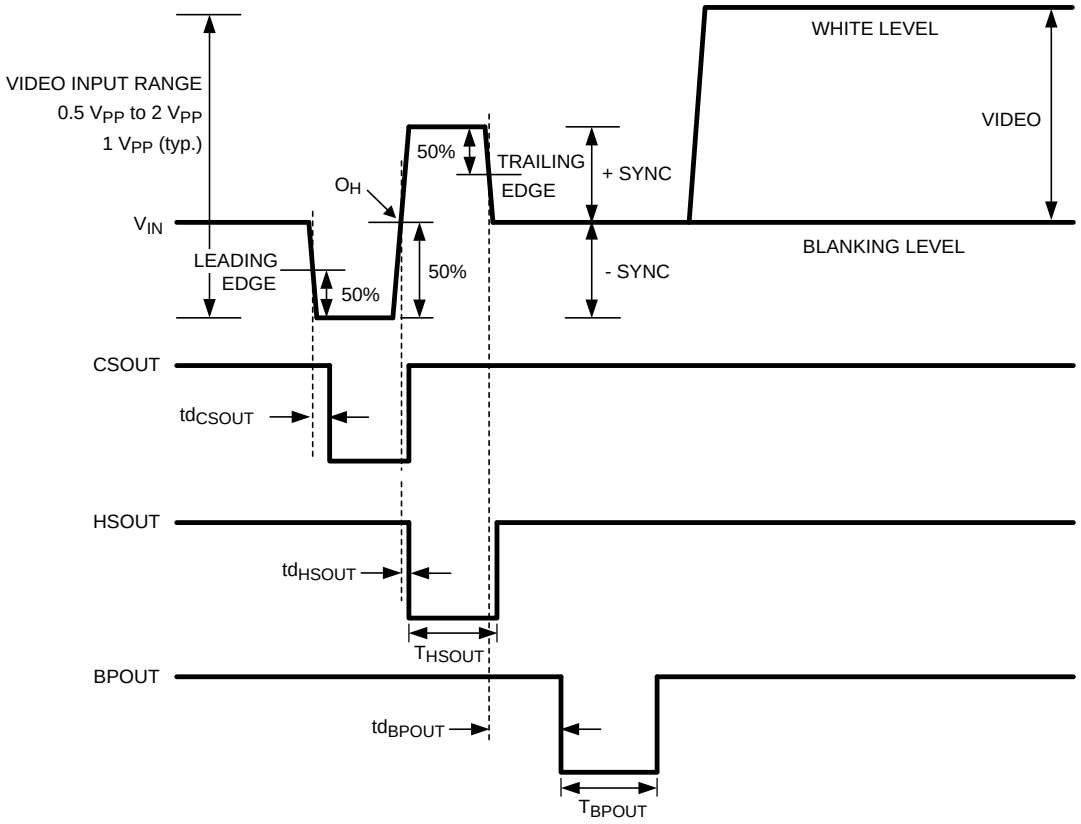


Figure 10. HDTV Horizontal Interval with Tri-level Sync

Table 3. HDTV Horizontal Interval Timing Characteristics(1)

Parameter		Test Conditions	Typ	Units
td_{CSOUT}	Composite Sync Output Propagation Delay from Input Sync Leading Edge	See Figure 10	150	ns
td_{HSOUT}	Horizontal Sync Output Propagation Delay from Input Sync Reference (O_H)	See Figure 10	60	ns
td_{BPOUT}	Burst/Back Porch Timing Output Propagation Delay from Input Sync Trailing Edge	See Figure 10	450	ns
T_{HSOUT}	Horizontal Sync Output Pulse Width	See Figure 10	525	ns
T_{BPOUT}	Burst/Back Porch Timing Output Pulse Width	See Figure 10	350	ns

(1) V_{CC} = 3.3V , T_A = 25°C, No Input Filter, 1080I Video Input from Tek TG700 Generator with AWVG7 HD module

APPLICATION INFORMATION

GENERAL DESCRIPTION

The LMH1980 is designed to extract the timing information from various video formats with standard and non-standard vertical serration and output the syncs and relevant timing signals in CMOS logic. Its advanced features and easy application make it ideal for consumer, professional, and industrial video systems where sync timing needs to be extracted from SD, HD, and PC video signals. The device can operate from a supply voltage between 3.3V and 5V. The only required external components are bypass capacitors between the V_{CC} and GND pins, input coupling capacitor (C_{IN}) from the signal source to the V_{IN} pin, and a fixed-value 1% precision resistor between the R_{EXT} and GND pins. Refer to the test circuit in Figure 2.

R_{EXT} Resistor

The precision external resistor (R_{EXT}) establishes the internal bias current and precise reference voltage for the LMH1980. For optimal performance, R_{EXT} should be a 10 kΩ 1% precision resistor with a low temperature coefficient to ensure proper operation over a wide temperature range. Using a R_{EXT} resistor with less precision may result in reduced performance (like worse performance, increased propagation delay variation, or reduced input sync amplitude range) against temperature, supply voltage, input signal, or part-to-part variations.

NOTE

The R_{EXT} resistor used with the LMH1980 serves a different function than the "R_{SET} resistor" used with other previous sync separators, like the LM1881. For the LM1881, the R_{SET} value needed to be adjusted externally to support different input line rates. For the LMH1980, the R_{EXT} value is fixed, and the device automatically detects the input line rate to support various video formats without electrical or physical intervention.

Automatic Format Detection and Switching

Automatic format detection eliminates the need for adjusting an external R_{SET} resistor or programming via a microcontroller. The device outputs will respond correctly to a switch in video format after a sufficient start-up time has been satisfied, usually within 1 to 2 fields of video. Unlike other sync separators, the LMH1980 does not require the power to be cycled in order to produce correct outputs after a significant change to the input signal. See START-UP TIME for more details.

Fixed-Level Sync Slicing

The LMH1980 uses fixed-level sync slicing for video inputs with an amplitude from $0.5V_{PP}$ to $2V_{PP}$, which allows for proper sync separation even for improperly terminated or attenuated input signals. The fixed-level sync slicing threshold is nominally 70 mV above the clamped sync tip. This means that for a minimum video input signal amplitude of $0.5V_{PP}$, the slicing level is near the mid-point of the sync pulse amplitude. This slicing level is independent of the input signal amplitude; therefore, for a $2V_{PP}$ input, the slicing level occurs at 12% of the sync pulse amplitude.

INPUT CONSIDERATIONS

The LMH1980 supports sync separation for analog CVBS, Y (luma) from Y/C and YP_BP_R, and G (sync on green) from GBR/RGsB, as specified in the following video standards.

- Composite Video (CVBS) and S-Video (Y/C):
  - SMPTE 170M (NTSC), ITU-R BT.470 (PAL)
- Component Video (YP_BP_R/GBR):
  - SDTV: SMPTE 125M, SMPTE 267M, ITU-R BT.601 (480I, 576I)
  - EDTV: ITU-R BT.1358 (480P, 576P)
  - HDTV: SMPTE 296M (720P), SMPTE 274M (1080I/P), SMPTE RP 211 (1080PsF)
- PC Graphics (RGsB):
  - VESA Monitor Timing Standards and Guidelines Version 1.0, Revision 0.8
- Non-Standard Video:

– Composite NTSC & PAL (or Component 480I & 576I) without vertical serration & equalization pulses (i.e.: from logical OR-ing of H & V signals)

Input Termination

The video source should be load terminated with a 75Ω resistor to ensure correct video signal amplitude and minimize signal distortion due to reflections. In extreme cases, the LMH1980 can handle non-terminated or double-terminated input conditions, assuming $1V_{PP}$ signal amplitude for normally terminated video.

Input Filtering

An external filter is recommended if the video signal has large chroma amplitude that extends near the sync tip and/or has considerable high-frequency noise, so they do not interfere with sync separation. A simple RC low-pass chroma filter with a series resistor (R_9) and a filter capacitor (C_2) to ground can be used to sufficiently attenuate chroma such that minimum peak of its amplitude is above the slicing level and also to improve the overall signal-to-noise ratio. To achieve the desired filter cutoff frequency, it's advised to vary C_2 and keep R_9 small (i.e.: 100Ω) to minimize sync tip clipping due to the voltage drop across R_9. Keep in mind that as the cutoff frequency decreases, the LMH1980 output propagation delays increase, which could affect the timing relationship between the sync and video signals.

In applications where the chroma filter needs to be disabled when HD video is input, it is possible to use a transistor switch (Q1) controlled by the $\overline{HD}$ flag (pin 5) to open C_2's connection to ground as shown in Figure 11. When a HD tri-level sync input signal is applied, $\overline{HD}$ will output logic low (following a brief delay for auto format detection) and Q1 will turn off to disable the chroma filter, which is intended for SD composite video only. When a SD bi-level sync signal (i.e.: NTSC/PAL) is applied, $\overline{HD}$ will output logic high and Q1 will turn on to enable the chroma filter.

Important: If the filter cutoff frequency (f_{CO}) is set too low and HD video is applied, the filter can severely roll off and attenuate the input's high-bandwidth tri-level sync pulses such that the LMH1980 cannot detect a valid HD input signal. If the LMH1980 cannot detect a valid HD input, then the $\overline{HD}$ flag will never change from logic high to low and the switch-controlled filter will never be disabled via Q1. In other words, f_{CO} should not be set too low that the filter impairs the LMH1980's ability to detect a valid HD input. The values of R_9 and C_2 shown in Figure 11 give f_{CO}=2.79 MHz (about -4 dB at 3.58 MHz NTSC subcarrier frequency) without impairing HD video format detection.

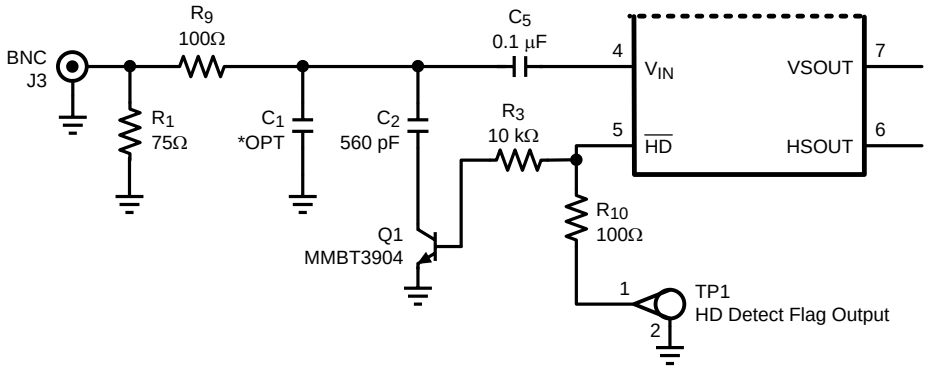


Figure 11. External Switch-Controlled Chroma Filter

If a PC video input with bi-level sync is to be used, C_2 should be removed to disable chroma filtering. This is necessary because $\overline{HD}$ will output logic high (like in the SD video input case) and enable the filter. A chroma filter could severely band-limit a high-bandwidth PC video signal, which could roll-off and attenuate the sync pulses such that the LMH1980 cannot detect a valid input signal.

If some high-frequency noise filtering is needed for all video inputs, a small capacitor (C_1) may be optionally used in parallel but outside of the transistor switch. When Q1 is turned on, then C_1 and C_2 will be connected in parallel (C_1+C_2)

Input Coupling Capacitor

The input signal should be AC coupled to the V_{IN} (pin 4) of the LMH1980 with a properly chosen coupling capacitor, C_{IN}.

The primary consideration in choosing C_{IN} is whether the LMH1980 will interface with video sources using an AC-coupled output stage. If AC-coupled video sources are expected in the end-application , then it's recommended to choose a small C_{IN} value such as 0.01 µF to avoid missing sync output pulses due to average picture level changes. It's important to note that video sources with an AC-coupled output will cause video-dependent jitter at the HSync output of the sync separator. When only DC-coupled video sources are expected, a larger value for C_{IN} may be used without concern for missing sync output pulses. A smaller C_{IN} value can be used to increase rejection of source AC hum components and also reduce start-up time regardless of the video source's output coupling type.

START-UP TIME

When there is a significant change to the video input signal, such as sudden signal switching in, signal attenuation (i.e.: load termination added via loop through) or signal gain (i.e.: load termination removed), the quiescent operation of the LMH1980 will be disrupted. During this dynamic input condition, the LMH1980 outputs may not be correct but will recover to valid signals after a predictable start-up time, which consists of an adjustable input settling time and a predetermined "sync lock time".

Input Settling Time and Coupling Capacitor Selection

Following a significant input condition, the negative sync tip of the AC-coupled signal settles to the input clamp voltage as the coupling capacitor, C_{IN}, recovers a quiescent DC voltage via the dynamic clamp current through V_{IN}. Because C_{IN} determines the input settling time, its capacitance value is critical when minimizing overall start-up time. A smaller C_{IN} value yields shorter settling time at the expense of increased line droop voltage, whereas a larger one yields reduced line droop but longer settling time. Settling time is proportional to the value of C_{IN}, so doubling C_{IN} will also double the settling time.

Sync Lock Time

In addition to settling time, the LMH1980 has a predetermined sync lock time, $T_{SYNC-LOCK}$, before the outputs are correct. Once the AC-coupled input has settled enough, the LMH1980 needs time to detect the valid video signal and apply fixed-level sync slicing before the output signals are correct.

For practical values of C_{IN}, $T_{SYNC-LOCK}$ is typically less than 1 or 2 video fields in duration starting from the 1st valid VSync output pulse to the valid HSync pulses beginning thereafter. VSync and HSync pulses are considered valid when they align correctly with the input's vertical and horizontal sync intervals.

It is recommended for the outputs to be applied to the system after the start-up time is satisfied and outputs are valid. For example, the oscilloscope screenshot in Figure 12 shows a typical start-up time within 1 video field from when an NTSC signal is just applied to when the LMH1980 outputs are valid.

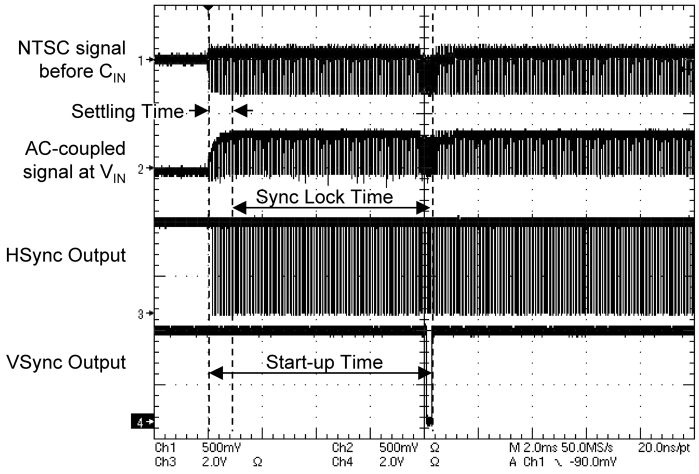


Figure 12. Typical Start-Up Time for NTSC Input to LMH1980 (C_{IN} = 0.1 µF)

LOGIC OUTPUTS

In the absence of a video input signal, the LMH1980 outputs are logic high except for the odd/even field, which is undefined and depends on its previous state, and the composite sync output.

Horizontal Sync Output

HSOUT (pin 6) produces a negative-polarity horizontal sync signal, or HSync, extracted from the input signal. For bi-level and tri-level sync signals, HSync's negative-going leading edge is derived from the input's sync reference, O_H, with a propagation delay.

Important: The HSync output has good performance on its negative-going leading edge, so it should be used as the reference to a negative-edge triggered PLL input. If HSync is used as the reference to a positive-edge triggered PLL input, like in some FPGAs, the signal must be inverted first to produce a positive-polarity HSync signal (i.e.: positive-going leading edge) before the PLL input. HSync's trailing edge **should not** be used as the reference to a PLL because for a NTSC/PAL input, the input's half-width pulses ($½T_{SYNC}$) in the vertical interval cause the trailing edges of the HSync output to occur earlier than for the normal-width sync pulses (T_{SYNC}). This bi-modal timing variation on HSync's trailing edge, as shown in Figure 13, could affect the performance of the PLL. The bi-modal trailing edge timing also occurs on the CSync output as well.

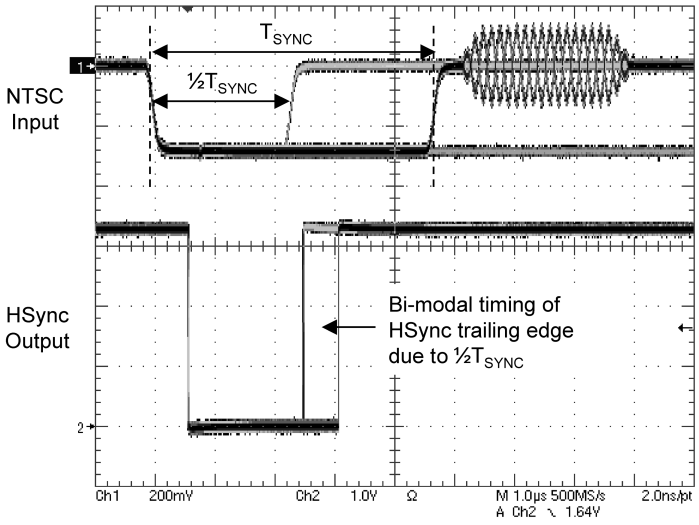


Figure 13. Bi-modal Timing on HSync's Trailing Edge for Half-Width Pulses for NTSC

Vertical Sync Output

VSOUT (pin 7) produces a negative-polarity vertical sync signal, or VSync. VSync's negative-going leading edge is derived from the first vertical serration pulse with a propagation delay, and its output pulse width, T_{VSOUT}, spans approximately three horizontal periods (3H). When there is no vertical serration pulses (i.e.: non-standard video signal), the LMH1980 will output a default VSync pulse derived from the input's vertical sync leading edge with a propagation delay.

Composite Sync Output

CSOUT (pin 8) simply reproduces the video input sync pulses below the video blanking level. This is obtained by clamping the video signal sync tip to the internal clamp voltage at V_{IN} and extracting the resultant composite sync signal, or CSync. For both bi-level and tri-level syncs, CSync's negative-going leading edge is derived from the input's negative-going leading edge with a propagation delay.

Burst/Back Porch Timing Output

BPOUT (pin 9) provides a negative-polarity burst/back porch signal, which is pulsed low for a fixed width during the back porch interval following the input's sync pulse. The burst/back porch timing pulse is useful as a burst gate signal for NTSC/PAL color burst synchronization and as a clamp signal for black level clamping (DC restoration) and sync stripping applications.

For SDTV formats, the back porch pulse's negative-going leading edge is derived from the input's positive-going sync edge with a propagation delay, and the pulse width spans an appropriate duration of the color burst envelope for NTSC/PAL. For EDTV formats, the back porch pulse behaves similar to the SDTV case except with a narrow pulse width. For HDTV formats, the pulse's leading edge is derived from the input's negative-going trailing sync edge with a propagation delay, and the pulse width is narrow to correspond with the short back porch durations. During the vertical sync period, the back porch output will be muted (no pulses) and remain logic high.

Odd/Even Field Output

OEOUT (pin 10) provides an odd/even field output signal, which facilitates identification of odd and even fields for interlaced or segmented frame (sF) formats. For interlaced or segmented frame formats, the odd/even output is logic high during an odd field (field 1) and logic low during an even field (field 2). The odd/even output edge transitions align with VSync's leading edge to designate the start of odd and even fields. For progressive (non-interlaced) video formats, the output is held constantly at logic high.

HD Detect Flag Output

$\overline{HD}$ (pin 5) is an active-low flag output that only outputs a logic low signal when a valid HD video input (i.e.: 720P, 1080I and 1080P) with tri-level sync is detected; otherwise, it will output logic high. Note that there is a processing delay (within 1 to 2 video fields) from when an HD video signal is applied to when the outputs are correct and the $\overline{HD}$ flag changes from logic high (default) to logic low, to indicate a valid HD input has been detected.

The $\overline{HD}$ flag can be used to disable an external switch-controlled SD chroma filter when HD video is detected and conversely, enable it when SD video is detected. This is important because a non-switched chroma filter attenuates signal components above 500 kHz to 3 MHz, which could roll-off and/or attenuate the high bandwidth HD tri-level sync signal prior to the LMH1980 and may increase output propagation delay and jitter. SeeInput Filtering for more information.

ADDITIONAL CONSIDERATIONS

Using an AC-Coupled Video Source into the LMH1980

An AC coupled video source typically has a 100 µF or larger output coupling capacitor (C_{OUT}) for protection and to remove the DC bias of the amplifier output from the video signal. When the video source is load terminated, the average value of the video signal will shift dynamically as the video duty cycle varies due to the averaging effect of the C_{OUT} and termination resistors. The average picture level or APL of the video content is closely related to the duty cycle.

For example, a significant decrease in APL such as a white-to-black field transition will cause a positive-going shift in the sync tips characterized by the source's RC time constant, $t_{RC\text{-}OUT}$ (150Ω*C_{OUT}). The LMH1980's input clamp circuitry may have difficulty stabilizing the input signal under this type of shifting; consequently, the unstable signal at V_{IN} may cause missing sync output pulses to result, **unless** a proper value for C_{IN} is chosen.

To avoid this potential problem when interfacing AC-coupled sources to the LMH1980, it's necessary to introduce a voltage droop component via C_{IN} to compensate for video signal shifting related to changes in the APL. This can be accomplished by selecting C_{IN} such that the effective time constant of the LMH1980's input circuit, $t_{RC\text{-}IN}$, is less than $t_{RC\text{-}OUT}$.

The effective time constant of the input circuit can be approximated as: $t_{RC\text{-}IN} = (R_S+R_I)*C_{IN}*T_{LINE}/T_{CLAMP}$, where R_S = 150Ω, R_I = 1 kΩ (input resistance when clamping), T_{LINE} ~ 64 µs for NTSC, and T_{CLAMP} = 250 ns (internal clamp duration). A white-to-black field transition in NTSC video through C_{OUT} will exhibit the maximum sync tip shifting due to its long line period (T_{LINE}). By setting $t_{RC\text{-}IN} < t_{RC\text{-}OUT}$, the maximum value of C_{IN} can be calculated to ensure proper operation under this worst-case condition.

For instance, $t_{RC\text{-}OUT}$ is about 33 ms for C_{OUT} = 220 µF. To ensure $t_{RC\text{-}IN}$ < 33 ms, C_{IN} must be about 100 nF or less. By choosing C_{IN} = 47 nF, the LMH1980 will function properly with AC-coupled video sources using $C_{OUT} \geq$ 220 µF.

PCB LAYOUT CONSIDERATIONS

Please refer to the "LMH1980 Evaluation Board Instruction Manual" Application Note (AN-1618 [SNLA096]) for a good PCB layout example, which adheres to the following suggestions for component placement and signal routing.

LMH1980 IC Placement

The LMH1980 should be placed such that critical signal paths are short and direct to minimize PCB parasitics from degrading the video input and logic output signals.

Ground Plane

A two-layer, FR-4 PCB is sufficient for this device. One of the PCB layers should be dedicated to a single, solid ground plane that connects to the GND pin of the device and connects to other components, serving as the common ground reference. It also helps to reduce trace inductances and minimize ground loops. Routing supply and signal traces on another layer can help to maintain as much ground plane continuity as possible.

Power Supply Routing

The power supply pin should be connected using short traces with minimal inductance. When routing the supply traces, try not to disrupt the solid ground plane.

For high frequency bypassing, place 0.1 µF and 0.01 µF SMD ceramic bypass capacitors with very short connections to V_{CC} and GND pins. Place a 4.7 or 10 µF SMD tantalum bypass capacitor nearby the V_{CC} for low frequency supply bypassing.

R_{EXT} Resistor

The R_{EXT} resistor should be a 10 kΩ 1% SMD precision resistor. Place R_{EXT} as close as possible to the device and connect to pin 1 and the ground plane using the shortest possible connections. All input and output signals should be kept as far as possible from this pin to prevent unwanted signals from coupling into this bias reference pin.

Video Input

The input signal path should be routed using short, direct traces between video source and input pin. Use a 75Ω load termination on the board, if not on the cable. If applicable, the chroma filter components should be connected using short traces and the filter capacitor should be connected to the ground plane. There should be a sufficient return path from the LMH1980 back to the input source via the ground plane.

Output Routing

The output signal paths should be routed using short, direct traces to minimize parasitic effects that may degrade these high-speed logic signals. The logic outputs do not have high output drive capability. Each output should have a resistive load of about 10kΩ or more and capacitive load of about 10pF including parasitic capacitances for optimal signal quality. Each output can be protected against brief short-circuit events using a small series resistor, like 100Ω, to limit output current.

REVISION HISTORY

Changes from Original (March 2013) to Revision A	Page
• Changed layout of National Data Sheet to TI format	16

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH1980MM/NOPB	ACTIVE	VSSOP	DGS	10	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	AL4A	Samples
LMH1980MMX/NOPB	ACTIVE	VSSOP	DGS	10	3500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	AL4A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

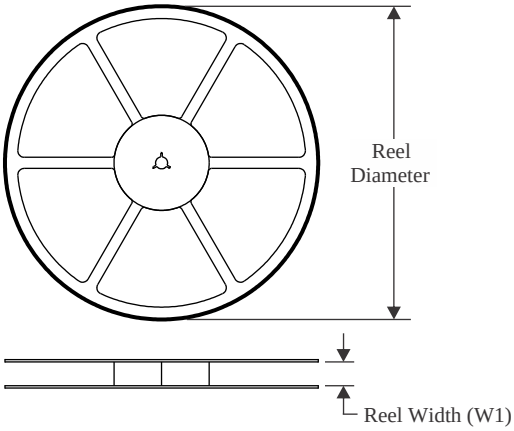
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

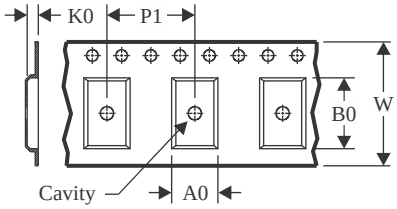
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

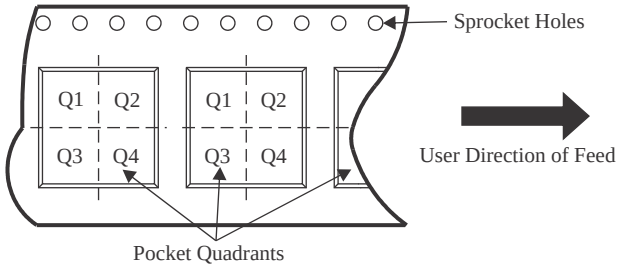


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

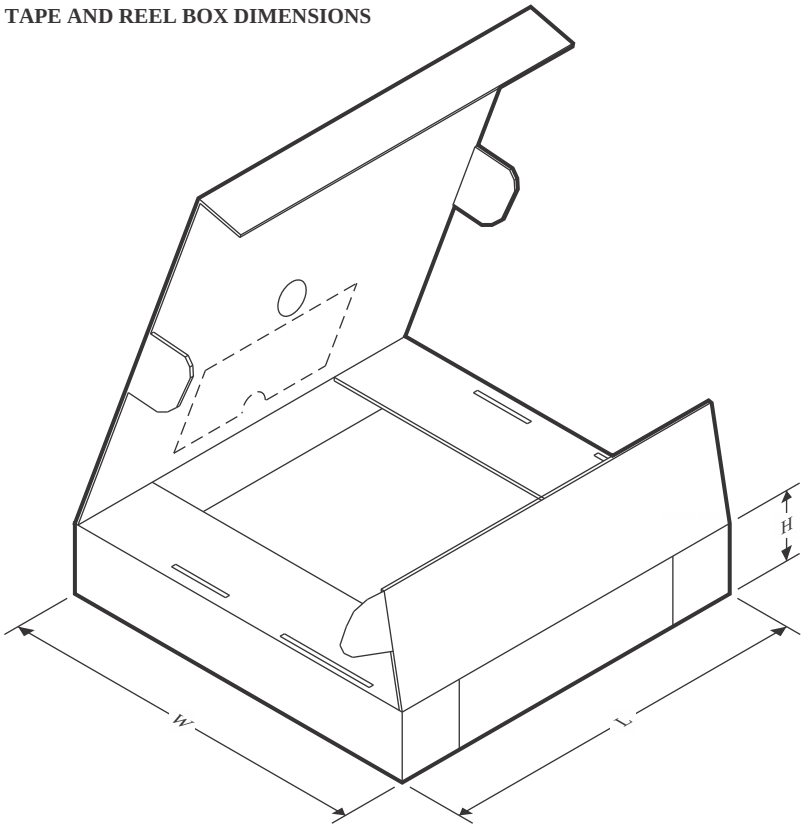
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH1980MM/NOPB	VSSOP	DGS	10	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMH1980MMX/NOPB	VSSOP	DGS	10	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

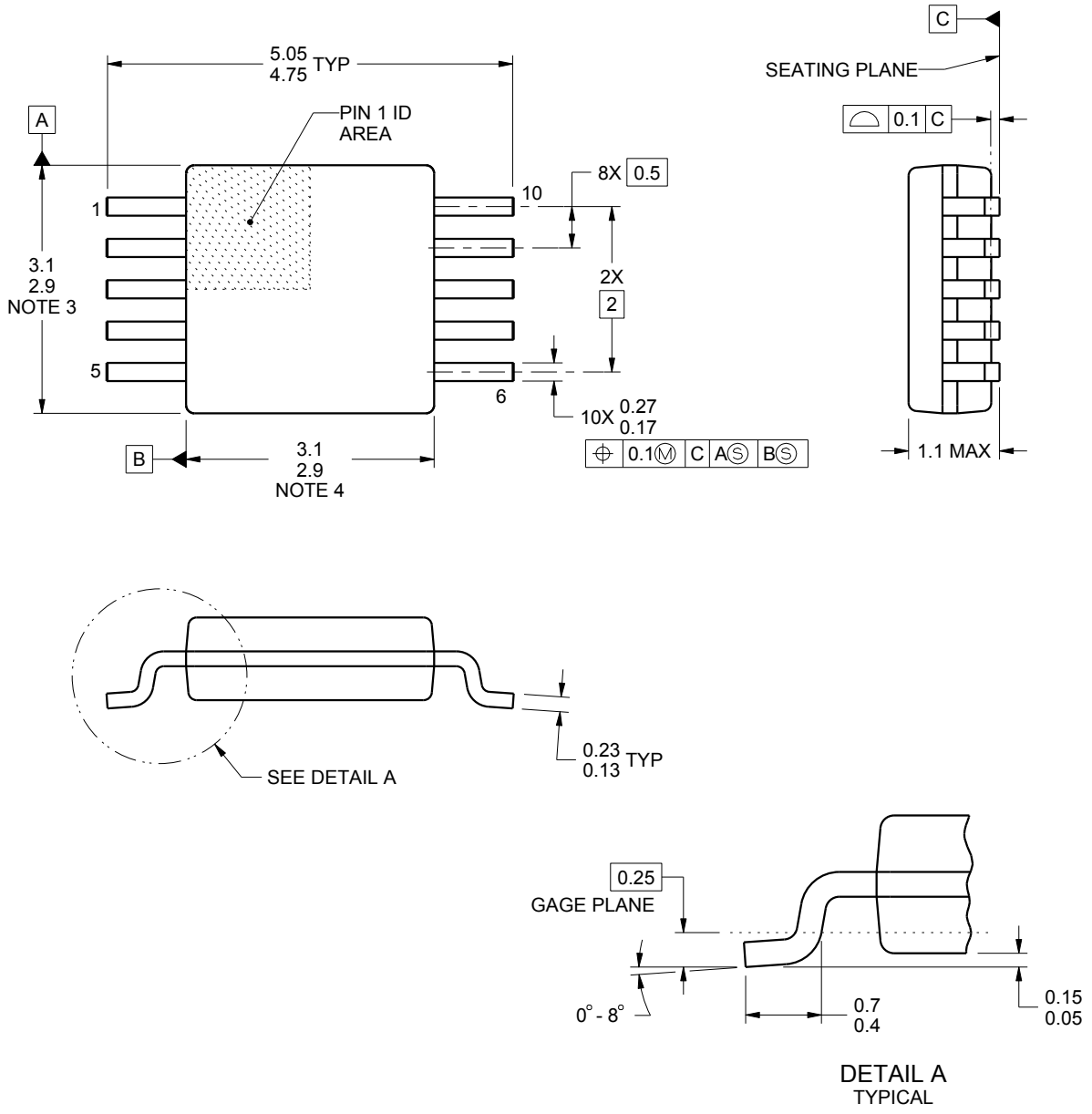
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH1980MM/NOPB	VSSOP	DGS	10	1000	208.0	191.0	35.0
LMH1980MMX/NOPB	VSSOP	DGS	10	3500	367.0	367.0	35.0

PACKAGE OUTLINE

DGS0010A

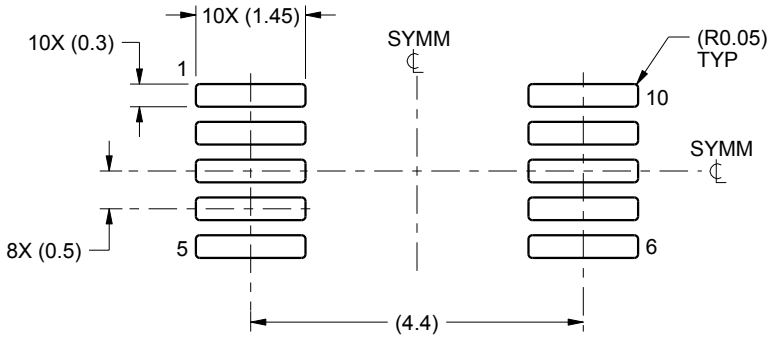
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

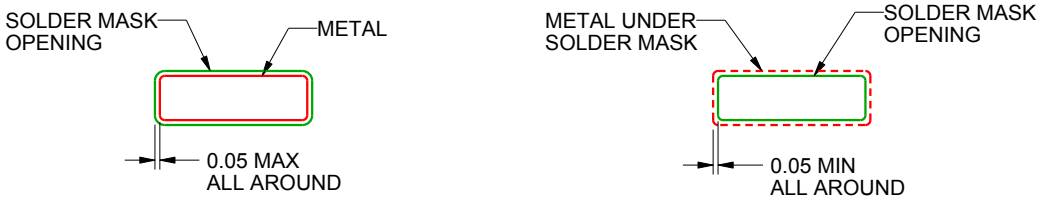


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

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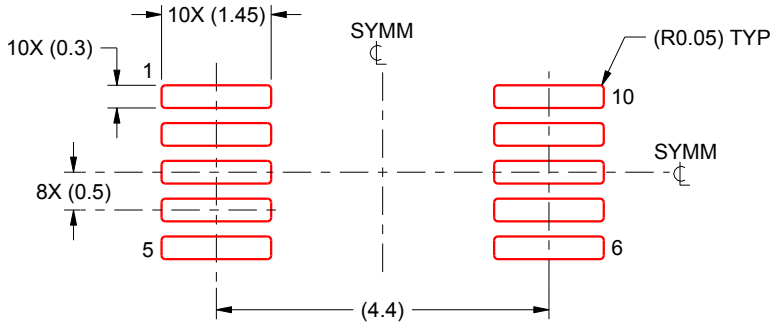
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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