PCM2912A Audio Codec With USB Interface, Mono Microphone Input and Stereo Headphone Output

1 Features

- On-Chip USB Interface:
  - With Full-Speed Transceivers
  - Fully Compliant With USB 2.0 Specification
  - Certified By USB-IF
  - Partially Programmable Descriptors
  - Adaptive Isochronous Transfer for Playback
  - Asynchronous-Isochronous Transfer for Record
  - Bus Powered
- 16-Bit Delta-Sigma ADC and DAC
- Sampling Rate:
  - 8, 11.025, 16, 22.05, 32, 44.1, or 48 kHz
- On-Chip Clock Generator:
  - With Single 6-MHz Clock Source
- Mono ADC with Microphone Input
  - Analog Performance at V_{BUS} = 5 V:
    - THD+N: 0.01%
    - SNR: 92 dB
    - Dynamic Range: 90 dB
  - Decimation Digital Filter
    - Passband Ripple: ±0.05 dB
    - Stop-Band Attenuation: –65 dB
  - Single-Ended Voltage Input
  - Antialiasing Filter Included
  - Digital HPF Included
  - Microphone Bias, Microphone Amplifier, and Input PGA
- Stereo DAC With Headphone Output
  - Analog Performance at V_{BUS} = 5.0 V:
    - THD+N: 0.01% (R_L > 10 kΩ)
    - THD+N: 0.02% (R_L = 32 Ω)
    - SNR: 92 dB
    - Dynamic Range: 90 dB
    - PO: 13 mW (R_L = 32 Ω)
    - PO: 25 mW (R_L = 16 Ω)
  - Oversampling Digital Filter
    - Passband Ripple: ±0.1 dB
    - Stop-Band Attenuation: –43 dB
    - Single-Ended Voltage Output
    - Analog LPF Included
    - Sidetone PGA, Output PGA, and HP Amplifier
- Multifunctions:
  - Suspend, Playback, and Record Status Flag
  - Microphone Amplifier, Mute, and Gain Control
- Pop/Click Noise-Free
- Single Power-Supply: 5 V Typical (V_{BUS})
- Package: 32-Pin TQFP

2 Applications

- USB Headset
- USB Headphone
- USB Speaker
- USB Featured Consumer Audio Product
- USB Audio Interface Box
- USB Monitor
- Video Conference System

3 Description

The PCM2912A is the Texas Instruments single-chip, USB stereo audio codec with a USB, 2.0-compliant, full-speed protocol controller and an analog front-end (AFE) function for headset applications.

The USB protocol controller works with no software code, but USB descriptors can be modified on request. The PCM2912A employs SpAct™ architecture, TI's unique system that recovers the audio clock from USB packet data. On-chip analog PLLs with SpAct enables independent playback and record sampling rates with low clock jitters.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
PCM2912A	TQFP (32)	7.00 mm × 7.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Block Diagram

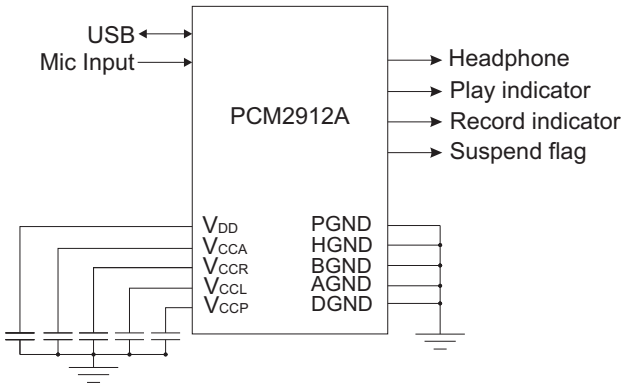


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

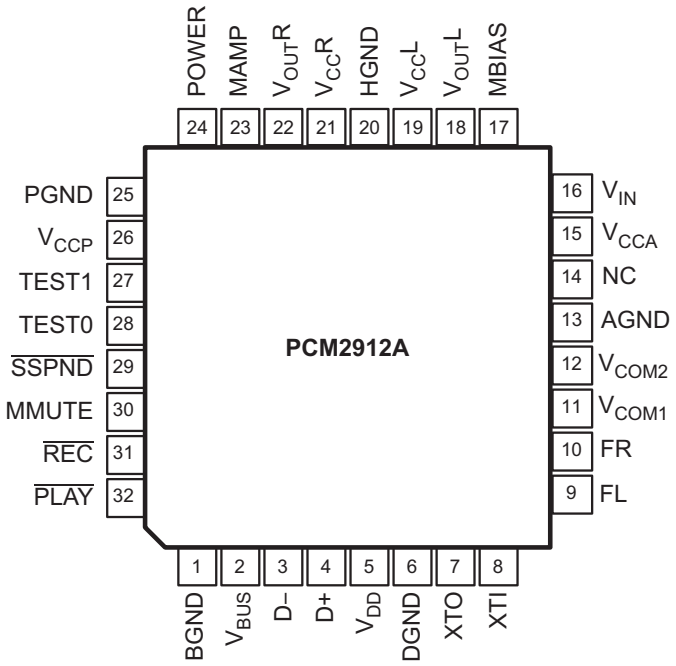
Changes from Original (September 2008) to Revision A	Page
• Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, *Device Comparison* table, and *Mechanical, Packaging, and Orderable Information* section	1

5 Device Comparison Table

FEATURE	PCM2900C	PCM2902C	PCM2903C	PCM2906C	PCM2912A
Supply voltage	5 V (Bus-Powered)	5 V (Bus-Powered)	3.3 V (Bus-Powered)	5 V (Bus-Powered)	5 V (Bus-Powered)
Additional features	—	S/PDIF I/O	S/PDIF I/O	S/PDIF I/O 500-mA Maximum Power Configuration	Mic Bias PGAs Sidetone

6 Pin Configuration and Functions

PJT Package
32-Pin TQFP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AGND	13	—	Analog ground
BGND	1	—	Reference for internal regulator
D–	3	I/O	USB differential input/output minus (1)
D+	4	I/O	USB differential input/output plus (1)
DGND	6		Digital ground
FL	9	—	External filter pin of L-channel (optional)
FR	10	—	External filter pin of R-channel (optional)
HGND	20	—	Analog ground for headphone amplifier
MAMP	23	I	Microphone preamplifier gain control (LOW: Preamplifier off, HIGH: Preamplifier on = +20 dB) (2)
MBIAS	17	O	Microphone bias output (0.75 V_{CCA})
MMUTE	30	I	Microphone mute control, active HIGH (LOW: Mute off, HIGH: Mute on) (3)
NC	14	—	Not connected

(1) LV-TTL level
(2) 3.3-V CMOS level input.
(3) 3.3-V CMOS level input with internal pulldown resistor.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
PGND	25	—	Analog ground for microphone bias, microphone amplifier, and PGA
$\overline{\text{PLAY}}$	32	O	Status output for playback (LOW: Playback, FLASH: Mute on playback, HIGH: Stop)(4)
POWER	24	I	Power consumption declaration select pin (LOW: 100 mA, HIGH: 500 mA) (2)
$\overline{\text{REC}}$	31	O	Status output for record (LOW: Record, FLASH: Mute on recode, HIGH: Stop)(4)
$\overline{\text{SSPND}}$	29	O	Suspend flag (LOW: Suspend, HIGH: Operational state)
TEST0	28	I	Test pin. Must be set to LOW(2)
TEST1	27	I	Test pin. Must be set to HIGH(2)
V_{BUS}	2	—	Connect to USB power (V_{BUS})
V_{CCA}	15	—	Analog power supply
$V_{CC}L$	19	—	Analog power supply for headphone amplifier of L-channel(5)
V_{CCP}	26	—	Analog power supply for PLL(5)
$V_{CC}R$	21	—	Analog power supply for headphone amplifier of R-channel(5)
V_{COM1}	11	—	Common voltage for ADC, DAC, and analog front-end (V_{CCA}/2). Decoupling capacitor must be connected to AGND.
V_{COM2}	12	—	Common voltage for headphone (V_{CCA}/2). Decoupling capacitor must be connected to AGND.
V_{DD}	5	—	Digital power supply(5)
V_{IN}	16	I	ADC microphone input
$V_{OUT}L$	18	O	Headphone output for L-channel
$V_{OUT}R$	22	O	Headphone output for R-channel
XTI	8	I	Crystal oscillator input(2)
XTO	7	O	Crystal oscillator output

(4) 5-V tolerant, open-drain.
(5) Connect decoupling capacitor to corresponding ground.

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted).(1)(2)

		MIN	MAX	UNIT
Supply voltage	V_{BUS}	–0.3	6.5	V
Ground voltage differences	BGND, PGND, AGND, HGND, DGND	–0.1	0.1	V
Input voltage	V_{CCP}, V_{CCA}, V_{CCL}, V_{CCR}, V_{DD}	–0.3	4	V
Digital input voltage	$\overline{PLAY}$, $\overline{REC}$	–0.3	6.5	V
	D+, D–, XTI, XTO, MMUTE, TEST0, TEST1, POWER, MAMP, $\overline{SSPND}$	–0.3	4	V
Analog input voltage	MBIAS, V_{IN}, V_{COM1}, V_{COM2}, $V_{OUT}L$, $V_{OUT}R$, FR, FL	–0.3	4	V
Input current (any pins except supplies)		–10	10	mA
Ambient temperature under bias		–40	125	°C
Junction temperature			150	
Storage temperature, T_{stg}		–55	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted).

		MIN	NOM	MAX	UNIT
V_{BUS}	Supply voltage	4.35	5	5.25	V
	Analog input voltage, full scale (–0 dB)		0.43 V_{CCA}		V_{PP}
	Digital input logic family		TTL		
	Digital input clock frequency	5.997	6	6.003	MHz
	Analog output load resistance	32			Ω
	Analog output load capacitance			100	pF
	Digital output load capacitance			10	pF
T_A	Operating free-air temperature	–25		70	°C

7.4 Thermal Information

THERMAL METRIC(1)		PCM2912A PJT (TQFP) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	69.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	10.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	34.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	33.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

All specifications at T_A = 25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{IN} = 1 kHz, and 16-bit data, unless otherwise noted. for Host interface, apply USB revision 2.0, full-speed. For audio data format, use UsB isochronous data format.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT LOGIC						
V_{IH}	Input logic high level		2		3.3	VDC
V_{IL}	Input logic low level				0.8	VDC
I_{IH}	Input logic high current(1) (2)	V_{IN} = 3.3 V	–10		10	µA
	Input logic high current(3)	V_{IN} = 3.3 V		65	100	µA
I_{IL}	Input logic low current(1) (2)	V_{IN} = 0 V	–10		10	µA
	Input logic low current(3)	V_{IN} = 0 V	–10		10	µA
OUTPUT LOGIC						
V_{OH}	Output logic high level(1)	I_{OH} = –10 mA	2.9			VDC
	Output logic high level(4)	I_{OH} = –2 mA	2.8			VDC
V_{OL}	Output logic low level(1)	I_{OL} = 10 mA			0.3	VDC
	Output logic low level(4)	I_{OL} = 2 mA			0.5	VDC
	Output logic low level(5)	I_{OL} = 8 mA			0.5	VDC
I_{OH}	Output leak current(5)	V_{IN} = 5 V			±10	µA
CLOCK FREQUENCY						
	Input clock frequency, XTI		5.997	6.000	6.003	MHz
MICROPHONE BIAS						
	Output voltage			0.75 V_{CCA}		VDC
	Output current			2		mA
	Output noise	R_L = 1 kΩ		5		μV_{RMS}
ANALOG-TO-DIGITAL CONVERTER (ADC) CHARACTERISTICS						
	Resolution			16		Bits
	Audio data channel			1		Channel
	Sampling frequency			8 11.025 16 22.05 32 44.1 48		kHz
ADC DYNAMIC PERFORMANCE(6)						
THD+N	Total harmonic distortion plus noise	V_{IN} = –1 dB of 0.43 V_{CCA}		0.01%	0.02%	
	Dynamic range	A-weighted	82	90		dB
SNR	Signal-to-noise ratio	A-weighted	84	92		dB
ADC DC ACCURACY						
	Gain error			±2	±10	% of FSR
	Bipolar zero error			±0		% of FSR
ANALOG INPUT						
	Input voltage			0.43 V_{CCA}		V_{PP}
	Center voltage			0.5 V_{CCA}		V
	Antialiasing filter frequency response	–3 dB		150		kHz
		f_{IN} = 20 kHz		–0.08		dB

(1) Pins 3, 4: D–, D+.
(2) Pins 8, 23, 24, 27, 28: XTI, MAMP, POWER, TEST1, TEST0
(3) Pin 30: MMUTE
(4) Pins 7, 29: XTO, $\overline{\text{SSPND}}$
(5) Pins 31, 32: $\overline{\text{REC}}$, $\overline{\text{PLAY}}$.
(6) f_{IN} = 1 kHz, using Audio Precision™ System Two™, RMS mode with 20-kHz LPF, 400-Hz HPF in calculation. Microphone amplifier = 0 dB, PGA = 0 dB.

Electrical Characteristics (continued)

All specifications at T_A = 25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{IN} = 1 kHz, and 16-bit data, unless otherwise noted. for Host interface, apply USB revision 2.0, full-speed. For audio data format, use UsB isochronous data format.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
MICROPHONE AMPLIFIER						
	Gain		0		20	dB
	Input impedance			20		kΩ
INPUT PGA						
	Gain range		–12		30	dB
	Gain step size			1		dB
ADC DIGITAL FILTER PERFORMANCE						
	Passband				0.454 f_S	Hz
	Stop band		0.583 f_S			Hz
	Passband ripple		–0.02		0.02	dB
	Stop-band attenuation		–65			dB
	Delay time			17.4/f_S		s
	HPF frequency response	–3 dB		0.078 f_S/1000		Hz
DIGITAL-TO-ANALOG CONVERTER (DAC) CHARACTERISTICS						
	Resolution			16		Bits
	Audio data channel			1, 2		Channel
	Sampling frequency			8 11.025 16 22.05 32 44.1 48		kHz
DAC DYNAMIC PERFORMANCE(7)						
THD+N	Total harmonic distortion plus noise	R_L > 10 kΩ, V_{OUT} = 0 dB of 0.6 V_{CCA}		0.01%	0.02%	
		R_L = 32 Ω, V_{OUT} = 0 dB of 0.55 V_{CCA}		0.02%	0.05%	
	Dynamic range	EIAJ, A-weighted	82	90		dB
SNR	Signal-to-noise ratio	EIAJ, A-weighted	84	92		dB
	Channel separation	R_L > 10 kΩ	80	88		dB
DAC DC ACCURACY						
	Gain mismatch channel-to-channel		–10	±2	10	% of FSR
	Gain error		–10	±2	10	% of FSR
	Bipolar zero error			±3		% of FSR
ANALOG OUTPUT						
	Output voltage	R_L > 10 kΩ		0.6 V_{CCA}		V_{PP}
		R_L = 32 Ω		0.55 V_{CCA}		
	Center voltage			0.5 V_{CCA}		V
	Output power	R_L = 32 Ω		13		mW
		R_L = 16 Ω		25		
	Load impedance (AC coupling)	Line	10			kΩ
		Headphone	16	32		Ω
	LPF frequency response	–3 dB		140		kHz
		f = 20 kHz		–0.1		dB

(7) f_{OUT} = 1 kHz, using Audio Precision System Two, RMS mode with 20-kHz LPF, 400-Hz HPF. Output attenuator = 0 dB, Sidetone = Mute.

Electrical Characteristics (continued)

All specifications at T_A = 25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{IN} = 1 kHz, and 16-bit data, unless otherwise noted. for Host interface, apply USB revision 2.0, full-speed. For audio data format, use UsB isochronous data format.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SIDETONE PROGRAMMABLE ATTENUATOR						
	Gain range		–76		0	dB
	Gain step size			1		dB
OUTPUT PROGRAMMABLE ATTENUATOR						
	Gain range		–76		0	dB
	Gain step size			1		dB
ANALOG LOOPBACK PERFORMANCE(8)						
THD+N	Total harmonic distortion plus noise	R_L > 10 kΩ, V_{IN} = 0 dB of 0.43 V_{CCA}		0.01%	0.02%	
		R_L = 32 Ω, V_{IN} = 0 dB of 0.43 V_{CCA}		0.02%	0.05%	
	Dynamic range	EIAJ, A-weighted	82	90		dB
SNR	Signal-to-noise ratio	EIAJ, A-weighted	84	92		dB
DAC DIGITAL FILTER PERFORMANCE						
	Passband				0.445 f_S	Hz
	Stop band		0.555 f_S			Hz
	Passband ripple				±0.1	dB
	Stop-band attenuation		–43			dB
	Delay time			14.3/f_S		s
POWER-SUPPLY REQUIREMENTS						
V_{BUS}	Voltage range	Bus-powered	4.35	5	5.25	VDC
	Supply current	ADC, DAC operation (R_L = 32 Ω)		85	100	mA
		Suspend mode(9)		220	300	µA
	Power dissipation	ADC, DAC Operation		425	500	mW
		Suspend mode(9)		0.8	1	mW
V_{CCP},V_{CCL} V_{CCR},V_{CCA} V_{DD}	Internally-generated power supply voltage(10)		3	3.3	3.6	VDC
TEMPERATURE RANGE						
	Operation temperature		–25		85	°C

(8) MIC Amp = 0 dB, Sidetone attenuator = 0 dB, Output attenuator = 0 dB.
(9) Under USB suspend state
(10) Pins 5, 15, 19, 21, 26: V_{DD}, V_{CCA}, V_{CCL}, V_{CCR}, V_{CCP}.

7.6 Typical Characteristics

7.6.1 ADC Digital Decimation Filter Frequency Response

All specifications at T_A = 25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{IN} = 1 kHz, and 16-bit data, unless otherwise noted.

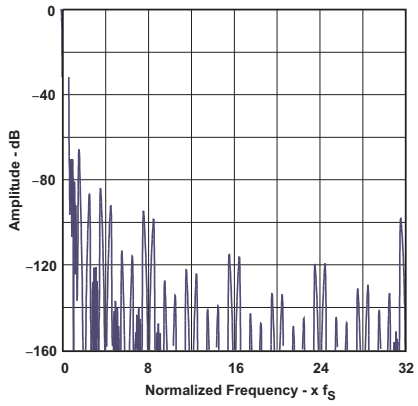


Figure 1. Overall Characteristic

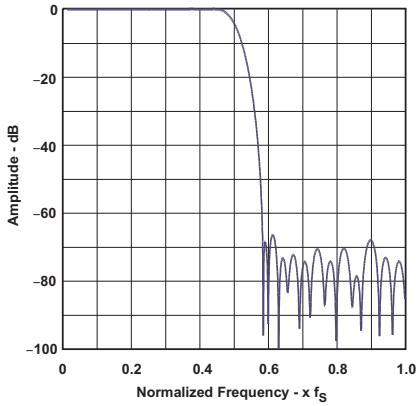


Figure 2. Stop Band Attenuation

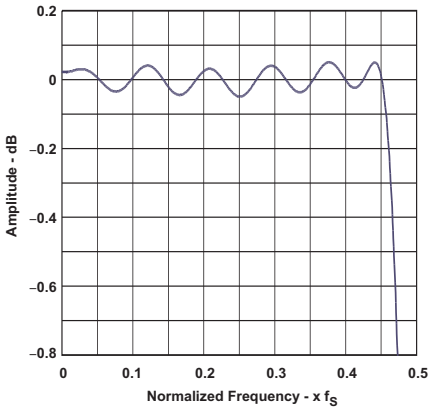


Figure 3. Passband Ripple

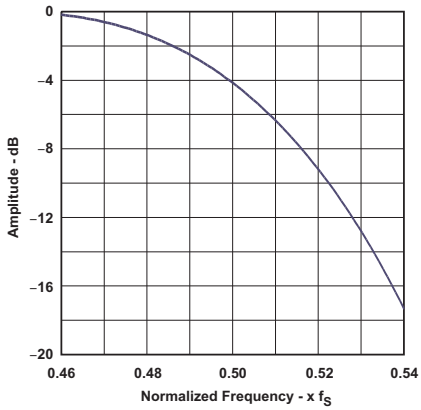


Figure 4. Transient Band Response

7.6.2 ADC Digital High-Pass Filter Frequency Response

All specifications at T_A = 25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{IN} = 1 kHz, and 16-bit data, unless otherwise noted.

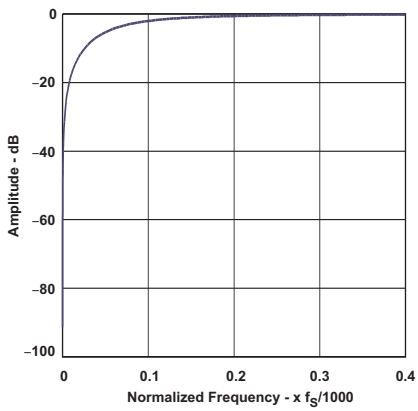


Figure 5. Stop Band Characteristic

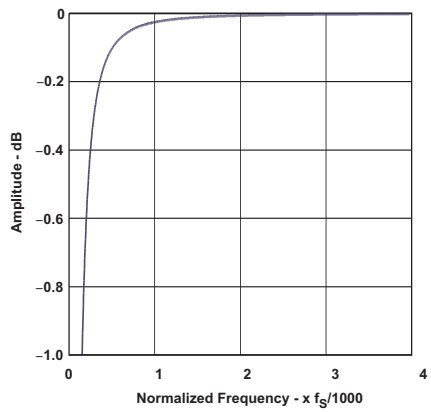


Figure 6. Passband Characteristic

7.6.3 ADC Analog Antialiasing Filter Frequency Response

All specifications at T_A = 25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{IN} = 1 kHz, and 16-bit data, unless otherwise noted.

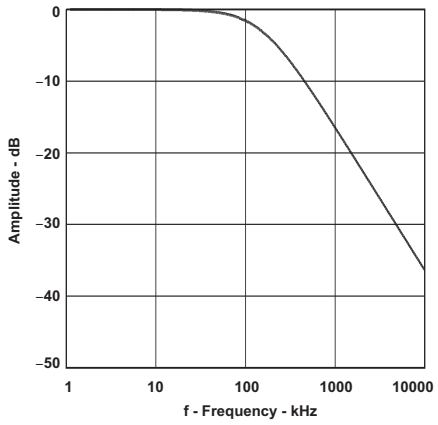


Figure 7. Stop Band Characteristic

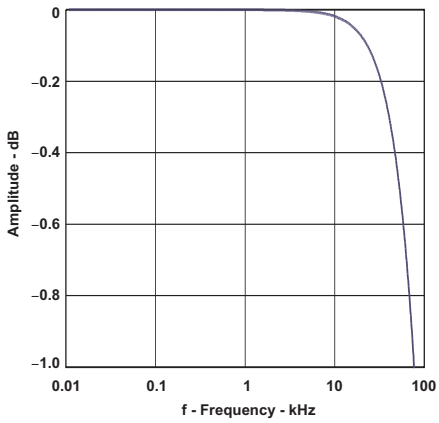


Figure 8. Passband Characteristic

7.6.4 DAC Digital Interpolation Filter Frequency Response

All specifications at T_A = 25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{IN} = 1 kHz, and 16-bit data, unless otherwise noted.

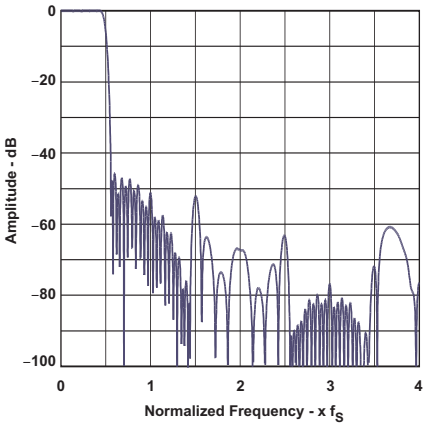


Figure 9. Stop Band Attenuation

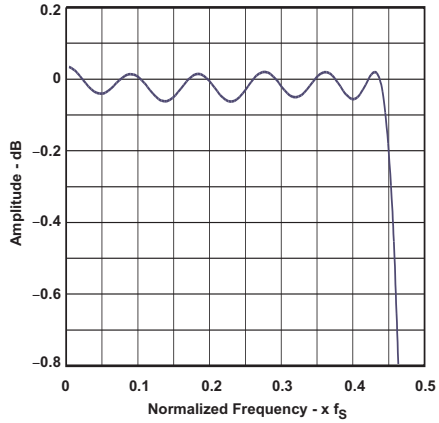


Figure 10. Passband Ripple

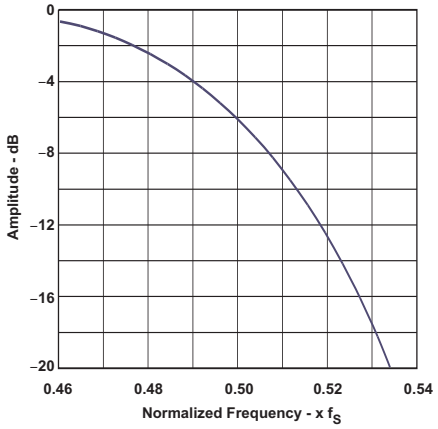


Figure 11. Transient Band Response

7.6.5 DAC Analog FIR Filter Frequency Response

All specifications at T_A = 25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{IN} = 1 kHz, and 16-bit data, unless otherwise noted.

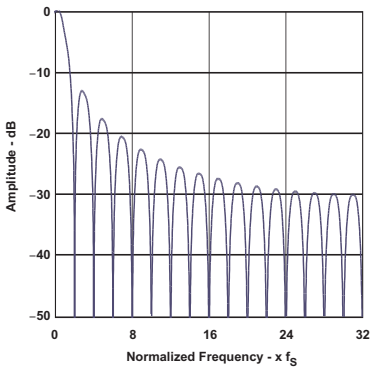


Figure 12. Stop Band Characteristic

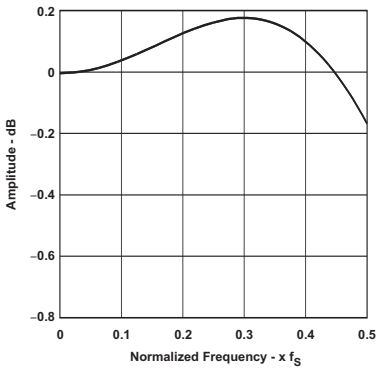


Figure 13. Passband Characteristic

7.6.6 DAC Analog Low-Pass Filter Frequency Response

All specifications at T_A = 25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{IN} = 1 kHz, and 16-bit data, unless otherwise noted.

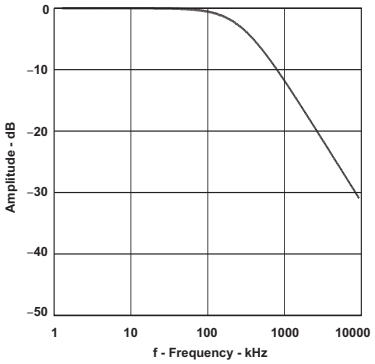


Figure 14. Stop Band Characteristic

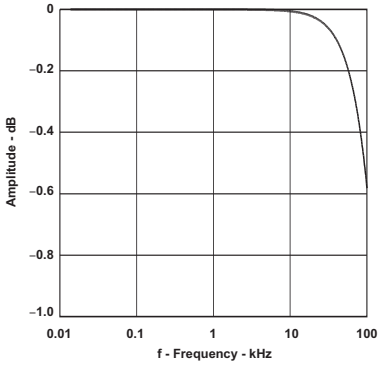


Figure 15. Passband Characteristic

7.6.7 ADC

All specifications at T_A = 25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{IN} = 1 kHz, and 16-bit data, unless otherwise noted.

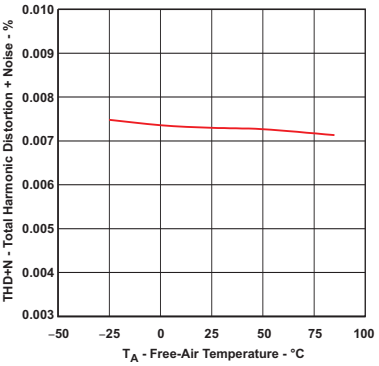


Figure 16. THD+N at –1 dB vs Temperature

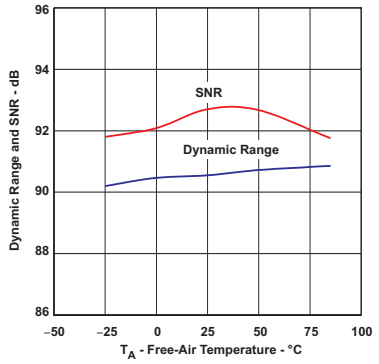


Figure 17. Dynamic Range and Signal-to-Noise Ratio vs Temperature

ADC (continued)

All specifications at T_A = 25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{IN} = 1 kHz, and 16-bit data, unless otherwise noted.

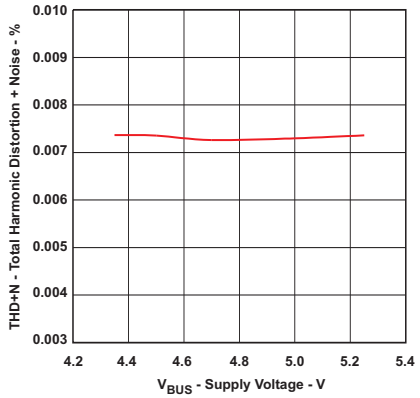


Figure 18. THD+N at –1 dB vs Supply Voltage

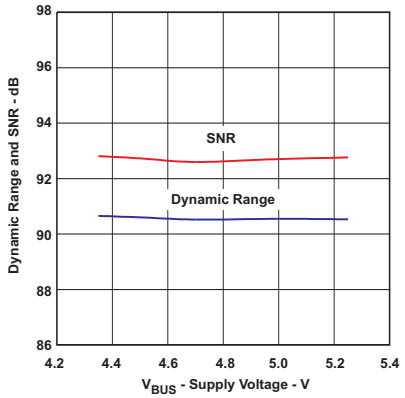


Figure 19. Dynamic Range and Signal-to-Noise Ratio vs Supply Voltage

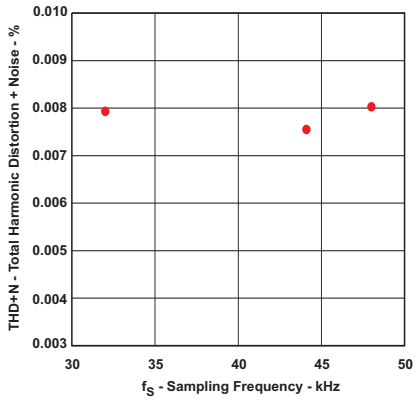


Figure 20. THD+N at –1 dB vs Sampling Frequency

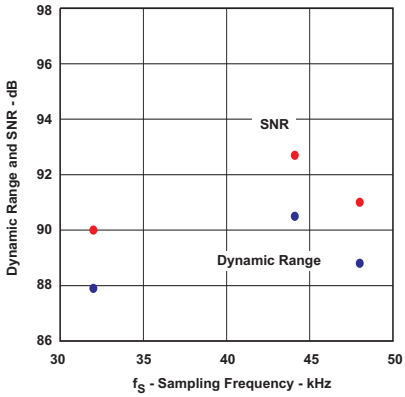


Figure 21. Dynamic Range and Signal-to-Noise Ratio vs Sampling Frequency

7.6.8 DAC

All specifications at T_A = 25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{IN} = 1 kHz, and 16-bit data, unless otherwise noted.

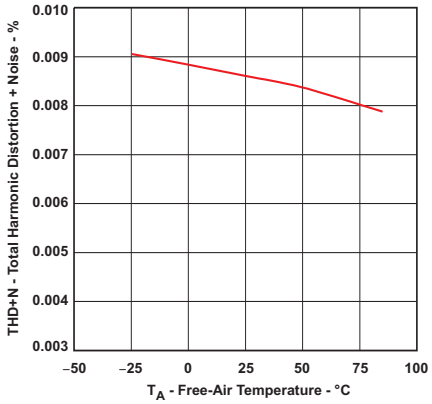


Figure 22. THD+N at 0 dB vs Temperature

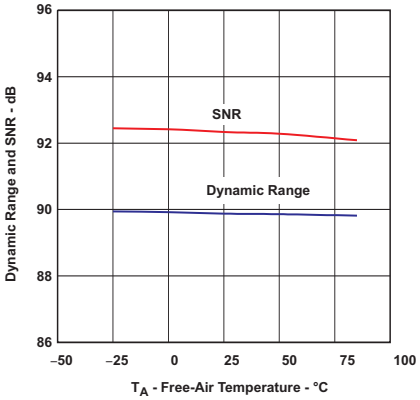


Figure 23. Dynamic Range and Signal-to-Noise Ratio vs Temperature

DAC (continued)

All specifications at T_A = 25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{IN} = 1 kHz, and 16-bit data, unless otherwise noted.

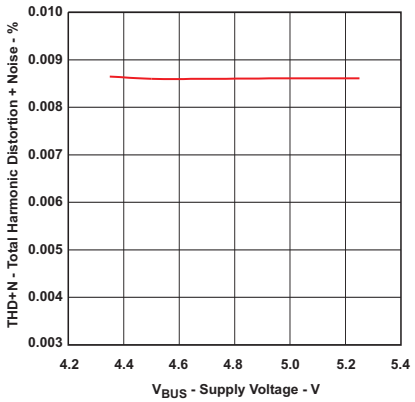


Figure 24. THD+N at 0 dB vs Supply Voltage

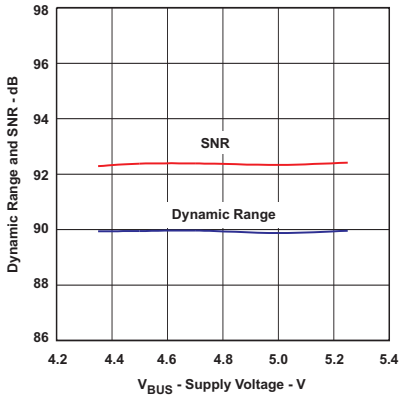


Figure 25. Dynamic Range and Signal-to-Noise Ratio vs Supply Voltage

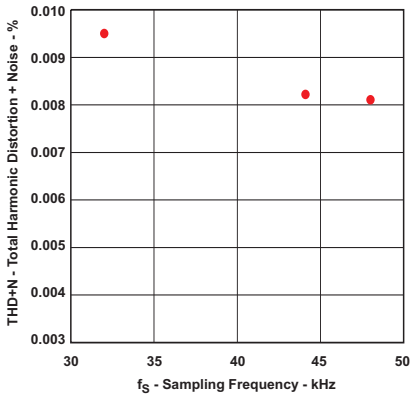


Figure 26. THD+N at 0 dB vs Sampling Frequency

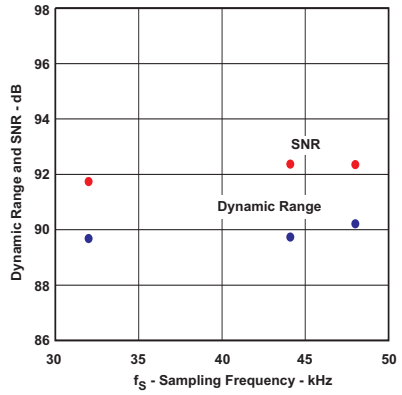


Figure 27. Dynamic Range and Signal-to-Noise Ratio vs Sampling Frequency

7.6.9 Supply Current

All specifications at T_A = 25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{IN} = 1 kHz, and 16-bit data, unless otherwise noted.

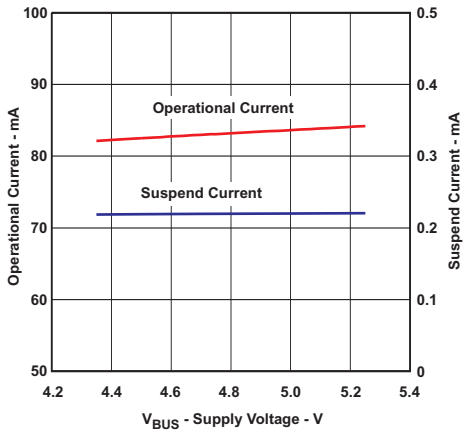


Figure 28. Supply Current vs Supply Voltage

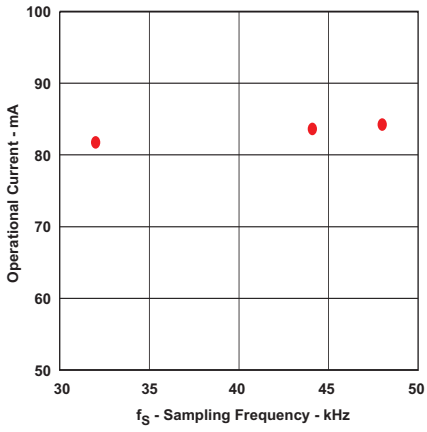


Figure 29. Supply Current vs Sampling Frequency

Supply Current (continued)

All specifications at T_A = 25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{IN} = 1 kHz, and 16-bit data, unless otherwise noted.

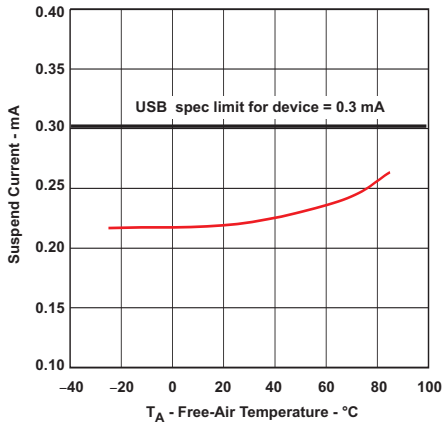


Figure 30. Supply Current vs Temperature at Suspend Mode

8 Parameter Measurement Information

All parameters are measured according to the conditions described in *Specifications*.

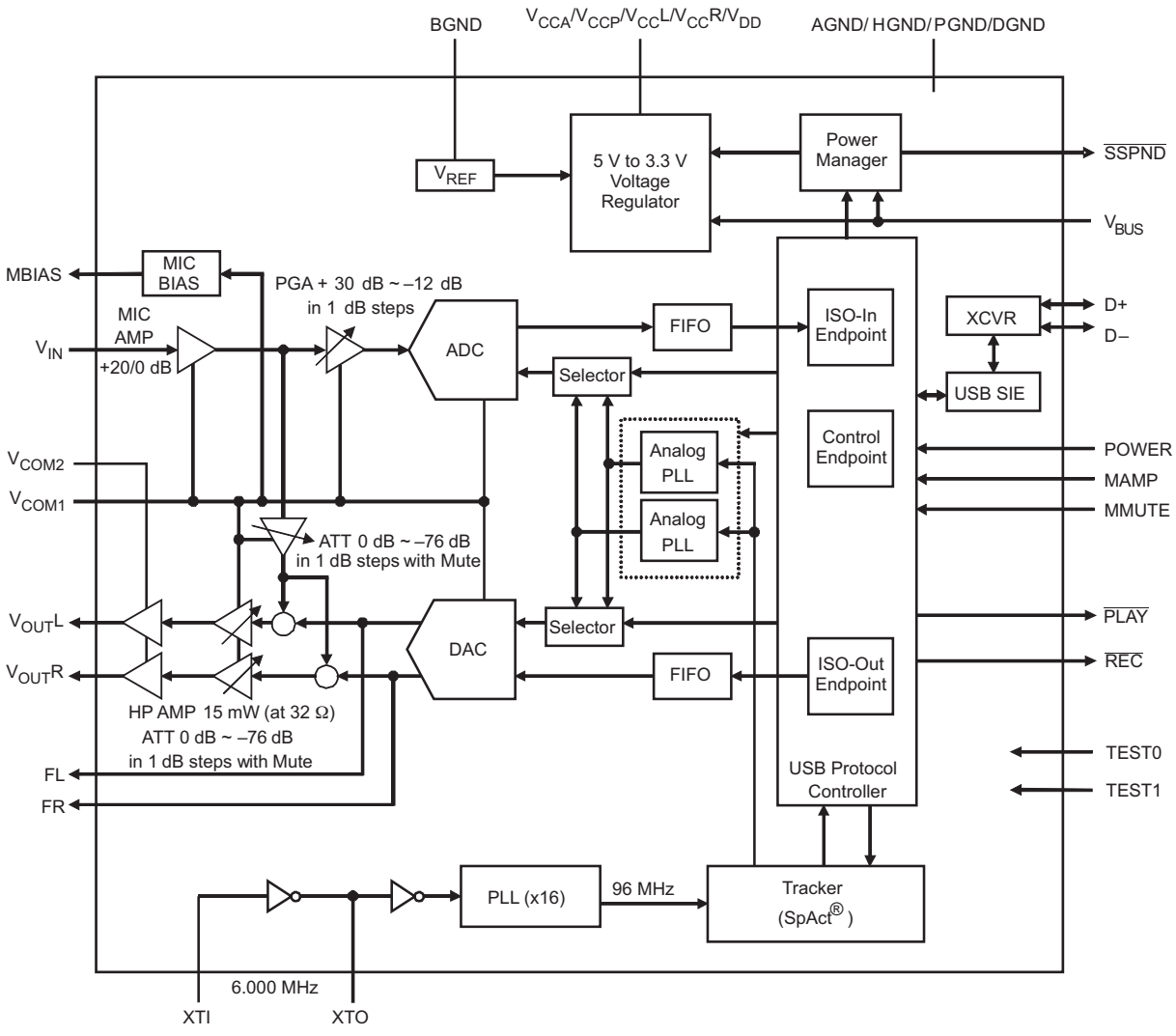
9 Detailed Description

9.1 Overview

The PCM2912A is an audio codec with USB connection capability and an analog front-end for headset applications.

The PCM2912A is a bus-powered device that uses the USB voltage source. The PCM2912A meets the requirements of USB2.0 standard connection. This device has analog and digital inputs and outputs; it has a digital USB interface for input and output data; the analog input is directly routed to the A/D converter and to the analog output. The microphone input has an optional mic amp with fixed +20 dB. The PCM2912A has 2 digital output flags that can be used as LED indicators for Playback and Record. The PCM2912A requires a 12-MHz clock; it can be provided by an external clock or generated by a built-in crystal resonator.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Clock and Reset

The PCM2912A requires a 6-MHz (±500 ppm) clock for USB function and audio function, which can be generated from a built-in crystal oscillator with a 6-MHz crystal resonator. The 6-MHz crystal resonator must be connected to XTI (pin 8) and XTO (pin 7) with one high (1-MΩ) resistor and two small capacitors, whose capacitance depends on the load capacitance of the crystal resonator. An external clock can be supplied through XTI; if an external clock is supplied, XTO must be left open. Because there is no clock disabling signal, using the external clock supply is not recommended. $\overline{\text{SSPND}}$ (pin 29) is unable to use clock disabling.

The PCM2912A has an internal power-on-reset circuit, which works automatically when V_{BUS} (pin 2) exceeds 2.5 V, typical (2.2 V to 2.7 V), and approximately 700 µs is required until the internal reset is released.

9.3.2 DAC

The PCM2912A has a stereo delta-sigma DAC that uses a 64-f_S oversampling technique with an 8-f_S oversampling digital filter. DAC outputs are provided through the headphone amplifier; $V_{OUT}L$ (pin 18) and $V_{OUT}R$ (pin 22) provide 13 mW at 32 Ω and 0.6 $V_{CC}L/V_{CC}R$ V_{PP} at a 10-kΩ load.

9.3.3 ADC

The PCM2912A has a mono delta-sigma ADC that uses a 64-f_S oversampling technique with a 1/64-f_S decimation digital filter. The microphone input, V_{IN} (pin 16), is fed to the ADC through a +20-dB microphone amplifier and the PGA, which has +30 dB to –12 dB in 1-dB steps.

9.3.4 Microphone Bias

The PCM2912A has a microphone bias generator, which provides a low-noise, 0.75-V_{CCA}, 2-mA source current output with appropriate output impedance for electret-microphone driving. This output, MBIAS (pin 17), should be bypassed to AGND (pin 13) through an appropriate capacitor to reduce the output noise level.

9.3.5 Microphone Amplifier

The PCM2912A has a low-noise, single-ended, mono microphone amplifier with a mute function that is controlled by MUTE (pin 30). The signal gain is selectable by MAMP (pin 23). The noise level at the input node is 5 μV_{RMS}, and the input impedance is 20 kΩ.

9.3.6 Input PGA

The PCM2912A also has a low-noise input, programmable gain amplifier (PGA) for the microphone amplifier output/ADC input, with a gain range of +30 dB to –12 dB in 1dB/step.

9.3.7 Sidetone Programmable Attenuator

The PCM2912A has a low-noise, sidetone programmable attenuator with a mute function for the sidetone signal path (microphone amplifier output to output PGA input), and a gain range of 0 dB to –76 dB in 1 dB/step.

9.3.8 Output Programmable Attenuator

The PCM2912A has a low-noise output programmable attenuator with a mute function for mixed signal, which affects DAC output signal and sidetone signal. The output PGA gain range is 0 dB to –76 dB in 1 dB/step.

9.3.9 V_{COM1} and V_{CCM2}

V_{COM2} (pin 12) is provided for the center voltage of the headphone amplifier. V_{COM1} (pin 11) is provided for the center voltage of all other analog circuits. Each V_{COM} pin must be decoupled with an appropriate capacitor. Because the headphone output is disconnected when entering the suspend state, determining the capacitance is important to prevent pop noise, especially for V_{COM2} (pin 12). The equivalent resistance of V_{COM2} is 500 kΩ, and V_{COM1} is 15 kΩ.

Feature Description (continued)

9.3.10 Filter Pins

FL (pin 9) and FR (pin 10) are provided to make a low-pass filter (LPF) to decrease the DAC outband noise, as shown in Figure 31. This filter is optional.

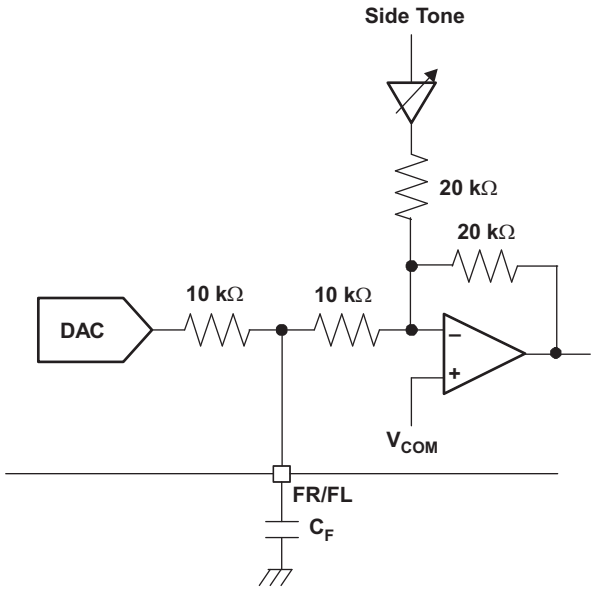


Figure 31. Filter Circuit

9.3.11 Interface Sequence

9.3.11.1 Power-On, Attach, and Play Back Sequence

The PCM2912A is ready for setup when the reset sequence has finished and the USB bus is attached. After a connection has been established, the PCM2912A is ready to accept USB audio data. While waiting for the audio data (that is, in an idle state), the analog output is set to bipolar zero (BPZ).

When receiving the audio data, the PCM2912A stores the first audio packet, which contains 1-ms audio data, into the internal storage buffer. The PCM2912A starts playing the audio data when the subsequent Start of Frame (SOF) packet is detected, as shown in Figure 32.

Feature Description (continued)

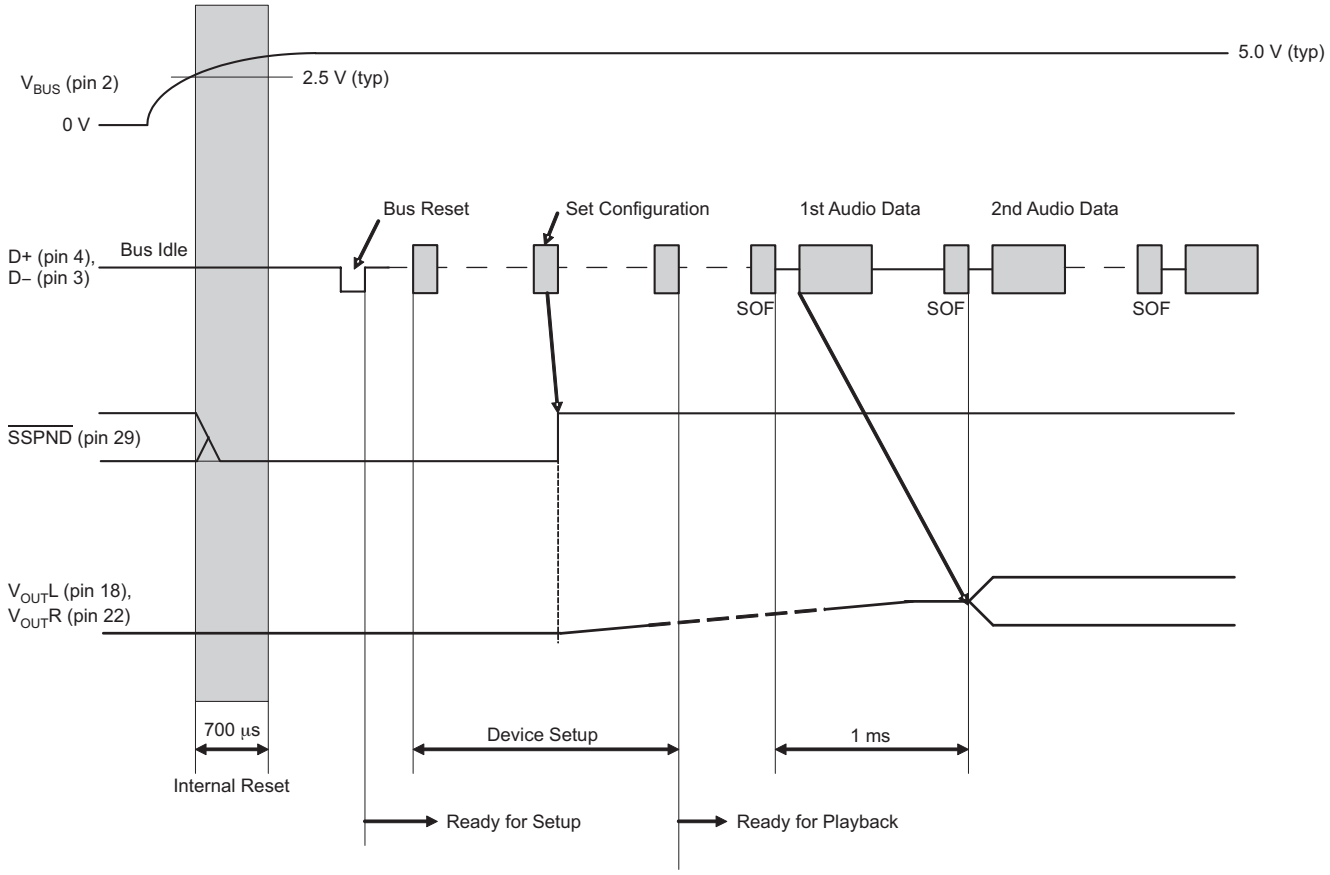


Figure 32. Initial Sequence

9.3.11.2 Play, Stop, and Detach Sequence

When the host finishes or aborts the play back process, the PCM2912A stops playing after last audio data has played, as shown in Figure 33.

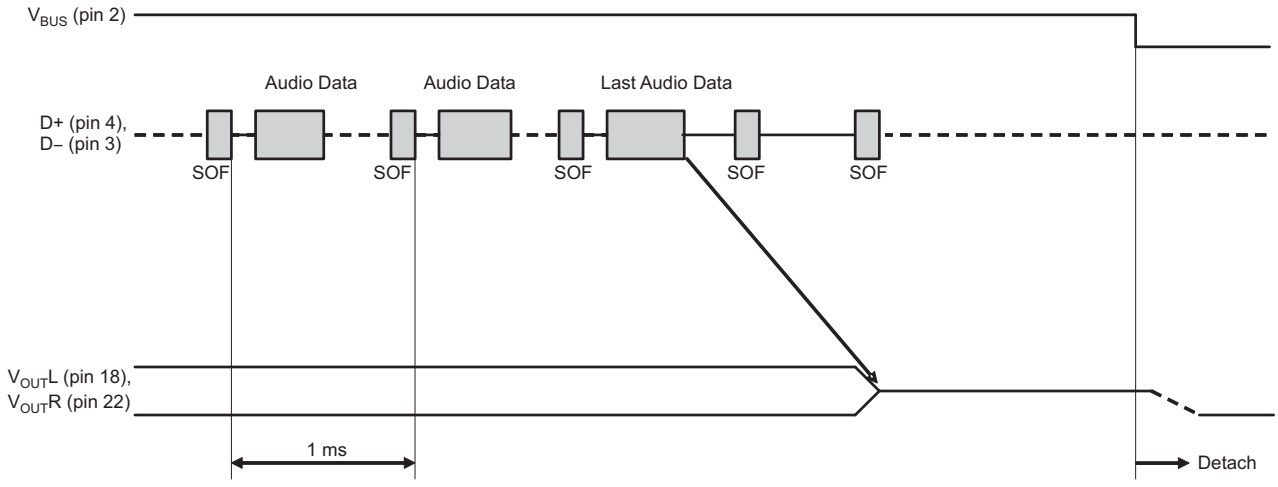


Figure 33. Play, Stop, and Detach

Feature Description (continued)

9.3.11.3 Record Sequence

Figure 34 illustrates how the PCM2912A records the audio into the internal memory after receiving the SET_INTERFACE command.

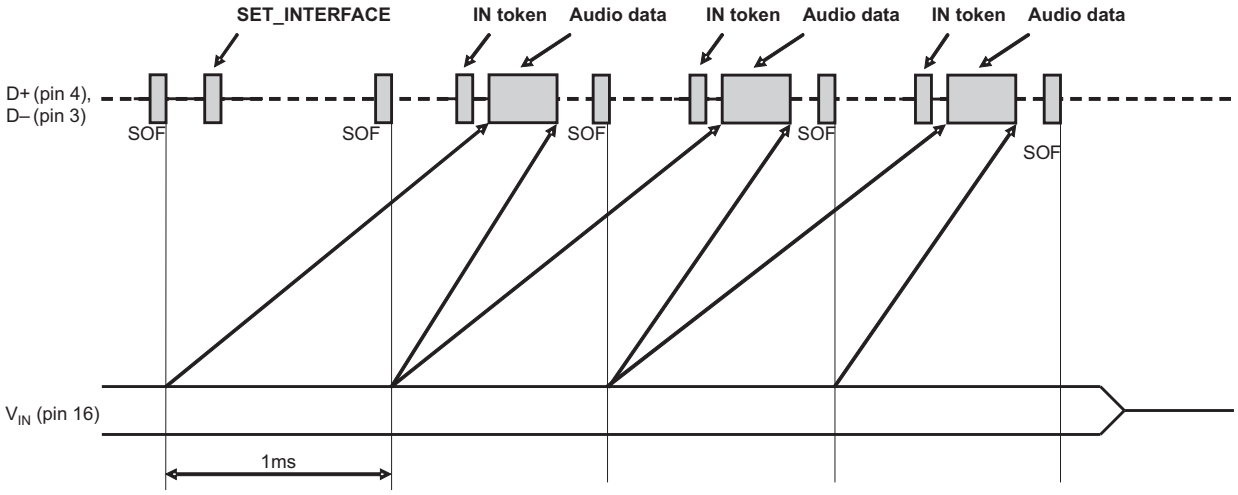


Figure 34. Record Sequence

9.3.11.4 Suspend and Resume Sequence

The PCM2912A enters a suspend state when it sees a constant idle state on the USB bus after approximately 5 ms. When the PCM2912A enters the suspend state, the $\overline{\text{SSPND}}$ flag (pin 29) is asserted. The PCM2912A wakes up immediately after detecting the non-idle state on the USB bus. Figure 35 illustrates these actions.

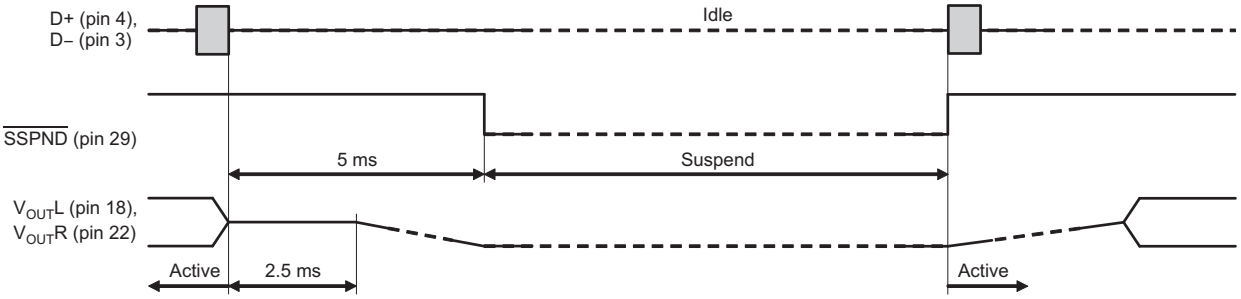


Figure 35. Suspend and Resume

9.4 Device Functional Modes

The PCM2912A is a USB-controlled device. The PCM2912A is a codec, with an analog input (that goes to an A/D converter) and analog output (that comes from a D/A converter), alongside the analog path that goes from the microphone input to the headphone output. A wider explanation of these operational modes is shown in *Feature Description*.

The PCM2912A has hardware controls to turn on and off the integrated microphone preamplifier and the microphone input itself (MAMP and MMUTE, respectively); the microphone preamplifier has +20-dB fixed gain.

9.5 Programming

9.5.1 USB Interface

Control data and audio data are transferred to the PCM2912A via D+ (pin 4) and D– (pin 3). All data transferred to/from the PCM2912A are performed at full speed. Table 1 summarizes the device descriptor. The device descriptor can be modified on request.

Table 1. Device Descriptor

DEVICE DESCRIPTOR	DESCRIPTION
USB revision	2.0 compliant
Device class	0x00 (device defined in interface level)
Device sub class	0x00 (not specified)
Device protocol	0x00 (not specified)
Maximum packet size for endpoint 0	8-byte
Vendor ID	0x08BB
Product ID	0x2912
Device release number	0x0100 (1.00)
Number of configurations	1
Vendor string	String #1 (refer to Table 3)
Product string	String #2 (refer to Table 3)
Serial number	Not supported

Table 2 lists the configuration descriptor. The configuration descriptor can be modified on request.

Table 2. Configuration Descriptor

CONFIGURATION DESCRIPTOR	DESCRIPTION
Interface	Three interfaces
Power attribute	0x80 (Bus powered, no remote wakeup)
Max power	0x32 (100 mA at POWER = Low) / 0xFA (500mA at POWER = High)

Table 3 summarizes the string descriptor. The string descriptor can be modified on request.

Table 3. String Descriptor

STRING DESCRIPTOR	DESCRIPTION
#0	0x0409
#1	Burr-Brown from TI
#2	USB audio CODEC

9.5.1.1 Device Configuration

Figure 36 illustrates the USB audio function topology. The PCM2912A has three interfaces. Each interface is constructed with some alternative settings.

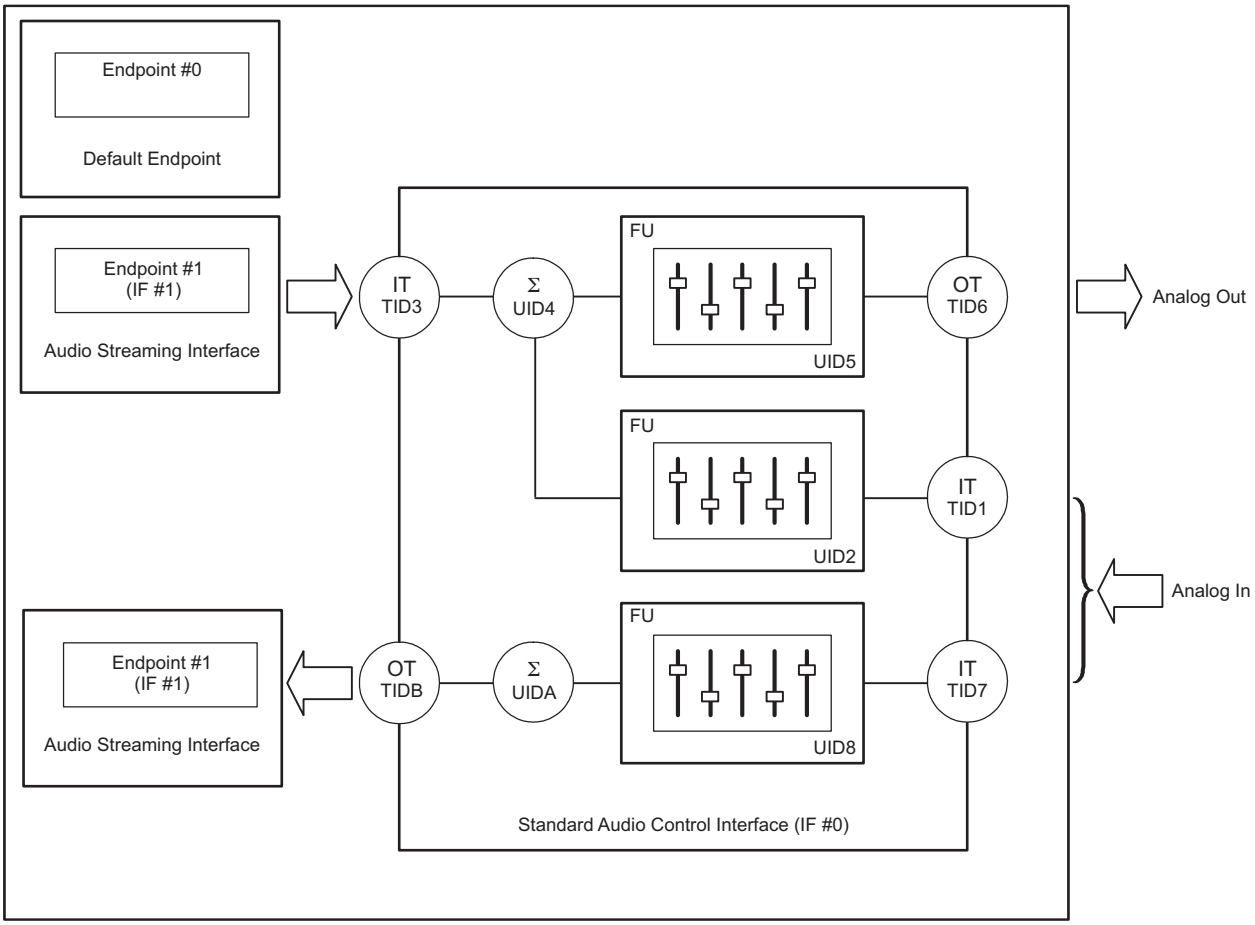


Figure 36. USB Audio Function Topology

9.5.1.2 Interface #0

Interface #0 is the control interface. Alternative setting #0 is the only possible setting for interface #0. Alternative setting #0 describes the standard audio control interface. The audio control interface is constructed with a series of terminal connections. The PCM2912A has the following 10 terminals:

- Input terminal (Terminal ID#1) for audio analog input for sidetone
- Feature unit (Unit ID#2) for sidetone PGA
- Input terminal (Terminal ID#3) for isochronous out stream
- Mixer unit (Unit ID#4) for sidetone mixing
- Feature unit (Unit ID#5) for analog output PGA
- Output terminal (Terminal ID#6) for audio analog output
- Input terminal (Terminal ID#7) for audio analog input
- Feature unit (Unit ID#8) for analog input PGA
- Mixer unit (Unit ID#A) for analog input
- Output terminal (Terminal ID#B) for isochronous in stream

Input terminal #3 is defined as *USB stream* (terminal type 0x0101). Input terminal #3 can accept two-channel audio streams constructed by the left and right channels. Output terminal #6 is defined as a *speaker* (terminal type 0x0301). Input terminals #1 and #7 are defined as *Microphone* (terminal type 0x0201). Physically, these two input terminals are the same input, but logically duplicated. Output terminal B is defined as a *USB stream* (terminal type 0x0101). Output terminal B is a single-channel audio stream. Mixer unit #4 multiplexes the analog input (sidetone) and the audio data of the digital-to-analog converter (DAC). Mixer unit A is placed in front of output terminal B. Mixer unit A has no impact on recording data. Mixer units #4 and A do not have programming capability.

Feature unit #5 supports the following sound control features for analog outputs:

- Volume control
- Mute control

The built-in volume controller can be manipulated by an audio-class-specific request from 0 dB to –76 dB in steps of 1 dB. An individual (L and R) channel can be set for different values. The built-in mute controller can be manipulated by an audio-class-specific request. Only the master mute control request is acceptable.

Feature unit #2 supports the following sound control features for analog input (sidetone):

- Volume control
- Mute control

The built-in volume controller can be manipulated by an audio-class-specific request from 0 dB to –76 dB in 1-dB steps. Only the master volume control is acceptable. The built-in mute controller can be manipulated by audio-class-specific request. Only the master mute control request is acceptable.

Feature unit #8 supports the following sound control features for analog input (microphone record input):

- Volume control
- Mute control

The built-in analog volume controller can be manipulated by an audio-class-specific request from +30 dB to –12 dB in 1-dB steps. The built-in mute controller can be manipulated by an audio-class-specific request. Only the master mute control request is acceptable.

9.5.1.3 Interface #1

Interface #1 is the audio streaming interface for data output. Table 4 lists the three alternative settings for Interface #1. Alternative setting #0 is the zero bandwidth setting. All other alternative settings are operational settings.

Table 4. Interface #1 Alternative Settings

ALTERNATIVE SETTING	DATA FORMAT			TRANSFER MODE	SAMPLING RATE (kHz)
00	Zero Bandwidth				
01	16 bit	Stereo	2s complement (PCM)	Adaptive	8, 11.025, 16, 22.05, 32, 44.1, 48
02	16 bit	Mono	2s complement (PCM)	Adaptive	8, 11.025, 16, 22.05, 32, 44.1, 48

9.5.1.4 Interface #2

Interface #2 is the audio streaming interface for data output. Table 5 shows the two alternative settings for Interface #2. Alternative setting #0 is the Zero Band Width setting. Alternative setting #1 is an operational setting.

Table 5. Interface #2 Alternative Settings

ALTERNATIVE SETTING	DATA FORMAT			TRANSFER MODE	SAMPLING RATE (kHz)
00	Zero Bandwidth				
01	16 bit	Mono	2s complement (PCM)	Asynchronous	8, 11.025, 16, 22.05, 32, 44.1, 48

9.5.1.5 Endpoints

The PCM2912A has the following three endpoints:

- Control endpoint (EP #0)
- Isochronous out audio data stream endpoint (EP #1)
- Isochronous in audio data stream endpoint (EP #2)

The control endpoint is the default endpoint. The control endpoint controls all functions of the PCM2912A by the standard USB request and USB audio class-specific request from the host. The isochronous out audio data stream endpoint is an audio sink endpoint, which receives the PCM audio data. The isochronous out audio data stream endpoint accepts the asynchronous transfer mode. The isochronous in audio data stream endpoint is an audio source endpoint, which transmits the PCM audio data. The isochronous in audio data stream endpoint uses synchronous transfer mode.

9.5.1.6 Internal Regulator

All required power sources are generated by five internal regulators.

Each regulator generates 3.3 V (typical, without load) from V_{BUS} (pin 2). Each regulator has an output pin and a ground return pin (as described in Table 6); this pair must be decoupled with an appropriate capacitor. Note that this capacitance affects inrush-current limitation. One band-gap reference circuit supplies reference voltage for all regulators. BGND (pin 1) is provided for reference ground of the band-gap reference.

Table 6. Internal Regulator Summary

SUPPLIED CIRCUIT	OUTPUT	RETURN
Digital	V_{DD} (pin 5)	DGND (pin 6)
Analog	V_{CCA} (pin 15)	AGND (pin 13)
Headphone (L-ch)	V_{CCL} (pin 19)	HGND (pin 20)
Headphone (R-ch)	V_{CCR} (pin 21)	HGND (pin 20)
PLL	V_{CCP} (pin 26)	PGND (pin 25)

10 Application and Implementation

NOTE

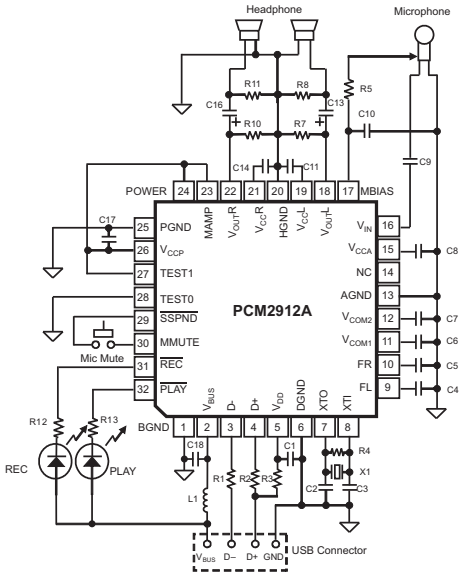
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The V_{BUS} alerts the device when it has been plugged to a USB connection port. The /SSPND flag notifies when the USB input is idle for at least 5 ms; this flag can be used to control or notify subsequent circuits. More functional details can be found in *Interface Sequence*.

10.2 Typical Application

A bus-powered (Hi-power), +20-dB microphone amplifier application example is shown in Figure 37.



NOTE: X_1: 6-MHz crystal resonator
C_1, C_8, C_{11}, C_{14}, C_{17}, C_{18}: 1 µF ceramic
C_2, C_3: 10 pF to 33 pF (depending on load capacitance of crystal resonator)
C_4, C_5: 100 pF ceramic
C_6, C_{10}: 3.3 µF
C_7: 0.1 µF
C_9: 0.22 µF electrolytic (depending on required frequency response for microphone input)
C_{13}, C_{16}: 100 µF electrolytic (depending on required frequency response for headphone output)
R_1, R_2: 22 Ω to 33 Ω
R_3: 1.5 kΩ
R_4: 1 MΩ
R_5: 1 kΩ (depending on microphone characteristic)
R_7, R_8, R_{10}, R_{11}: 3.3 kΩ
R_{12}, R_{13}: 820 Ω (depending on LED drive current)
L_1: 1 µH (DC resistance < 0.6 Ω)
It is possible to change maximum power if total power of actual application does not require over 100 mA (set POWER = *low* to configure as *low-power* device).

Figure 37. USB Headset Application

Typical Application (continued)

NOTE

The circuit in Figure 37 is for information only. Total board design should be considered in order to meet the USB specification as a USB-compliant product.

10.2.1 Design Requirements

For this design example, use the parameters listed in Table 7.

Table 7. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	4.35 V to 5.25 V
Current	80 mA to 100 mA
Input clock frequency	11.994 MHz to 12.006 MHz

10.2.2 Detailed Design Procedure

The PCM2912A is a simple design device, as can connect directly to a USB port. The device only requires decoupling capacitors on the voltage source pins and the output filter for the headphone amplifier; a recommended output filter is the one implemented in the PCM2912AEVM, shown in the user's guide (SBAU141).

10.2.3 Application Curves

For the application curves, see the graphs listed in Table 8.

Table 8. Table of Graphs

		FIGURE
ADC Digital Decimation Filter Frequency Response	Overall Characteristic	Figure 1
	Stop Band Attenuation	Figure 2
	Passband Ripple	Figure 3
	Transient Band Response	Figure 4
ADC Digital High-Pass Filter Frequency Response	Stop Band Characteristic	Figure 5
	Passband Characteristic	Figure 6
ADC Analog Antialiasing Filter Frequency Response	Stop Band Characteristic	Figure 7
	Passband Characteristic	Figure 8
DAC Digital Interpolation Filter Frequency Response	Stop Band Attenuation	Figure 9
	Passband Ripple	Figure 10
	Transient Band Response	Figure 11
DAC Analog FIR Filter Frequency Response	Stop Band Characteristic	Figure 12
	Passband Characteristic	Figure 13
DAC Analog Low-Pass Filter Frequency Response	Stop Band Characteristic	Figure 14
	Passband Characteristic	Figure 15
ADC	THD+N at – 1 dB vs Temperature	Figure 16
	Dynamic Range and Signal-to-Noise Ratio vs Temperature	Figure 17
	THD+N at – 1 dB vs Supply Voltage	Figure 18
	Dynamic Range and Signal-to-Noise Ratio vs Supply Voltage	Figure 19
	THD+N at – 1 dB vs Sampling Frequency	Figure 20
	Dynamic Range and Signal-to-Noise Ratio vs Sampling Frequency	Figure 21

Table 8. Table of Graphs (continued)

		FIGURE
DAC	THD+N at 0 dB vs Temperature	Figure 22
	Dynamic Range and Signal-to-Noise Ratio vs Temperature	Figure 23
	THD+N at 0 dB vs Supply Voltage	Figure 24
	Dynamic Range and Signal-to-Noise Ratio vs Supply Voltage	Figure 25
	THD+N at 0 dB vs Sampling Frequency	Figure 26
	Dynamic Range and Signal-to-Noise Ratio vs Sampling Frequency	Figure 27
Supply Current	Supply Current vs Supply Voltage	Figure 28
	Supply Current vs Sampling Frequency	Figure 29
	Supply Current vs Temperature at Suspend Mode	Figure 30

11 Power Supply Recommendations

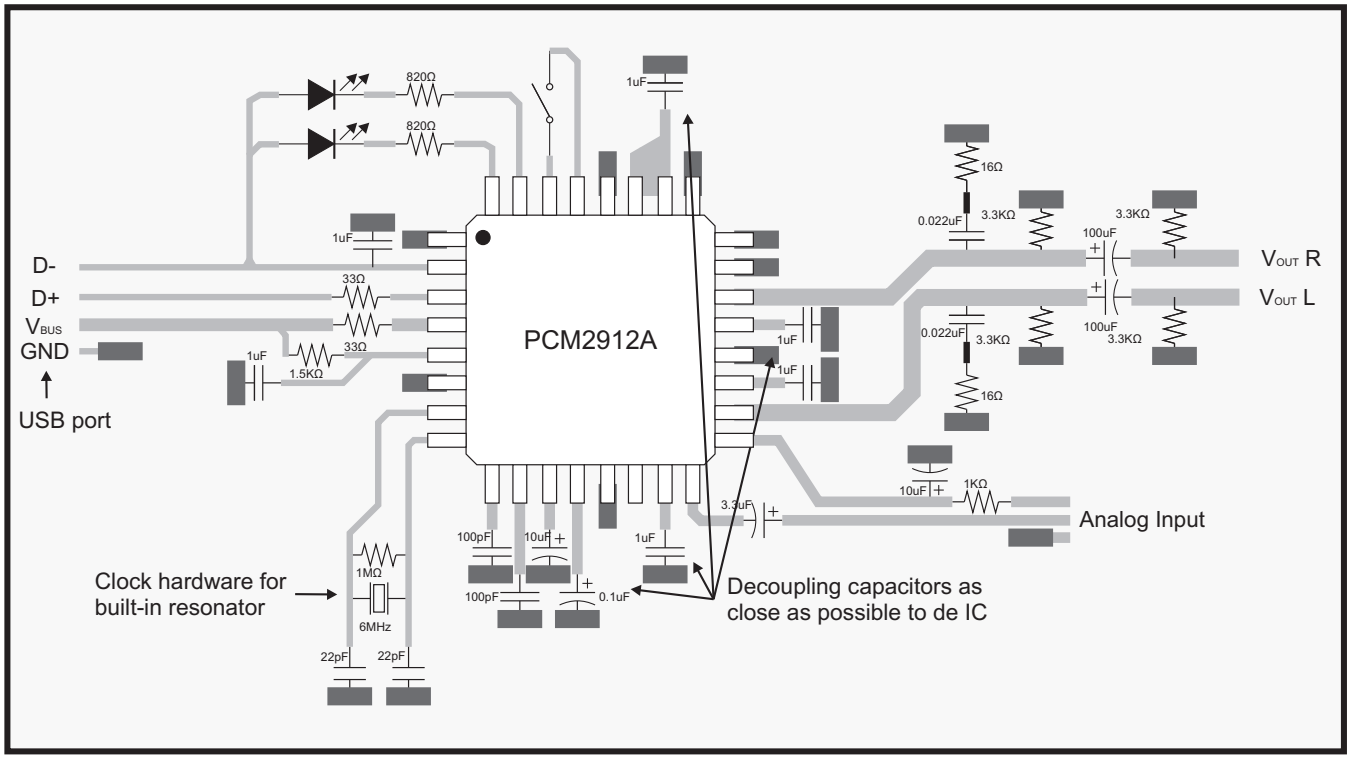
The voltage source to power the PCM2912A must be between 4.35 V and 5.25 V for proper operation (USB voltage). TI recommends placing a decoupling capacitor in every voltage source pin to help filter lower frequency power supply noise. Place these decoupling capacitors as close as possible to the PCM2912A.

12 Layout

12.1 Layout Guidelines

The decoupling capacitors must be as close as possible to the PCM2912A pins. TI recommends following the output filter for the headphone amplifier used in the PCM2912A EVM. The analog input needs a series capacitor to eliminate any possible offset level. The PCM2912A is a low-power device, thus there is no need for a special heat sink PCB design.

12.2 Layout Example



Connection to ground plane

Top layer traces

Top layer ground plane

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation, see the following:

- *Operating Envronments for PCM2912 Applications*, SLAA387
- EVM User's Guide, SBAU141

13.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.3 Trademarks

SpAct, E2E are trademarks of Texas Instruments.
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13.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCM2912APJT	ACTIVE	TQFP	PJT	32	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM2912A	Samples
PCM2912APJTR	ACTIVE	TQFP	PJT	32	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM2912A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

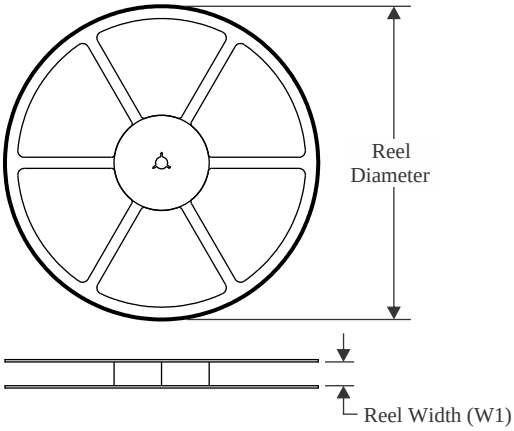
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

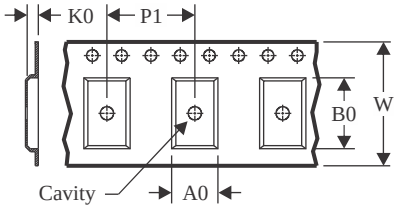
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

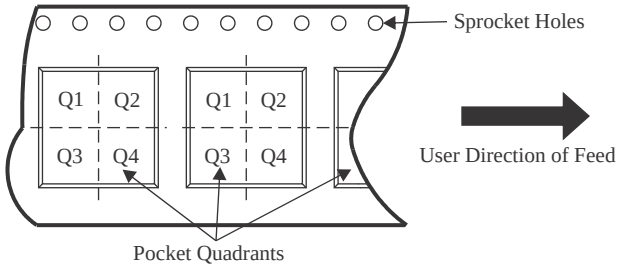


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

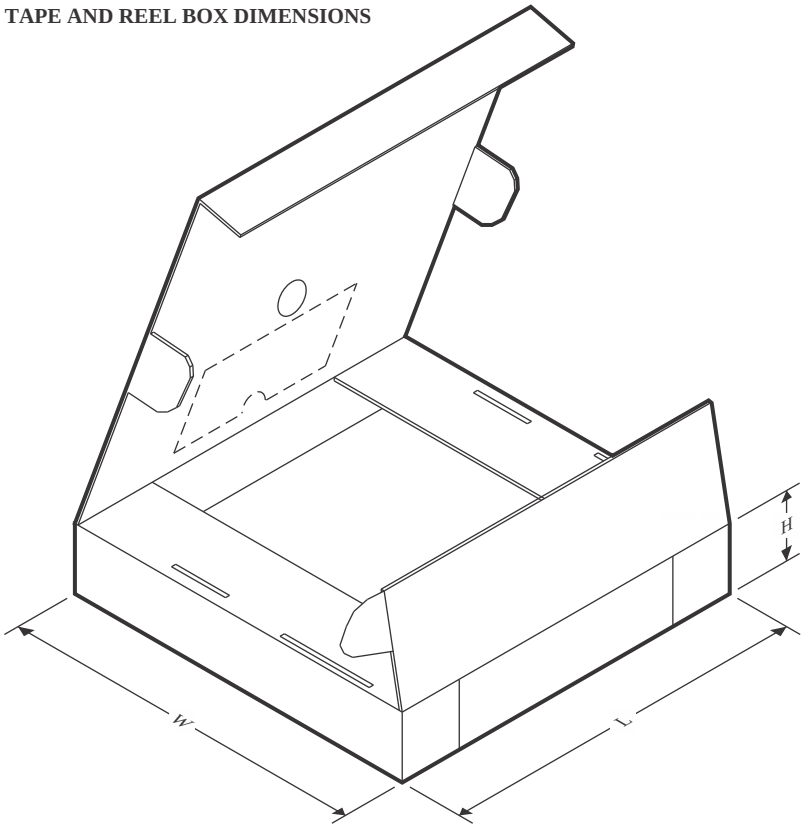
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCM2912APJTR	TQFP	PJT	32	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2

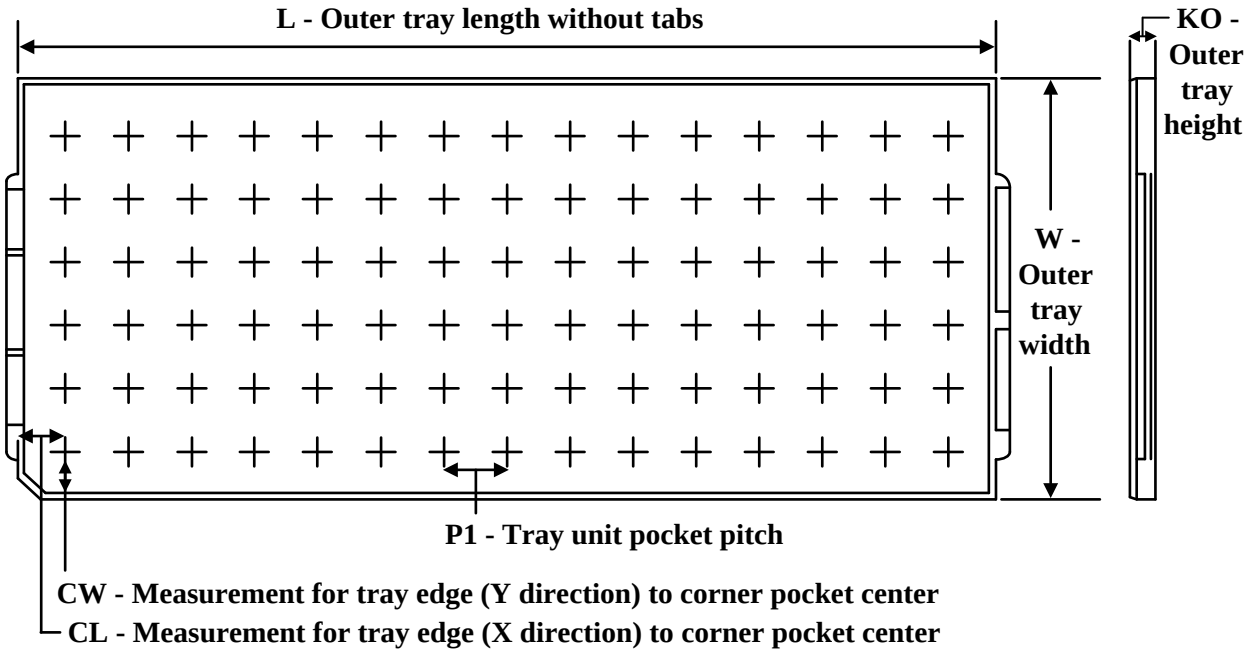
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCM2912APJTR	TQFP	PJT	32	1000	350.0	350.0	43.0

TRAY



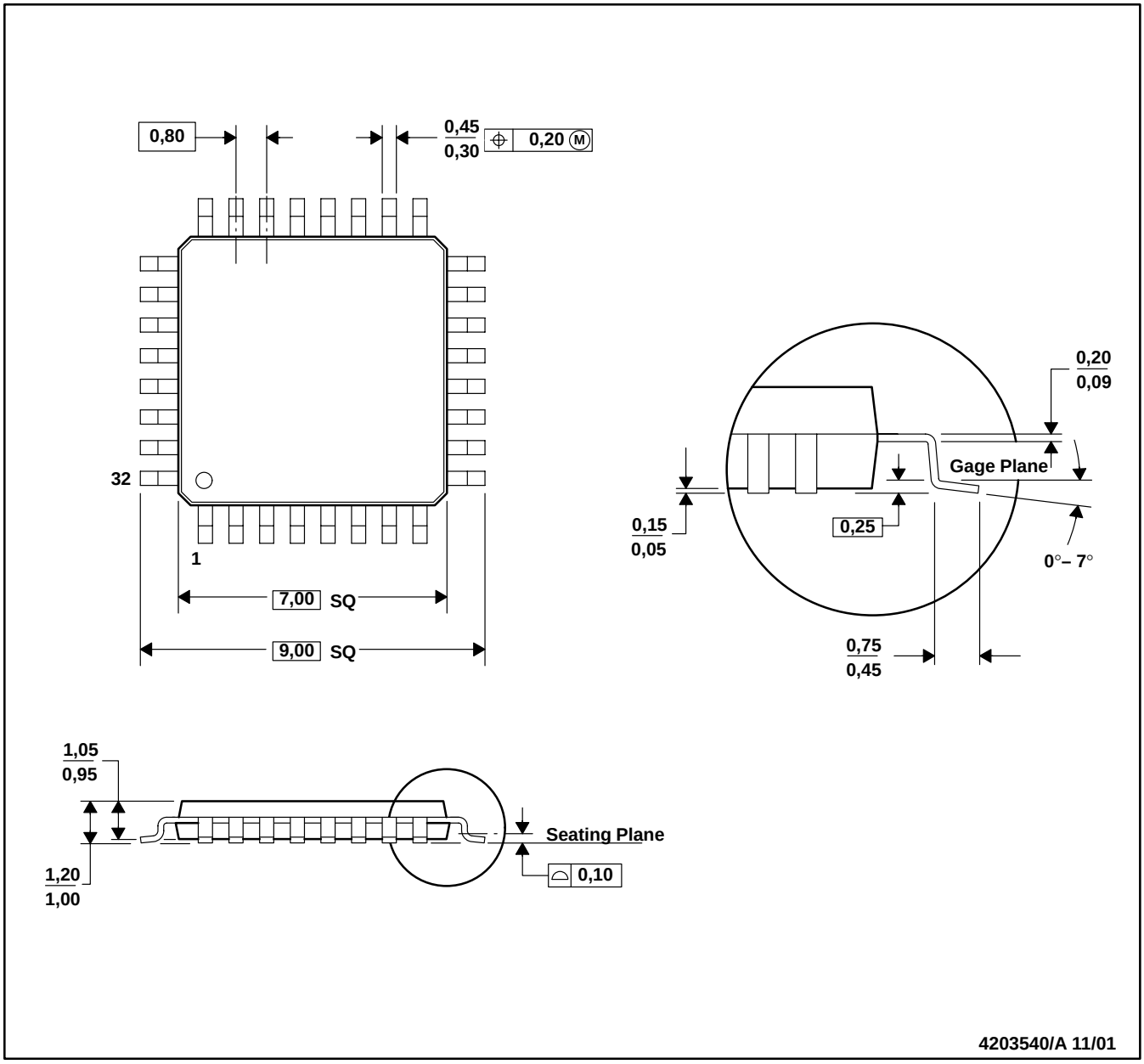
Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
PCM2912APJT	PJT	TQFP	32	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25

MPQF112 – NOVEMBER 2001

PJT (S-PQFP–N32) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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