# 20-W DIGITAL AUDIO-POWER AMPLIFIER WITH EQ, DRC, AND 2.1 MODE

**Check for Samples: TAS5711**

## FEATURES

- **Audio Input/Output**
  - **20-W Into an 8-Ω Load From an 18-V Supply**
  - **Wide PVDD Range, From 8 V to 26 V**
  - **Efficient Class-D Operation Eliminates Need for Heatsinks**
  - **One Serial Audio Input (Two Audio Channels)**
  - **2.1 Mode (2 SE + 1 BTL)**
  - **2.0 Mode (2 BTL)**
  - **Single-Filter PBTL Mode Support**
  - **I$^2$C Address Selection Pin (Chip Select)**
  - **Supports 8-kHz to 48-kHz Sample Rate (LJ/RJ/I$^2$S)**
- **Audio/PWM Processing**
  - **Independent Channel Volume Controls With 24-dB to Mute**
  - **Separate Dynamic Range Control for Satellite and Subchannels**
  - **21 Programmable Biquads for Speaker EQ and Other Audio Processing Features**
  - **Programmable Coefficients for DRC Filters**
  - **DC Blocking Filters**
  - **Support for 3D Effects**
- **General Features**
  - **Serial Control Interface Operational Without MCLK**
  - **Factory-Trimmed Internal Oscillator for Automatic Rate Detection**
  - **Surface Mount, 48-Pin, 7-mm × 7-mm HTQFP Package**
  - **Thermal and Short-Circuit Protection**
  - **Support for AD or BD Mode**

- **Benefits**
  - **Up to 90% Efficient**
  - **AD and BD Filter Mode Support**
  - **SNR: 106 dB, A-Weighted**
  - **EQ: Speaker Equalization Improves Audio Performance**
  - **DRC: Dynamic Range Compression. Can Be Used As Power Limiter. Enables Speaker Protection, Easy Listening, Night-Mode Listening.**
  - **Separate DRC for Satellite and Subchannels**
  - **Autobank Switching: Preload Coefficients for Different Sample Rates. No Need to Write new Coefficients to the Part When Sample Rate Changes.**
  - **Autodetect: Automatically Detects Sample-Rate Changes. No Need for External Microprocessor Intervention**
- **Requires Only 3.3 V and PVDD**

## APPLICATIONS

- **Television**
- **iPod™ Dock**
- **Sound Bar**

## DESCRIPTION

The TAS5711 is a 20-W, efficient, digital audio power amplifier for driving stereo bridge-tied speakers. One serial data input allows processing of up to two discrete audio channels and seamless integration to most digital audio processors and MPEG decoders. The device accepts a wide range of input data and data rates. A fully programmable data path routes these channels to the internal speaker drivers.

The TAS5711 is an I$^2$S slave-only device receiving all clocks from external sources. The TAS5711 operates with a PWM carrier between 384-kHz switching rate and 352-KHz switching rate depending on the input sample rate. Oversampling combined with a fourth-order noise shaper provides a flat noise floor and excellent dynamic range from 20 Hz to 20 kHz.
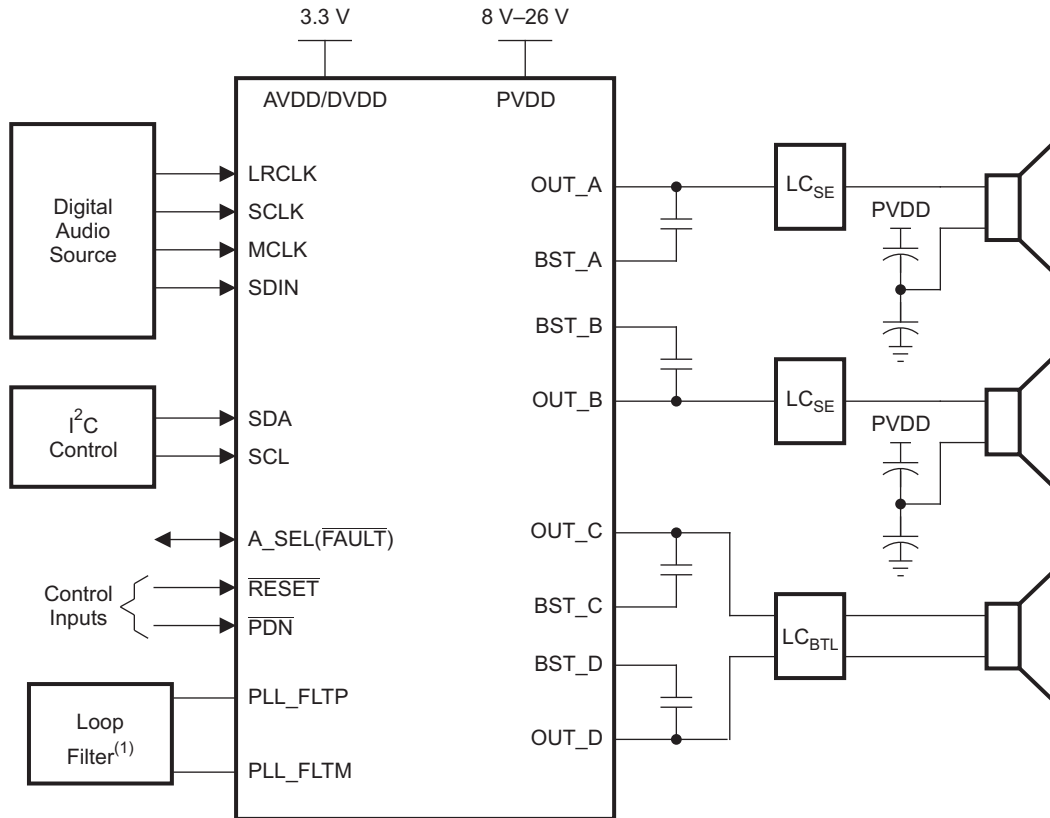
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.
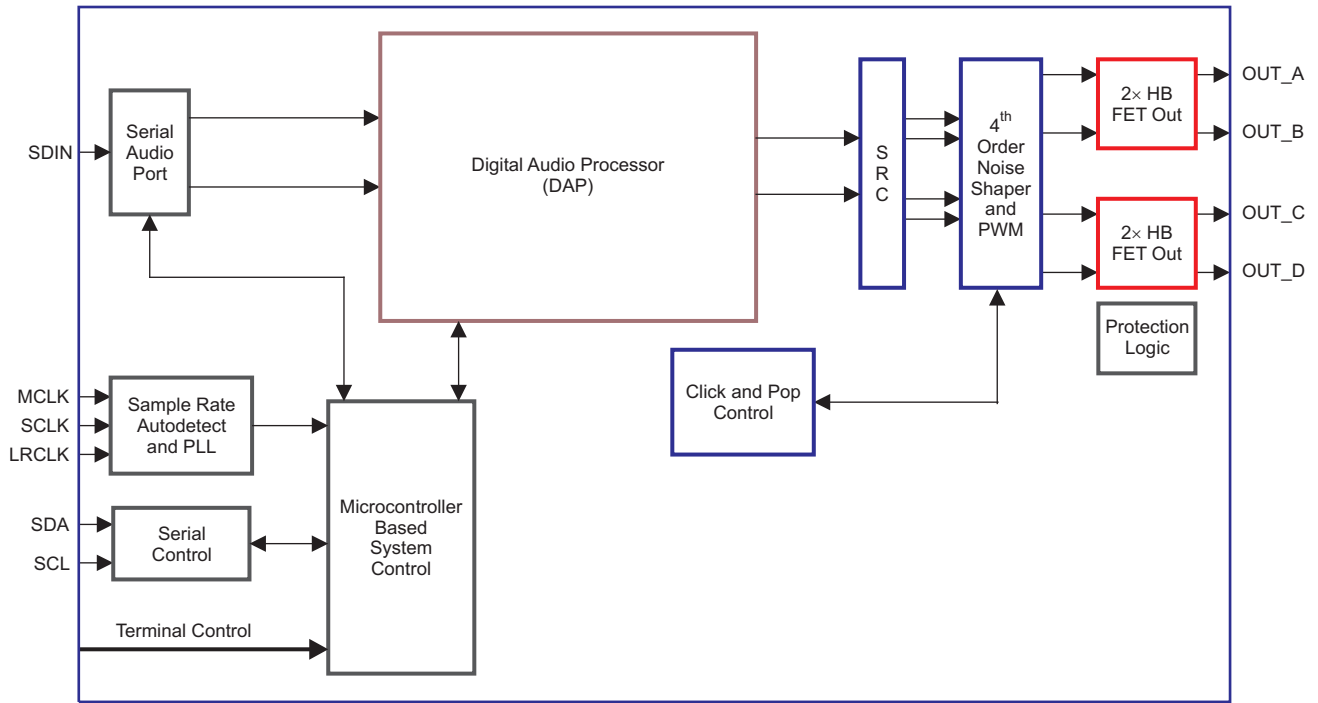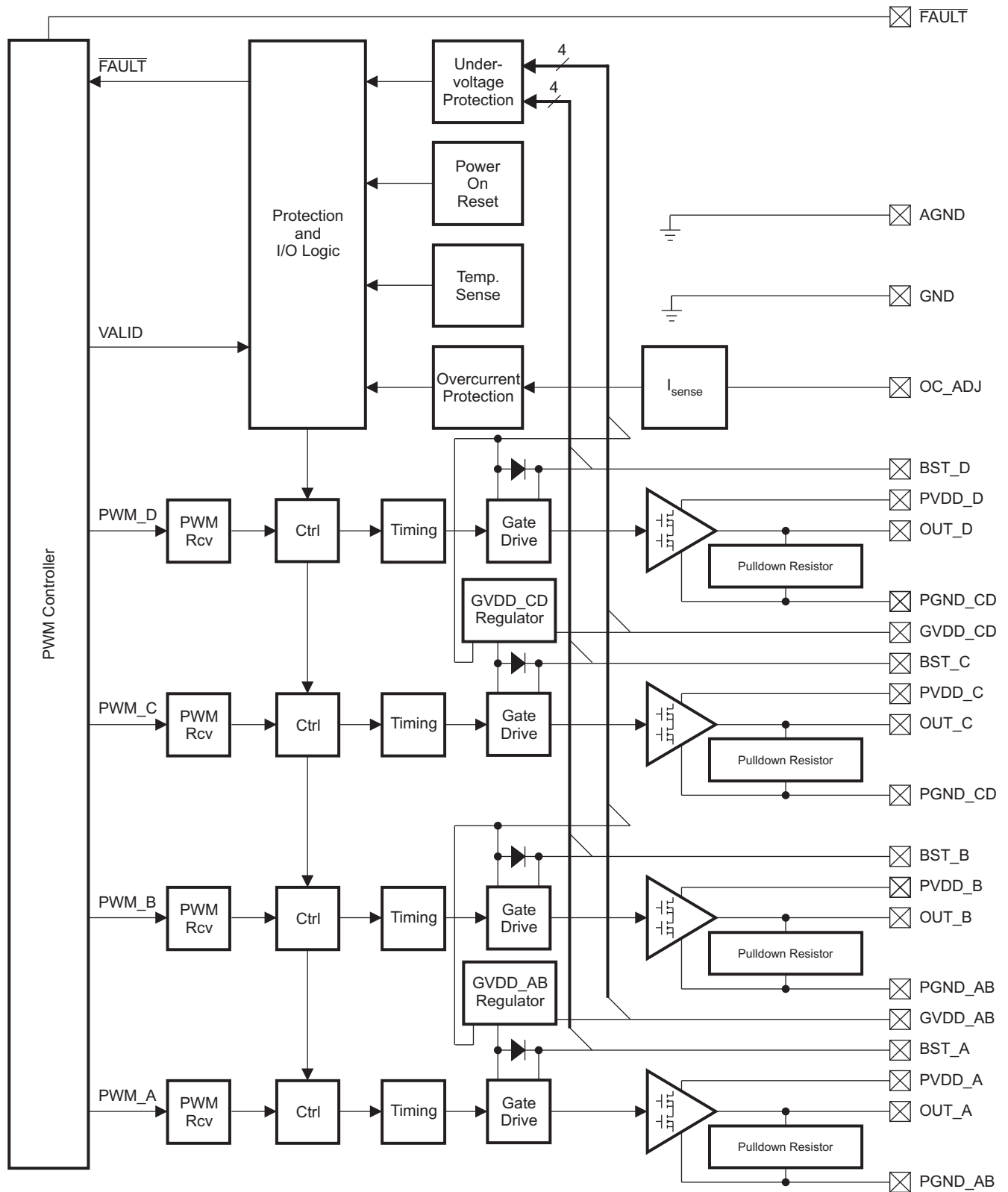
## SIMPLIFIED APPLICATION DIAGRAM



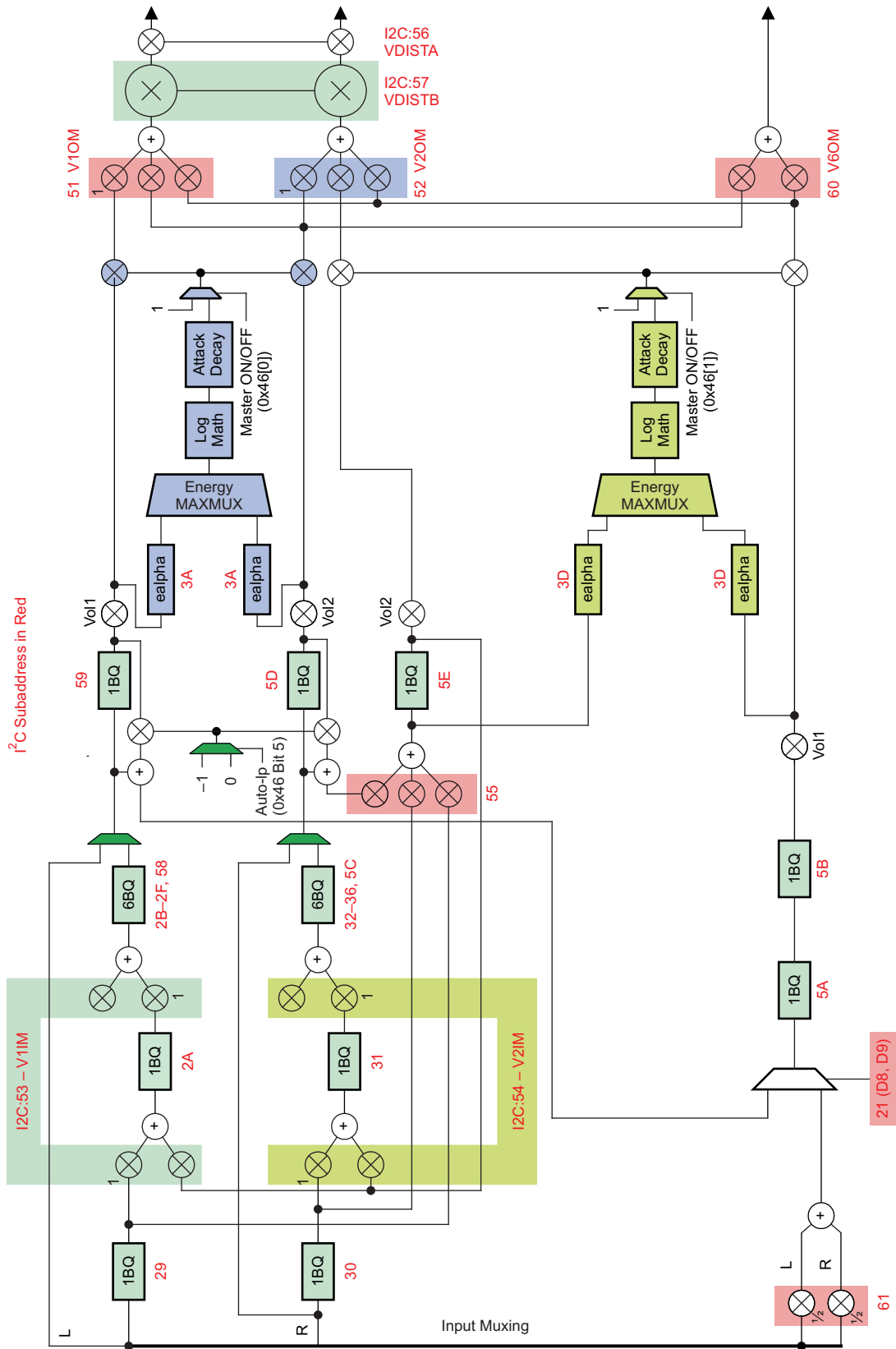(1) See TAS5711 EVM User's Guide (SLOU280) for loop filter values.

## FUNCTIONAL VIEW


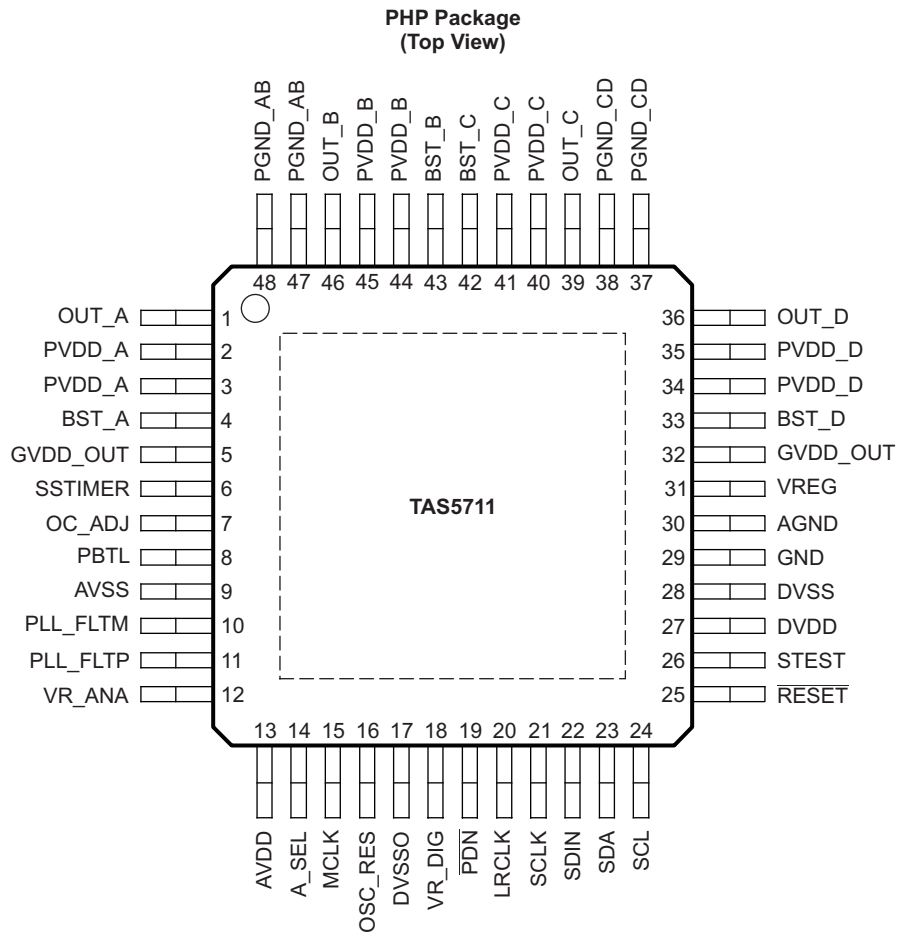
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**Figure 1. Power Stage Functional Block Diagram**

## DAP Process Structure

# DEVICE INFORMATION

## PIN ASSIGNMENT

**PHP Package
(Top View)**



P0075-08

## PIN FUNCTIONS

| PIN | | TYPE[1] | 5-V TOLERANT | TERMINATION[2] | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | NO. | | | | |
| AGND | 30 | P | | | Analog ground for power stage |
| A_SEL | 14 | DIO | | | A value of 0 (15-kΩ pulldown) makes the I²C device address 0x34, and a value of 1 (15-kΩ pullup) makes it 0x36. This pin can be programmed after RESET to be an output by writing 1 to bit 0 of I²C register 0x05. In that mode, the A_SEL pin is redefined as FAULT (see ERROR REPORTING for details). |
| AVDD | 13 | P | | | 3.3-V analog power supply |
| AVSS | 9 | P | | | Analog 3.3-V supply ground |
| BST_A | 4 | P | | | High-side bootstrap supply for half-bridge A |
| BST_B | 43 | P | | | High-side bootstrap supply for half-bridge B |
| BST_C | 42 | P | | | High-side bootstrap supply for half-bridge C |
| BST_D | 33 | P | | | High-side bootstrap supply for half-bridge D |
| DVDD | 27 | P | | | 3.3-V digital power supply |
| DVSSO | 17 | P | | | Oscillator ground |

(1)    TYPE: A = analog; D = 3.3-V digital; P = power/ground/decoupling; I = input; O = output
(2)    All pullups are weak pullups and all pulldowns are weak pulldowns. The pullups and pulldowns are included to assure proper input logic
         levels if the pins are left unconnected (pullups → logic 1 input; pulldowns → logic 0 input).

Product Folder Link(s): *TAS5711*

## PIN FUNCTIONS (continued)

| PIN NAME | PIN NO. | TYPE[1] | 5-V TOLERANT | TERMINATION[2] | DESCRIPTION |
|---|---|---|---|---|---|
| DVSS | 28 | P | | | Digital ground |
| GND | 29 | P | | | Analog ground for power stage |
| GVDD_OUT | 5, 32 | P | | | Gate drive internal regulator output. This pin must not be used to drive external devices. |
| LRCLK | 20 | DI | 5-V | Pulldown | Input serial audio data left/right clock (sample rate clock) |
| MCLK | 15 | DI | 5-V | Pulldown | Master clock input |
| OC_ADJ | 7 | AO | | | Analog overcurrent programming. Requires resistor to ground. |
| OSC_RES | 16 | AO | | | Oscillator trim resistor. Connect an 18.2-kΩ 1% resistor to DVSSO. |
| OUT_A | 1 | O | | | Output, half-bridge A |
| OUT_B | 46 | O | | | Output, half-bridge B |
| OUT_C | 39 | O | | | Output, half-bridge C |
| OUT_D | 36 | O | | | Output, half-bridge D |
| PBTL | 8 | DI | | | Low means BTL or SE mode; high means PBTL mode. Information goes directly to power stage. |
| $\overline{PDN}$ | 19 | DI | 5-V | Pullup | Power down, active-low. $\overline{PDN}$ prepares the device for loss of power supplies by shutting down the Noise Shaper and initiating PWM stop sequence. |
| PGND_AB | 47, 48 | P | | | Power ground for half-bridges A and B |
| PGND_CD | 37, 38 | P | | | Power ground for half-bridges C and D |
| PLL_FLTM | 10 | AO | | | PLL negative loop filter terminal |
| PLL_FLTP | 11 | AO | | | PLL positive loop filter terminal |
| PVDD_A | 2, 3 | P | | | Power supply input for half-bridge output A |
| PVDD_B | 44, 45 | P | | | Power supply input for half-bridge output B |
| PVDD_C | 40, 41 | P | | | Power supply input for half-bridge output C |
| PVDD_D | 34, 35 | P | | | Power supply input for half-bridge output D |
| $\overline{RESET}$ | 25 | DI | 5-V | Pullup | Reset, active-low. A system reset is generated by applying a logic low to this pin. $\overline{RESET}$ is an asynchronous control signal that restores the DAP to its default conditions, and places the PWM in the hard mute state (tristated). |
| SCL | 24 | DI | 5-V | | I$^2$C serial control clock input |
| SCLK | 21 | DI | 5-V | Pulldown | Serial audio data clock (shift clock). SCLK is the serial audio port input data bit clock. |
| SDA | 23 | DIO | 5-V | | I$^2$C serial control data interface input/output |
| SDIN | 22 | DI | 5-V | Pulldown | Serial audio data input. SDIN supports three discrete (stereo) data formats. |
| SSTIMER | 6 | AI | | | Controls ramp time of OUT_x to minimize pop. Leave this pin floating for BD mode. Requires capacitor of 2.2 nF to GND in AD mode. The capacitor determines the ramp time. |
| STEST | 26 | DI | | | Factory test pin. Connect directly to DVSS. |
| VR_ANA | 12 | P | | | Internally regulated 1.8-V analog supply voltage. This pin must not be used to power external devices. |
| VR_DIG | 18 | P | | | Internally regulated 1.8-V digital supply voltage. This pin must not be used to power external devices. |
| VREG | 31 | P | | | Digital regulator output. Not to be used for powering external circuitry. |

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) [1]

| | | VALUE | UNIT |
|---|---|---|---|
| Supply voltage | DVDD, AVDD | −0.3 to 3.6 | V |
| | PVDD_x | −0.3 to 30 | V |
| Input voltage | OC_ADJ | −0.3 to 4.2 | V |
| | 3.3-V digital input | −0.5 to DVDD + 0.5 | V |
| | 5-V tolerant [2] digital input (except MCLK) | −0.5 to DVDD + 2.5 [3] | V |
| | 5-V tolerant MCLK input | −0.5 to AVDD + 2.5 [3] | V |
| OUT_x to PGND_x | | 32 [4] | V |
| BST_x to PGND_x | | 43 [4] | V |
| Input clamp current, $I_{IK}$ | | ±20 | mA |
| Output clamp current, $I_{OK}$ | | ±20 | mA |
| Operating free-air temperature | | 0 to 85 | °C |
| Operating junction temperature range | | 0 to 150 | °C |
| Storage temperature range, $T_{stg}$ | | −40 to 125 | °C |

(1) Stresses beyond those listed under *absolute ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operation conditions* are not implied. Exposure to absolute-maximum conditions for extended periods may affect device reliability.
(2) 5-V tolerant inputs are PDN, RESET, SCLK, LRCLK, MCLK, SDIN, SDA, and SCL.
(3) Maximum pin voltage should not exceed 6.0V
(4) DC voltage + peak ac waveform measured at the pin should be below the allowed limit for all conditions.

## THERMAL INFORMATION

| THERMAL METRIC[1][2] | | TAS5711 | UNITS |
|---|---|---|---|
| | | PHP (48 PIN) | |
| $\theta_{JA}$ | Junction-to-ambient thermal resistance | 29.9 | °C/W |
| $\theta_{JCtop}$ | Junction-to-case (top) thermal resistance | 20.5 | |
| $\theta_{JB}$ | Junction-to-board thermal resistance | 12.5 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.3 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 7.3 | |
| $\theta_{JCbot}$ | Junction-to-case (bottom) thermal resistance | 0.7 | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) For thermal estimates of this device based on PCB copper area, see the TI PCB Thermal Calculator.

## RECOMMENDED OPERATING CONDITIONS

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| | Digital/analog supply voltage | DVDD, AVDD | 3 | 3.3 | 3.6 | V |
| | Half-bridge supply voltage | PVDD_x | 8 | | 26 | V |
| $V_{IH}$ | High-level input voltage | 5-V tolerant | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | 5-V tolerant | | | 0.8 | V |
| $T_A$ | Operating ambient temperature range | | 0 | | 85 | °C |
| $T_J$ [1] | Operating junction temperature range | | 0 | | 125 | °C |
| $R_L$ (BTL) | Load impedance | Output filter: L = 15 µH, C = 680 nF. | 6 | 8 | | Ω |
| $L_O$ (BTL) | Output-filter inductance | Minimum output inductance under short-circuit condition | 10 | | | µH |

(1) Continuous operation above the recommended junction temperature may result in reduced reliability and/or lifetime of the device.

Product Folder Link(s): TAS5711

## PWM OPERATION AT RECOMMENDED OPERATING CONDITIONS

| PARAMETER | TEST CONDITIONS | VALUE | UNIT |
|---|---|---|---|
| Output sample rate | 11.025/22.05/44.1-kHz data rate ±2% | 352.8 | kHz |
| | 48/24/12/8/16/32-kHz data rate ±2% | 384 | |

## PLL INPUT PARAMETERS AND EXTERNAL FILTER COMPONENTS

| | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{MCLKI}$ | MCLK Frequency | | 2.8224 | | 24.576 | MHz |
| | MCLK duty cycle | | 40% | 50% | 60% | |
| tr / $tf_{(MCLK)}$ | Rise/fall time for MCLK | | | | 5 | ns |
| | LRCLK allowable drift before LRCLK reset | | | | 4 | MCLKs |
| | External PLL filter capacitor C1 | SMD 0603 X7R | | 47 | | nF |
| | External PLL filter capacitor C2 | SMD 0603 X7R | | 4.7 | | nF |
| | External PLL filter resistor R | SMD 0603, metal film | | 470 | | Ω |

# ELECTRICAL CHARACTERISTICS

## DC Characteristics

TA = 25°, PVCC_x = 18V, DVDD = AVDD = 3.3V, $R_L$ = 8Ω, BTL AD Mode, FS = 48KHz (unless otherwise noted)

| | PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | $\overline{A\_SEL}$ and SDA | $I_{OH}$ = −4 mA DVDD = AVDD = 3 V | 2.4 | | | V |
| $V_{OL}$ | Low-level output voltage | $\overline{A\_SEL}$ and SDA | $I_{OL}$ = 4 mA DVDD = AVDD = 3 V | | | 0.5 | V |
| $I_{IL}$ | Low-level input current | | $V_I < V_{IL}$ ; DVDD = AVDD = 3.6V | | | 75 | µA |
| $I_{IH}$ | High-level input current | | $V_I > V_{IH}$ ; DVDD = AVDD = 3.6V | | | 75[1] | µA |
| $I_{DD}$ | 3.3 V supply current | 3.3 V supply voltage (DVDD, AVDD) | Normal Mode | | 48 | 70 | mA |
| | | | Reset ($\overline{RESET}$ = low, $\overline{PDN}$ = high) | | 24 | 32 | |
| $I_{PVDD}$ | Half-bridge supply current | No load (PVDD_x) | Normal Mode | | 30 | 55 | mA |
| | | | Reset ($\overline{RESET}$ = low, $\overline{PDN}$ = high) | | 5 | 13 | |
| $r_{DS(on)}$ [2] | Drain-to-source resistance, LS | $T_J$ = 25°C, includes metallization resistance | | | 180 | | mΩ |
| | Drain-to-source resistance, HS | $T_J$ = 25°C, includes metallization resistance | | | 180 | | |
| **I/O Protection** | | | | | | | |
| $V_{uvp}$ | Undervoltage protection limit | PVDD falling | | | 7.2 | | V |
| $V_{uvp,hyst}$ | Undervoltage protection limit | PVDD rising | | | 7.6 | | V |
| OTE [3] | Overtemperature error | | | | 150 | | °C |
| $OTE_{HYST}$ [3] | Extra temperature drop required to recover from error | | | | 30 | | °C |
| OLPC | Overload protection counter | $f_{PWM}$ = 384 kHz | | | 0.63 | | ms |
| $I_{OC}$ | Overcurrent limit protection | Resistor—programmable, max. current, $R_{OCP}$ = 22 kΩ | | | 4.5 | | A |
| $I_{OCT}$ | Overcurrent response time | | | | 150 | | ns |
| $R_{OCP}$ | OC programming resistor range | Resistor tolerance = 5% for typical value; the minimum resistance should not be less than 20 kΩ. | 20 | 22 | | kΩ |
| $R_{PD}$ | Internal pulldown resistor at the output of each half-bridge | Connected when drivers are tristated to provide bootstrap capacitor charge. | | 3 | | kΩ |

(1)  $I_{IH}$ for the PBTL pin has a maximum limit of 200 µA due to an intenal pulldown on the pin.
(2)  This does not include bond-wire or pin resistance.
(3)  Specified by design

## AC Characteristics (BTL)

PVDD_x = 18 V, BTL AD mode, FS = 48 KHz, $R_L$ = 8 Ω, $R_{OCP}$ = 22 KΩ, $C_{BST}$ = 33 nF, audio frequency = 1 kHz, AES17 filter, $f_{PWM}$ = 384 kHz, $T_A$ = 25°C (unless otherwise specified). All performance is in accordance with recommended operating conditions (unless otherwise specified).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $P_O$ | Power output per channel | PVDD = 18 V, 10% THD, 1-kHz input signal | | 21 | | W |
| | | PVDD = 18 V, 7% THD, 1-kHz input signal | | 20 | | |
| | | PVDD = 12 V, 10% THD, 1-kHz input signal | | 9.5 | | |
| | | PVDD = 12 V, 7% THD, 1-kHz input signal | | 9 | | |
| | | PVDD = 8 V, 10% THD, 1-kHz input signal | | 4.1 | | |
| | | PVDD = 8 V, 7% THD, 1-kHz input signal | | 3.9 | | |
| | | PBTL mode, PVDD = 12 V, $R_L$ = 4 Ω, 10% THD, 1-kHz input signal | | 19.2 | | |
| | | PBTL mode, PVDD = 12 V, $R_L$ = 4 Ω, 7% THD, 1-kHz input signal | | 18 | | |
| | | PBTL mode, PVDD = 18 V, $R_L$ = 4 Ω, 10% THD, 1-kHz input signal | | 42.8 | | |
| | | PBTL mode, PVDD = 18 V, $R_L$ = 4 Ω, 7% THD, 1-kHz input signal | | 40 | | |
| | | SE mode, PVDD = 12 V, $R_L$ = 4 Ω, 10% THD, 1-kHz input signal | | 4.6 | | |
| | | SE mode, PVDD = 12 V, $R_L$ = 4 Ω, 7% THD, 1-kHz input signal | | 4.3 | | |
| | | SE mode, PVDD = 24 V, $R_L$ = 4 Ω, 10% THD, 1-kHz input signal | | 17.8 | | |
| | | SE mode, PVDD = 24 V, $R_L$ = 4 Ω, 7% THD, 1-kHz input signal | | 16 | | |
| THD+N | Total harmonic distortion + noise | PVDD = 18 V, $P_O$ = 1 W | | 0.06% | | |
| | | PVDD = 12 V, $P_O$ = 1 W | | 0.08% | | |
| | | PVDD = 8 V, $P_O$ = 1 W | | 0.2% | | |
| $V_n$ | Output integrated noise (rms) | A-weighted | | 44 | | μV |
| | Crosstalk | $P_O$ = 0.25 W, f = 1 kHz (BD Mode) | | −82 | | dB |
| | | $P_O$ = 0.25 W, f = 1 kHz (AD Mode) | | −69 | | dB |
| SNR | Signal-to-noise ratio[1] | A-weighted, f = 1 kHz, maximum power at THD < 1% | | 106 | | dB |

(1) SNR is calculated relative to 0-dBFS input level.

Product Folder Link(s): *TAS5711*

## SERIAL AUDIO PORTS SLAVE MODE

over recommended operating conditions (unless otherwise noted)

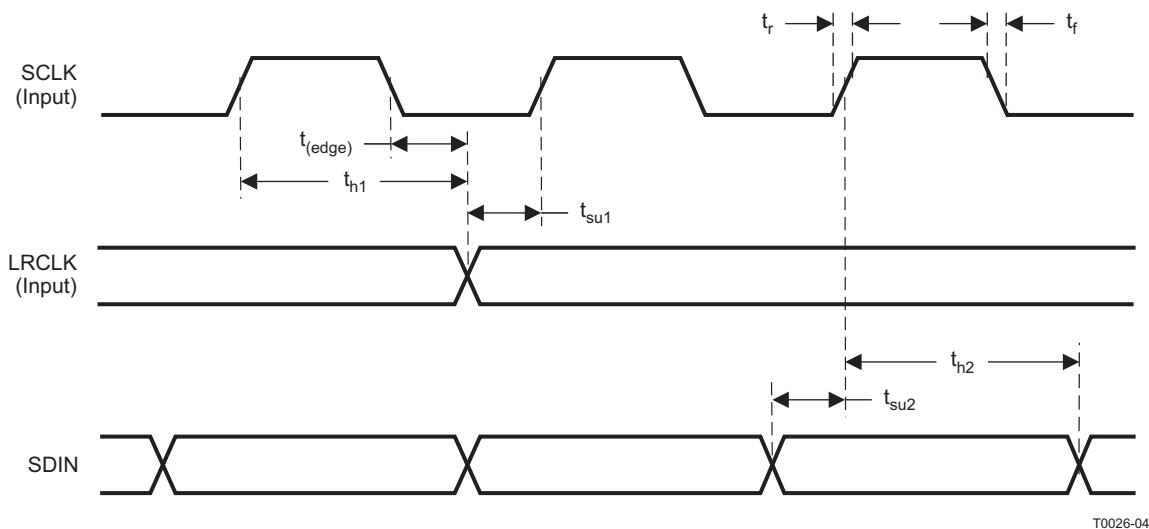| | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{SCLKIN}$ | Frequency, SCLK 32 × $f_S$, 48 × $f_S$, 64 × $f_S$ | $C_L$ = 30 pF | 1.024 | | 12.288 | MHz |
| $t_{su1}$ | Setup time, LRCLK to SCLK rising edge | | 10 | | | ns |
| $t_{h1}$ | Hold time, LRCLK from SCLK rising edge | | 10 | | | ns |
| $t_{su2}$ | Setup time, SDIN to SCLK rising edge | | 10 | | | ns |
| $t_{h2}$ | Hold time, SDIN from SCLK rising edge | | 10 | | | ns |
| | LRCLK frequency | | 8 | 48 | 48 | kHz |
| | SCLK duty cycle | | 40% | 50% | 60% | |
| | LRCLK duty cycle | | 40% | 50% | 60% | |
| | SCLK rising edges between LRCLK rising edges | | 32 | | 64 | SCLK edges |
| $t_{(edge)}$ | LRCLK clock edge with respect to the falling edge of SCLK | | −1/4 | | 1/4 | SCLK period |
| $t_r/t_f$ | Rise/fall time for SCLK/LRCLK | | | | 8 | ns |



**Figure 2. Slave Mode Serial Data Interface Timing**

## I²C SERIAL CONTROL PORT OPERATION

Timing characteristics for I²C Interface signals over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $f_{SCL}$ | Frequency, SCL | No wait states | | 400 | kHz |
| $t_{w(H)}$ | Pulse duration, SCL high | | 0.6 | | μs |
| $t_{w(L)}$ | Pulse duration, SCL low | | 1.3 | | μs |
| $t_r$ | Rise time, SCL and SDA | | | 300 | ns |
| $t_f$ | Fall time, SCL and SDA | | | 300 | ns |
| $t_{su1}$ | Setup time, SDA to SCL | | 100 | | ns |
| $t_{h1}$ | Hold time, SCL to SDA | | 0 | | ns |
| $t_{(buf)}$ | Bus free time between stop and start condition | | 1.3 | | μs |
| $t_{su2}$ | Setup time, SCL to start condition | | 0.6 | | μs |
| $t_{h2}$ | Hold time, start condition to SCL | | 0.6 | | μs |
| $t_{su3}$ | Setup time, SCL to stop condition | | 0.6 | | μs |
| $C_L$ | Load capacitance for each bus line | | | 400 | pF |
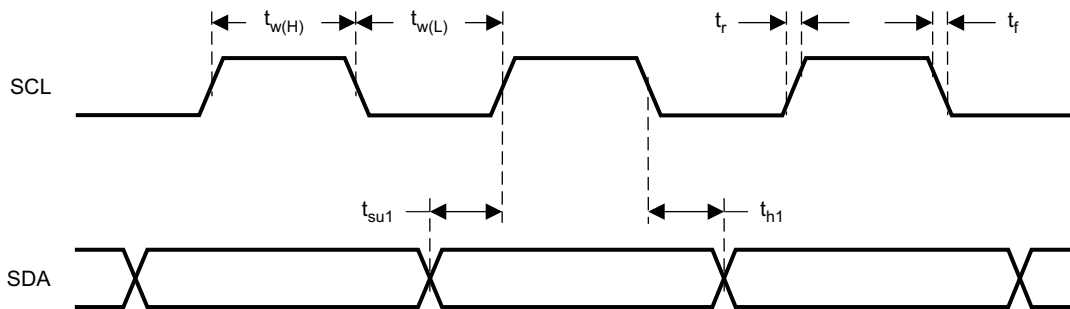


**Figure 3. SCL and SDA Timing**
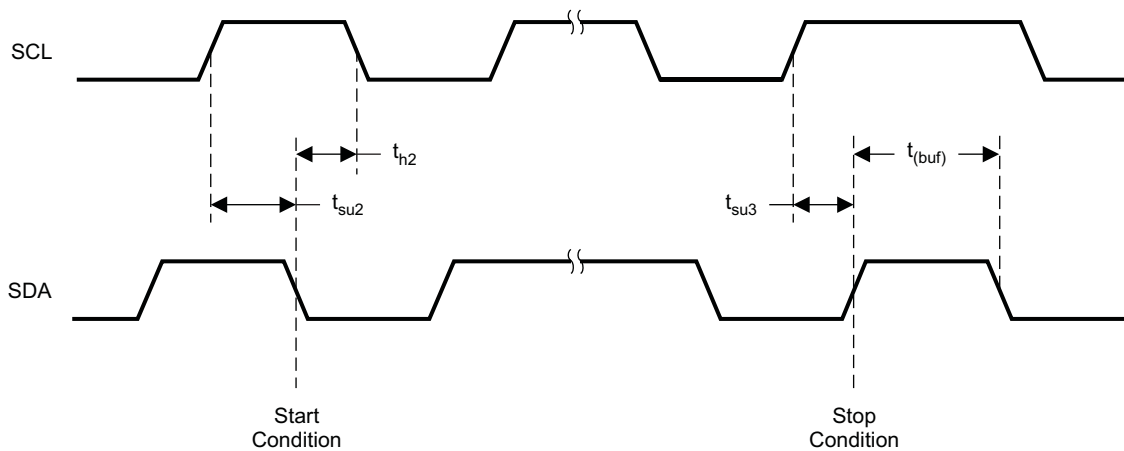


**Figure 4. Start and Stop Conditions Timing**

Product Folder Link(s): *TAS5711*

## RESET TIMING ($\overline{\text{RESET}}$)

Control signal parameters over recommended operating conditions (unless otherwise noted). Please refer to Recommended Use Model section on usage of all terminals.

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{w(RESET)}$ | Pulse duration, $\overline{\text{RESET}}$ active | 100 | | | µs |
| $t_{d(I2C\_ready)}$ | Time to enable I$^2$C | | | 12.0 | ms |
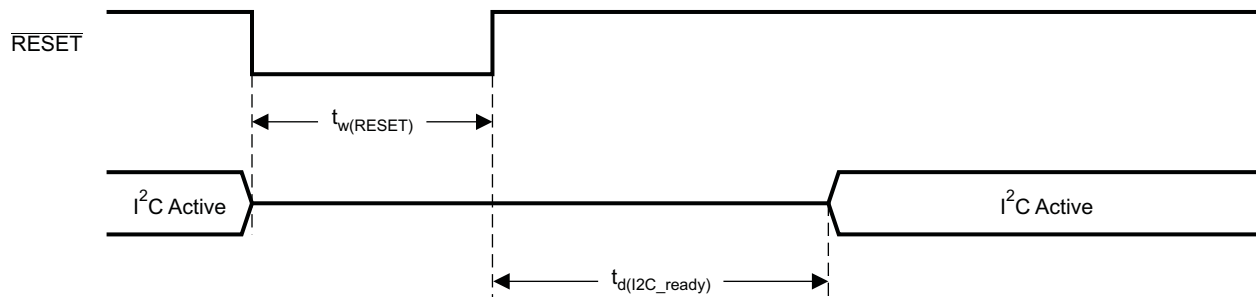


System Initialization.
Enable via I$^2$C.

T0421-01

NOTES: On power up, it is recommended that the TAS5711 $\overline{\text{RESET}}$ be held LOW for at least 100 µs after DVDD has reached 3 V.

If the $\overline{\text{RESET}}$ is asserted LOW while $\overline{\text{PDN}}$ is LOW, then the $\overline{\text{RESET}}$ must continue to be held LOW for at least 100 µs after $\overline{\text{PDN}}$ is deasserted (HIGH).

**Figure 5. Reset Timing**

# TYPICAL CHARACTERISTICS, BTL CONFIGURATION

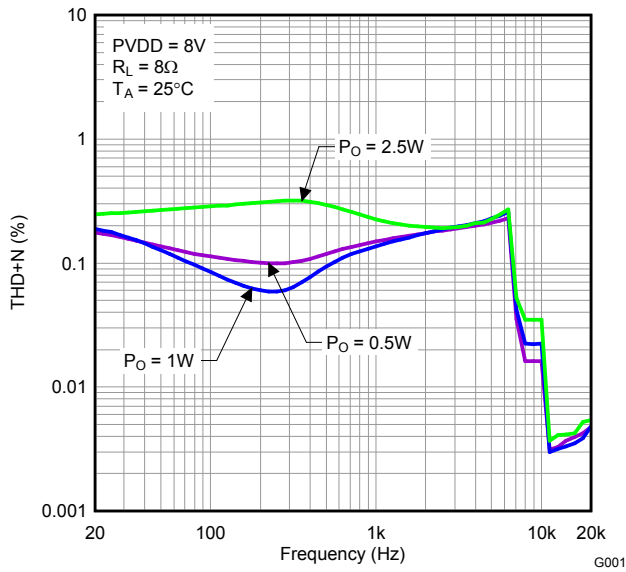TOTAL HARMONIC DISTORTION + NOISE
vs
FREQUENCY



**Figure 6.**
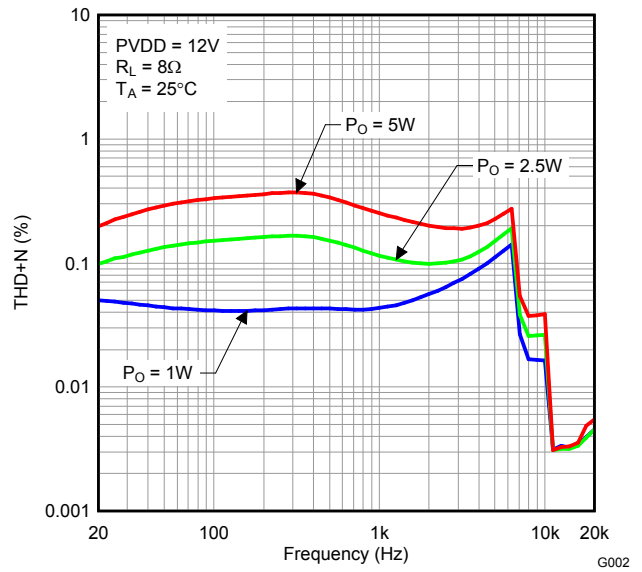
TOTAL HARMONIC DISTORTION + NOISE
vs
FREQUENCY



**Figure 7.**

TOTAL HARMONIC DISTORTION + NOISE
vs
FREQUENCY
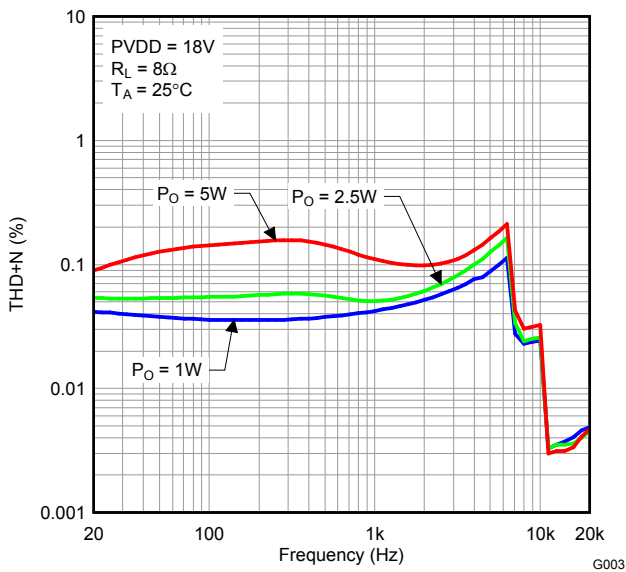


**Figure 8.**

TOTAL HARMONIC DISTORTION + NOISE
vs
FREQUENCY



**Figure 9.**

Product Folder Link(s): *TAS5711*

## TYPICAL CHARACTERISTICS, BTL CONFIGURATION (continued)

**TOTAL HARMONIC DISTORTION + NOISE**
**vs**
**OUTPUT POWER**
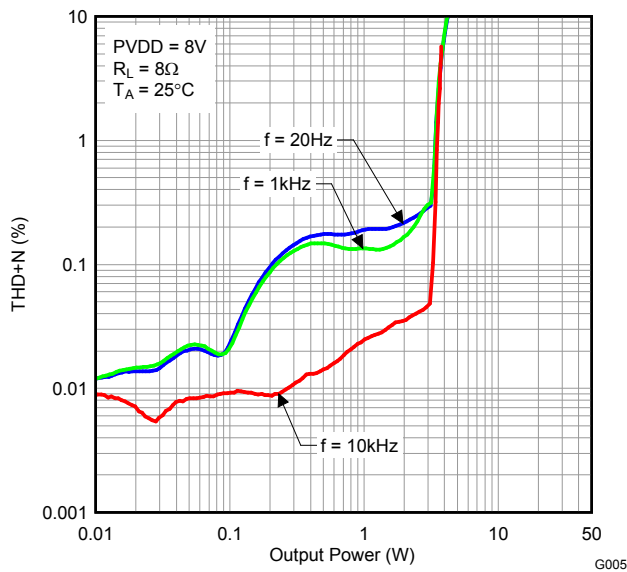


**Figure 10.**

**TOTAL HARMONIC DISTORTION + NOISE**
**vs**
**OUTPUT POWER**
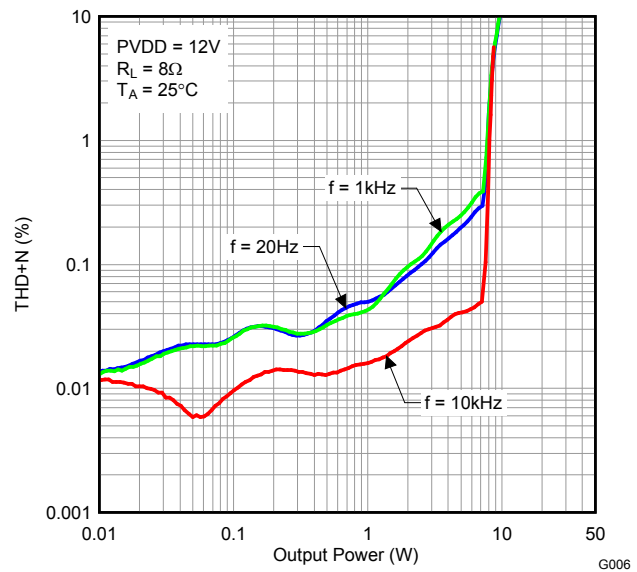


**Figure 11.**

**TOTAL HARMONIC DISTORTION + NOISE**
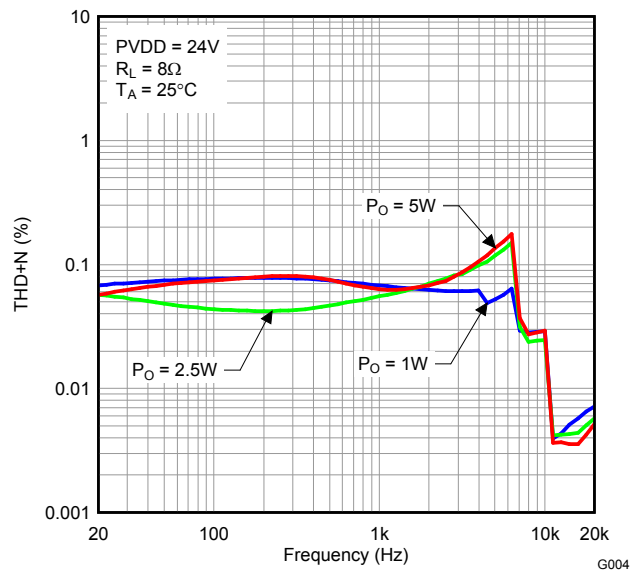**vs**
**OUTPUT POWER**
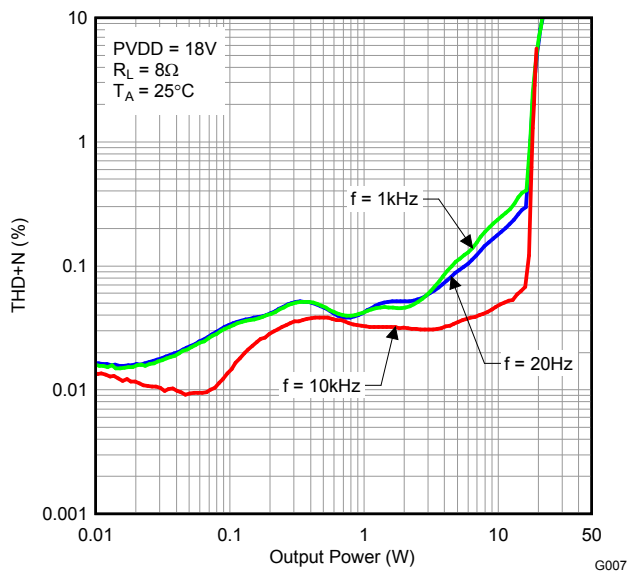


**Figure 12.**

**TOTAL HARMONIC DISTORTION + NOISE**
**vs**
**OUTPUT POWER**
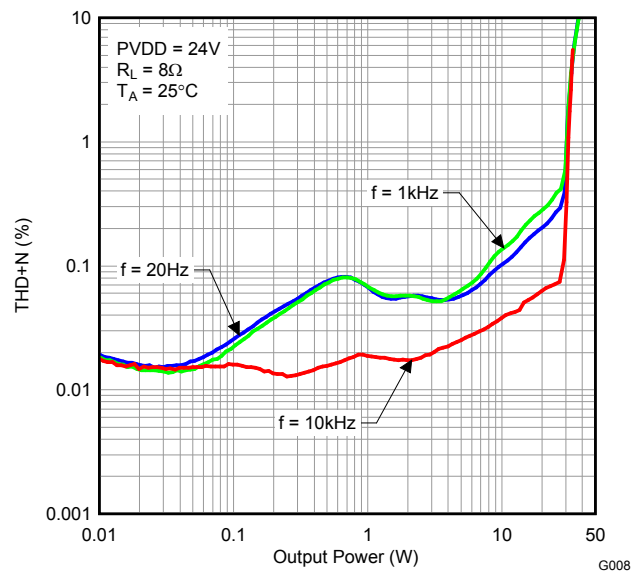


**Figure 13.**

## TYPICAL CHARACTERISTICS, BTL CONFIGURATION (continued)
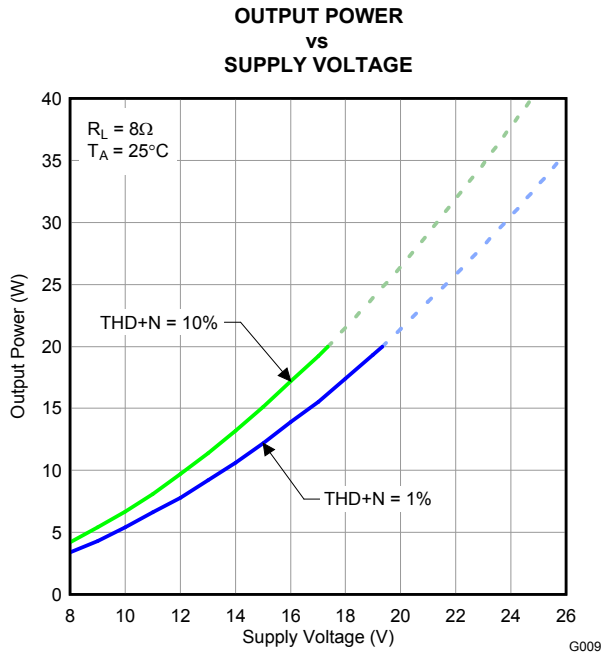
**OUTPUT POWER
vs
SUPPLY VOLTAGE**



NOTE: Dashed lines represent thermally limited region.

**Figure 14.**

**EFFICIENCY
vs
TOTAL OUTPUT POWER**



NOTE: Dashed lines represent thermally limited region.

**Figure 15.**

**CROSSTALK
vs
FREQUENCY**



**Figure 16.**

**CROSSTALK
vs
FREQUENCY**



**Figure 17.**

Product Folder Link(s): *TAS5711*
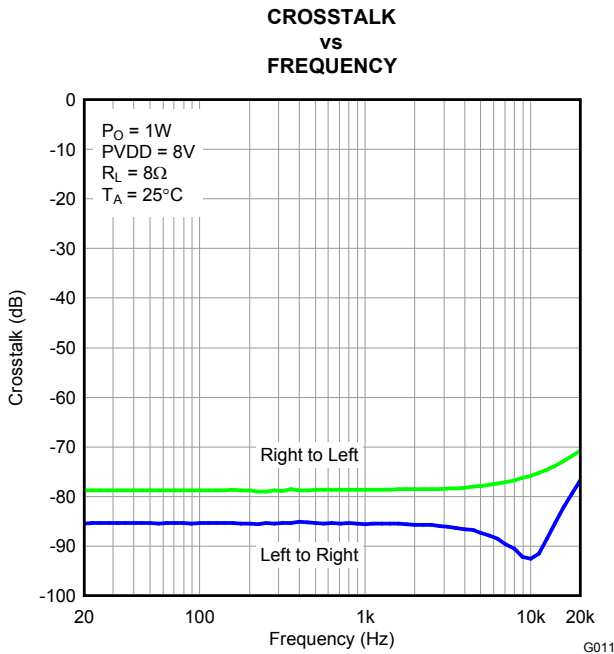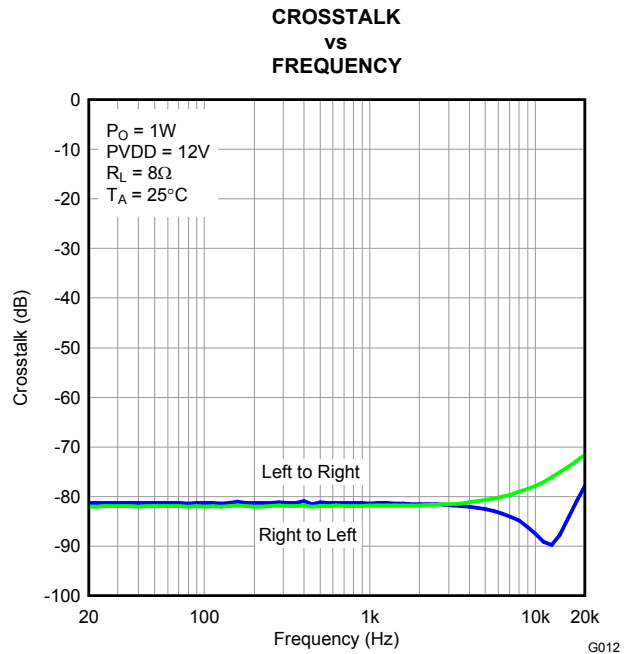
# TYPICAL CHARACTERISTICS, BTL CONFIGURATION (continued)

**CROSSTALK**
**vs**
**FREQUENCY**
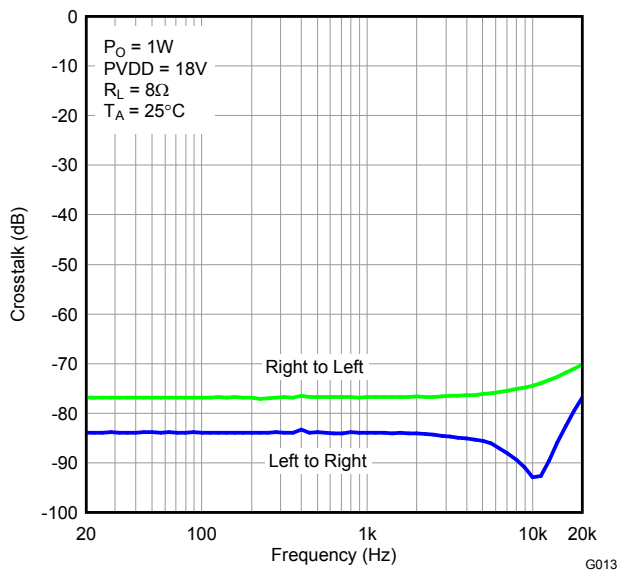


**Figure 18.**

**CROSSTALK**
**vs**
**FREQUENCY**
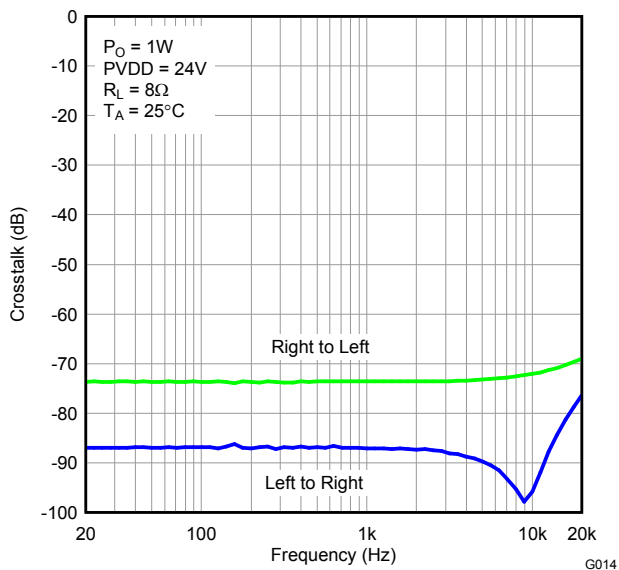


**Figure 19.**

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Product Folder Link(s): TAS5711

# TYPICAL CHARACTERISTICS, SE CONFIGURATION

TOTAL HARMONIC DISTORTION + NOISE
vs
FREQUENCY



PVDD = 12V
$R_L$ = 4Ω
$T_A$ = 25°C

$P_O$ = 2.5W

$P_O$ = 1W

$P_O$ = 0.5W

THD+N (%)

Frequency (Hz)

G015
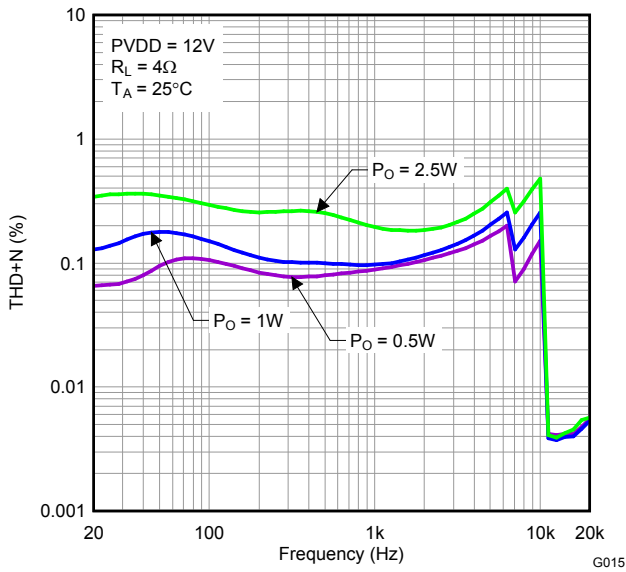
Figure 20.

TOTAL HARMONIC DISTORTION + NOISE
vs
FREQUENCY



PVDD = 18V
$R_L$ = 4Ω
$T_A$ = 25°C

$P_O$ = 5W

$P_O$ = 2.5W

$P_O$ = 1W

THD+N (%)

Frequency (Hz)

G016
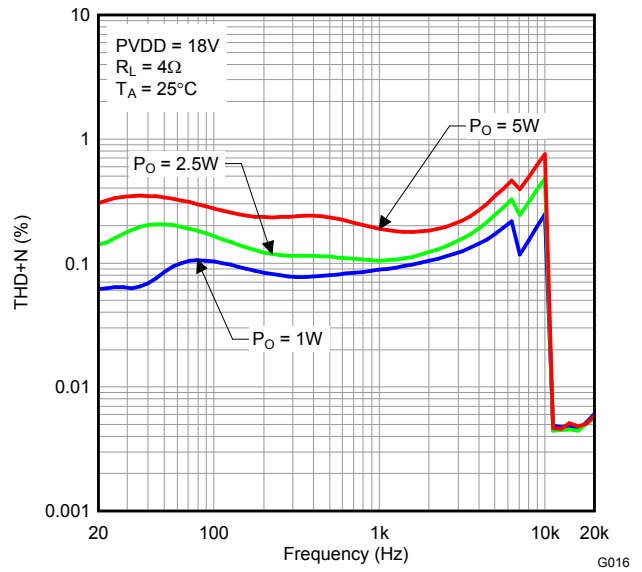
Figure 21.

TOTAL HARMONIC DISTORTION + NOISE
vs
FREQUENCY



PVDD = 24V
$R_L$ = 4Ω
$T_A$ = 25°C

$P_O$ = 5W

$P_O$ = 2.5W

$P_O$ = 1W

THD+N (%)

Frequency (Hz)

G017
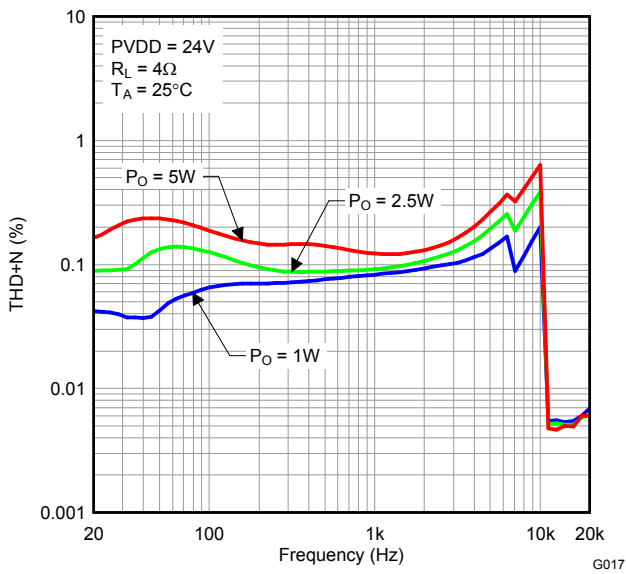
Figure 22.

TOTAL HARMONIC DISTORTION + NOISE
vs
OUTPUT POWER
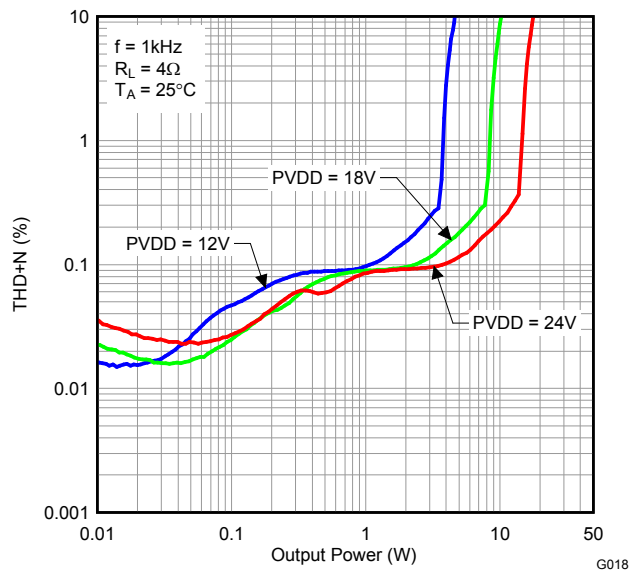


f = 1kHz
$R_L$ = 4Ω
$T_A$ = 25°C

PVDD = 18V

PVDD = 12V

PVDD = 24V

THD+N (%)

Output Power (W)

G018

Figure 23.

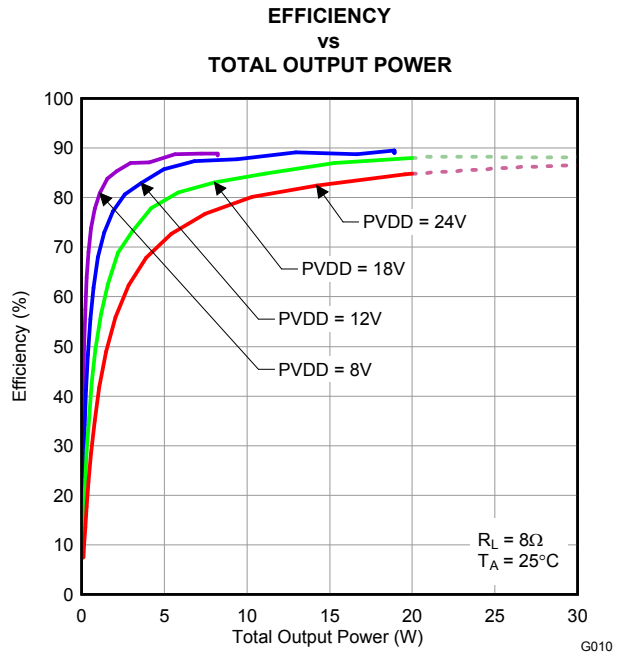Product Folder Link(s): *TAS5711*

# TYPICAL CHARACTERISTICS, SE CONFIGURATION (continued)

**OUTPUT POWER**
**vs**
**SUPPLY VOLTAGE**



NOTE:   Dashed lines represent thermally limited region.

**Figure 24.**

**EFFICIENCY**
**vs**
**TOTAL OUTPUT POWER**



**Figure 25.**

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Product Folder Link(s): TAS5711

**TEXAS INSTRUMENTS**

## TYPICAL CHARACTERISTICS, PBTL CONFIGURATION

**TOTAL HARMONIC DISTORTION + NOISE**
**vs**
**FREQUENCY**



PVDD = 8V
$R_L$ = 4Ω
$T_A$ = 25°C

$P_O$ = 5W
$P_O$ = 1W
$P_O$ = 2W

G021

**Figure 26.**

**TOTAL HARMONIC DISTORTION + NOISE**
**vs**
**FREQUENCY**



PVDD = 12V
$R_L$ = 4Ω
$T_A$ = 25°C

$P_O$ = 5W
$P_O$ = 1W
$P_O$ = 2W

G022

**Figure 27.**

**TOTAL HARMONIC DISTORTION + NOISE**
**vs**
**FREQUENCY**



PVDD = 18V
$R_L$ = 4Ω
$T_A$ = 25°C

$P_O$ = 5W
$P_O$ = 2W
$P_O$ = 1W

G023

**Figure 28.**

**TOTAL HARMONIC DISTORTION + NOISE**
**vs**
**FREQUENCY**



PVDD = 24V
$R_L$ = 4Ω
$T_A$ = 25°C

$P_O$ = 2W
$P_O$ = 5W
$P_O$ = 1W

G024

**Figure 29.**

Product Folder Link(s): *TAS5711*
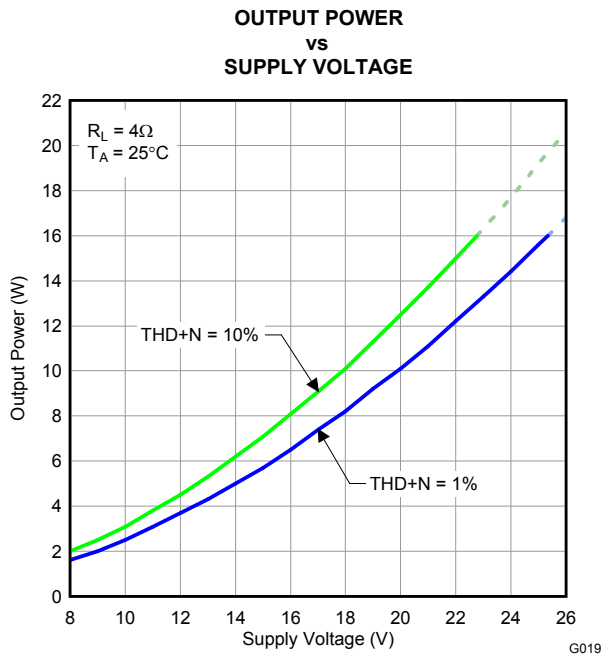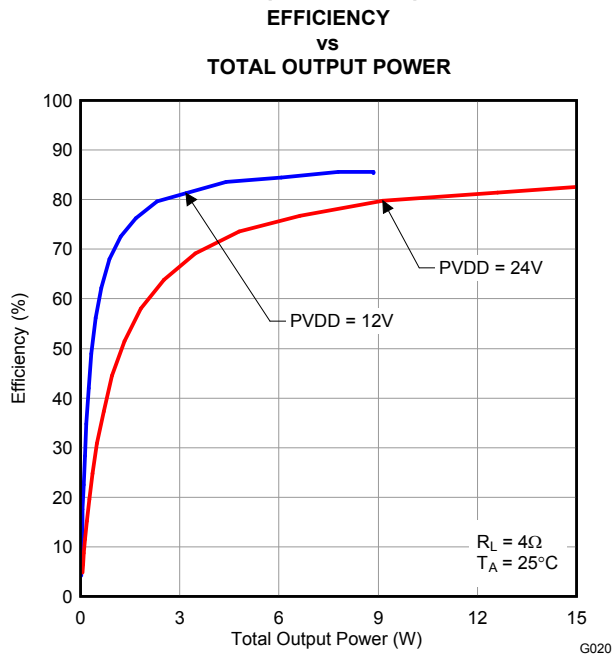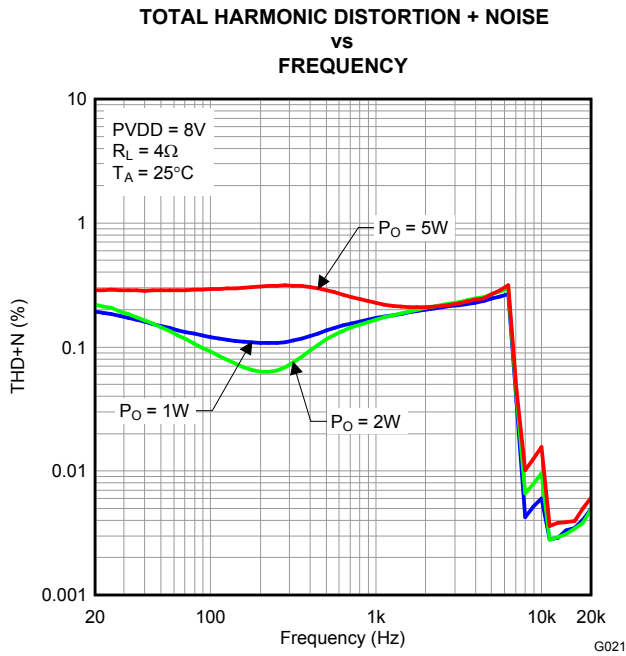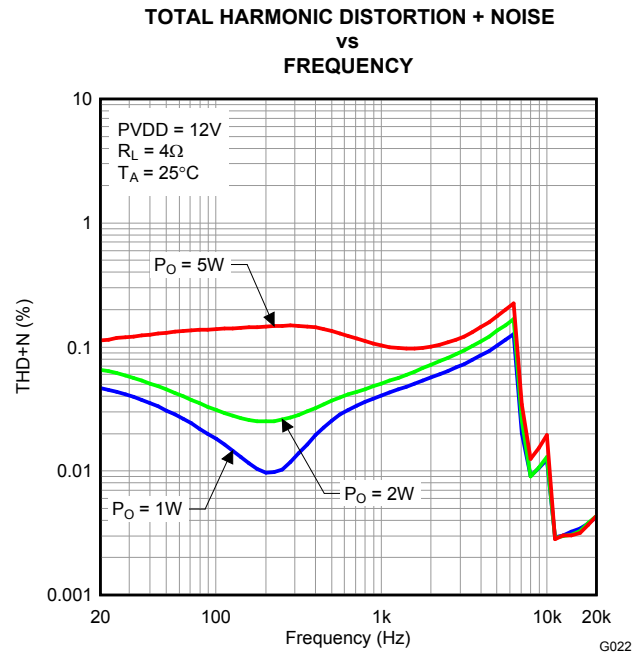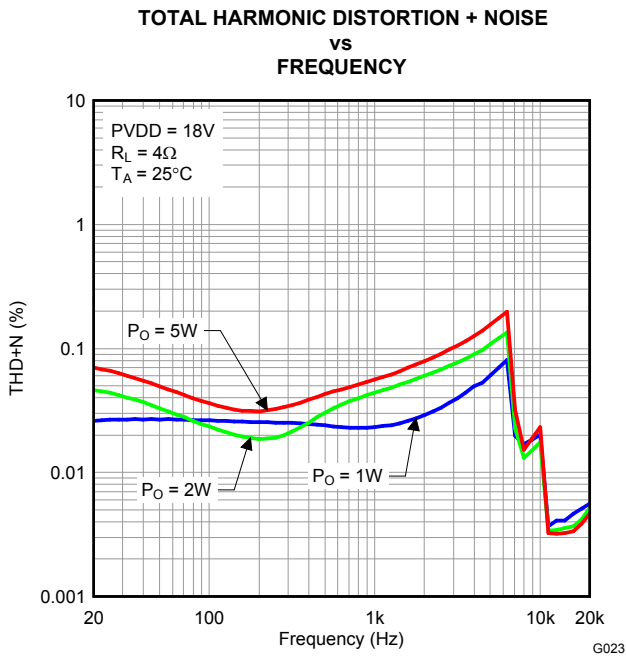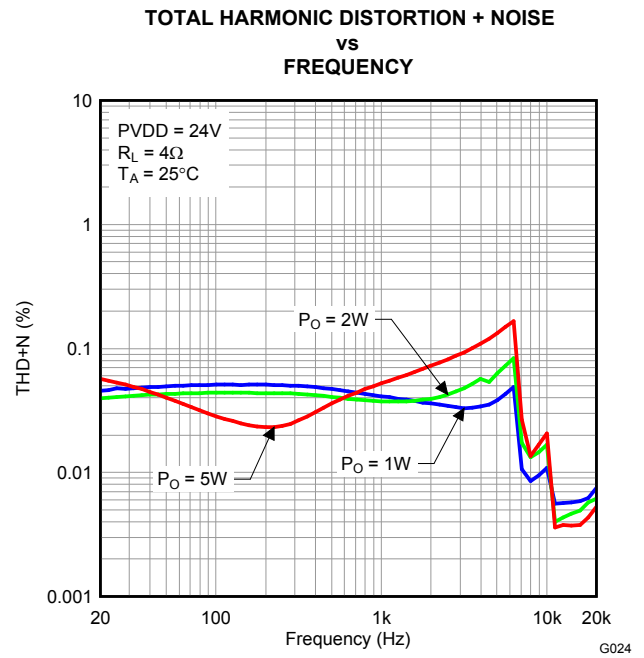
# TYPICAL CHARACTERISTICS, PBTL CONFIGURATION (continued)

**TOTAL HARMONIC DISTORTION + NOISE**
**vs**
**OUTPUT POWER**
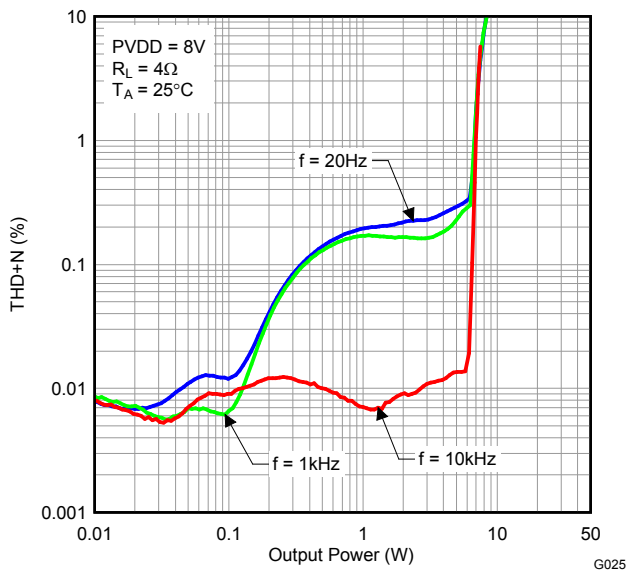


**Figure 30.**

**TOTAL HARMONIC DISTORTION + NOISE**
**vs**
**OUTPUT POWER**
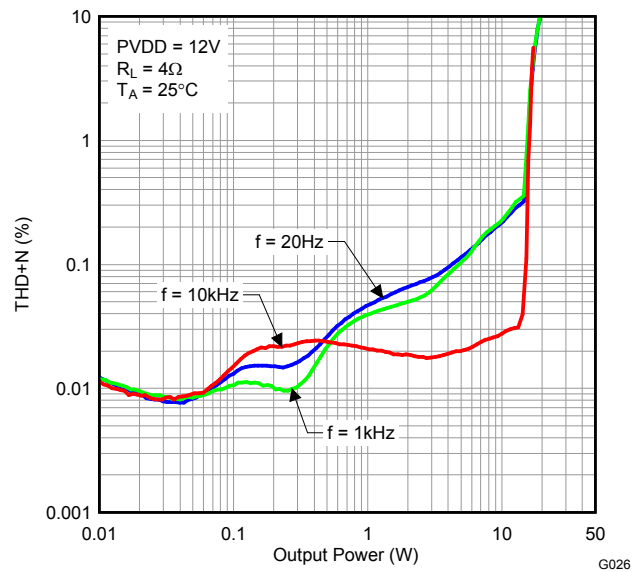


**Figure 31.**

**TOTAL HARMONIC DISTORTION + NOISE**
**vs**
**OUTPUT POWER**
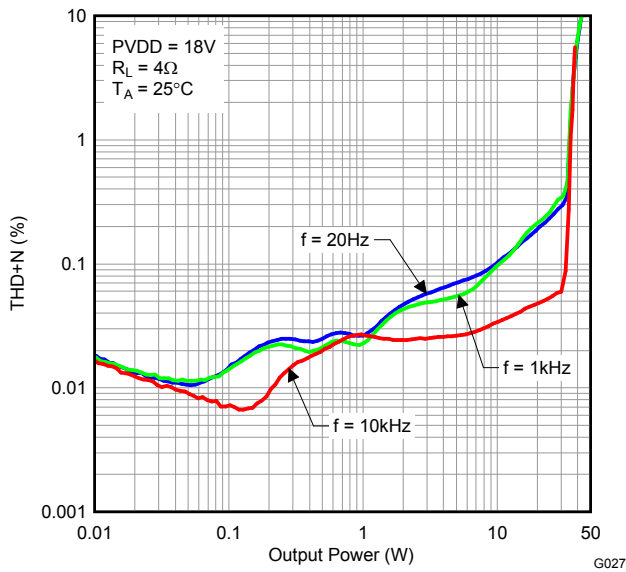


**Figure 32.**

**TOTAL HARMONIC DISTORTION + NOISE**
**vs**
**OUTPUT POWER**
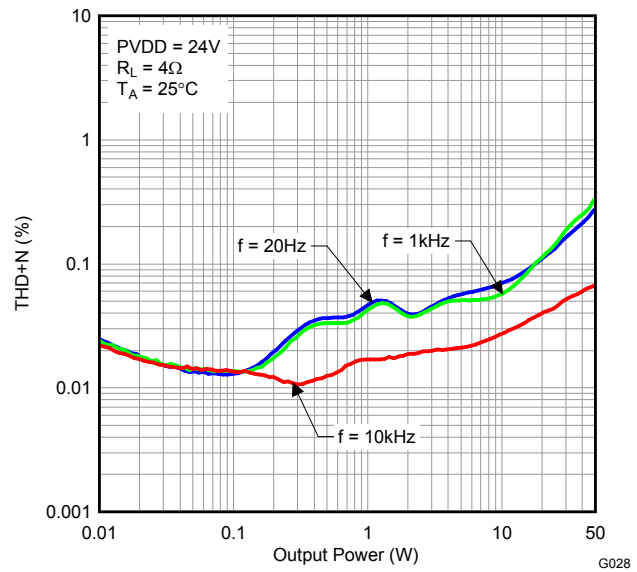


**Figure 33.**
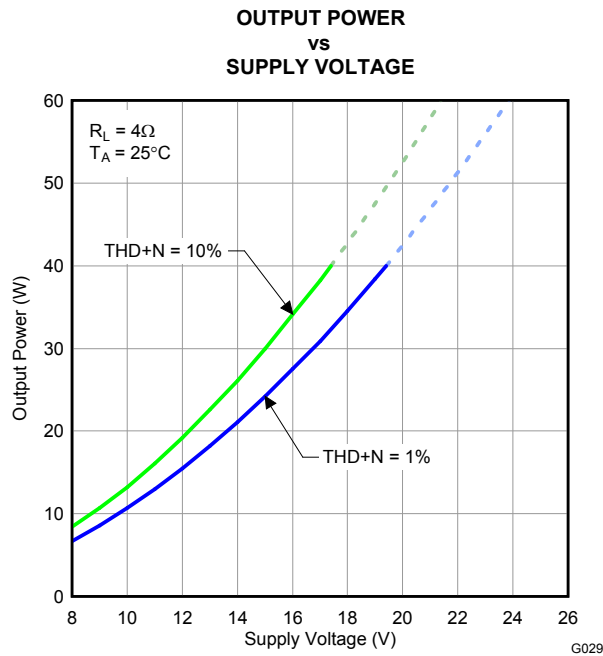
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Product Folder Link(s): TAS5711

## TYPICAL CHARACTERISTICS, PBTL CONFIGURATION (continued)

**OUTPUT POWER**
**vs**
**SUPPLY VOLTAGE**



NOTE:   Dashed lines represent thermally limited region.
**Figure 34.**

**EFFICIENCY**
**vs**
**TOTAL OUTPUT POWER**



NOTE:   Dashed lines represent thermally limited region.
**Figure 35.**

Product Folder Link(s): *TAS5711*
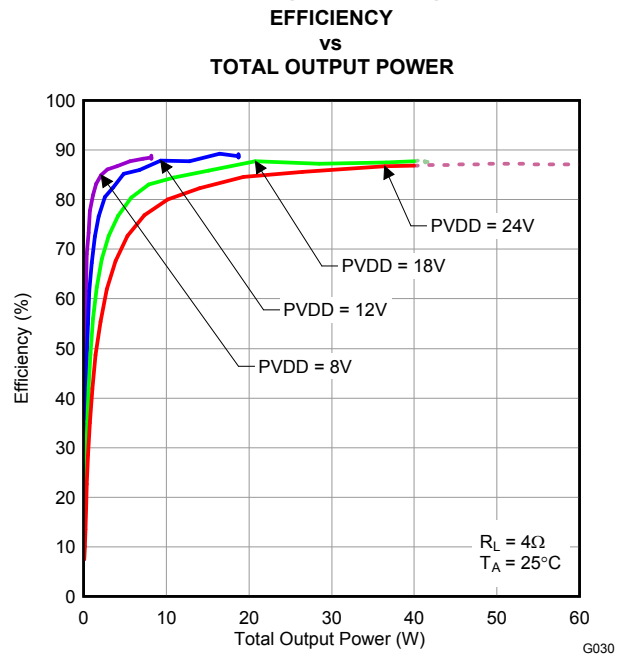
## DETAILED DESCRIPTION

### POWER SUPPLY

To facilitate system design, the TAS5711 needs only a 3.3-V supply in addition to the (typical) 18-V power-stage supply. An internal voltage regulator provides suitable voltage levels for the gate drive circuitry. Additionally, all circuitry requiring a floating voltage supply, e.g., the high-side gate drive, is accommodated by built-in bootstrap circuitry requiring only a few external capacitors.

In order to provide good electrical and acoustical characteristics, the PWM signal path for the output stage is designed as identical, independent half-bridges. For this reason, each half-bridge has separate bootstrap pins (BST_x), and power-stage supply pins (PVDD_x). The gate drive voltages (GVDD_AB and GVDD_CD) are derived from the PVDD voltage. Special attention should be paid to placing all decoupling capacitors as close to their associated pins as possible. In general, inductance between the power-supply pins and decoupling capacitors must be avoided.

For a properly functioning bootstrap circuit, a small ceramic capacitor must be connected from each bootstrap pin (BST_x) to the power-stage output pin (OUT_x). When the power-stage output is low, the bootstrap capacitor is charged through an internal diode connected between the gate-drive regulator output pin (GVDD_x) and the bootstrap pin. When the power-stage output is high, the bootstrap capacitor potential is shifted above the output potential and thus provides a suitable voltage supply for the high-side gate driver. In an application with PWM switching frequencies in the range from 352 kHz to 384 kHz, it is recommended to use 33-nF 50-V X7R capacitors, size 0603 or 0805, for the bootstrap supply. These 33-nF capacitors ensure sufficient energy storage, even during minimal PWM duty cycles, to keep the high-side power stage FET (LDMOS) fully turned on during the remaining part of the PWM cycle.

Special attention should be paid to the power-stage power supply; this includes component selection, PCB placement, and routing. As indicated, each half-bridge has independent power-stage supply pins (PVDD_x). For optimal electrical performance, EMC compliance, and system reliability, it is important that each PVDD_x pin is decoupled with a 100-nF ceramic capacitor placed as close as possible to each supply pin.

The TAS5711 is fully protected against erroneous power-stage turnon due to parasitic gate charging.

### ERROR REPORTING

The A_SEL pin has two functions: I²C device-address select and fault indication. On RESET, this pin is an input and defines the I²C address. But this pin can be programmed after RESET to be an output by writing 1 to bit 0 of I²C register 0x05. In that mode, the A_SEL pin has the definition shown in Table 1.

Any fault resulting in device shutdown is signaled by the A_SEL pin going low (see Table 1). A latched version of this pin is available on D1 of register 0x02. The bit can be cleared only by an I²C write.

**Table 1. $\overline{\text{FAULT}}$ Output States**

| $\overline{\text{FAULT}}$ | DESCRIPTION |
| --- | --- |
| 0 | Overcurrent (OC) or undervoltage (UVP) error or overtemperature error (OTE) or over voltage ERROR |
| 1 | No faults (normal operation) |

Product Folder Link(s): TAS5711

**Table 1. $\overline{\text{FAULT}}$ Output States (continued)**
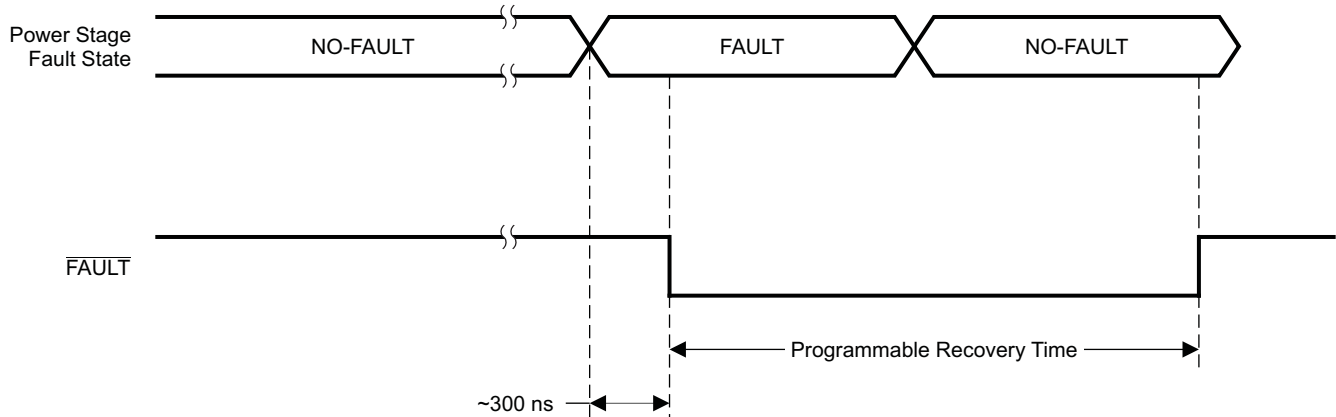


**Figure 36. Fault Timing Diagram**

## DEVICE PROTECTION SYSTEM

### Overcurrent (OC) Protection With Current Limiting

The device has independent, fast-reacting current detectors on all high-side and low-side power-stage FETs. The detector outputs are closely monitored by two protection systems. The first protection system controls the power stage in order to prevent the output current further increasing, i.e., it performs a cycle-by-cycle current-limiting function, rather than prematurely shutting down during combinations of high-level music transients and extreme speaker load impedance drops. If the high-current condition situation persists, i.e., the power stage is being overloaded, a second protection system triggers a latching shutdown, resulting in the power stage being set in the high-impedance (Hi-Z) state. The device returns to normal operation once the fault condition (i.e., a short circuit on the output) is removed. Current limiting and overcurrent protection are not independent for half-bridges. That is, if the bridge-tied load between half-bridges A and B causes an overcurrent fault, half-bridges A, B, C, and D are shut down.

### Overtemperature Protection

The TAS5711 has over temperature-protection system. If the device junction temperature exceeds 150°C (nominal), the device is put into thermal shutdown, resulting in all half-bridge outputs being set in the high-impedance (Hi-Z) state and $\overline{\text{FAULT}}$ being asserted low. The TAS5711 recovers automatically once the temperature drops approximately 30°.

### Undervoltage Protection (UVP) and Power-On Reset (POR)

The UVP and POR circuits of the TAS5711 fully protect the device in any power-up/down and brownout situation. While powering up, the POR circuit resets the overload circuit and ensures that all circuits are fully operational when the PVDD and AVDD supply voltages reach 7.6 V and 2.7 V, respectively. Although PVDD and AVDD are independently monitored, a supply voltage drop below the UVP threshold on AVDD or either PVDD pin results in all half-bridge outputs immediately being set in the high-impedance (Hi-Z) state and $\overline{\text{FAULT}}$ being asserted low.

## SSTIMER FUNCTIONALITY

The SSTIMER pin uses a capacitor connected between this pin and ground to control the output duty cycle when exiting all-channel shutdown. The capacitor on the SSTIMER pin is slowly charged through an internal current source, and the charge time determines the rate at which the output transitions from a near zero duty cycle to the desired duty cycle. This allows for a smooth transition that minimizes audible pops and clicks. When the part is shutdown the drivers are tristated and transition slowly down through a 3K resistor, similarly minimizing pops and clicks. The shutdown transition time is independent of SSTIMER pin capacitance. Larger capacitors will increase the start-up time, while capacitors smaller than 2.2 nF will decrease the start-up time. The SSTIMER pin should be left floating for BD modulation (BTL and PBTL modes) and in 2.1 mode.

## CLOCK, AUTO DETECTION, AND PLL

The TAS5711 is a slave device. It accepts MCLK, SCLK, and LRCLK. The digital audio processor (DAP) supports all the sample rates and MCLK rates that are defined in the clock control register .

The TAS5711 checks to verify that SCLK is a specific value of 32 $f_S$, 48 $f_S$, or 64 $f_S$. The DAP only supports a 1 × $f_S$ LRCLK. The timing relationship of these clocks to SDIN is shown in subsequent sections. The clock section uses MCLK or the internal oscillator clock (when MCLK is unstable, out of range, or absent) to produce the internal clock (DCLK) running at 512 time the PWM switching frequency.

The DAP can autodetect and set the internal clock control logic to the appropriate settings for all supported clock rates as defined in the clock control register.

TAS5711 has robust clock error handling that uses the bulit-in trimmed oscillator clock to quickly detect changes/errors. Once the system detects a clock change/error, it will mute the audio (through a single step mute) and then force PLL to limp using the internal oscillator as a reference clock. Once the clocks are stable, the system will auto detect the new rate and revert to normal operation. During this process, the default volume will be restored in a single step (also called hard unmute). The ramp process can be programmed to ramp back slowly (also called soft unmute) as defined in volume register (0x0E).

## SERIAL DATA INTERFACE

Serial data is input on SDIN. The PWM outputs are derived from SDIN. The TAS5711 DAP accepts serial data in 16-, 20-, or 24-bit left-justified, right-justified, and I²S serial data formats.

## PWM Section

The TAS5711 DAP device uses noise-shaping and sophisticated non-linear correction algorithms to achieve high power efficiency and high-performance digital audio reproduction. The DAP uses a fourth-order noise shaper to increase dynamic range and SNR in the audio band. The PWM section accepts 24-bit PCM data from the DAP and outputs two BTL PWM audio output channels.

The PWM section has individual channel dc blocking filters that can be enabled and disabled. The filter cutoff frequency is less than 1 Hz. Individual channel de-emphasis filters for 44.1- and 48-kHz are included and can be enabled and disabled.

Finally, the PWM section has an adjustable maximum modulation limit of 93.8% to 99.2%.

For detailed description of using audio processing features like DRC, EQ, 3D, and Bass Boost, please refer to User's Guide and TAS570X GDE software development tool documentation. Also refer to GDE software development tool for device data path.

## SERIAL INTERFACE CONTROL AND TIMING

The I²S mode is set by writing to register 0x04.

### I²S Timing

I²S timing uses LRCLK to define when the data being transmitted is for the left channel and when it is for the right channel. LRCLK is low for the left channel and high for the right channel. A bit clock running at 32, 48, or 64 × $f_S$ is used to clock in the data. There is a delay of one bit clock from the time the LRCLK signal changes state to the first bit of data on the data lines. The data is written MSB first and is valid on the rising edge of bit clock. The DAP masks unused trailing data bit positions.

2-Channel I²S (Philips Format) Stereo Input
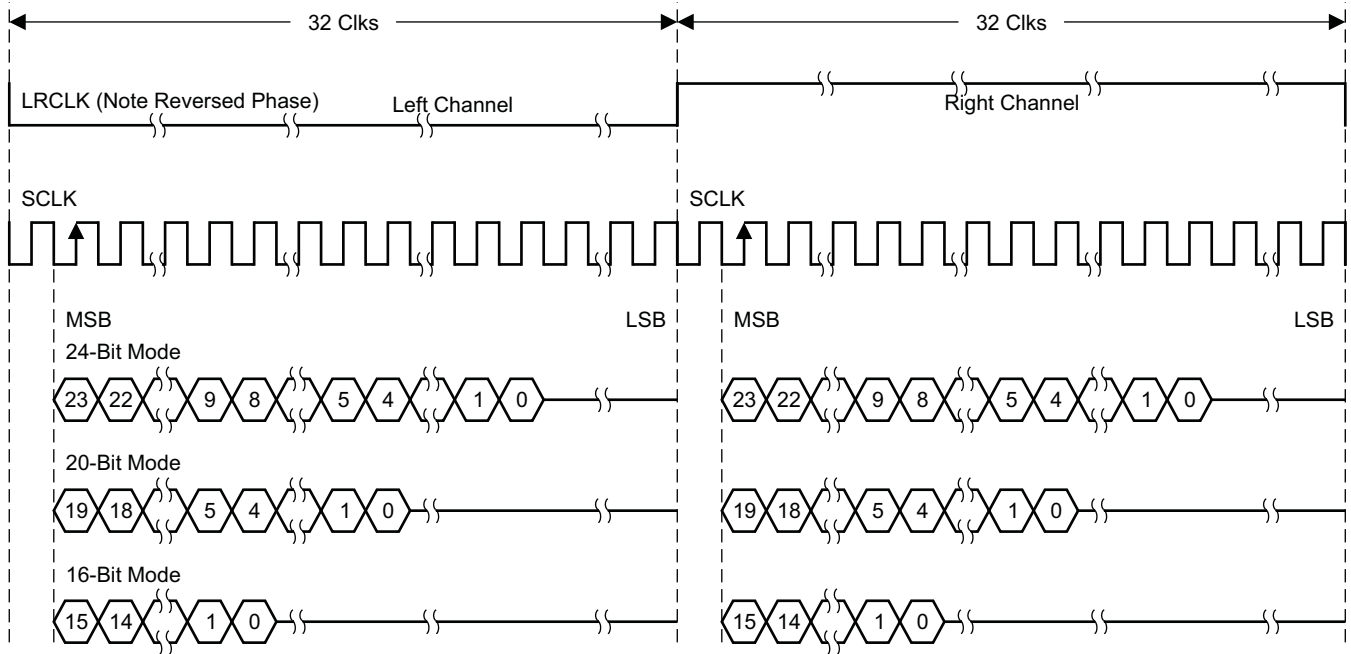


NOTE: All data presented in 2s-complement form with MSB first.

**Figure 37. I²S 64-f$_S$ Format**

2-Channel I²S (Philips Format) Stereo Input/Output (24-Bit Transfer Word Size)
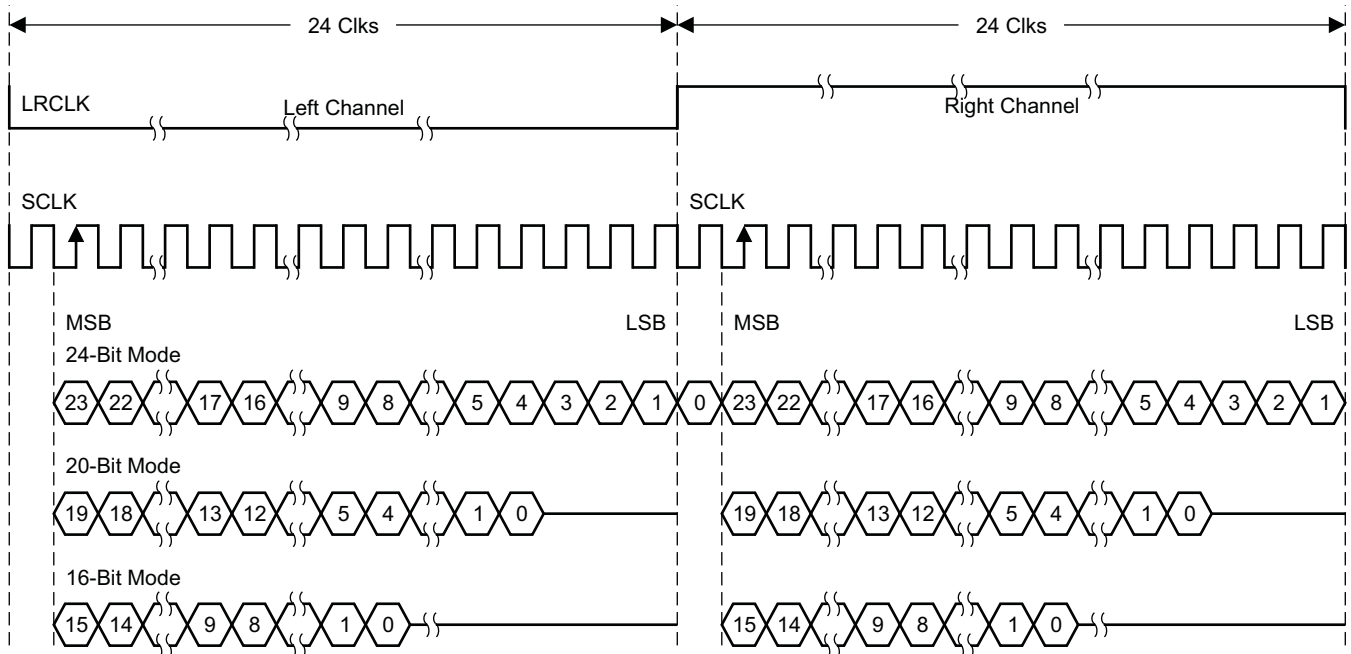


NOTE: All data presented in 2s-complement form with MSB first.

**Figure 38. I²S 48-f$_S$ Format**

Product Folder Link(s): *TAS5711*

2-Channel I²S (Philips Format) Stereo Input
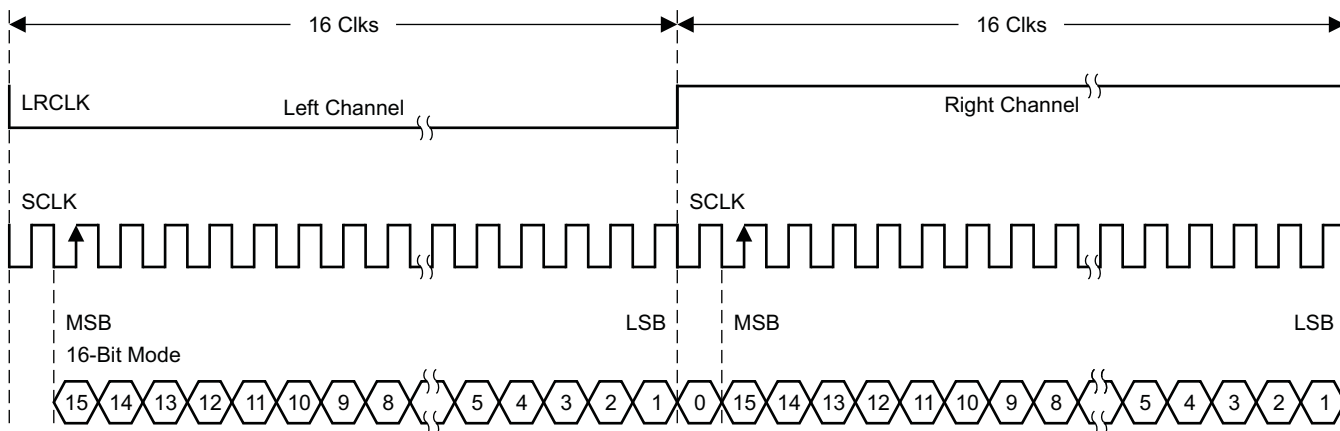


NOTE:  All data presented in 2s-complement form with MSB first.

**Figure 39.  I²S 32-f$_S$ Format**

## Left-Justified

Left-justified (LJ) timing uses LRCLK to define when the data being transmitted is for the left channel and when it is for the right channel. LRCLK is high for the left channel and low for the right channel. A bit clock running at 32, 48, or 64 × f$_S$ is used to clock in the data. The first bit of data appears on the data lines at the same time LRCLK toggles. The data is written MSB first and is valid on the rising edge of the bit clock. The DAP masks unused trailing data bit positions.

2-Channel Left-Justified Stereo Input
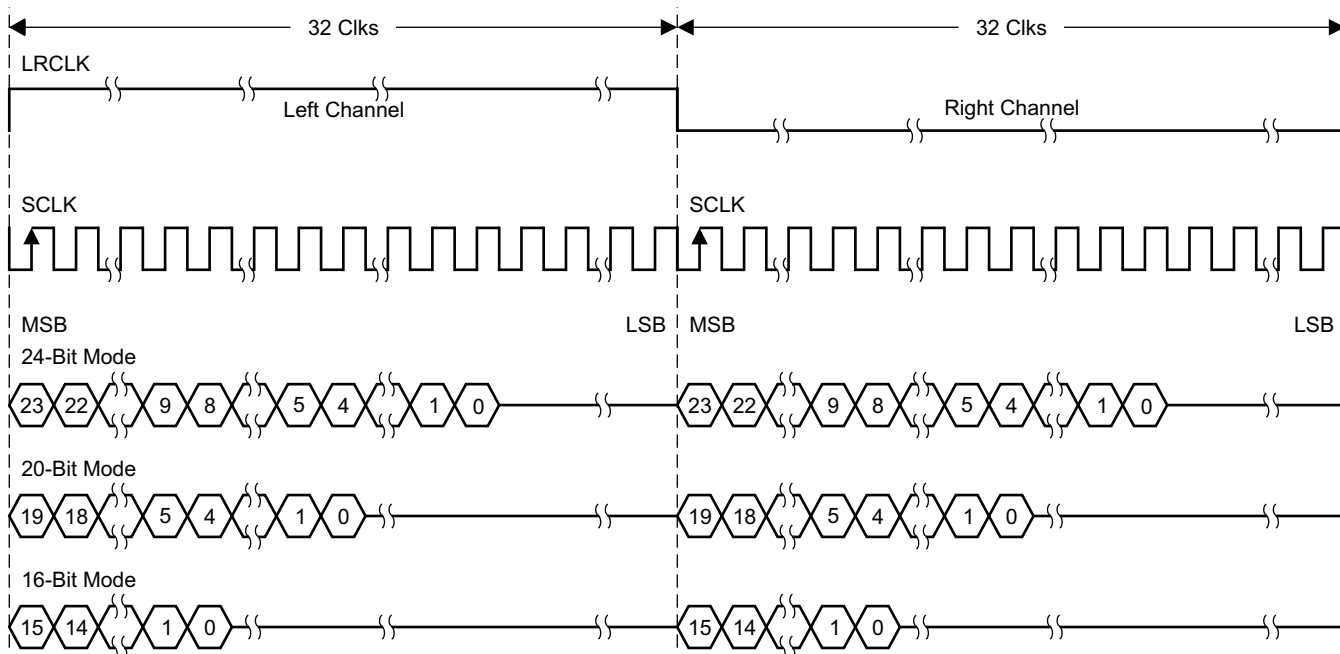


NOTE:  All data presented in 2s-complement form with MSB first.

**Figure 40.  Left-Justified 64-f$_S$ Format**

2-Channel Left-Justified Stereo Input (24-Bit Transfer Word Size)
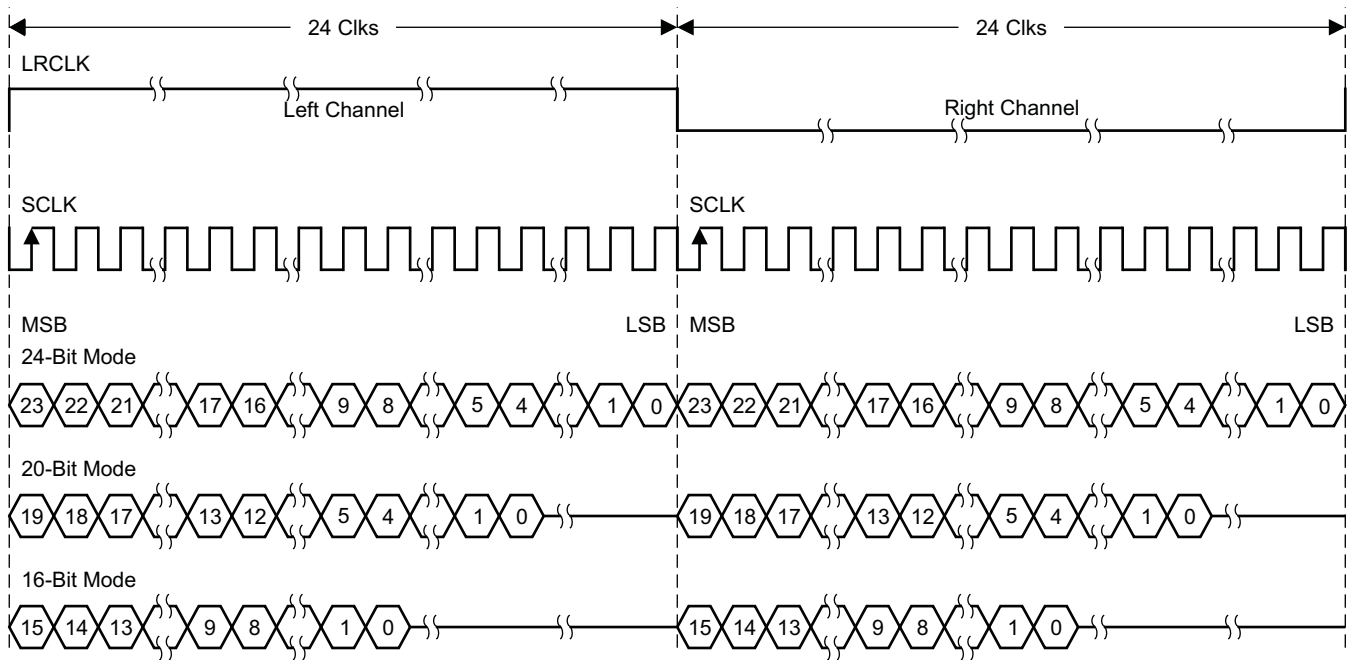


NOTE: All data presented in 2s-complement form with MSB first.

**Figure 41. Left-Justified 48-f$_S$ Format**

2-Channel Left-Justified Stereo Input
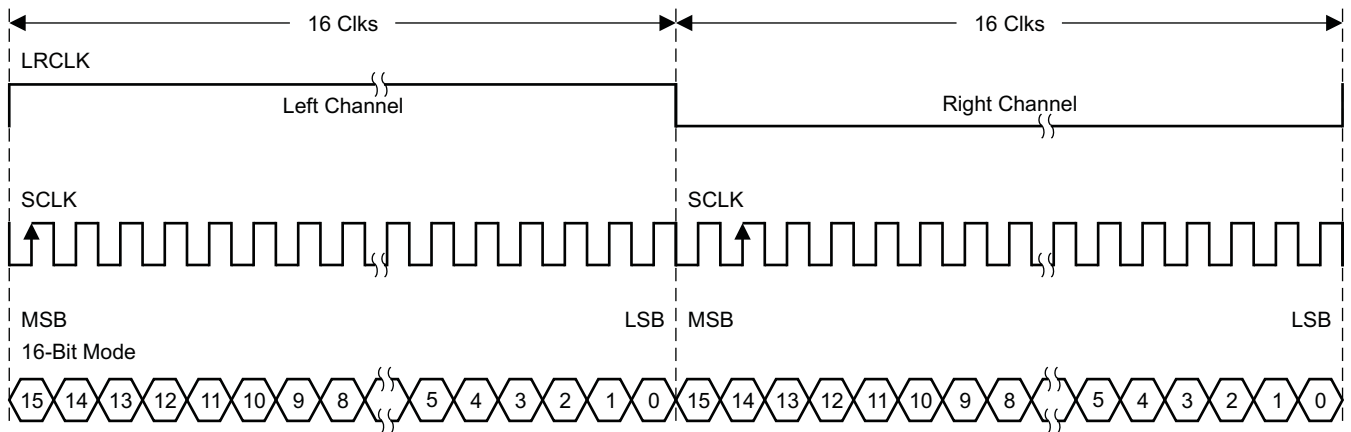


NOTE: All data presented in 2s-complement form with MSB first.

**Figure 42. Left-Justified 32-f$_S$ Format**

## Right-Justified

Right-justified (RJ) timing uses LRCLK to define when the data being transmitted is for the left channel and when

it is for the right channel. LRCLK is high for the left channel and low for the right channel. A bit clock running at 32, 48, or 64 × f$_S$ is used to clock in the data. The first bit of data appears on the data 8 bit-clock periods (for 24-bit data) after LRCLK toggles. In RJ mode the LSB of data is always clocked by the last bit clock before LRCLK transitions. The data is written MSB first and is valid on the rising edge of bit clock. The DAP masks unused leading data bit positions.

2-Channel Right-Justified (Sony Format) Stereo Input
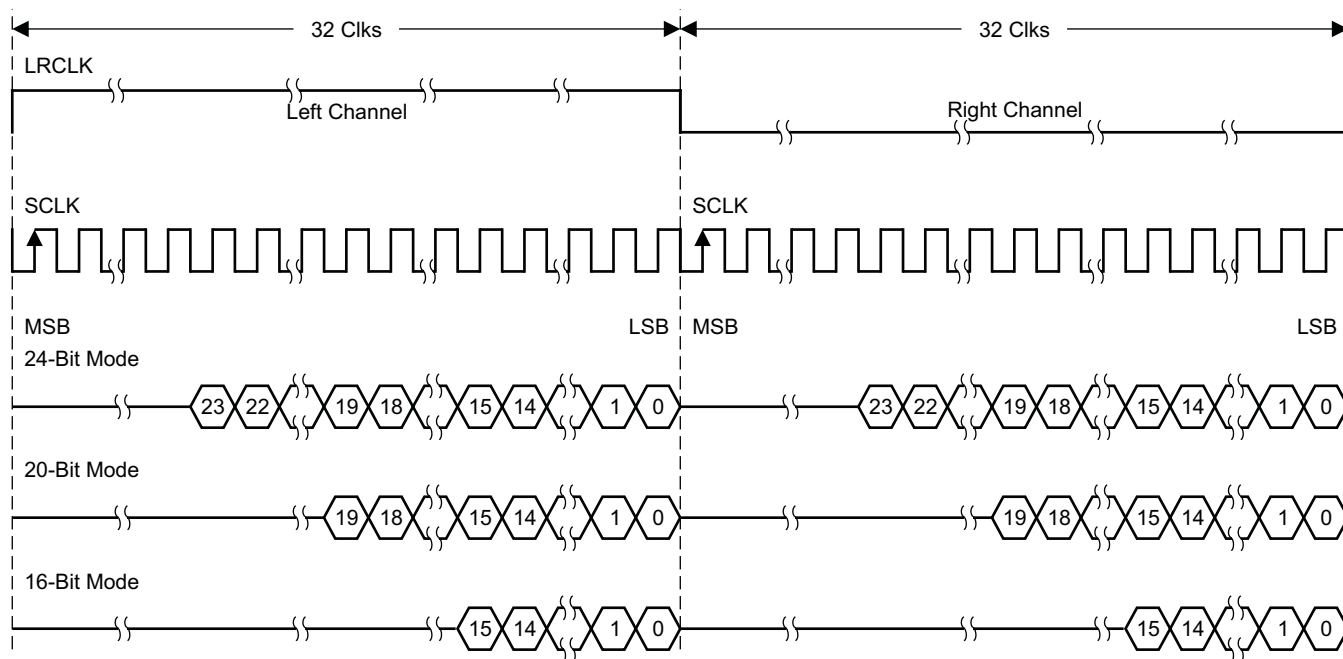
**Figure 43. Right Justified 64-f$_S$ Format**

2-Channel Right-Justified Stereo Input (24-Bit Transfer Word Size)
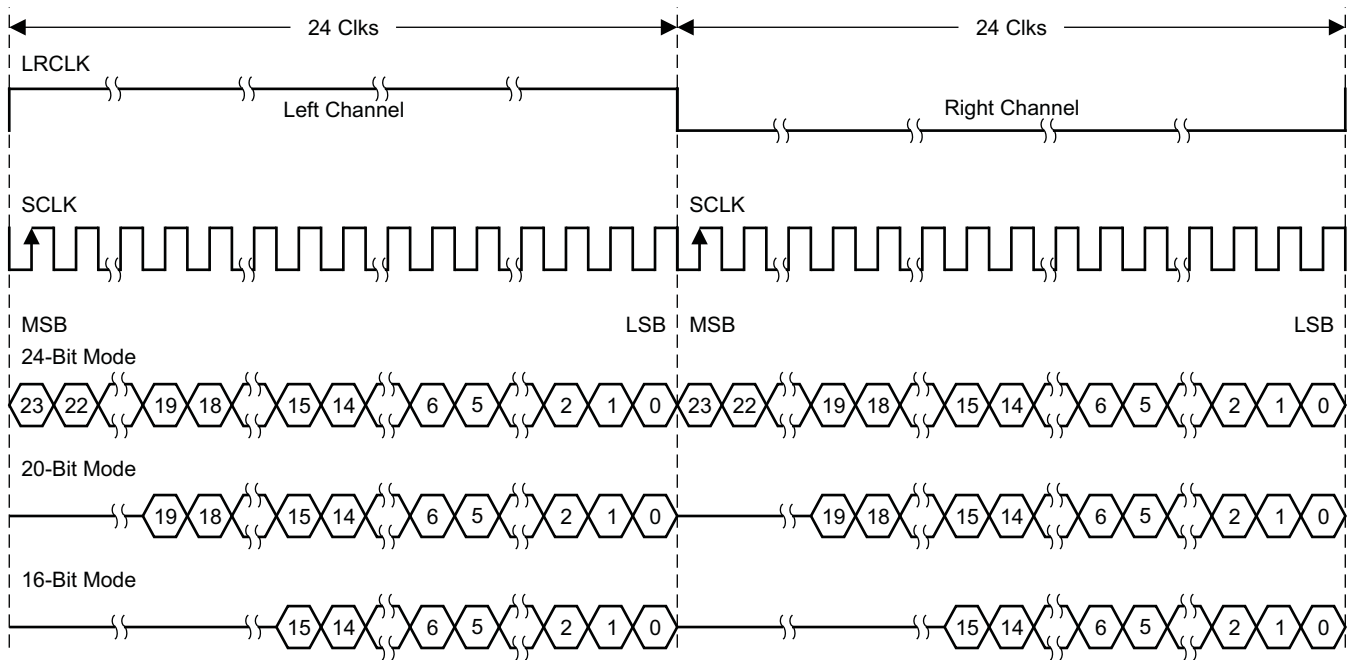


**Figure 44. Right Justified 48-f$_S$ Format**

2-Channel Right-Justified (Sony Format) Stereo Input
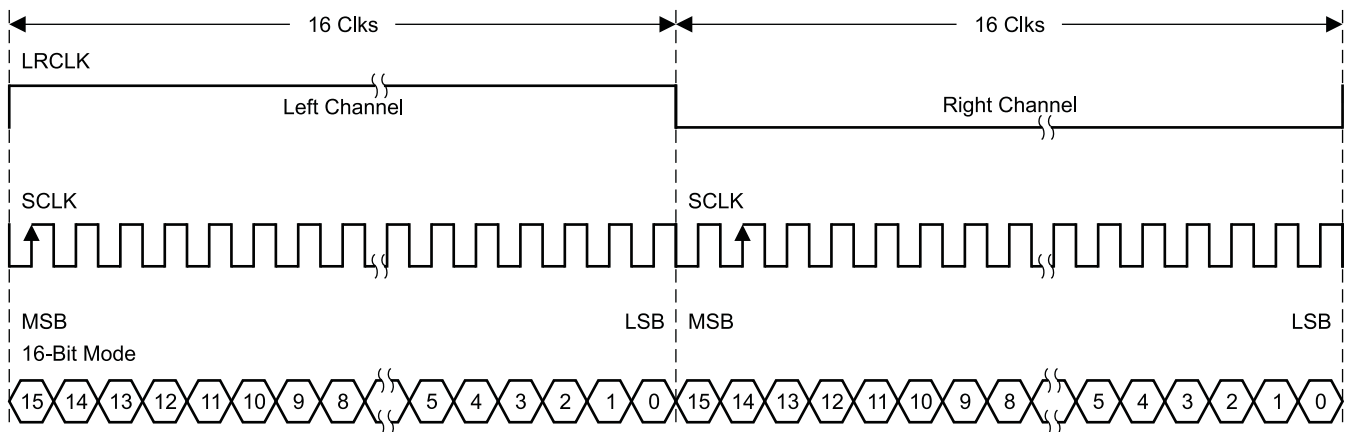


**Figure 45. Right Justified 32-f$_S$ Format**

Product Folder Link(s): TAS5711

## I²C SERIAL CONTROL INTERFACE

The TAS5711 DAP has a bidirectional I²C interface that compatible with the I²C (Inter IC) bus protocol and supports both 100-kHz and 400-kHz data transfer rates for single and multiple byte write and read operations. This is a slave only device that does not support a multimaster bus environment or wait state insertion. The control interface is used to program the registers of the device and to read device status.

The DAP supports the standard-mode I²C bus operation (100 kHz maximum) and the fast I²C bus operation (400 kHz maximum). The DAP performs all I²C operations without I²C wait cycles.

### General I²C Operation

The I²C bus employs two signals; SDA (data) and SCL (clock), to communicate between integrated circuits in a system. Data is transferred on the bus serially one bit at a time. The address and data can be transferred in byte (8-bit) format, with the most significant bit (MSB) transferred first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus. The bus uses transitions on the data pin (SDA) while the clock is high to indicate a start and stop conditions. A high-to-low transition on SDA indicates a start and a low-to-high transition indicates a stop. Normal data bit transitions must occur within the low time of the clock period. These conditions are shown in Figure 46. The master generates the 7-bit slave address and the read/write (R/W̄) bit to open communication with another device and then waits for an acknowledge condition. The TAS5711 holds SDA low during the acknowledge clock period to indicate an acknowledgment. When this occurs, the master transmits the next byte of the sequence. Each device is addressed by a unique 7-bit slave address plus R/W̄ bit (1 byte). All compatible devices share the same signals via a bidirectional bus using a wired-AND connection. An external pullup resistor must be used for the SDA and SCL signals to set the high level for the bus.
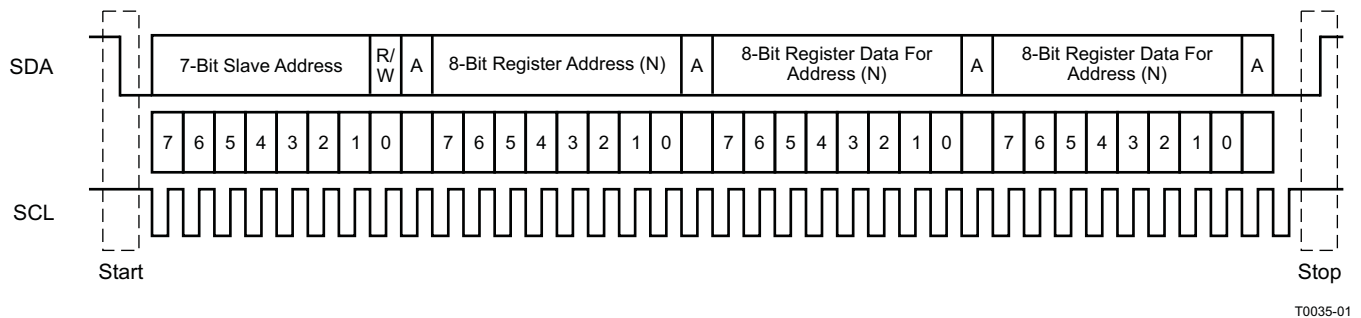


**Figure 46. Typical I²C Sequence**

There is no limit on the number of bytes that can be transmitted between start and stop conditions. When the last word transfers, the master generates a stop condition to release the bus. A generic data transfer sequence is shown in Figure 46.

Pin A̅_̅S̅E̅L̅ defines the I²C device address. An external 15-kΩ pulldown on this pin gives a device address of 0x34 and a 15-kΩ pullup gives a device address of 0x36. The 7-bit address is 0011011 (0x36) or 0011010 (0x34).

### I²C Device Address Change Procedure

- Write to device address change enable register, 0xF8 with a value of 0xF9 A5 A5 A5.
- Write to device register 0xF9 with a value of 0x0000 00XX, where XX is the new address.
- Any writes after that should use the new device address XX.

### Single- and Multiple-Byte Transfers

The serial control interface supports both single-byte and multiple-byte read/write operations for subaddresses 0x00 to 0x1F. However, for the subaddresses 0x20 to 0xFF, the serial control interface supports only multiple-byte read/write operations (in multiples of 4 bytes).

During multiple-byte read operations, the DAP responds with data, a byte at a time, starting at the subaddress assigned, as long as the master device continues to respond with acknowledges. If a particular subaddress does not contain 32 bits, the unused bits are read as logic 0.

During multiple-byte write operations, the DAP compares the number of bytes transmitted to the number of bytes that are required for each specific subaddress. For example, if a write command is received for a biquad subaddress, the DAP expects to receive five 32-bit words. If fewer than five 32-bit data words have been received when a stop command (or another start command) is received, the data received is discarded.

Supplying a subaddress for each subaddress transaction is referred to as random I²C addressing. The TAS5711 also supports sequential I²C addressing. For write transactions, if a subaddress is issued followed by data for that subaddress and the 15 subaddresses that follow, a sequential I²C write transaction has taken place, and the data for all 16 subaddresses is successfully received by the TAS5711. For I²C sequential write transactions, the subaddress then serves as the start address, and the amount of data subsequently transmitted, before a stop or start is transmitted, determines how many subaddresses are written. As was true for random addressing, sequential addressing requires that a complete set of data be transmitted. If only a partial set of data is written to the last subaddress, the data for the last subaddress is discarded. However, all other data written is accepted; only the incomplete data is discarded.

### Single-Byte Write

As shown in Figure 47, a single-byte data write transfer begins with the master device transmitting a start condition followed by the I²C device address and the read/write bit. The read/write bit determines the direction of the data transfer. For a write data transfer, the read/write bit will be a 0. After receiving the correct I²C device address and the read/write bit, the DAP responds with an acknowledge bit. Next, the master transmits the address byte or bytes corresponding to the TAS5711 internal memory address being accessed. After receiving the address byte, the TAS5711 again responds with an acknowledge bit. Next, the master device transmits the data byte to be written to the memory address being accessed. After receiving the data byte, the TAS5711 again responds with an acknowledge bit. Finally, the master device transmits a stop condition to complete the single-byte data write transfer.
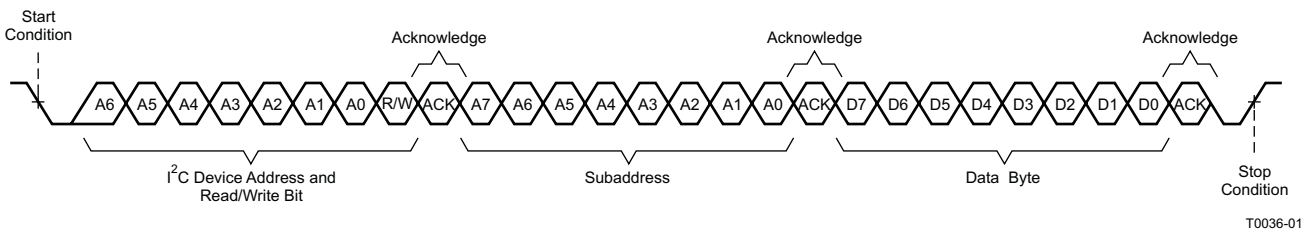


**Figure 47. Single-Byte Write Transfer**

### Multiple-Byte Write

A multiple-byte data write transfer is identical to a single-byte data write transfer except that multiple data bytes are transmitted by the master device to the DAP as shown in Figure 48. After receiving each data byte, the TAS5711 responds with an acknowledge bit.
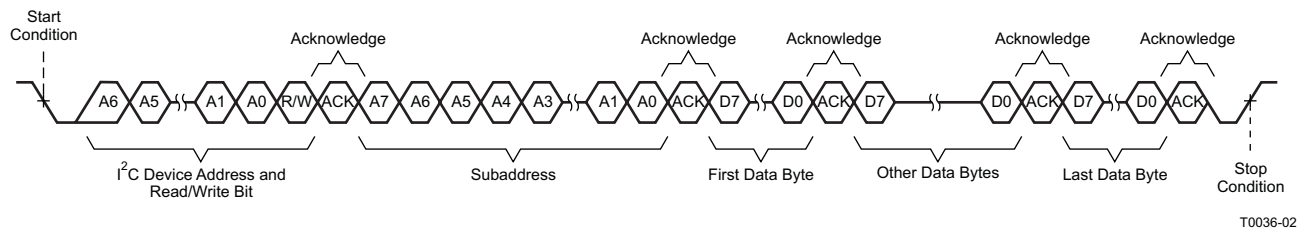


**Figure 48. Multiple-Byte Write Transfer**

Product Folder Link(s): *TAS5711*

## Single-Byte Read

As shown in Figure 49, a single-byte data read transfer begins with the master device transmitting a start condition followed by the I²C device address and the read/write bit. For the data read transfer, both a write followed by a read are actually done. Initially, a write is done to transfer the address byte or bytes of the internal memory address to be read. As a result, the read/write bit becomes a 0. After receiving the TAS5711 address and the read/write bit, TAS5711 responds with an acknowledge bit. In addition, after sending the internal memory address byte or bytes, the master device transmits another start condition followed by the TAS5711 address and the read/write bit again. This time the read/write bit becomes a 1, indicating a read transfer. After receiving the address and the read/write bit, the TAS5711 again responds with an acknowledge bit. Next, the TAS5711 transmits the data byte from the memory address being read. After receiving the data byte, the master device transmits a not acknowledge followed by a stop condition to complete the single byte data read transfer.
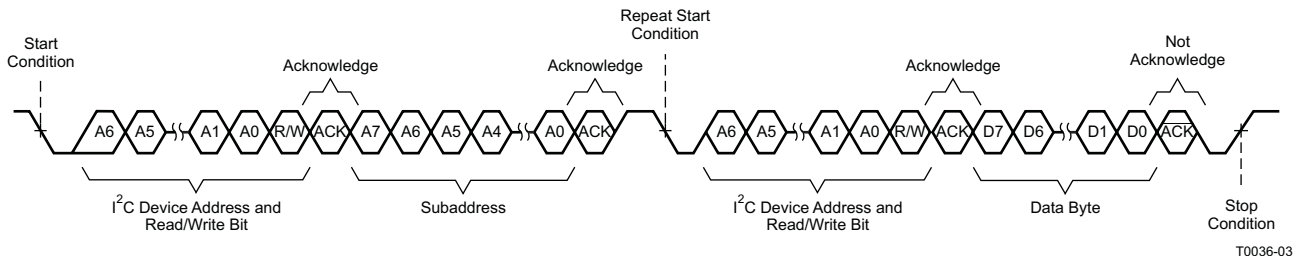


**Figure 49. Single-Byte Read Transfer**

## Multiple-Byte Read

A multiple-byte data read transfer is identical to a single-byte data read transfer except that multiple data bytes are transmitted by the TAS5711 to the master device as shown in Figure 50. Except for the last data byte, the master device responds with an acknowledge bit after receiving each data byte.
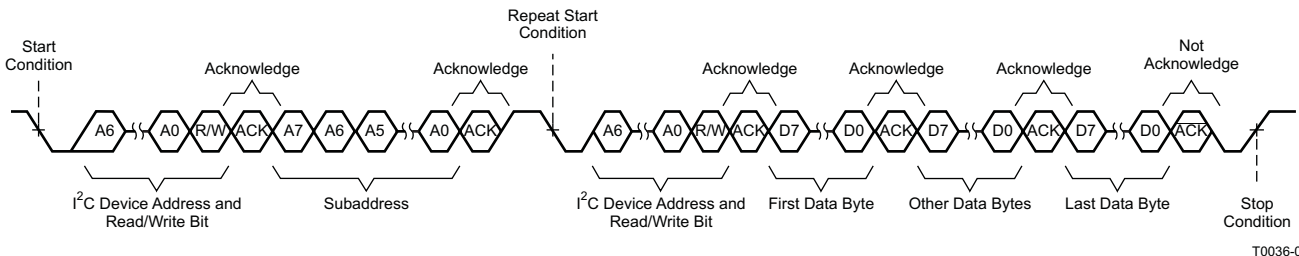


**Figure 50. Multiple Byte Read Transfer**

## Output Mode and MUX Selection
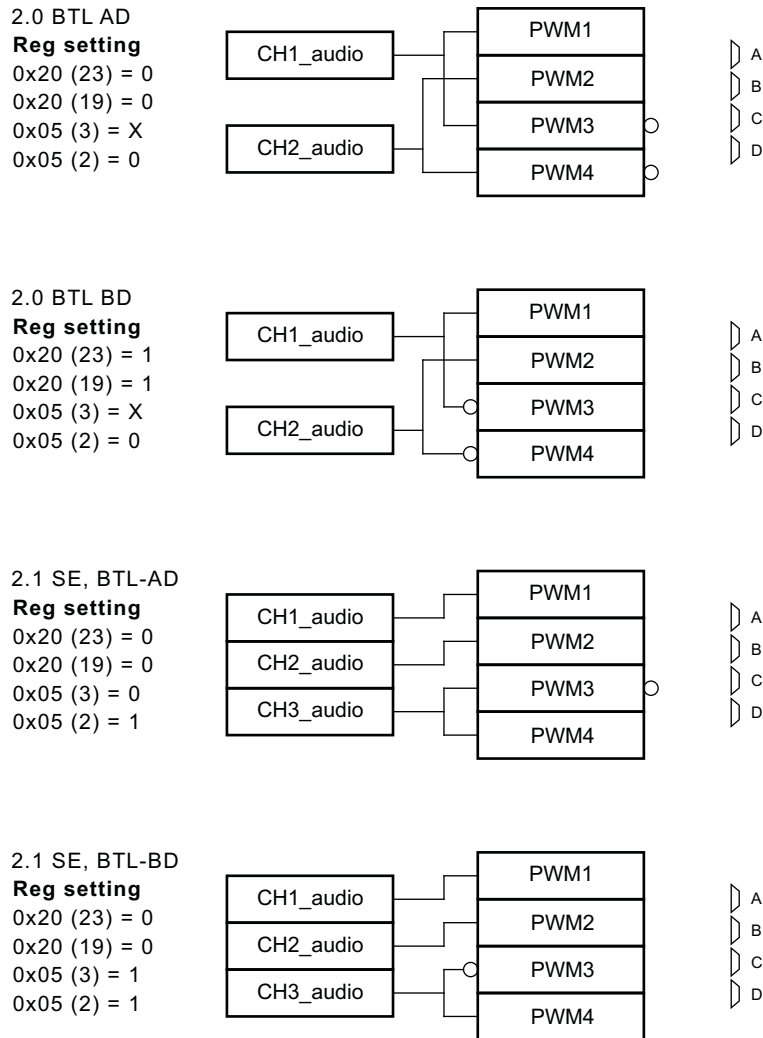


**Figure 51. Output Mode and MUX Selection**

## 2.1-Mode Support

The TAS5711 uses a special *mid-Z ramp* sequence to reduce click and pop in SE-mode and 2.1-mode operation.To enable the mid-Z ramp, register 0x05 bit D7 must be set to 1. To enable 2.1 mode, register 0x05 bit D2 must be set to 1. The SSTIMER pin should be left floating in this mode.

## Single-Filter PBTL-Mode Support

The TAS5711 supports parallel BTL (PBTL) mode with OUT_A/OUT_B (and OUT_C/OUT_D) connected before the LC filter. In order to put the part in PBTL configuration, drive PBTL (pin 8) HIGH. This synchronizes the turnoff of half-bridges A and B (and similarly C/D) if an overcurrent condition is detected in either half-bridge. There is a pulldown resistor on the PBTL pin that configures the part in BTL mode if the pin is left floating.

PWM output multiplexers should be updated to set the device in PBTL mode. Output Mux Register (0x25) should be written with a value of 0x01 10 32 45. Also, the PWM shutdown register (0x19) should be written with a value of 0x3A.

Product Folder Link(s): *TAS5711*

## Dynamic Range Control (DRC)

The DRC scheme has a single threshold, offset, and slope (all programmable). There is one ganged DRC for the left/right channels and one DRC for the subchannel.

The DRC input/output diagram is shown in Figure 52.

Refer to GDE software tool for more description on T, K, and O parameters.
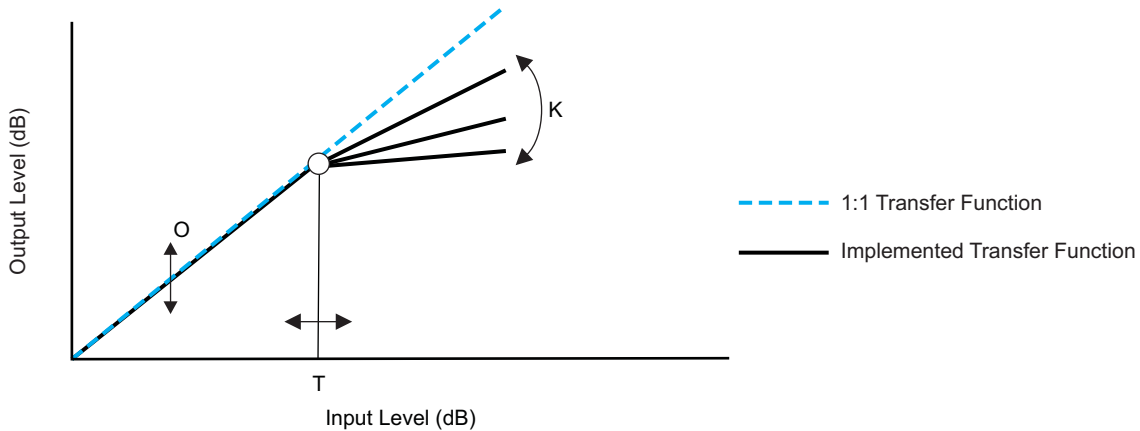


Professional-quality dynamic range compression automatically adjusts volume to flatten volume level.
- Each DRC has adjustable threshold, offset, and compression levels
- Programmable energy, attack, and decay time constants
- *Transparent compression*: compressors can attack fast enough to avoid apparent clipping before engaging, and decay times can be set slow enough to avoid pumping.

**Figure 52.  Dynamic Range Control**



| | $\alpha, \omega$ | T, K, O | $\alpha_a, \omega_a / \alpha_d, \omega_d$ |
|---|---|---|---|
| DRC1 | 0x3A | 0x40, 0x41, 0x42 | 0x3B / 0x3C |
| DRC2 | 0x3D | 0x43, 0x44, 0x45 | 0x3E / 0x3F |
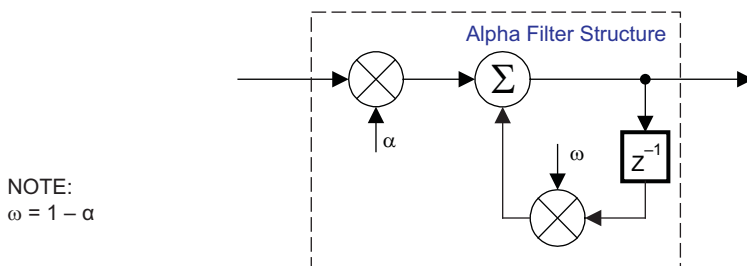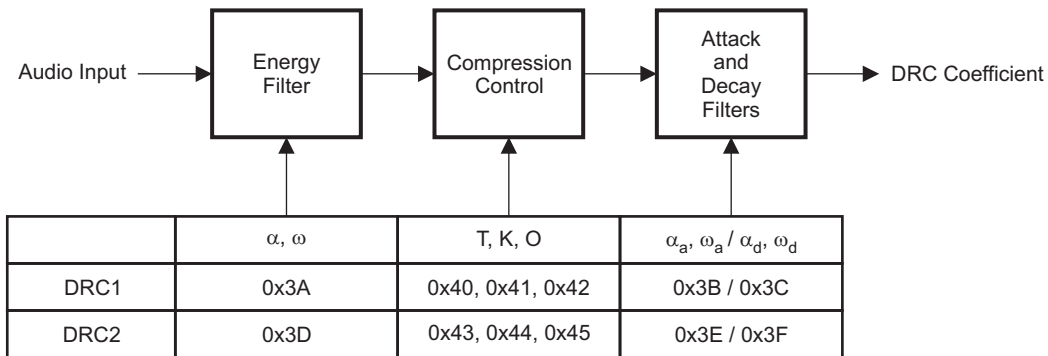


NOTE:
$\omega = 1 - \alpha$

T = 9.23 format, all other DRC coefficients are 3.23 format

**Figure 53.  DRC Structure**

Product Folder Link(s): *TAS5711*

## BANK SWITCHING

The TAS5711 uses an approach called *bank switching* together with automatic sample-rate detection. All processing features that must be changed for different sample rates are stored internally in three banks. The user can program which sample rates map to each bank. By default, bank 1 is used in 32kHz mode, bank 2 is used in 44.1/48 kHz mode, and bank 3 is used for all other rates. Combined with the clock-rate autodetection feature, bank switching allows the TAS5711 to detect automatically a change in the input sample rate and switch to the appropriate bank without any MCU intervention.

An external controller configures bankable locations (0x29-0x36, 0x3A-0x3F, and 0x58-0x5F) for all three banks during the initialization sequence.

If auto bank switching is enabled (register 0x50, bits 2:0) , then the TAS5711 automatically swaps the coefficients for subsequent sample rate changes, avoiding the need for any external controller intervention for a sample rate change.

By default, bits 2:0 have the value 000; indicating that bank switching is disabled. In that state, updates to bankable locations take immediate effect. A write to register 0x50 with bits 2:0 being 001, 010, or 011 brings the system into the coefficient-bank-update state *update bank1*, *update bank2,* or *update bank3*, respectively. Any subsequent write to bankable locations updates the coefficient banks stored outside the DAP. After updating all the three banks, the system controller should issue a write to register 0x50 with bits 2:0 being 100; this changes the system state to automatic bank switching mode. In automatic bank switching mode, the TAS5711 automatically swaps banks based on the sample rate.

---

**Command sequences for updating DAP coefficients can be summarized as follows:**

1. **Bank switching disabled (default):** DAP coefficient writes take immediate effect and are not influenced by subsequent sample rate changes.

    OR
    **Bank switching enabled:**
    (a)    Update bank-1 mode: Write "001" to bits 2:0 of reg 0x50. Load the 32 kHz coefficients.
    (b)    Update bank-2 mode: Write "010" to bits 2:0 of reg 0x50. Load the 48 kHz coefficients.
    (c)    Update bank-3 mode: Write "011" to bits 2:0 of reg 0x50. Load the other coefficients.
    (d)    Enable automatic bank switching by writing "100" to bits 2:0 of reg 0x50.

---

## 26-Bit 3.23 Number Format

All mixer gain coefficients are 26-bit coefficients using a 3.23 number format. Numbers formatted as 3.23 numbers means that there are 3 bits to the left of the decimal point and 23 bits to the right of the decimal point. This is shown in Figure 54 .
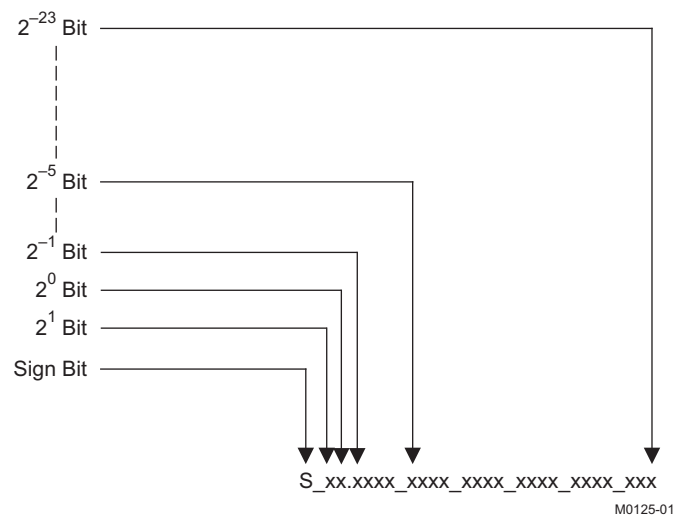


**Figure 54. 3.23 Format**

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Product Folder Link(s): *TAS5711*

The decimal value of a 3.23 format number can be found by following the weighting shown in Figure 54. If the most significant bit is logic 0, the number is a positive number, and the weighting shown yields the correct number. If the most significant bit is a logic 1, then the number is a negative number. In this case every bit must be inverted, a 1 added to the result, and then the weighting shown in Figure 55 applied to obtain the magnitude of the negative number.

$2^1$ Bit        $2^0$ Bit        $2^{-1}$ Bit        $2^{-4}$ Bit        $2^{-23}$ Bit

(1 or 0) $\times 2^1$ + (1 or 0) $\times 2^0$ + (1 or 0) $\times 2^{-1}$ + ....... (1 or 0) $\times 2^{-4}$ + ....... (1 or 0) $\times 2^{-23}$

M0126-01

**Figure 55. Conversion Weighting Factors—3.23 Format to Floating Point**

Gain coefficients, entered via the I$^2$C bus, must be entered as 32-bit binary numbers. The format of the 32-bit number (4-byte or 8-digit hexadecimal number) is shown in Figure 56

M0127-01
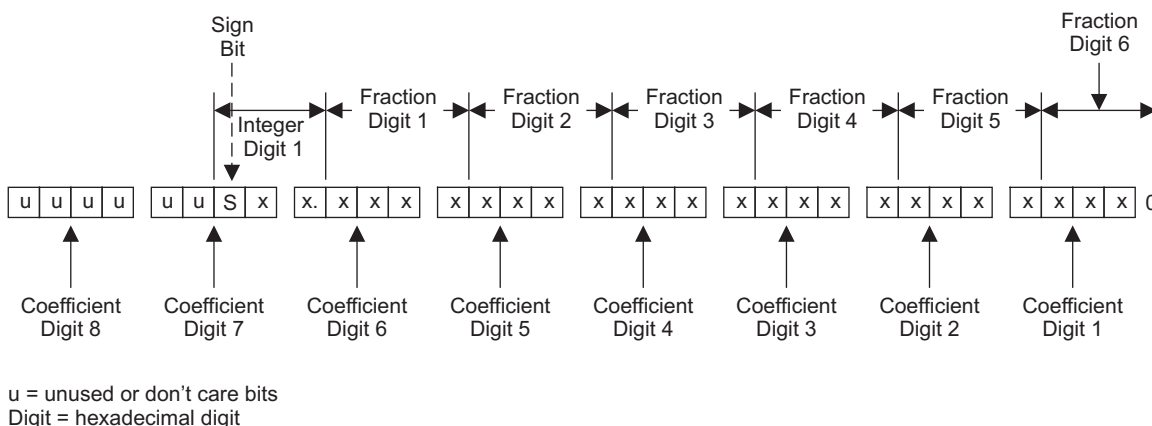
**Figure 56. Alignment of 3.23 Coefficient in 32-Bit I2C Word**

u = unused or don't care bits
Digit = hexadecimal digit

**Table 2. Sample Calculation for 3.23 Format**

| dB | Linear | Decimal | Hex (3.23 Format) |
|----|--------|---------|-------------------|
| 0 | 1 | 8,388,608 | 0080 0000 |
| 5 | 1.7782794 | 14,917,288 | 00E3 9EA8 |
| −5 | 0.5623413 | 4,717,260 | 0047 FACC |
| X | L = $10^{(X/20)}$ | D = 8,388,608 × L | H = dec2hex (D, 8) |

**Table 3. Sample Calculation for 9.17 Format**

| dB | Linear | Decimal | Hex (9.17 Format) |
|----|--------|---------|-------------------|
| 0 | 1 | 131,072 | 2 0000 |
| 5 | 1.77 | 231,997 | 3 8A3D |
| −5 | 0.56 | 73,400 | 1 1EB8 |
| X | L = $10^{(X/20)}$ | D = 131,072 × L | H = dec2hex (D, 8) |

## Recommended Use Model
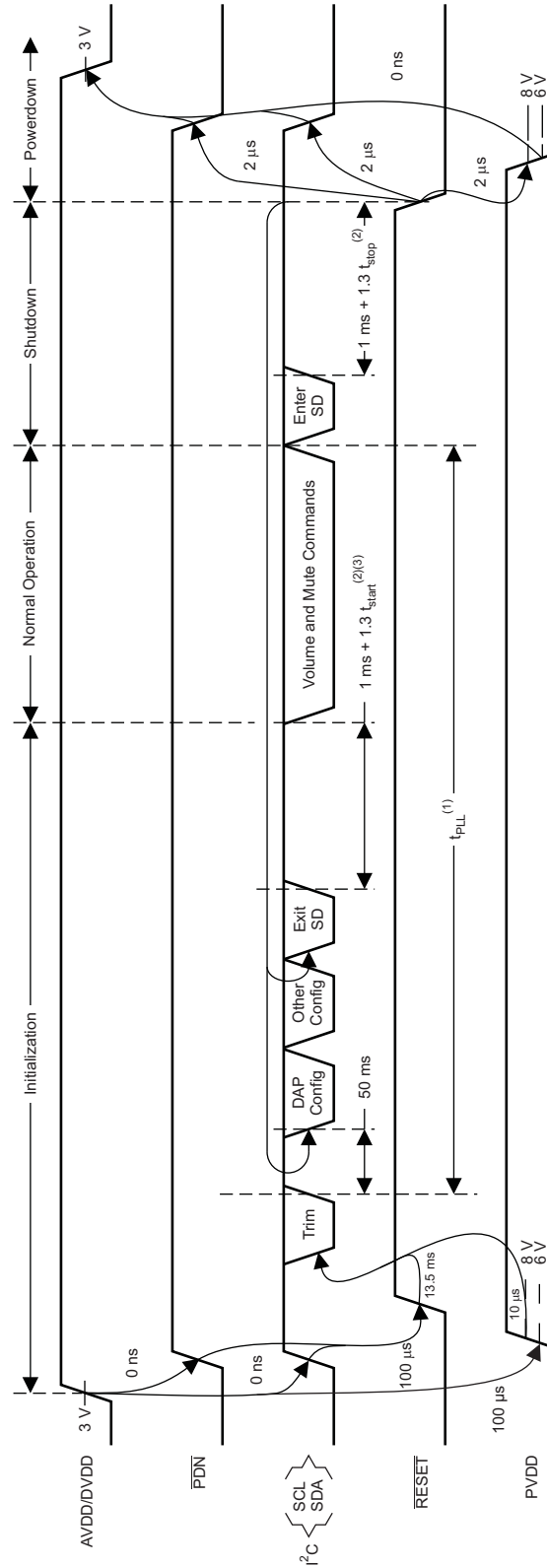


**Figure 57.  Recommended Command Sequence**
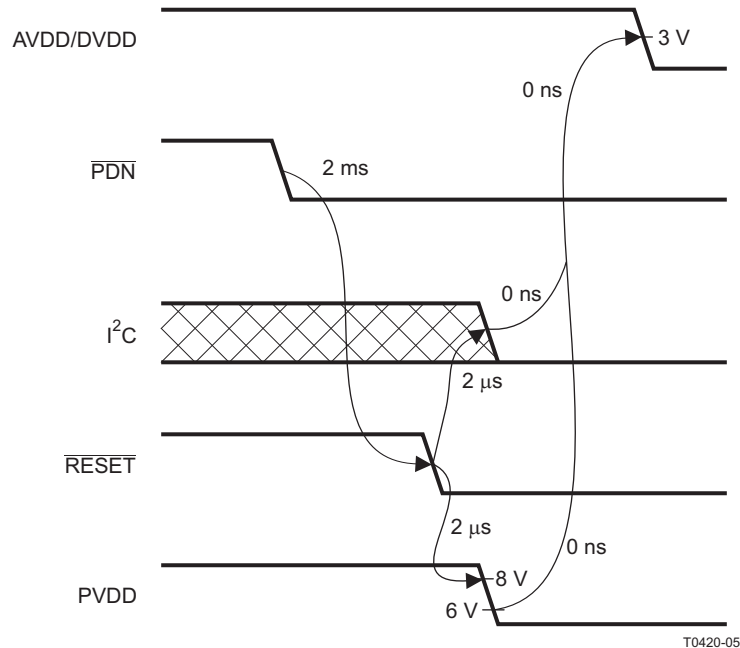
**Figure 58. Power Loss Sequence**

## Recommended Command Sequences

### Initialization Sequence

Use the following sequence to power-up and initialize the device:

1.  Hold all digital inputs low and ramp up AVDD/DVDD to at least 3 V.
2.  Initialize digital inputs and PVDD supply as follows:
    *   Drive $\overline{\text{RESET}}$ = 0, $\overline{\text{PDN}}$ = 1, and other digital inputs to their desired state while ensuring that all are never more than 2.5 V above AVDD/DVDD. Wait at least 100 μs, drive $\overline{\text{RESET}}$ = 1, and wait at least another 13.5 ms.
    *   Ramp up PVDD to at least 8 V while ensuring that it remains below 6 V for at least 100 μs after AVDD/DVDD reaches 3 V. Then wait at least another 10 μs.
3.  Trim oscillator (write 0x00 to register 0x1B) and wait at least 50 ms.
4.  Configure the DAP via I²C (see Users's Guide for typical values).
5.  Configure remaining registers.
6.  Exit shutdown (sequence defined below).

### Normal Operation

The following are the only events supported during normal operation:

1.  Writes to master/channel volume registers.
2.  Writes to soft mute register.
3.  Enter and exit shutdown (sequence defined below).

**Note:** Event 3 is not supported for 240 ms + 1.3 × $t_{start}$ after trim following AVDD/DVDD powerup ramp (where $t_{start}$ is 300 ms when mid-Z ramp is enabled and is otherwise specified by register 0x1A).

**Shutdown Sequence**

Enter:

1. Write 0x40 to register 0x05.

2. Wait at least 1 ms + 1.3 × $t_{stop}$ (where $t_{stop}$ is specified by register 0x1A).

3. If desired, reconfigure by returning to step 4 of initialization sequence.

Exit:

1. Write 0x00 to register 0x05 (exit shutdown command may not be serviced for as much as 240 ms after trim following AVDD/DVDD powerup ramp).

2. Wait at least 1 ms + 1.3 × $t_{start}$ (where $t_{start}$ is 300 ms when mid-Z ramp is enabled and is otherwise specified by register 0x1A).

3. Proceed with normal operation.

**Power-Down Sequence**

Use the following sequence to powerdown the device and its supplies:

1. If time permits, enter shutdown (sequence defined above); else, in case of sudden power loss, assert $\overline{PDN}$ = 0 and wait at least 2 ms.

2. Assert $\overline{RESET}$ = 0.

3. Drive digital inputs low and ramp down PVDD supply as follows:

    • Drive all digital inputs low after $\overline{RESET}$ has been low for at least 2 μs.

    • Ramp down PVDD while ensuring that it remains above 8 V until $\overline{RESET}$ has been low for at least 2 μs.

4. Ramp down AVDD/DVDD while ensuring that it remains above 3 V until PVDD is below 6 V and that it is never more than 2.5 V below the digital inputs.

Product Folder Link(s): *TAS5711*

**Table 4. Serial Control Interface Register Summary**

| SUBADDRESS | REGISTER NAME | NO. OF BYTES | CONTENTS | INITIALIZATION VALUE |
|---|---|---|---|---|
| | | | A u indicates unused bits. | |
| 0x00 | Clock control register | 1 | Description shown in subsequent section | 0x6C |
| 0x01 | Device ID register | 1 | Description shown in subsequent section | 0x70 |
| 0x02 | Error status register | 1 | Description shown in subsequent section | 0x00 |
| 0x03 | System control register 1 | 1 | Description shown in subsequent section | 0xA0 |
| 0x04 | Serial data interface register | 1 | Description shown in subsequent section | 0x05 |
| 0x05 | System control register 2 | 1 | Description shown in subsequent section | 0x40 |
| 0x06 | Soft mute register | 1 | Description shown in subsequent section | 0x00 |
| 0x07 | Master volume | 1 | Description shown in subsequent section | 0xFF (mute) |
| 0x08 | Channel 1 vol | 1 | Description shown in subsequent section | 0x30 (0 dB) |
| 0x09 | Channel 2 vol | 1 | Description shown in subsequent section | 0x30 (0 dB) |
| 0x0A | Channel 3 vol | 1 | Description shown in subsequent section | 0x30 (0 dB) |
| 0x0B - 0x0D | | 1 | Reserved[1] | |
| 0x0E | Volume configuration register | 1 | Description shown in subsequent section | 0x91 |
| 0x0F | | 1 | Reserved[1] | |
| 0x10 | Modulation limit register | 1 | Description shown in subsequent section | 0x02 |
| 0x11 | IC delay channel 1 | 1 | Description shown in subsequent section | 0xAC |
| 0x12 | IC delay channel 2 | 1 | Description shown in subsequent section | 0x54 |
| 0x13 | IC delay channel 3 | 1 | Description shown in subsequent section | 0xAC |
| 0x14 | IC delay channel 4 | 1 | Description shown in subsequent section | 0x54 |
| 0x15-0x18 | | 1 | Reserved[1] | |
| 0x19 | PWM channel shutdown group register | 1 | Description shown in subsequent section | 0x30 |
| 0x1A | Start/stop period register | 1 | | 0x0F |
| 0x1B | Oscillator trim register | 1 | | 0x82 |
| 0x1C | BKND_ERR register | 1 | | 0x02 |
| 0x1D–0x1F | | 1 | Reserved[1] | |
| 0x20 | Input MUX register | 4 | Description shown in subsequent section | 0x0001 7772 |
| 0x21 | Ch 4 source select register | 4 | Description shown in subsequent section | 0x0000 4303 |
| 0x22 -0x24 | | 4 | Reserved[1] | |
| 0x25 | PWM MUX register | 4 | Description shown in subsequent section | 0x0102 1345 |
| 0x26-0x28 | | 4 | Reserved[1] | |
| 0x29 | ch1_bq[0] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x2A | ch1_bq[1] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |

(1) Reserved registers should not be accessed.

**Table 4. Serial Control Interface Register Summary (continued)**

| SUBADDRESS | REGISTER NAME | NO. OF BYTES | CONTENTS | INITIALIZATION VALUE |
|---|---|---|---|---|
| 0x2B | ch1_bq[2] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x2C | ch1_bq[3] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x2D | ch1_bq[4] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x2E | ch1_bq[5] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x2F | ch1_bq[6] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x30 | ch2_bq[0] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x31 | ch2_bq[1] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x32 | ch2_bq[2] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x33 | ch2_bq[3] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |

Product Folder Link(s): *TAS5711*

**Table 4. Serial Control Interface Register Summary (continued)**

| SUBADDRESS | REGISTER NAME | NO. OF BYTES | CONTENTS | INITIALIZATION VALUE |
|---|---|---|---|---|
| 0x34 | ch2_bq[4] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x35 | ch2_bq[5] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x36 | ch2_bq[6] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x37 - 0x39 | | 4 | Reserved[2] | |
| 0x3A | DRC1 ae[3] | 8 | u[31:26], ae[25:0] | 0x0080 0000 |
| | DRC1 (1 − ae) | | u[31:26], (1 − ae)[25:0] | 0x0000 0000 |
| 0x3B | DRC1 aa | 8 | u[31:26], aa[25:0] | 0x0080 0000 |
| | DRC1 (1 − aa) | | u[31:26], (1 − aa)[25:0] | 0x0000 0000 |
| 0x3C | DRC1 ad | 8 | u[31:26], ad[25:0] | 0x0080 0000 |
| | DRC1 (1 − ad) | | u[31:26], (1 − ad)[25:0] | 0x0000 0000 |
| 0x3D | DRC2 ae | 8 | u[31:26], ae[25:0] | 0x0080 0000 |
| | DRC 2 (1 − ae) | | u[31:26], (1 − ae)[25:0] | 0x0000 0000 |
| 0x3E | DRC2 aa | 8 | u[31:26], aa[25:0] | 0x0080 0000 |
| | DRC2 (1 − aa) | | u[31:26], (1 − aa)[25:0] | 0x0000 0000 |
| 0x3F | DRC2 ad | 8 | u[31:26], ad[25:0] | 0x0080 0000 |
| | DRC2 (1 − ad) | | u[31:26], (1 − ad)[25:0] | 0x0000 0000 |
| 0x40 | DRC1-T | 4 | T1[31:0] (9.23 format) | 0xFDA2 1490 |
| 0x41 | DRC1-K | 4 | u[31:26], K1[25:0] | 0x0384 2109 |
| 0x42 | DRC1-O | 4 | u[31:26], O1[25:0] | 0x0008 4210 |
| 0x43 | DRC2-T | 4 | T2[31:0] (9.23 format) | 0xFDA2 1490 |
| 0x44 | DRC2-K | 4 | u[31:26], K2[25:0] | 0x0384 2109 |
| 0x45 | DRC2-O | 4 | u[31:26], O2[25:0] | 0x0008 4210 |
| 0x46 | DRC control | 4 | Description shown in subsequent section | 0x0000 0000 |
| 0x47–0x4F | | 4 | Reserved[2] | |
| 0x50 | Bank switch control | 4 | Description shown in subsequent section | 0x0F70 8000 |
| 0x51 | Ch 1 output mixer | 12 | Ch 1 output mix1[2] | 0x0080 0000 |
| | | | Ch 1 output mix1[1] | 0x0000 0000 |
| | | | Ch 1 output mix1[0] | 0x0000 0000 |
| 0x52 | Ch 2 output mixer | 12 | Ch 2 output mix2[2] | 0x0080 0000 |
| | | | Ch 2 output mix2[1] | 0x0000 0000 |
| | | | Ch 2 output mix2[0] | 0x0000 0000 |

(2) Reserved registers should not be accessed.
(3) "ae" stands for $\propto$ of energy filter, "aa" stands for $\propto$ of attack filter and "ad" stands for $\propto$ of decay filter and 1- $\propto$ = $\omega$.

**Table 4. Serial Control Interface Register Summary (continued)**

| SUBADDRESS | REGISTER NAME | NO. OF BYTES | CONTENTS | INITIALIZATION VALUE |
|---|---|---|---|---|
| 0x53 | Ch 1 input mixer | 16 | Ch 1 input mixer[3] | 0x0080 0000 |
| | | | Ch 1 input mixer[2] | 0x0000 0000 |
| | | | Ch 1 input mixer[1] | 0x0000 0000 |
| | | | Ch 1 input mixer[0] | 0x0080 0000 |
| 0x54 | Ch 2 input mixer | 16 | Ch 2 input mixer[3] | 0x0080 0000 |
| | | | Ch 2 input mixer[2] | 0x0000 0000 |
| | | | Ch 2 input mixer[1] | 0x0000 0000 |
| | | | Ch 2 input mixer[0] | 0x0080 0000 |
| 0x55 | Channel 3 input mixer | 12 | Channel 3 input mixer [2] | 0x0080 0000 |
| | | | Channel 3 input mixer [1] | 0x0000 0000 |
| | | | Channel 3 input mixer [0] | 0x0000 0000 |
| 0x56 | Output post-scale | 4 | u[31:26], post[25:0] | 0x0080 0000 |
| 0x57 | Output pre-scale | 4 | u[31:26], pre[25:0] (9.17 format) | 0x0002 0000 |
| 0x58 | ch1 BQ[7] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x59 | ch1 BQ[8] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x5A | Subchannel BQ[0] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x5B | Subchannel BQ[1] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x5C | ch2 BQ[7] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x5D | ch2 BQ[8] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |

Product Folder Link(s): *TAS5711*

**Table 4. Serial Control Interface Register Summary (continued)**

| SUBADDRESS | REGISTER NAME | NO. OF BYTES | CONTENTS | INITIALIZATION VALUE |
|---|---|---|---|---|
| 0x5E | pseudo_ch2 BQ[0] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x5F | | 4 | Reserved[4] | |
| 0x60 | Channel 4 (subchannel) output mixer | 8 | Ch 4 output mixer[1] | 0x0000 0000 |
| | | | Ch 4 output mixer[0] | 0x0080 0000 |
| 0x61 | Channel 4 (subchannel) input mixer | 8 | Ch 4 input mixer[1] | 0x0040 0000 |
| | | | Ch 4 input mixer[0] | 0x0040 0000 |
| 0x62 | IDF post scale | 4 | Post-IDF attenuation register | 0x0000 0080 |
| 0x63–0xF7 | | | Reserved[4] | 0x0000 0000 |
| 0xF8 | Device address enable register | 4 | Write F9 A5 A5 A5 in this register to enable write to device address update (0xF9) | 0x0000 0000 |
| 0xF9 | Device address Update Register | 4 | u[31:8], New Dev Id[7:1] , ZERO[0] (New Dev Id (7:1) defines the new device address | 0X0000 0036 |
| 0xFB–0xFF | | 4 | Reserved[4] | 0x0000 0000 |

(4)   Reserved registers should not be accessed.

All DAP coefficients are 3.23 format unless specified otherwise.

## CLOCK CONTROL REGISTER (0x00)

The clocks and data rates are automatically determined by the TAS5711. The clock control register contains the auto-detected clock status. Bits D7–D5 reflect the sample rate. Bits D4–D2 reflect the MCLK frequency. The device accepts a 64 $f_S$ or 32 $f_S$ SCLK rate for all MCLK ratios, but accepts a 48 $f_S$ SCLK rate for MCLK ratios of 192 $f_S$ and 384 $f_S$ only.

**Table 5. Clock Control Register (0x00)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|----|----|----|----|----|----|----|----|----------|
| 0 | 0 | 0 | – | – | – | – | – | $f_S$ = 32-kHz sample rate |
| 0 | 0 | 1 | – | – | – | – | – | Reserved[1] |
| 0 | 1 | 0 | – | – | – | – | – | Reserved[1] |
| **0** | **1** | **1** | **–** | **–** | **–** | **–** | **–** | **$f_S$ = 44.1/48-kHz sample rate** [2] |
| 1 | 0 | 0 | – | – | – | – | – | fs = 16-kHz sample rate |
| 1 | 0 | 1 | – | – | – | – | – | fs = 22.05/24 -kHz sample rate |
| 1 | 1 | 0 | – | – | – | – | – | fs = 8-kHz sample rate |
| 1 | 1 | 1 | – | – | – | – | – | fs = 11.025/12 -kHz sample rate |
| – | – | – | 0 | 0 | 0 | – | – | MCLK frequency = 64 × $f_S$ [3] |
| – | – | – | 0 | 0 | 1 | – | – | MCLK frequency = 128 × $f_S$ [3] |
| – | – | – | 0 | 1 | 0 | – | – | MCLK frequency = 192 × $f_S$ [4] |
| **–** | **–** | **–** | **0** | **1** | **1** | **–** | **–** | **MCLK frequency = 256 × $f_S$** [2] [5] |
| – | – | – | 1 | 0 | 0 | – | – | MCLK frequency = 384 × $f_S$ |
| – | – | – | 1 | 0 | 1 | – | – | MCLK frequency = 512 × $f_S$ |
| – | – | – | 1 | 1 | 0 | – | – | Reserved[1] |
| – | – | – | 1 | 1 | 1 | – | – | Reserved[1] |
| **–** | **–** | **–** | **–** | **–** | **–** | **0** | **–** | **Reserved**[1] [2] |
| **–** | **–** | **–** | **–** | **–** | **–** | **–** | **0** | **Reserved**[1] [2] |

(1) Reserved registers should not be accessed.
(2) Default values are in **bold**.
(3) Only available for 44.1 kHz and 48 kHz rates.
(4) Rate only available for 32/44.1/48 KHz sample rates
(5) Not available at 8 kHz

## DEVICE ID REGISTER (0x01)

The device ID register contains the ID code for the firmware revision.

**Table 6. General Status Register (0x01)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|----|----|----|----|----|----|----|----|----------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | **Identification code** |

Product Folder Link(s): *TAS5711*

## ERROR STATUS REGISTER (0x02)

The error bits are sticky and are not cleared by the hardware. This means that the software must clear the register (write zeroes) and then read them to determine if they are persistent errors.

Error Definitions:
- MCLK Error : MCLK frequency is changing. The number of MCLKs per LRCLK is changing.
- SCLK Error: The number of SCLKs per LRCLK is changing.
- LRCLK Error: LRCLK frequency is changing.
- Frame Slip: LRCLK phase is drifting with respect to internal Frame Sync.

### Table 7. Error Status Register (0x02)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|----|----|----|----|----|----|----|----|----------|
| 1 | - | – | – | – | – | – | – | MCLK error |
| – | 1 | – | – | – | – | – | – | PLL autolock error |
| – | – | 1 | – | – | – | – | – | SCLK error |
| – | – | – | 1 | – | – | – | – | LRCLK error |
| – | – | – | – | 1 | – | – | – | Frame slip |
| – | – | – | – | – | 1 | – | – | Clip indicator |
| – | – | – | – | – | – | 1 | – | Overcurrent, overtemperature, overvoltage or undervoltage errors |
| – | – | – | – | – | – | – | **0** | **Reserved** |
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | – | **No errors** [1] |

(1)   Default values are in **bold**.

## SYSTEM CONTROL REGISTER 1 (0x03)

The system control register 1 has several functions:

Bit D7:        If 0, the dc-blocking filter for each channel is disabled.
             If 1, the dc-blocking filter (–3 dB cutoff <1 Hz) for each channel is enabled (default).

Bit D5:        If 0, use soft unmute on recovery from clock error. This is a slow recovery. Unmute takes the same time as the volume ramp defined in register 0x0E.
             If 1, use hard unmute on recovery from clock error (default). This is a fast recovery, a single step volume ramp

Bits D1–D0:  Select de-emphasis

### Table 8. System Control Register 1 (0x03)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|----|----|----|----|----|----|----|----|----------|
| 0 | – | – | – | – | – | – | – | PWM high-pass (dc blocking) disabled |
| **1** | – | – | – | – | – | – | – | **PWM high-pass (dc blocking) enabled** [1] |
| – | **0** | – | – | – | – | – | – | **Reserved** [1] |
| – | – | 0 | – | – | – | – | – | Soft unmute on recovery from clock error |
| – | – | **1** | – | – | – | – | – | **Hard unmute on recovery from clock error** [1] |
| – | – | – | **0** | – | – | – | – | **Reserved** [1] |
| – | – | – | – | **0** | – | – | – | **Reserved** [1] |
| – | – | – | – | – | **0** | – | – | **Reserved** [1] |
| – | – | – | – | – | – | **0** | **0** | **No de-emphasis** [1] |
| – | – | – | – | – | – | 0 | 1 | De-emphasis for $f_S$ = 32 kHz |
| – | – | – | – | – | – | 1 | 0 | De-emphasis for $f_S$ = 44.1 kHz |
| – | – | – | – | – | – | 1 | 1 | De-emphasis for $f_S$ = 48 kHz |

(1)   Default values are in **bold**.

## SERIAL DATA INTERFACE REGISTER (0x04)

As shown in Table 9, the TAS5711 supports 9 serial data modes. The default is 24-bit, I²S mode,

**Table 9. Serial Data Interface Control Register (0x04) Format**

| RECEIVE SERIAL DATA INTERFACE FORMAT | WORD LENGTH | D7–D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|
| Right-justified | 16 | 0000 | 0 | 0 | 0 | 0 |
| Right-justified | 20 | 0000 | 0 | 0 | 0 | 1 |
| Right-justified | 24 | 0000 | 0 | 0 | 1 | 0 |
| I²S | 16 | 000 | 0 | 0 | 1 | 1 |
| I²S | 20 | 0000 | 0 | 1 | 0 | 0 |
| **I²S** (1) | **24** | **0000** | **0** | **1** | **0** | **1** |
| Left-justified | 16 | 0000 | 0 | 1 | 1 | 0 |
| Left-justified | 20 | 0000 | 0 | 1 | 1 | 1 |
| Left-justified | 24 | 0000 | 1 | 0 | 0 | 0 |
| Reserved | | 0000 | 1 | 0 | 0 | 1 |
| Reserved | | 0000 | 1 | 0 | 1 | 0 |
| Reserved | | 0000 | 1 | 0 | 1 | 1 |
| Reserved | | 0000 | 1 | 1 | 0 | 0 |
| Reserved | | 0000 | 1 | 1 | 0 | 1 |
| Reserved | | 0000 | 1 | 1 | 1 | 0 |
| Reserved | | 0000 | 1 | 1 | 1 | 1 |

(1) Default values are in **bold**.

Product Folder Link(s): *TAS5711*

## SYSTEM CONTROL REGISTER 2 (0x05)

When bit D6 is set low, the system exits all channel shutdown and starts playing audio; otherwise, the outputs are shut down(hard mute).

**Table 10. System Control Register 2 (0x05)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|----|----|----|----|----|----|----|----|----------|
| **0** | – | – | – | – | – | – | – | **Mid-Z ramp disabled** [1] |
| 1 | – | – | – | – | – | – | – | Mid-Z ramp enabled |
| – | 0 | – | – | – | – | – | – | Exit all-channel shutdown (normal operation) |
| – | **1** | – | – | – | – | – | – | **Enter all-channel shutdown (hard mute)**[1] |
| – | – | – | – | 0 | – | – | – | Subchannel in AD mode |
| – | – | – | – | 1 | – | – | – | Subchannel in BD mode |
| – | – | – | – | – | **0** | – | – | **2.0 mode [2.0 BTL]** [1] |
| – | – | – | – | – | 1 | – | – | 2.1 mode [2 SE + 1 BTL] |
| – | 0 | – | – | – | – | – | – | Exit all-channel shutdown (normal operation) |
| – | – | – | – | – | – | **0** | – | **A_SEL configured as input**[1] |
| – | – | – | – | – | – | 1 | – | A_SEL configured as $\overline{FAULT}$ output |
| – | – | **0** | **0** | – | – | – | **0** | **Reserved** [1] |

(1)   Default values are in **bold**.

## SOFT MUTE REGISTER (0x06)

Writing a 1 to any of the following bits sets the output of the respective channel to 50% duty cycle (soft mute).

**Table 11. Soft Mute Register (0x06)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|----|----|----|----|----|----|----|----|----------|
| **0** | **0** | **0** | **0** | **0** | – | – | – | **Reserved** [1] |
| – | – | – | – | – | **0** | – | – | **Soft unmute channel 3** [1] |
| – | – | – | – | – | 1 | – | – | Soft mute channel 3 |
| – | – | – | – | – | – | **0** | – | **Soft unmute channel 2** [1] |
| – | – | – | – | – | – | 1 | – | Soft mute channel 2 |
| – | – | – | – | – | – | – | **0** | **Soft unmute channel 1** [1] |
| – | – | – | – | – | – | – | 1 | Soft mute channel 1 |

(1)   Default values are in **bold**.

## VOLUME REGISTERS (0x07, 0x08, 0x09, 0x0A)

Step size is 0.5 dB.

| | | |
|---|---|---|
| Master volume | – 0x07 (default is mute) | |
| Channel-1 volume | – 0x08 (default is 0 dB) | |
| Channel-2 volume | – 0x09 (default is 0 dB) | |
| Channel-3 volume | – 0x0A (default is 0 dB) | |

**Table 12. Volume Registers (0x07, 0x08, 0x09, 0x0A)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|----|----|----|----|----|----|----|----|----------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 24 dB |
| **0** | **0** | **1** | **1** | **0** | **0** | **0** | **0** | **0 dB (default for individual channel volume)** [1] |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | –103 dB |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | Soft mute |

(1) Default values are in **bold**.

## VOLUME CONFIGURATION REGISTER (0x0E)

Bits
D2–D0:    Volume slew rate (Used to control volume change and MUTE ramp rates). These bits control the number of steps in a volume ramp.Volume steps occur at a rate that depends on the sample rate of the I2S data as follows

| | |
|---|---|
| Sample Rate (KHz) | Approximate Ramp Rate |
| 8/16/32 | 125 us/step |
| 11.025/22.05/44.1 | 90.7 us/step |
| 12/24/48 | 83.3 us/step |

**Table 13. Volume Control Register (0x0E)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|----|----|----|----|----|----|----|----|----------|
| **1** | **–** | **–** | **1** | **0** | **–** | **–** | **–** | **Reserved** [1] |
| – | **0** | – | – | – | – | – | – | **Subchannel (ch4) volume = ch1 volume** [2] [1] |
| – | 1 | – | – | – | – | – | – | Subchannel volume = register 0x0A [2] |
| – | – | **0** | – | – | – | – | – | **Ch3 volume = ch2 volume** [1] |
| – | – | 1 | – | – | – | – | – | Ch3 volume = register 0x0A |
| – | – | – | – | – | 0 | 0 | 0 | Volume slew 512 steps (43-ms volume ramp time at 48 kHz) |
| – | – | – | – | – | **0** | **0** | **1** | **Volume slew 1024 steps (85-ms volume ramp time at 48 kHz)** [1] |
| – | – | – | – | – | 0 | 1 | 0 | Volume slew 2048 steps (171- ms volume ramp time at 48 kHz) |
| – | – | – | – | – | 0 | 1 | 1 | Volume slew 256 steps (21-ms volume ramp time at 48 kHz) |
| – | – | – | – | – | 1 | X | X | Reserved |

(1) Default values are in **bold**.
(2) Bits 6:5 can be changed only when volume is in MUTE [master volume = MUTE (register 0x07 = 0xFF)].

Product Folder Link(s): *TAS5711*

## MODULATION LIMIT REGISTER (0x10)

The modulation limit is the maximum duty cycle of the PWM output waveform.

**Table 14. Modulation Limit Register (0x10)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | MODULATION LIMIT |
|----|----|----|----|----|----|----|----|------------------|
| – | – | – | – | – | 0 | 0 | 0 | 99.2% |
| – | – | – | – | – | 0 | 0 | 1 | 98.4% |
| – | – | – | – | – | **0** | **1** | **0** | **97.7%** [1] |
| – | – | – | – | – | 0 | 1 | 1 | 96.9% |
| – | – | – | – | – | 1 | 0 | 0 | 96.1% |
| – | – | – | – | – | 1 | 0 | 1 | 95.3% |
| – | – | – | – | – | 1 | 1 | 0 | 94.5% |
| – | – | – | – | – | 1 | 1 | 1 | 93.8% |
| 0 | 0 | 0 | 0 | 0 | – | – | – | RESERVED |

(1)    Default values are in **bold**.

## INTERCHANNEL DELAY REGISTERS (0x11, 0x12, 0x13, and 0x14)

Internal PWM Channels 1, 2, $\overline{1}$, and $\overline{2}$ are mapped into registers 0x11, 0x12, 0x13, and 0x14.

**Table 15. Channel Interchannel Delay Register Format**

| BITS DEFINITION | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|-----------------|----|----|----|----|----|----|----|----|----------|
| | 0 | 0 | 0 | 0 | 0 | 0 | – | – | Minimum absolute delay, 0 DCLK cycles |
| | 0 | 1 | 1 | 1 | 1 | 1 | – | – | Maximum positive delay, 31 × 4 DCLK cycles |
| | 1 | 0 | 0 | 0 | 0 | 0 | – | – | Maximum negative delay, −32 × 4 DCLK cycles |
| | | | | | | | 0 | 0 | RESERVED |
| **SUBADDRESS** | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | **Delay = (value) × 4 DCLKs** |
| **0x11** | **1** | **0** | **1** | **0** | **1** | **1** | – | – | **Default value for channel 1** [1] |
| **0x12** | **0** | **1** | **0** | **1** | **0** | **1** | – | – | **Default value for channel 2** [1] |
| **0x13** | **1** | **0** | **1** | **0** | **1** | **1** | – | – | **Default value for $\overline{\text{channel 1}}$** [1] |
| **0x14** | **0** | **1** | **0** | **1** | **0** | **1** | – | – | **Default value for $\overline{\text{channel 2}}$** [1] |

(1)    Default values are in **bold**.

ICD settings have high impact on audio performance (e.g., dynamic range, THD, crosstalk etc.). Therefore, appropriate ICD settings must be used. By default, the device has ICD settings for AD mode. If used in BD mode, then update these registers before coming out of all-channel shutdown.

| REGISTER | AD MODE | BD MODE |
|----------|---------|---------|
| 0x11 | AC | B8 |
| 0x12 | 54 | 60 |
| 0x13 | AC | A0 |
| 0x14 | 54 | 48 |

## PWM SHUTDOWN GROUP REGISTER (0x19)

Settings of this register determine which PWM channels are active. The value should be 0x30 for BTL mode and 0x3A for PBTL mode. The default value of this register is 0x30. The functionality of this register is tied to the state of bit D5 in the system control register.

This register defines which channels belong to the shutdown group (SDG). If a 1 is set in the shutdown group register, that particular channel is **not** started following an exit *out of all-channel shutdown* command (if bit D5 is set to 0 in system control register 2, 0x05).

### Table 16. Shutdown Group Register

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|----|----|----|----|----|----|----|----|----------|
| **0** | – | – | – | – | – | – | – | **Reserved** [1] |
| – | **0** | – | – | – | – | – | – | **Reserved** [1] |
| – | – | **1** | – | – | – | – | – | **Reserved** [1] |
| – | – | – | **1** | – | – | – | – | **Reserved** [1] |
| – | – | – | – | **0** | – | – | – | **PWM channel 4 does not belong to shutdown group.** [1] |
| – | – | – | – | 1 | – | – | – | PWM channel 4 belongs to shutdown group. |
| – | – | – | – | – | **0** | – | – | **PWM channel 3 does not belong to shutdown group.** [1] |
| – | – | – | – | – | 1 | – | – | PWM channel 3 belongs to shutdown group. |
| – | – | – | – | – | – | **0** | – | **PWM channel 2 does not belong to shutdown group.** [1] |
| – | – | – | – | – | – | 1 | – | PWM channel 2 belongs to shutdown group. |
| – | – | – | – | – | – | – | **0** | **PWM channel 1 does not belong to shutdown group.** [1] |
| – | – | – | – | – | – | – | 1 | PWM channel 1 belongs to shutdown group. |

(1) Default values are in **bold**.

Product Folder Link(s): *TAS5711*

## START/STOP PERIOD REGISTER (0x1A)

This register is used to control the soft-start and soft-stop period following an enter/exit all channel shut down command or change in the PDN state. This helps reduce pops and clicks at start-up and shutdown.The times are only approximate and vary depending on device activity level and I2S clock stability.

### Table 17. Start/Stop Period Register (0x1A)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|----|----|----|----|----|----|----|----|----------|
| **0** | – | – | – | – | – | – | – | **SSTIMER enabled**[1] |
| 1 | – | – | – | – | – | – | – | SSTIMER disabled |
| – | **0** | **0** | – | – | – | – | – | **Reserved** [1] |
| – | – | – | 0 | 0 | – | – | – | No 50% duty cycle start/stop period |
| – | – | – | 0 | 1 | 0 | 0 | 0 | 16.5-ms 50% duty cycle start/stop period |
| – | – | – | 0 | 1 | 0 | 0 | 1 | 23.9-ms 50% duty cycle start/stop period |
| – | – | – | 0 | 1 | 0 | 1 | 0 | 31.4-ms 50% duty cycle start/stop period |
| – | – | – | 0 | 1 | 0 | 1 | 1 | 40.4-ms 50% duty cycle start/stop period |
| – | – | – | 0 | 1 | 1 | 0 | 0 | 53.9-ms 50% duty cycle start/stop period |
| – | – | – | 0 | 1 | 1 | 0 | 1 | 70.3-ms 50% duty cycle start/stop period |
| – | – | – | 0 | 1 | 1 | 1 | 0 | 94.2-ms 50% duty cycle start/stop period |
| – | – | – | **0** | **1** | **1** | **1** | **1** | **125.7-ms 50% duty cycle start/stop period**[1] |
| – | – | – | 1 | 0 | 0 | 0 | 0 | 164.6-ms 50% duty cycle start/stop period |
| – | – | – | 1 | 0 | 0 | 0 | 1 | 239.4-ms 50% duty cycle start/stop period |
| – | – | – | 1 | 0 | 0 | 1 | 0 | 314.2-ms 50% duty cycle start/stop period |
| – | – | – | 1 | 0 | 0 | 1 | 1 | 403.9-ms 50% duty cycle start/stop period |
| – | – | – | 1 | 0 | 1 | 0 | 0 | 538.6-ms 50% duty cycle start/stop period |
| – | – | – | 1 | 0 | 1 | 0 | 1 | 703.1-ms 50% duty cycle start/stop period |
| – | – | – | 1 | 0 | 1 | 1 | 0 | 942.5-ms 50% duty cycle start/stop period |
| – | – | – | 1 | 0 | 1 | 1 | 1 | 1256.6-ms 50% duty cycle start/stop period |
| – | – | – | 1 | 1 | 0 | 0 | 0 | 1728.1-ms 50% duty cycle start/stop period |
| – | – | – | 1 | 1 | 0 | 0 | 1 | 2513.6-ms 50% duty cycle start/stop period |
| – | – | – | 1 | 1 | 0 | 1 | 0 | 3299.1-ms 50% duty cycle start/stop period |
| – | – | – | 1 | 1 | 0 | 1 | 1 | 4241.7-ms 50% duty cycle start/stop period |
| – | – | – | 1 | 1 | 1 | 0 | 0 | 5655.6-ms 50% duty cycle start/stop period |
| – | – | – | 1 | 1 | 1 | 0 | 1 | 7383.7-ms 50% duty cycle start/stop period |
| – | – | – | 1 | 1 | 1 | 1 | 0 | 9897.3-ms 50% duty cycle start/stop period |
| – | – | – | 1 | 1 | 1 | 1 | 1 | 13,196.4-ms 50% duty cycle start/stop period |

(1)   Default values are in **bold**.

## OSCILLATOR TRIM REGISTER (0x1B)

The TAS5711 PWM processor contains an internal oscillator to support autodetect of I2S clock rates. This reduces system cost because an external reference is not required. Currently, TI recommends a reference resistor value of 18.2 kΩ (1%). This should be connected between OSC_RES and DVSSO.

Writing 0x00 to register 0x1B enables the trim that was programmed at the factory.

Note that trim must always be run following reset of the device.

**Table 18. Oscillator Trim Register (0x1B)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|----|----|----|----|----|----|----|----|----------|
| **1** | – | – | – | – | – | – | – | **Reserved** [1] |
| – | **0** | – | – | – | – | – | – | **Oscillator trim not done (read-only)** [1] |
| – | 1 | – | – | – | – | – | – | Oscillator trim done (read only) |
| – | – | **0** | **0** | **0** | **0** | – | – | **Reserved** [1] |
| – | – | – | – | – | – | 0 | – | Select factory trim (Write a 0 to select factory trim; default is 1.) |
| – | – | – | – | – | – | **1** | – | **Factory trim disabled** [1] |
| – | – | – | – | – | – | – | **0** | **Reserved** [1] |

(1) Default values are in **bold**.

## BKND_ERR REGISTER (0x1C)

When a back-end error signal is received from the internal power stage, the power stage is reset stopping all PWM activity. Subsequently, the modulator waits approximately for the time listed in Table 19 before attempting to re-start the power stage.

**Table 19. BKND_ERR Register (0x1C)[1]**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|----|----|----|----|----|----|----|----|----------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | X | Reserved |
| – | – | – | – | **0** | **0** | **1** | **0** | **Set back-end reset period to 299 ms** [2] |
| – | – | – | – | 0 | 0 | 1 | 1 | Set back-end reset period to 449 ms |
| – | – | – | – | 0 | 1 | 0 | 0 | Set back-end reset period to 598 ms |
| – | – | – | – | 0 | 1 | 0 | 1 | Set back-end reset period to 748 ms |
| – | – | – | – | 0 | 1 | 1 | 0 | Set back-end reset period to 898 ms |
| – | – | – | – | 0 | 1 | 1 | 1 | Set back-end reset period to 1047 ms |
| – | – | – | – | 1 | 0 | 0 | 0 | Set back-end reset period to 1197 ms |
| – | – | – | – | 1 | 0 | 0 | 1 | Set back-end reset period to 1346 ms |
| – | – | – | – | 1 | 0 | 1 | X | Set back-end reset period to 1496 ms |
| – | – | – | – | 1 | 1 | X | X | Set back-end reset period to 1496 ms |

(1) This register can be written only with a "non-Reserved" value. Also this register can be written once after the reset.
(2) Default values are in **bold**.

Product Folder Link(s): *TAS5711*

## INPUT MULTIPLEXER REGISTER (0x20)

This register controls the modulation scheme (AD or BD mode) as well as the routing of I2S audio to the internal channels.

**Table 20. Input Multiplexer Register (0x20)**

| D31 | D30 | D29 | D28 | D27 | D26 | D25 | D24 | FUNCTION |
|-----|-----|-----|-----|-----|-----|-----|-----|----------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | **Reserved** [1] |

| D23 | D22 | D21 | D20 | D19 | D18 | D17 | D16 | FUNCTION |
|-----|-----|-----|-----|-----|-----|-----|-----|----------|
| 0 | – | – | – | – | – | – | – | **Channel-1 AD mode** [1] |
| 1 | – | – | – | – | – | – | – | Channel-1 BD mode |
| – | 0 | 0 | 0 | – | – | – | – | **SDIN-L to channel 1** [1] |
| – | 0 | 0 | 1 | – | – | – | – | SDIN-R to channel 1 |
| – | 0 | 1 | 0 | – | – | – | – | Reserved |
| – | 0 | 1 | 1 | – | – | – | – | Reserved |
| – | 1 | 0 | 0 | – | – | – | – | Reserved |
| – | 1 | 0 | 1 | – | – | – | – | Reserved |
| – | 1 | 1 | 0 | – | – | – | – | Ground (0) to channel 1 |
| – | 1 | 1 | 1 | – | – | – | – | Reserved |
| – | – | – | – | 0 | – | – | – | **Channel 2 AD mode** [1] |
| – | – | – | – | 1 | – | – | – | Channel 2 BD mode |
| – | – | – | – | – | 0 | 0 | 0 | SDIN-L to channel 2 |
| – | – | – | – | – | 0 | 0 | 1 | **SDIN-R to channel 2** [1] |
| – | – | – | – | – | 0 | 1 | 0 | Reserved |
| – | – | – | – | – | 0 | 1 | 1 | Reserved |
| – | – | – | – | – | 1 | 0 | 0 | Reserved |
| – | – | – | – | – | 1 | 0 | 1 | Reserved |
| – | – | – | – | – | 1 | 1 | 0 | Ground (0) to channel 2 |
| – | – | – | – | – | 1 | 1 | 1 | Reserved |

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | FUNCTION |
|-----|-----|-----|-----|-----|-----|-----|-----|----------|
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | **Reserved** [1] |

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|-----|-----|-----|-----|-----|-----|-----|-----|----------|
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | **Reserved** [1] |

(1)    Default values are in **bold**.

## CHANNEL 4 SOURCE SELECT REGISTER (0x21)

This register selects the channel 4 source.

### Table 21. Subchannel Control Register (0x21)

| D31 | D30 | D29 | D28 | D27 | D26 | D25 | D24 | FUNCTION |
|-----|-----|-----|-----|-----|-----|-----|-----|----------|
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **Reserved**[1] |
| D23 | D22 | D21 | D20 | D19 | D18 | D17 | D16 | FUNCTION |
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **Reserved** [1] |
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | FUNCTION |
| **0** | **1** | **0** | **0** | **0** | **0** | **1** | | **Reserved** [1] |
| – | – | – | – | – | – | **–** | 0 | (L + R)/2 |
| – | – | – | – | – | – | – | 1 | **Left-channel post-BQ** [1] |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
| **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **Reserved** [1] |

(1)   Default values are in **bold**.

## PWM OUTPUT MUX REGISTER (0x25)

This DAP output mux selects which internal PWM channel is output to the external pins. Any channel can be output to any external output pin.

Bits D21–D20:      Selects which PWM channel is output to OUT_A

Bits D17–D16:      Selects which PWM channel is output to OUT_B

Bits D13–D12:      Selects which PWM channel is output to OUT_C

Bits D09–D08:      Selects which PWM channel is output to OUT_D

Note that channels are encoded so that channel 1 = 0x00, channel 2 = 0x01, …, channel 4 = 0x03. **See Figure 51 for details.**

### Table 22. PWM Output Mux Register (0x25)

| D31 | D30 | D29 | D28 | D27 | D26 | D25 | D24 | FUNCTION |
|-----|-----|-----|-----|-----|-----|-----|-----|----------|
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **Reserved**[1] |
| D23 | D22 | D21 | D20 | D19 | D18 | D17 | D16 | FUNCTION |
| **0** | **0** | – | – | – | – | – | – | **Reserved**[1] |
| **–** | **–** | **0** | **0** | – | – | – | – | **Multiplex PWM 1 to OUT_A** [1] |
| – | – | 0 | 1 | – | – | – | – | Multiplex PWM 2 to OUT_A |
| – | – | 1 | 0 | – | – | – | – | Multiplex PWM 3 to OUT_A |
| – | – | 1 | 1 | – | – | – | – | Multiplex PWM 4 to OUT_A |
| – | – | – | – | **0** | **0** | – | – | **Reserved** [1] |
| – | – | – | – | – | – | 0 | 0 | Multiplex PWM 1 to OUT_B |
| – | – | – | – | – | – | 0 | 1 | Multiplex PWM 2 to OUT_B |
| – | – | – | – | – | – | **1** | **0** | **Multiplex PWM 3 to OUT_B** [1] |
| – | – | – | – | – | – | 1 | 1 | Multiplex PWM 4 to OUT_B |
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | FUNCTION |
| **0** | **0** | – | – | – | – | – | – | **Reserved** [1] |
| – | – | 0 | 0 | – | – | – | – | Multiplex PWM 1 to OUT_C |
| – | – | **0** | **1** | – | – | – | – | **Multiplex PWM 2 to OUT_C**[1] |

(1)   Default values are in **bold**.

Product Folder Link(s): *TAS5711*

**Table 22. PWM Output Mux Register (0x25) (continued)**

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| – | – | 1 | 0 | – | – | – | – | Multiplex PWM 3 to OUT_C |
| – | – | 1 | 1 | – | – | – | – | Multiplex PWM 4 to OUT_C |
| – | – | – | – | **0** | **0** | – | – | **Reserved** [1] |
| – | – | – | – | – | – | 0 | 0 | Multiplex PWM 1 to OUT_D |
| – | – | – | – | – | – | 0 | 1 | Multiplex PWM 2 to OUT_D |
| – | – | – | – | – | – | 1 | 0 | Multiplex PWM 3 to OUT_D |
| – | – | – | – | – | – | **1** | **1** | **Multiplex PWM 4 to OUT_D** [1] |

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| **0** | **1** | **0** | **0** | **0** | **1** | **0** | **1** | **Reserved**[1] |

## DRC CONTROL (0x46)

Each DRC can be enabled independently using the DRC control register. The DRCs are disabled by default.

**Table 23. DRC Control Register**

| D31 | D30 | D29 | D28 | D27 | D26 | D25 | D24 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **Reserved** [1] |

| D23 | D22 | D21 | D20 | D19 | D18 | D17 | D16 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **Reserved** [1] |

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **Reserved** [1] |

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| **0** | **0** | – | – | – | – | – | – | **Reserved** [1] |
| – | – | 0 | – | – | – | – | – | Disable complementary (1 - H) low-pass filter generation |
| – | – | 1 | – | – | – | – | – | Enable complementary (1 - H) low-pass filter generation |
| – | – | – | **0** | – | – | – | – | |
| – | – | – | 1 | – | – | – | – | |
| | | | | **0** | **0** | | | **Reserved** [1] |
| – | – | – | – | – | – | **0** | – | **DRC2 turned OFF** [1] |
| – | – | – | – | – | – | 1 | – | DRC2 turned ON |
| – | – | – | – | – | – | – | **0** | **DRC1 turned OFF** [1] |
| – | – | – | – | – | – | – | 1 | DRC1 turned ON |

(1)    Default values are in **bold**.

## BANK SWITCH AND EQ CONTROL (0x50)

### Table 24. Bank Switching Command

| D31 | D30 | D29 | D28 | D27 | D26 | D25 | D24 | FUNCTION |
|-----|-----|-----|-----|-----|-----|-----|-----|----------|
| **0** | – | – | – | – | – | – | – | **32 kHz, does not use bank 3** [1] |
| 1 | – | – | – | – | – | – | – | 32 kHz, uses bank 3 |
| – | **0** | – | – | – | – | – | – | **Reserved**[1] |
| – | – | **0** | – | – | – | – | – | **Reserved**[1] |
| – | – | – | **0** | – | – | – | – | **44.1/48 kHz, does not use bank 3** [1] |
| – | – | – | 1 | – | – | – | – | 44.1/48 kHz, uses bank 3 |
| – | – | – | – | 0 | – | – | – | 16 kHz, does not use bank 3 |
| – | – | – | – | **1** | – | – | – | **16 kHz, uses bank 3** [1] |
| – | – | – | – | – | 0 | – | – | 22.025/24 kHz, does not use bank 3 |
| – | – | – | – | – | **1** | – | – | **22.025/24 kHz, uses bank 3** [1] |
| – | – | – | – | – | – | 0 | – | 8 kHz, does not use bank 3 |
| – | – | – | – | – | – | **1** | – | **8 kHz, uses bank 3** [1] |
| – | – | – | – | – | – | – | 0 | 11.025 kHz/12, does not use bank 3 |
| – | – | – | – | – | – | – | **1** | **11.025/12 kHz, uses bank 3** [1] |

| D23 | D22 | D21 | D20 | D19 | D18 | D17 | D16 | FUNCTION |
|-----|-----|-----|-----|-----|-----|-----|-----|----------|
| **0** | – | – | – | – | – | – | – | **32 kHz, does not use bank 2** [1] |
| 1 | – | – | – | – | – | – | – | 32 kHz, uses bank 2 |
| – | **1** | – | – | – | – | – | – | **Reserved** [1] |
| – | – | **1** | – | – | – | – | – | **Reserved** [1] |
| – | – | – | 0 | – | – | – | – | 44.1/48 kHz, does not use bank 2 |
| – | – | – | **1** | – | – | – | – | **44.1/48 kHz, uses bank 2** [1] |
| – | – | – | – | **0** | – | – | – | **16 kHz, does not use bank 2** [1] |
| – | – | – | – | 1 | – | – | – | 16 kHz, uses bank 2 |
| – | – | – | – | – | **0** | – | – | **22.025/24 kHz, does not use bank 2** [1] |
| – | – | – | – | – | 1 | – | – | 22.025/24 kHz, uses bank 2 |
| – | – | – | – | – | – | **0** | – | **8 kHz, does not use bank 2** [1] |
| – | – | – | – | – | – | 1 | – | 8 kHz, uses bank 2 |
| – | – | – | – | – | – | – | **0** | **11.025/12 kHz, does not use bank 2** [1] |
| – | – | – | – | – | – | – | 1 | 11.025/12 kHz, uses bank 2 |

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | FUNCTION |
|-----|-----|-----|-----|-----|-----|-----|-----|----------|
| 0 | – | – | – | – | – | – | – | 32 kHz, does not use bank 1 |
| **1** | – | – | – | – | – | – | – | **32 kHz, uses bank 1** [1] |
| – | **0** | – | – | – | – | – | – | **Reserved**[1] |
| – | – | **0** | – | – | – | – | – | **Reserved**[1] |
| – | – | – | **0** | – | – | – | – | **44.1/48 kHz, does not use bank 1** [1] |
| – | – | – | 1 | – | – | – | – | 44.1/48 kHz, uses bank 1 |
| – | – | – | – | **0** | – | – | – | **16 kHz, does not use bank 1** [1] |
| – | – | – | – | 1 | – | – | – | 16 kHz, uses bank 1 |
| – | – | – | – | – | **0** | – | – | **22.025/24 kHz, does not use bank 1** [1] |
| – | – | – | – | – | 1 | – | – | 22.025/24 kHz, uses bank 1 |
| – | – | – | – | – | – | **0** | – | **8 kHz, does not use bank 1** [1] |
| – | – | – | – | – | – | 1 | – | 8 kHz, uses bank 1 |
| – | – | – | – | – | – | – | **0** | **11.025/12 kHz, does not use bank 1** [1] |
| – | – | – | – | – | – | – | 1 | 11.025/12 kHz, uses bank 1 |

(1) Default values are in **bold**.

Product Folder Link(s): TAS5711

**Table 24. Bank Switching Command (continued)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|----|----|----|----|----|----|----|----|----------|
| **0** | | | | | | | | **EQ ON** |
| 1 | – | – | – | – | – | – | – | EQ OFF (bypass BQ 0-7 of channels 1 and 2) |
| – | **0** | – | – | – | – | – | – | **Reserved** [2] |
| – | – | **0** | – | – | – | – | – | **Ignore bank-mapping in bits D31–D8.Use default mapping.** [2] |
| | | 1 | | | | | | Use bank-mapping in bits D31–D8. |
| – | – | – | **0** | – | – | – | – | **L and R can be written independently.** [2] |
| – | – | – | 1 | – | – | – | – | L and R are ganged for EQ biquads; a write to left-channel BQ is also written to right-channel BQ. (0x29–0x2F is ganged to 0x30–0x36.Also 0x58–0x5B is ganged to 0x5C–0x5F) |
| – | – | **–** | **–** | **0** | – | – | – | **Reserved** [2] |
| – | – | – | – | – | **0** | **0** | **0** | **No bank switching. All updates to DAP** [2] |
| – | – | – | – | – | 0 | 0 | 1 | Configure bank 1 (32 kHz by default) |
| – | – | – | – | – | 0 | 1 | 0 | Configure bank 2 (44.1/48 kHz by default) |
| – | – | – | – | – | 0 | 1 | 1 | Configure bank 3 (other sample rates by default) |
| – | – | – | – | – | 1 | 0 | 0 | Automatic bank selection |
| – | – | – | – | – | 1 | 0 | 1 | Reserved |
| – | – | – | – | – | 1 | 1 | X | Reserved |

(2)    Default values are in **bold**.


# REVISION HISTORY

# PACKAGE OPTION ADDENDUM

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TAS5711PHP | ACTIVE | HTQFP | PHP | 48 | 250 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | 0 to 85 | TAS5711 | Samples |
| TAS5711PHPR | ACTIVE | HTQFP | PHP | 48 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | 0 to 85 | TAS5711 | Samples |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2)** **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
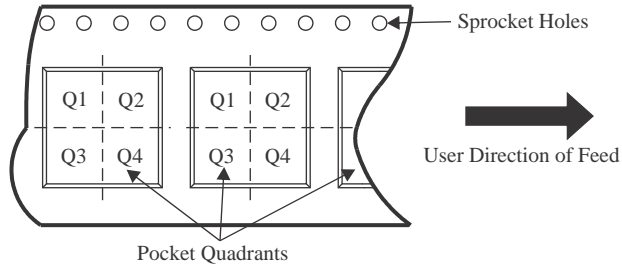
**(6)** Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

![Texas Instruments logo] **PACKAGE MATERIALS INFORMATION**

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

**TAPE DIMENSIONS**



| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TAS5711PHPR | HTQFP | PHP | 48 | 1000 | 330.0 | 16.4 | 9.6 | 9.6 | 1.5 | 12.0 | 16.0 | Q2 |

# PACKAGE MATERIALS INFORMATION

**TAPE AND REEL BOX DIMENSIONS**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TAS5711PHPR | HTQFP | PHP | 48 | 1000 | 336.6 | 336.6 | 31.8 |

## TRAY



L - Outer tray length without tabs

KO - Outer tray height

W - Outer tray width

P1 - Tray unit pocket pitch

CW - Measurement for tray edge (Y direction) to corner pocket center

CL - Measurement for tray edge (X direction) to corner pocket center
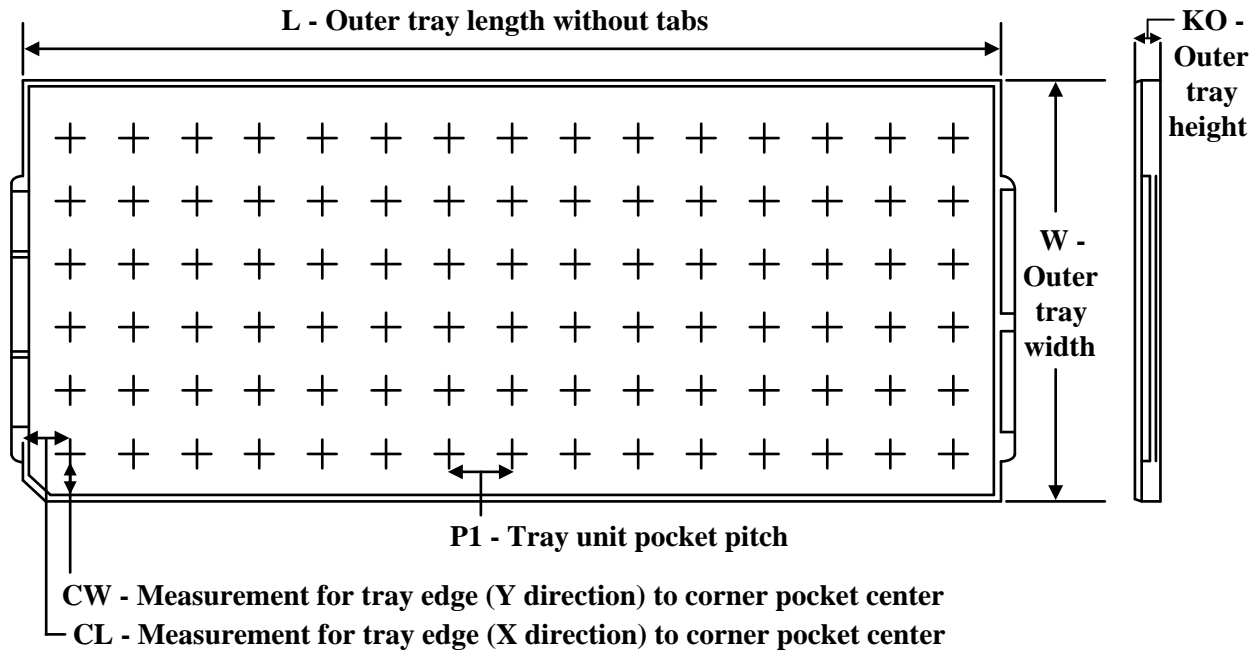
Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | Unit array matrix | Max temperature (°C) | L (mm) | W (mm) | K0 (µm) | P1 (mm) | CL (mm) | CW (mm) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TAS5711PHP | PHP | HTQFP | 48 | 250 | 10 x 25 | 150 | 315 | 135.9 | 7620 | 12.2 | 11.1 | 11.25 |
| TAS5711PHP | PHP | HTQFP | 48 | 250 | 10 x 25 | 150 | 315 | 135.9 | 7620 | 12.2 | 11.1 | 11.25 |

**PHP 48**

**7 x 7, 0.5 mm pitch**

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.
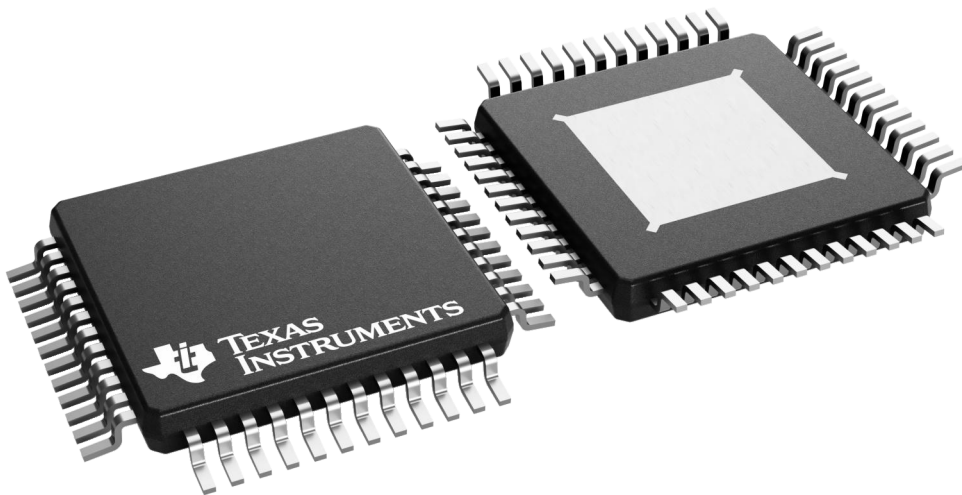


4226443/A

PHP (S−PQFP−G48)          PowerPAD™ PLASTIC QUAD FLATPACK



4146927/B 08/03

NOTES:   A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion
         D.   This package is designed to be soldered to a thermal pad on the board.  Refer to Technical Brief, PowerPad
              Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding
              recommended board layout.  This document is available at www.ti.com <http://www.ti.com>.
         E.   Falls within JEDEC MS−026

**PowerPAD is a trademark of Texas Instruments.**

PHP (S−PQFP−G48)                    PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

36                    25

37                    0,38 ⟋B⟍        24

                              Exposed Thermal Pad

4,03
3,16

48                    13

1                     12

5,17
4,04

Top View

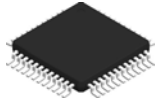Exposed Thermal Pad Dimensions

4206329−18/P   03/15

NOTE:   A.  All linear dimensions are in millimeters

        ⟋B⟍ Tie strap features may not be present.

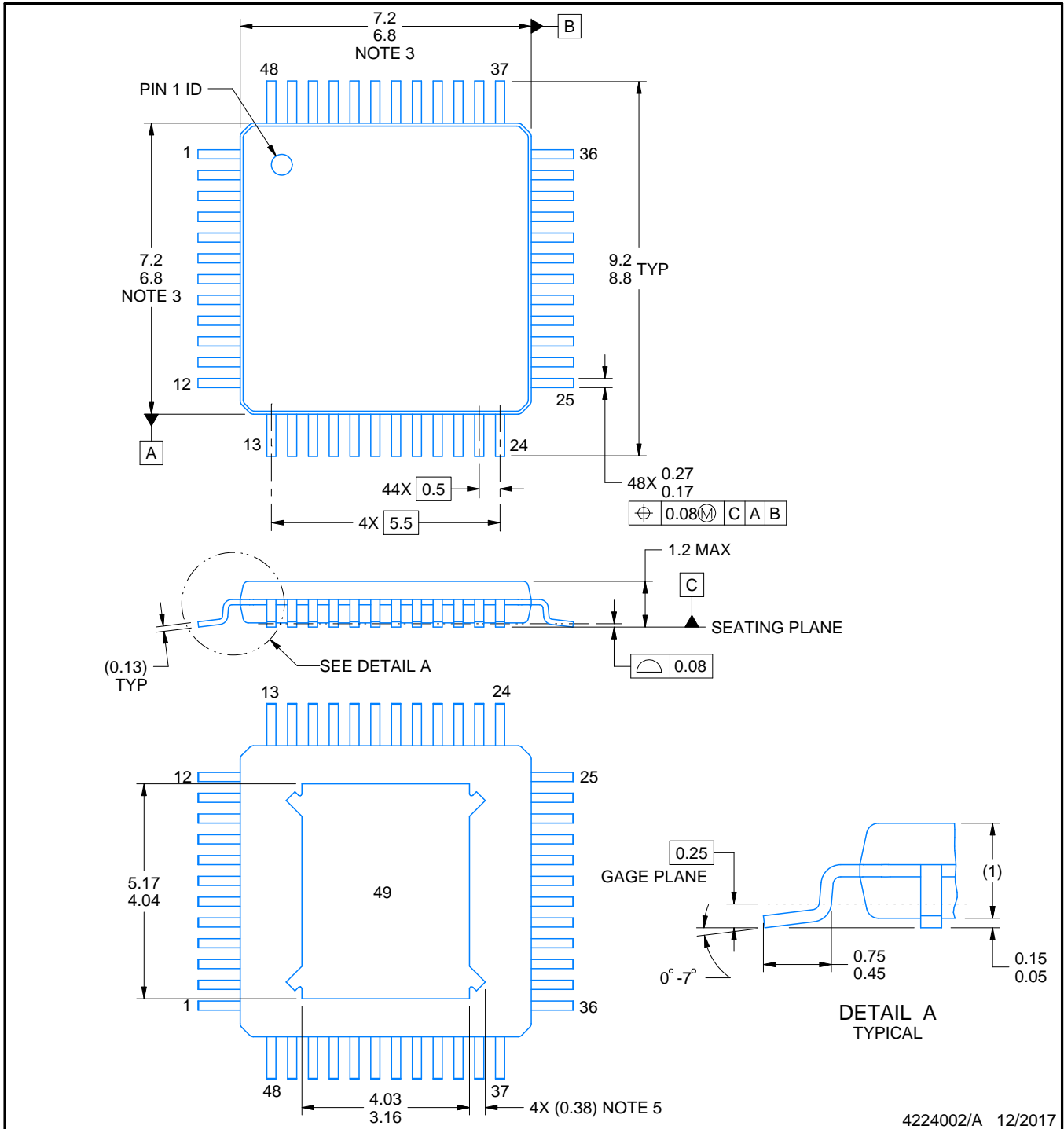**PowerPAD is a trademark of Texas Instruments**

PIN 1 ID

48

37

1

36

7.2
6.8
NOTE 3

7.2
6.8
NOTE 3

9.2
8.8 TYP

12

25

A

13

24

44X 0.5

48X 0.27
0.17

4X 5.5

⊕ 0.08Ⓜ C A B

1.2 MAX

C

(0.13)
TYP

SEE DETAIL A

SEATING PLANE

⌒ 0.08

13

24

12

25

5.17
4.04

49

0.25

GAGE PLANE

(1)

1

36

0°-7°

0.75
0.45

0.15
0.05

48

37

4X (0.38) NOTE 5

4.03
3.16

DETAIL A
TYPICAL

4224002/A   12/2017

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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.
5. Feature may not be present.

## PHP0048K

### PowerPAD™ HTQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK

(□6.5)
NOTE 10

(4.03)

SYMM
℄

48        37

SOLDER MASK
DEFINED PAD

48X (1.6)

1

48X (0.3)

36

(5.17)

SYMM
℄

49

(1.1 TYP)

(8.5)

44X (0.5)

12

25

(R0.05) TYP

(Ø 0.2) TYP
VIA

13        24

(1.1 TYP)

METAL COVERED
BY SOLDER MASK

SEE DETAILS

(8.5)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

0.05 MAX
ALL AROUND

METAL

EXPOSED METAL

SOLDER MASK
OPENING

NON SOLDER MASK
DEFINED

0.05 MIN
ALL AROUND

SOLDER MASK
OPENING

EXPOSED METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4224002/A   12/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. See technical brief, Powerpad thermally enhanced package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.

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(4.03)
BASED ON
0.125 THICK STENCIL

SYMM

48

37

SEE TABLE FOR
DIFFERENT OPENINGS
FOR OTHER STENCIL
THICKNESSES

48X (1.6)

1

36

48X (0.3)

SYMM

49

(5.17)
BASED ON
0.125 THICK
STENCIL

(8.5)

44X (0.5)

12

25

(R0.05) TYP

METAL COVERED
BY SOLDER MASK

13

24

(8.5)

SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

| STENCIL THICKNESS | SOLDER STENCIL OPENING |
|---|---|
| 0.1 | 4.51 X 5.78 |
| 0.125 | 4.03 X 5.17 (SHOWN) |
| 0.150 | 3.68 X 4.72 |
| 0.175 | 3.41 X 4.37 |

4224002/A   12/2017

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PHP (S−PQFP−G48)          PowerPAD™  PLASTIC QUAD FLATPACK



0,50

$\frac{0,27}{0,17}$

⊕ | 0,08 Ⓜ

36    25

37    24

Thermal Pad
(See Note D)

48    13

1    12

5,50 TYP

$\frac{7,20}{6,80}$ SQ

$\frac{9,20}{8,80}$ SQ

$\frac{1,05}{0,95}$

1,20 MAX

Seating Plane

⌒ | 0,08

0,13 NOM

Gage Plane

$\frac{0,15}{0,05}$

0,25

0°−7°

$\frac{0,75}{0,45}$

4146927/B 08/03

NOTES:   A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion
         D.   This package is designed to be soldered to a thermal pad on the board.  Refer to Technical Brief, PowerPad
              Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding
              recommended board layout.   This document is available at www.ti.com <http://www.ti.com>.
         E.   Falls within JEDEC MS−026

**PowerPAD is a trademark of Texas Instruments.**

PHP (S−PQFP−G48)                    PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

Top View

Exposed Thermal Pad Dimensions

4206329−9/P  03/15

NOTE:   A.   All linear dimensions are in millimeters

⚠B   Tie strap features may not be present.

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## PHP (S−PQFP−G48)  PowerPAD™ PLASTIC QUAD FLATPACK

Example Board Layout
Via pattern and copper pad size
may vary depending on layout constraints

0,127mm Thick Stencil Design Example
Reference table below for other
solder stencil thicknesses
(Note E)

44x0,5

Via Keep Out
(0,4mm x 0,6mm)

Note D

1,0

48x1,55

44x0,5

5,17

8,2

4,04

48x0,25

4,04 Y

8,2

1,0

5,17

20x∅0,3

X

Pin 1

8,2

8,2

Non Solder Mask Defined Pad

Example Solder Mask Opening
(Note F)

0,3

| Center Power Pad Solder Stencil Opening | | |
|---|---|---|
| Stencil Thickness | X | Y |
| 0.1mm | 5.55 | 4.25 |
| 0.127mm | 5.17 | 4.04 |
| 0.152mm | 4.90 | 3.70 |
| 0.178mm | 4.50 | 3.50 |

1,6

0,05
All Around

Pad Geometry
(Note C)

4207626−7/I 10/15
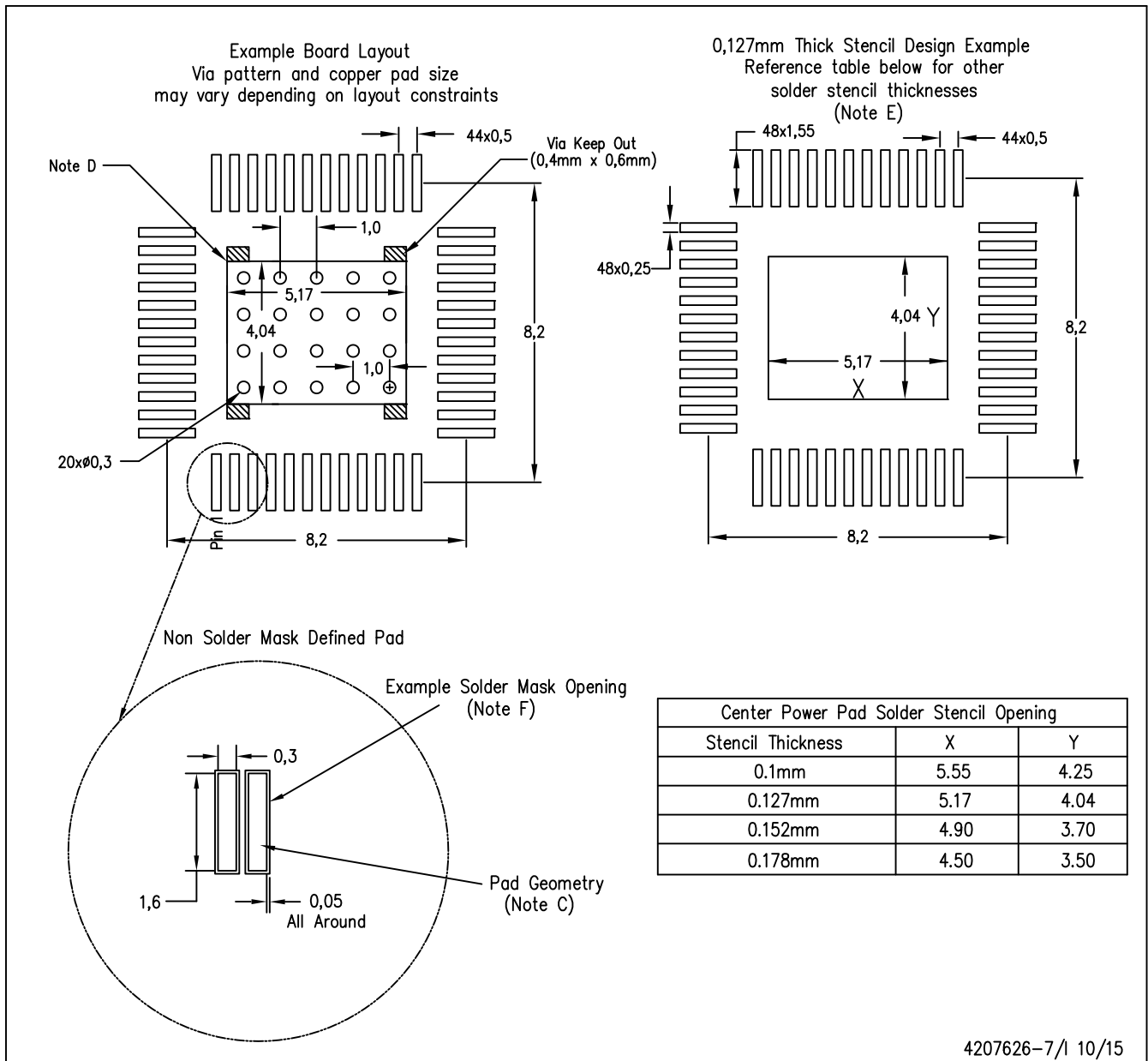
NOTES:   A.   All linear dimensions are in millimeters.
        B.   This drawing is subject to change without notice.
        C.   Publication IPC−7351 is recommended for alternate designs.
        D.   This package is designed to be soldered to a thermal pad on the board.  Refer to Technical Brief, PowerPad
            Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets
            for specific thermal information, via requirements, and recommended board layout.  These documents are available at
            www.ti.com <http://www.ti.com>.
        E.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release.  Customers should
            contact their board assembly site for stencil design recommendations.  Refer to IPC 7525 for stencil design considerations.
        F.   Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting
            options for vias placed in the thermal pad.

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