TPA6133A2 138-mW DirectPath™ Stereo Headphone Amplifier

1 Features

- DirectPath™ Ground-Referenced Outputs
  - Eliminates Output DC Blocking Capacitors
  - Reduces Board Area
  - Reduces Component Height and Cost
  - Full Bass Response Without Attenuation
- Power Supply Voltage Range: 2.5 V to 5.5 V
- High Power Supply Rejection Ratio (>100 dB PSRR)
- Differential Inputs for Maximum Noise Rejection (69 dB CMRR)
- High-Impedance Outputs When Disabled
- Advanced Pop and Click Suppression Circuitry
- GPIO Control for Shutdown
- 20 Pin, 4 mm x 4 mm WQFN Package

2 Applications

- Mobile Phones
- Audio Headsets
- Notebook Computers
- High Fidelity Applications

3 Description

The TPA6133A2 is a stereo DirectPath™ headphone amplifier with GPIO control. The TPA6133A2 has minimal quiescent current consumption, with a typical I_{DD} of 4.2 mA, making it optimal for portable applications. The GPIO control allows the device to be put in a low power shutdown mode.

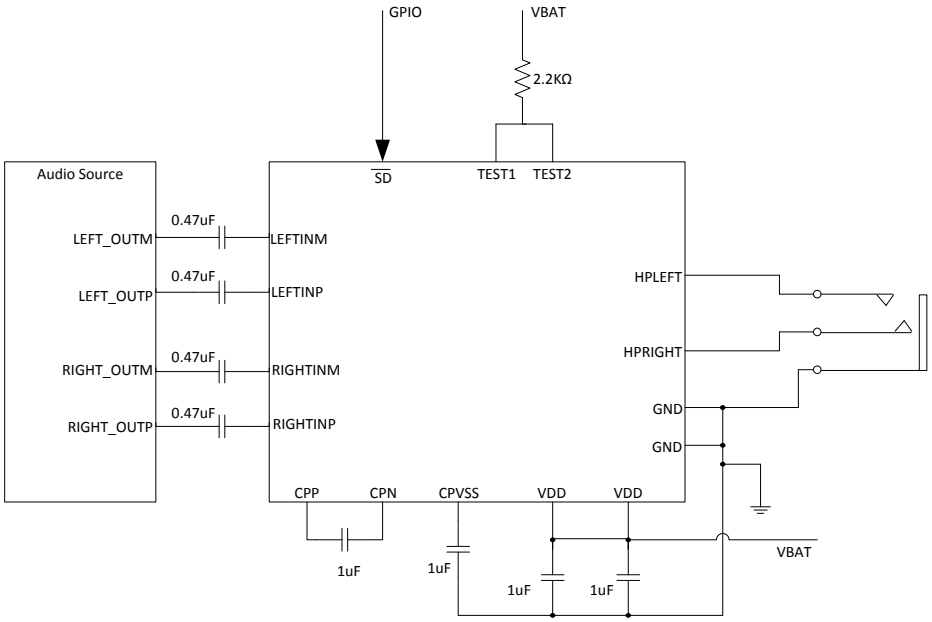
The TPA6133A2 is a high fidelity amplifier with an SNR of 93 dB. A PSRR greater than 100 dB enables direct-to-battery connections without compromising the listening experience. The output noise of 12 µVrms (typical *A-weighted*) provides a minimal noise background during periods of silence. Configurable differential inputs and high CMRR allow for maximum noise rejection in the noisy environment of a mobile device.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPA6133A2	WQFN (20)	4.00 mm x 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Simplified Application Diagram



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (August 2014) to Revision B — **Page**

- Changed "PIN QFN" To: "NUMBER" in the Pin Functions table ... 3
- Added a NOTE to the Applications and Implementation section ... 13
- Added new paragraph to the Application Information section ... 13

Changes from Original (June 2013) to Revision A — **Page**

- Added Handling Rating table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section. ... 1
- Added the Device Information Table ... 1
- Moved "Minimum Load Impedance" From the Absolute Maximum Ratings table To the Recommended Operating Conditions table ... 4
- Added the Thermal Information Table ... 4
- Changed text in the Overview section From: "toggling the $\overline{SD}$ pin to logic 1." To: "asserting the $\overline{SD}$ pin to logic 1." ... 10
- Changed text in the Headphone Amplifier section From: "the output signal is severely clipped" To: "power consumption will be higher" ... 11
- Added the Optional Test Setup section ... 15
- Added the Layout Example image ... 17

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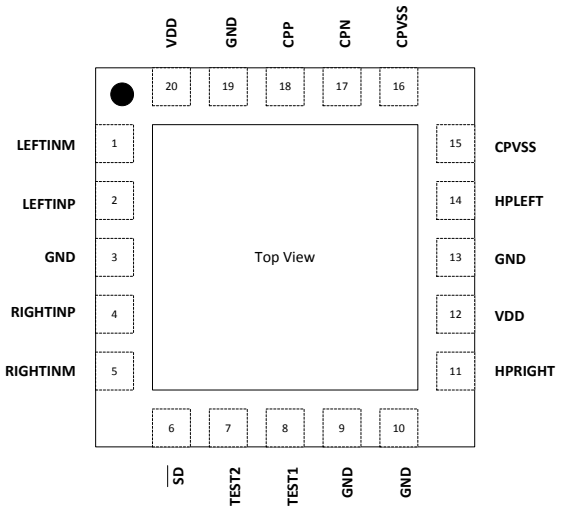
6 Pin Configuration and Functions

RTJ Package
(Top VIEW)



Pin Functions

PIN		INPUT, OUTPUT, POWER	DESCRIPTION
NAME	NUMBER		
LEFTINM	1	I	Left channel negative differential input. Impedance must be matched to LEFTINP. Connect the left input to LEFTINM when using single-ended inputs.
LEFTINP	2	I	Left channel positive differential input. Impedance must be matched to LEFTINM. AC ground LEFTINP near signal source while maintaining matched impedance to LEFTINM when using single-ended inputs.
RIGHTINP	4	I	Right channel positive differential input. Impedance must be matched to RIGHTINM. AC ground RIGHTINP near signal source while maintaining matched impedance to RIGHTINM when using single-ended inputs.
GND	3, 9, 10, 13	P	Analog ground. Must be connected to common supply GND. It is recommended that this pin be used to decouple V_{DD} for analog. Use pin 13 to decouple pin 12 on the QFN package.
RIGHTINM	5	I	Right channel negative differential input. Impedance must be matched to RIGHTINP. Connect the right input to RIGHTINM when using single-ended inputs.
$\overline{SD}$	6	I	Shutdown. Active low logic. 5V tolerant input.
TEST2	7	I	Factory test pins. Pull up to VDD supply. See Applications Diagram.
TEST1	8	I	Factory test pins. Pull up to VDD supply. See Applications Diagram.
HPRIGHT	11	O	Headphone light channel output. Connect to the right terminal of the headphone jack.
V_{DD}	12	P	Analog V_{DD}. V_{DD} must be connected to common V_{DD} supply. Decouple with its own 1-µF capacitor to analog ground (pin 13).
HPLEFT	14	O	Headphone left channel output. Connect to left terminal of headphone jack.
CPVSS	15, 16	P	Negative supply generated by the charge pump. Decouple to pin 19 or a GND plane. Use a 1 µF capacitor.
CPN	17	P	Charge pump flying capacitor negative terminal. Connect one side of the flying capacitor to CPN.
CPP	18	P	Charge pump flying capacitor positive terminal. Connect one side of the flying capacitor to CPP.
GND	19	P	Charge pump ground. GND must be connected to common supply GND. It is recommended that this pin be decoupled to the V_{DD} of the charge pump pin (pin 20 on the QFN).
V_{DD}	20	P	Charge pump voltage supply. V_{DD} must be connected to the common V_{DD} voltage supply. Decouple to GND (pin 19) with its own 1 µF capacitor.
Thermal pad	Die Pad	P	Solder the thermal pad on the bottom of the QFN package to the GND plane of the PCB. It is required for mechanical stability and will enhance thermal performance.

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7 Specification

7.1 Absolute Maximum Ratings(1)

over operating free-air temperature range, T_A = 25°C (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage, V_{DD}		–0.3	6	V
Input voltage	RIGHTINx, LEFTINx	CPVSS-0.2 V to minimum of (3.6 V, VDD+0.2 V)		
	$\overline{SD}$, TEST1, TEST2	–0.3	7	V
Output continuous total power dissipation		See the Thermal Information Table		
Operating free-air temperature range, T_A		–40	85	°C
Operating junction temperature range, T_J		–40	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	–3	3	kV
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	–750	750	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

			MIN	MAX	UNIT
	Supply voltage, V_{DD}		2.5	5.5	V
V_{IH}	High-level input voltage	TEST1, TEST2, $\overline{SD}$	1.3		V
V_{IL}	Low-level input voltage	$\overline{SD}$		0.35	V
	Minimum Load Impedance		12.8		Ω
T_A	Operating free-air temperature		–40	85	°C

7.4 Thermal Information

THERMAL METRIC(1)		RTJ 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	34.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	32.5	
$R_{\theta JB}$	Junction-to-board thermal resistance	11.6	
ψ_{JT}	Junction-to-top characterization parameter	0.4	
ψ_{JB}	Junction-to-board characterization parameter	11.6	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.1	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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7.5 Electrical Characteristics

T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$\|V_{OS}\|$	Output offset voltage	V_{DD} = 2.5 V to 5.5 V, inputs grounded			135	400	µV
PSRR	DC Power supply rejection ratio	V_{DD} = 2.5 V to 5.5 V, inputs grounded			–101	-85	dB
CMRR	Common mode rejection ratio	V_{DD} = 2.5 V to 5.5 V			–69		dB
$\|I_{IH}\|$	High-level input current	V_{DD} = 5.5 V, V_I = V_{DD}	TEST1, TEST2			1	µA
			$\overline{SD}$			10	
$\|I_{IL}\|$	Low-level input current	V_{DD} = 5.5 V, V_I = 0 V	$\overline{SD}$			1	µA
I_{DD}	Supply current	V_{DD} = 2.5 V to 5.5 V, $\overline{SD}$ = V_{DD}			4.2	6	mA
		Shutdown mode, V_{DD} = 2.5V to 5.5 V, $\overline{SD}$ = 0 V			0.08	1	µA

7.6 Operating Characteristics

V_{DD} = 3.6 V , T_A = 25°C, R_L = 16 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
P_O	Output power	Stereo, Outputs out of phase, THD = 1%, f = 1 kHz, Gain = +4 dB	V_{DD} = 2.5V		63		mW
			V_{DD} = 3.6V		133		
			V_{DD} = 5V		142		
THD+N	Total harmonic distortion plus noise	P_O = 35 mW	f = 100 Hz		0.0096%		
			f = 1 kHz		0.007%		
			f = 20 kHz		0.0021%		
k_{SVR}	Supply ripple rejection ratio	200 mV_{pp} ripple, f = 217 Hz			-94.3	-85	dB
		200 mV_{pp} ripple, f = 1 kHz			-92		
		200 mV_{pp} ripple, f = 20 kHz			-77.1		
A_v	Channel DC Gain	$\overline{SD}$ = V_{DD}			1.597		V/V
ΔA_v	Gain matching				0.1%		
	Slew rate				0.4		V/µs
V_n	Noise output voltage	V_{DD} = 3.6V, A-weighted, Gain = +4 dB			12		$µV_{RMS}$
f_{osc}	Charge pump switching frequency			300	381	500	kHz
	Start-up time from shutdown				4.8		ms
	Differential input impedance				36.6		kΩ
SNR	Signal-to-noise ratio	P_o = 35 mW			93		dB
	Thermal shutdown	Threshold			180		°C
		Hysteresis			35		°C
Z_O	HW Shutdown HP output impedance	$\overline{SD}$ = 0 V, measured output to ground.			112		Ω
C_O	Output capacitance				80		pF

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7.7 Typical Characteristics

Table 1. Table of Graphs

		Figure
Total harmonic distortion + noise	versus Output power	Figure 1–Figure 4
Total harmonic distortion + noise	versus Frequency	Figure 5–Figure 12
Supply voltage rejection ratio	versus Frequency	Figure 13-Figure 14
Common mode rejection ratio	versus Frequency	Figure 15-Figure 16
Crosstalk	versus Frequency	Figure 17-Figure 18

$C_{(PUMP,\ DECOUPLE,\ ,BYPASS,\ CPVSS)}$ = 1 µF, C_I = 2.2 µF.
All THD + N graphs taken with outputs out of phase (unless otherwise noted).

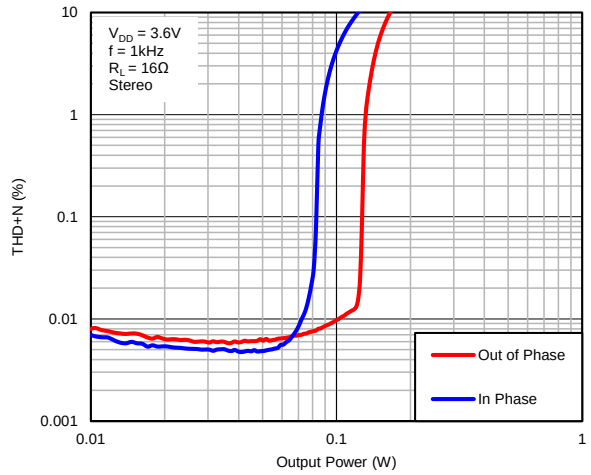

Figure 1. Total Harmonic Distortion + Noise vs Output Power

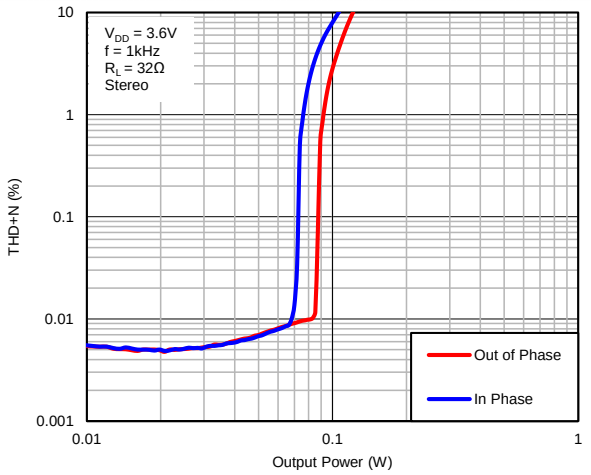

Figure 2. Total Harmonic Distortion + Noise vs Output Power

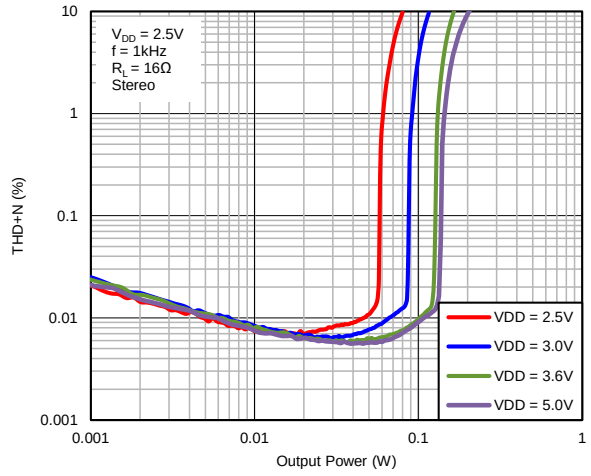

Figure 3. Total Harmonic Distortion + Noise vs Output Power

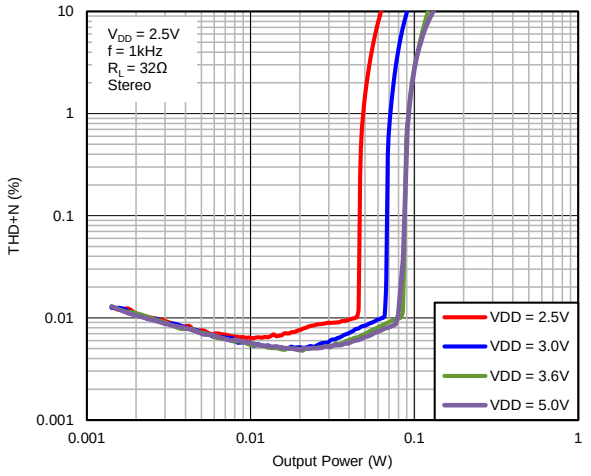

Figure 4. Total Harmonic Distortion + Noise vs Output Power

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All THD + N graphs taken with outputs out of phase (unless otherwise noted).

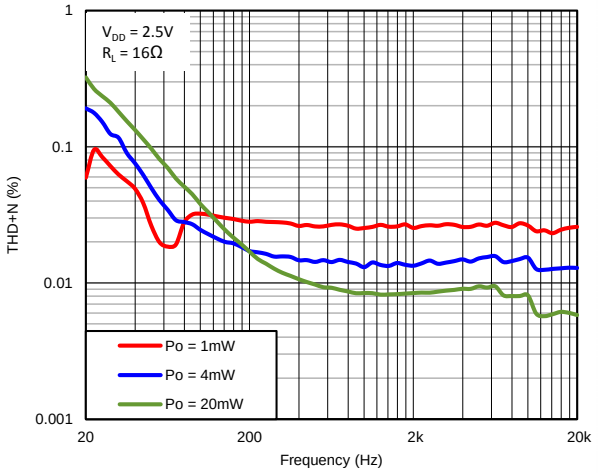

Figure 5. Total Harmonic Distortion + Noise vs Frequency

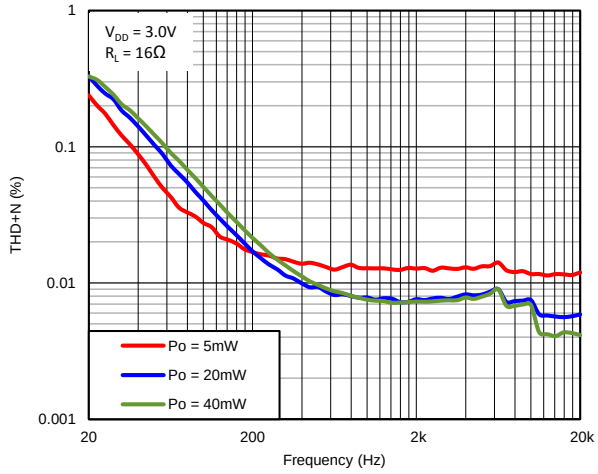

Figure 6. Total Harmonic Distortion + Noise vs Frequency

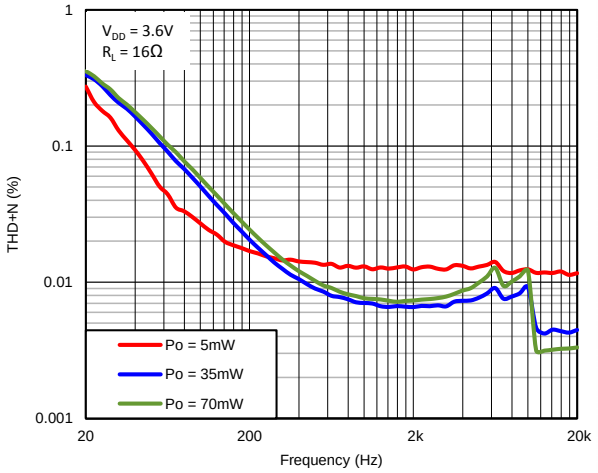

Figure 7. Total Harmonic Distortion + Noise vs Frequency

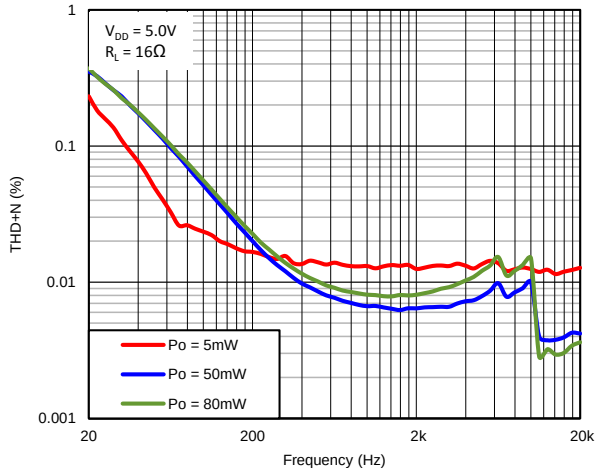

Figure 8. Total Harmonic Distortion + Noise vs Frequency

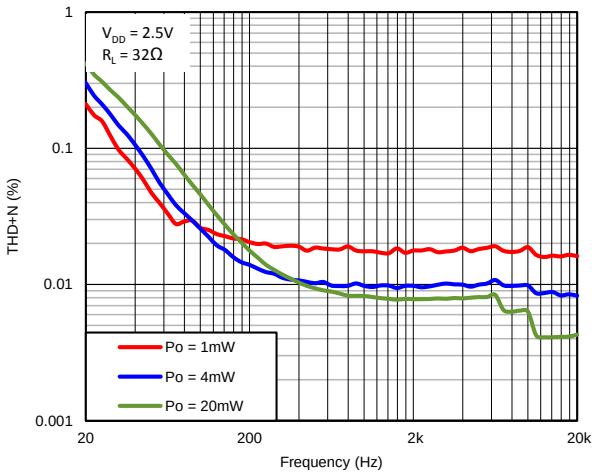

Figure 9. Total Harmonic Distortion + Noise vs Frequency

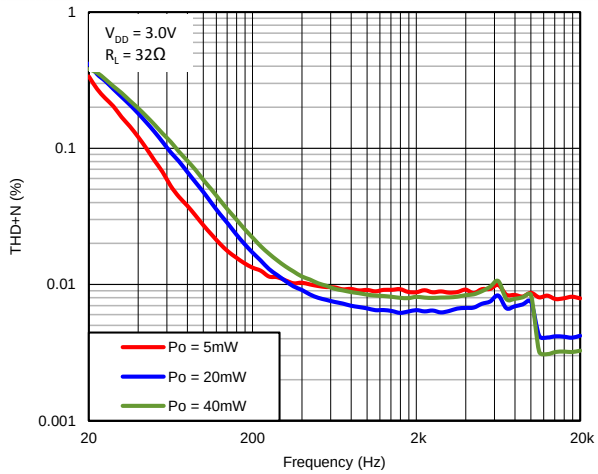

Figure 10. Total Harmonic Distortion + Noise vs Frequency

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All THD + N graphs taken with outputs out of phase (unless otherwise noted).

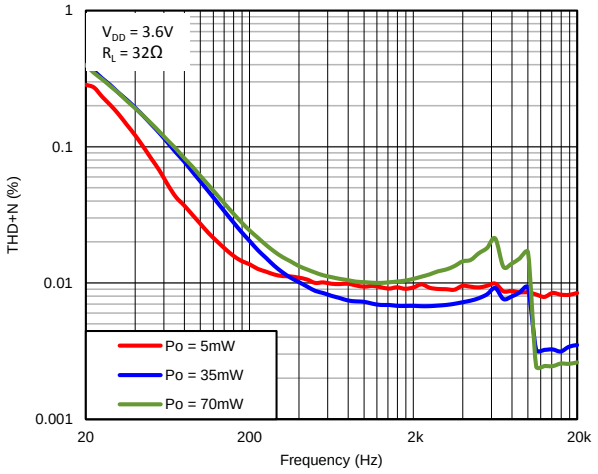

Figure 11. Total Harmonic Distortion + Noise vs Frequency

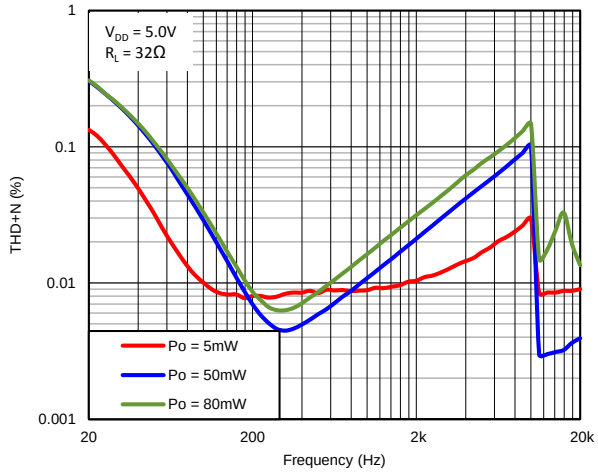

Figure 12. Total Harmonic Distortion + Noise vs Frequency

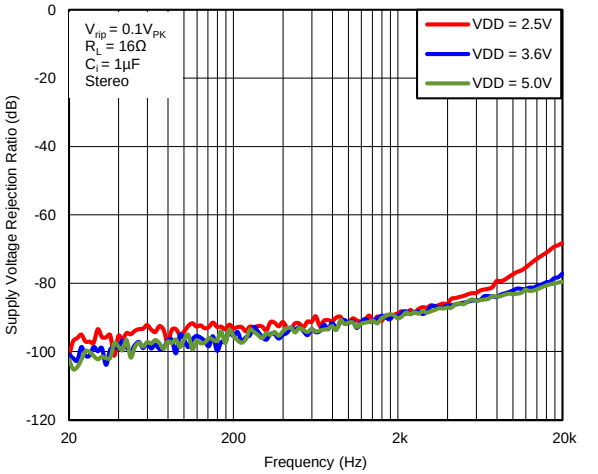

Figure 13. Supply Voltage Rejection Ratio vs Frequency

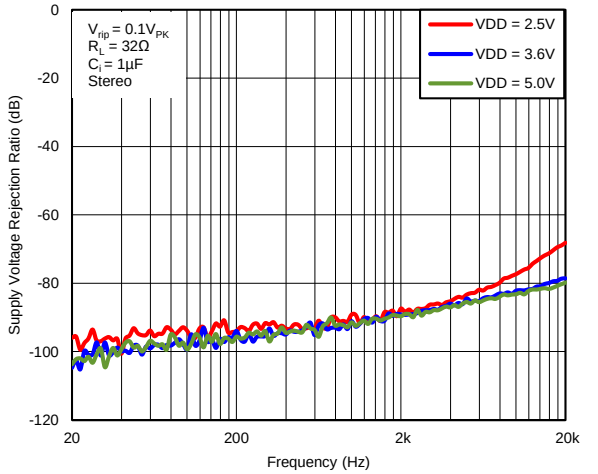

Figure 14. Supply Voltage Rejection Ratio vs Frequency

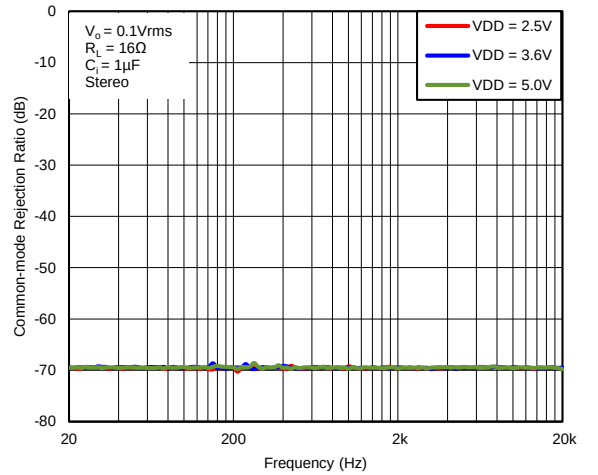

Figure 15. Common Mode Rejection Ratio vs Frequency

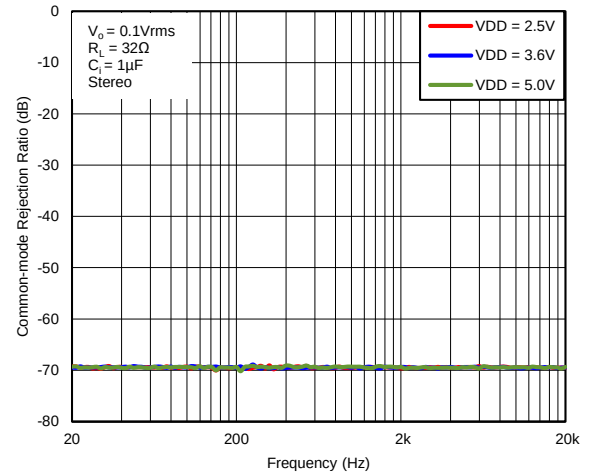

Figure 16. Common Mode Rejection Ratio vs Frequency

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All THD + N graphs taken with outputs out of phase (unless otherwise noted).

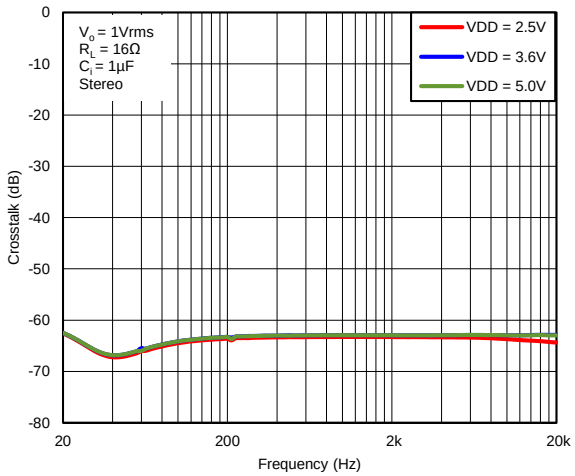

Figure 17. Crosstalk vs Frequency

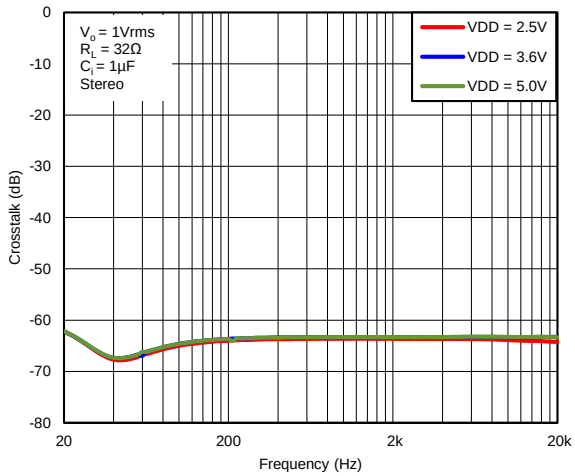

Figure 18. Crosstalk vs Frequency

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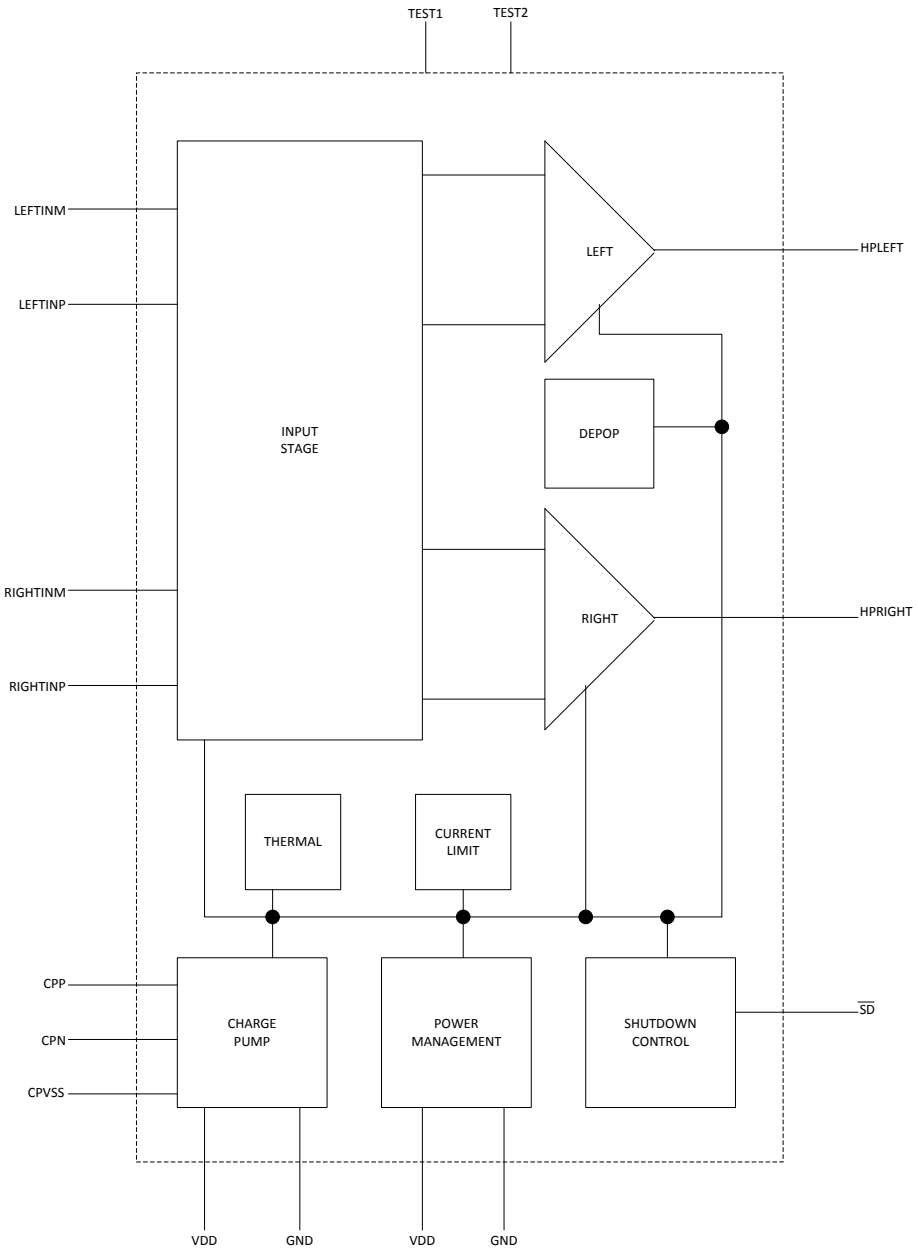
8 Detailed Description

8.1 Overview

Headphone channels and the charge pump are activated by asserting the $\overline{SD}$ pin to logic 1. The charge pump generates a negative supply voltage for the output amplifiers. This allows a 0 V bias at the outputs, eliminating the need for bulky output capacitors. The thermal block detects faults and shuts down the device before damage occurs. The current limit block prevents the output current from getting high enough to damage the device. The De-Pop block eliminates audible pops during power-up, power-down, and amplifier enable and disable events.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Headphone Amplifiers

Single-supply headphone amplifiers typically require dc-blocking capacitors. The capacitors are required because most headphone amplifiers have a dc bias on the outputs pin. If the dc bias is not removed, power consumption will be higher, and large amounts of dc current rush through the headphones, potentially damaging them. The top drawing in Figure 19 illustrates the conventional headphone amplifier connection to the headphone jack and output signal.

DC blocking capacitors are often large in value. The headphone speakers (typical resistive values of 16 Ω or 32 Ω) combine with the dc blocking capacitors to form a high-pass filter. Equation 1 shows the relationship between the load impedance (R_L), the capacitor (C_O), and the cutoff frequency (f_C).

$$f_c = \frac{1}{2\pi R_L C_O} \tag{1}$$

C_O can be determined using Equation 2, where the load impedance and the cutoff frequency are known.

$$C_O = \frac{1}{2\pi R_L f_c} \tag{2}$$

If f_c is low, the capacitor must then have a large value because the load resistance is small. Large capacitance values require large package sizes. Large package sizes consume PCB area, stand high above the PCB, increase cost of assembly, and can reduce the fidelity of the audio output signal.

Two different headphone amplifier applications are available that allow for the removal of the output dc blocking capacitors. The capless amplifier architecture is implemented in the same manner as the conventional amplifier with the exception of the headphone jack shield pin. This amplifier provides a reference voltage, which is connected to the headphone jack shield pin. This is the voltage on which the audio output signals are centered. This voltage reference is half of the amplifier power supply to allow symmetrical swing of the output voltages. Do not connect the shield to any GND reference or large currents will result. The scenario can happen if, for example, an accessory other than a floating GND headphone is plugged into the headphone connector. See the second block diagram and waveform in Figure 19.

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Feature Description (continued)

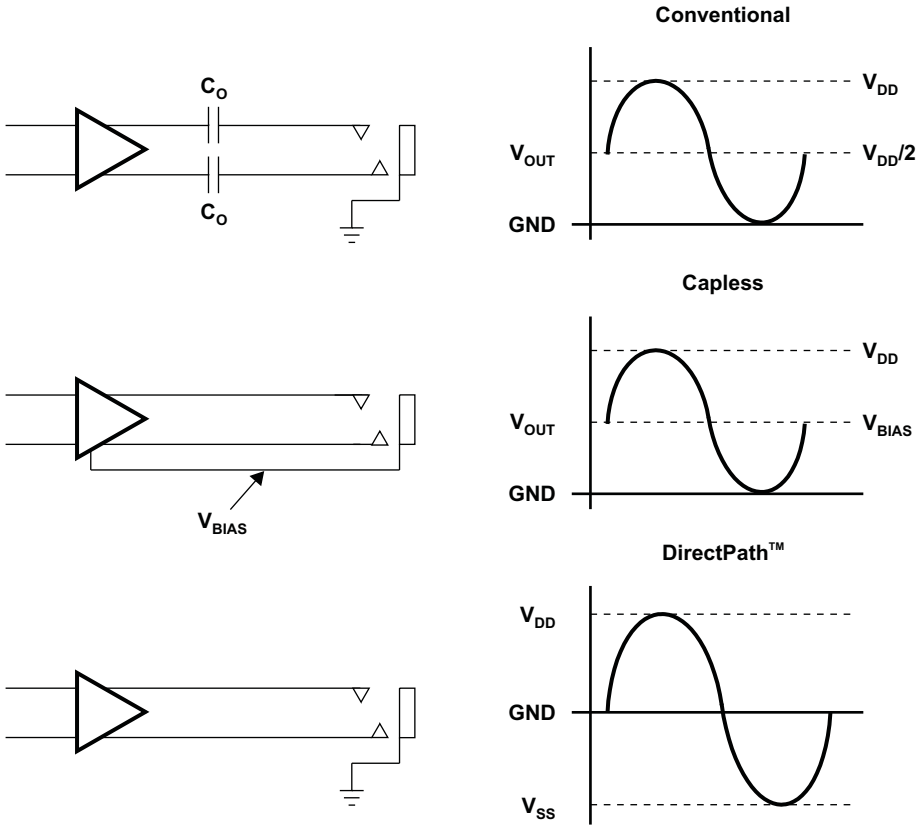

Figure 19. Amplifier Applications

The DirectPath™ amplifier architecture operates from a single supply but makes use of an internal charge pump to provide a negative voltage rail. Combining the user provided positive rail and the negative rail generated by the IC, the device operates in what is effectively a split supply mode. The output voltages are now centered at zero volts with the capability to swing to the positive rail or negative rail. The DirectPath™ amplifier requires no output dc blocking capacitors, and does not place any voltage on the sleeve. The bottom block diagram and waveform of Figure 19 illustrate the ground-referenced headphone architecture. This is the architecture of the TPA6133A2.

8.4 Device Functional Modes

8.4.1 Modes of Operation

The TPA6133A2 supports two modes of operation. When the $\overline{SD}$ pin is driven to logic 0, the device is in low power mode where the charge pump is powered down, the headphone channel is disabled and the outputs are pulled to ground. When the $\overline{SD}$ pin is driven to logic 1, the device enters an active mode with charge pump powered up and headphone channel enabled with channel gain of +4dB. The transition from inactive to active and active to inactive states is done softly to avoid audible artifacts.

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPA6133A2 is a stereo DirectPath™ headphone amplifier with GPIO control. The TPA6133A2 has minimal quiescent current consumption, with a typical I_{DD} of 4.2 mA, making it optimal for portable applications.

9.2 Typical Application

Figure 20 shows a typical application circuit for the TPA6133A2 with a stereo headphone jack and supporting power supply decupling capacitors.

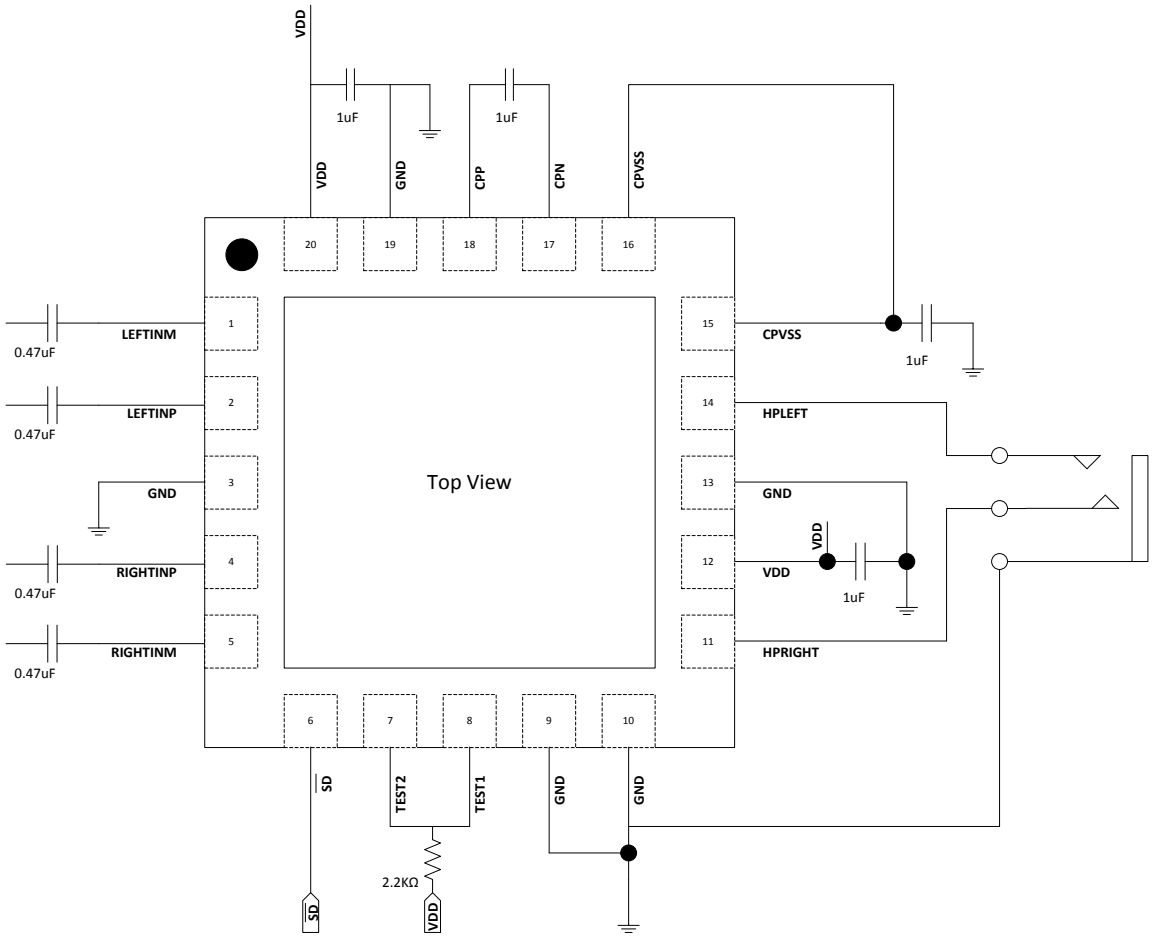

Figure 20. Simplified Applications Circuit

Typical Application (continued)

9.2.1 Design Requirements

For this design example, use the following as the input parameters.

Table 2. Design Parameters

DESIGN PARAMTER	EXAMPLE VALUE
Input voltage	2.5 V – 5.5 V
Minimum current limit	4 mA
Maximum current limit	6 mA

9.2.2 Detailed Design Procedure

9.2.2.1 Input-Blocking Capacitors

DC input-blocking capacitors block the dc portion of the audio source, and allow the inputs to properly bias. Maximum performance is achieved when the inputs of the TPA6133A2 are properly biased. Performance issues such as pop are optimized with proper input capacitors.

The dc input-blocking capacitors may be removed provided the inputs are connected differentially and within the input common mode range of the amplifier, the audio signal does not exceed ±3 V, and pop performance is sufficient.

C_{IN} is a theoretical capacitor used for mathematical calculations only. Its value is the series combination of the dc input-blocking capacitors, $C_{(DCINPUT-BLOCKING)}$. Use Equation 3 to determine the value of $C_{(DCINPUT-BLOCKING)}$. For example, if C_{IN} is equal to 0.22 µF, then $C_{(DCINPUT-BLOCKING)}$ is equal to about 0.47 µF.

$$C_{IN} = \frac{1}{2} C_{(DCINPUT-BLOCKING)} \quad (3)$$

The two $C_{(DCINPUT-BLOCKING)}$ capacitors form a high-pass filter with the input impedance of the TPA6133A2. Use Equation 3 to calculate C_{IN}, then calculate the cutoff frequency using C_{IN} and the differential input impedance of the TPA6133A2, R_{IN}, using Equation 4. Note that the differential input impedance changes with gain. The frequency and/or capacitance can be determined when one of the two values are given.

$$fc_{IN} = \frac{1}{2\pi R_{IN} C_{IN}} \quad \text{or} \quad C_{IN} = \frac{1}{2\pi fc_{IN} R_{IN}} \quad (4)$$

If a high pass filter with a -3 dB point of no more than 20 Hz is desired over all gain settings, the minimum impedance would be used in the above equation. The capacitor value by the above equation would be 0.215 µF. However, this is C_{IN}, and the desired value is for $C_{(DCINPUT-BLOCKING)}$. Multiplying C_{IN} by 2 yields 0.43 µF, which is close to the standard capacitor value of 0.47 µF. Place 0.47 µF capacitors at each input terminal of the TPA6133A2 to complete the filter.

9.2.2.2 Charge Pump Flying Capacitor and CPVSS Capacitor

The charge pump flying capacitor serves to transfer charge during the generation of the negative supply voltage. The CP_{VSS} capacitor must be at least equal to the flying capacitor in order to allow maximum charge transfer. Low ESR capacitors are an ideal selection, and a value of 1 µF is typical.

9.2.2.3 Decoupling Capacitors

The TPA6133A2 is a DirectPath™ headphone amplifier that requires adequate power supply decoupling to ensure that the noise and total harmonic distortion (THD) are low. Use good low equivalent-series-resistance (ESR) ceramic capacitors, typically 1.0 µF. Find the smallest package possible, and place as close as possible to the device V_{DD} lead. Placing the decoupling capacitors close to the TPA6133A2 is important for the performance of the amplifier. Use a 10 µF or greater capacitor near the TPA6133A2 to filter lower frequency noise signals. The high PSRR of the TPA6133A2 will make the 10 µF capacitor unnecessary in most applications.

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9.2.2.4 Optional Test Setup

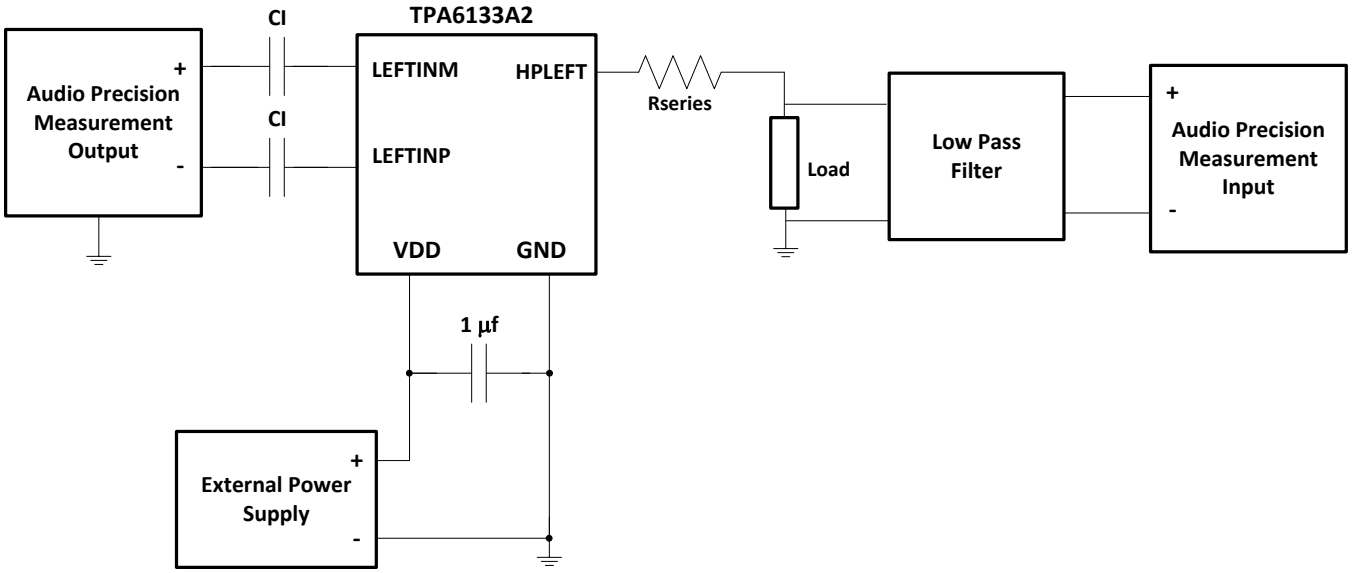

Figure 21. Test Setup

NOTE

Separate power supply decoupling caps are used on all VDD and CPVSS Pins

The low pass filter is used to remove harmonic content above the audible range.

9.2.3 Application Curves

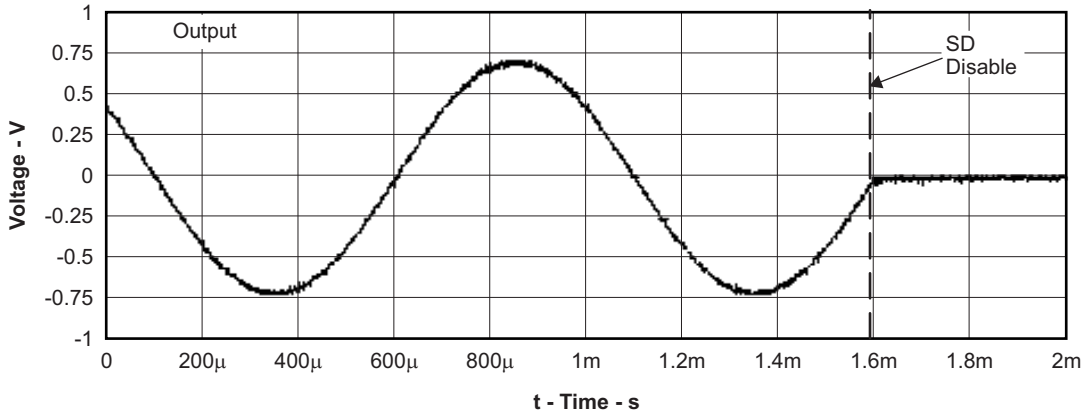

Figure 22. Shutdown Time

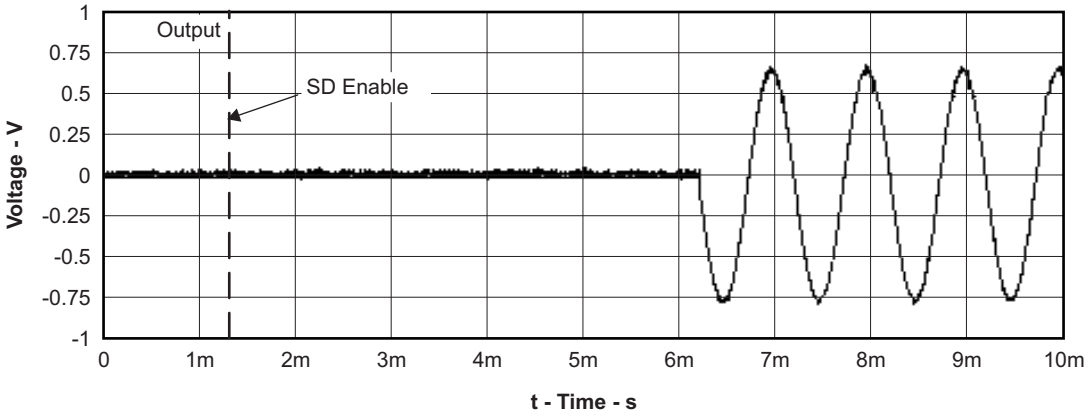

Figure 23. Startup Time

10 Power Supply Recommendations

The device is designed to operate from an input voltage supply range of 2.5 V to 5.5 V. Therefore, the output voltage range of power supply should be within this range and well regulated. The current capability of upper power should not exceed the max current limit of the power switch.

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11 Layout

11.1 Layout Guidelimes

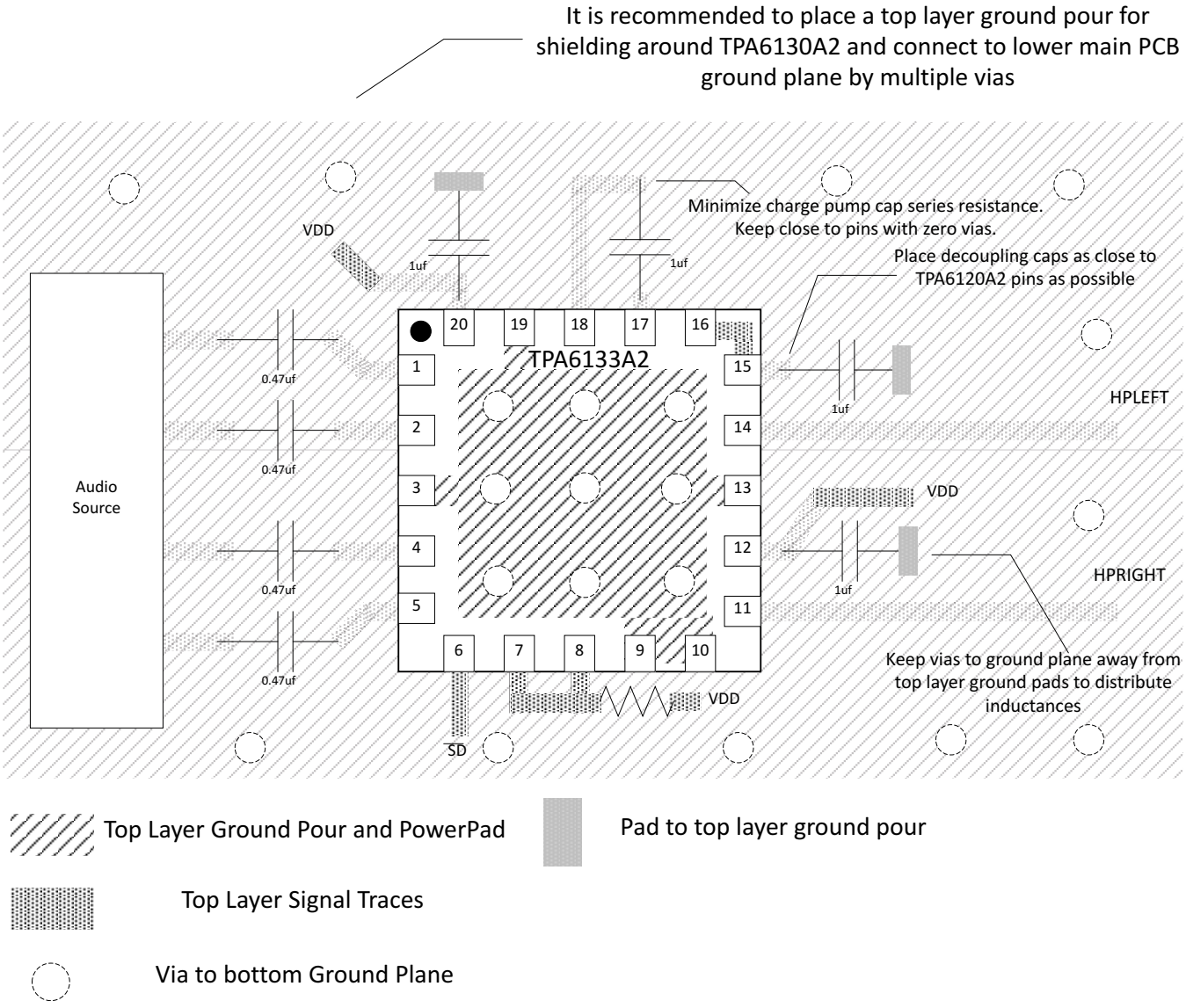
11.1.1 Exposed Pad On TPA6133A2RTJ Package

- Solder the exposed metal pad on the TPA6133A2RTJ QFN package to the a pad on the PCB. *The pad on the PCB may be grounded or may be allowed to float (not be connected to ground or power).*
- If the pad is grounded, it must be connected to the same ground as the GND pins (3, 9, 10, 13, and 19). See the layout and mechanical drawings at the end of the datasheet for proper sizing.
- Soldering the thermal pad improves mechanical reliability, improves grounding of the device, and enhances thermal conductivity of the package.

11.1.2 GND Connections

- The GND pin for charge pump should be decoupled to the charge pump V_{DD} pin, and the GND pin adjacent to the Analog V_{DD} pin should be separately decoupled to each other.

11.2 Layout Example



12 Device and Documentation Support

12.1 Trademarks

DirectPath is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPA6133A2RTJR	ACTIVE	QFN	RTJ	20	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SIZ	Samples
TPA6133A2RTJT	ACTIVE	QFN	RTJ	20	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SIZ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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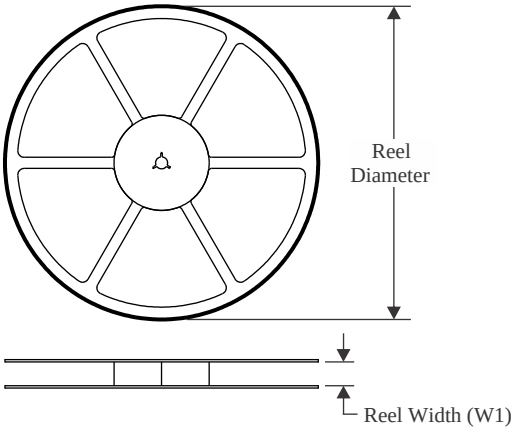
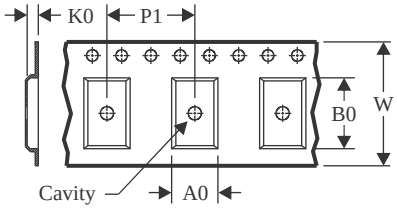
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

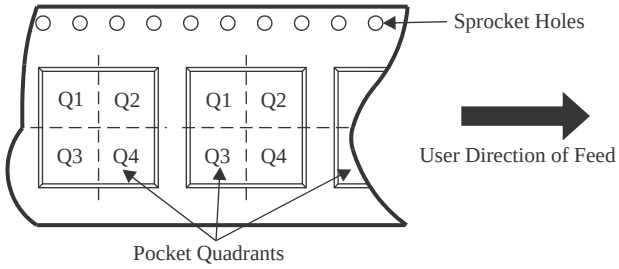


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

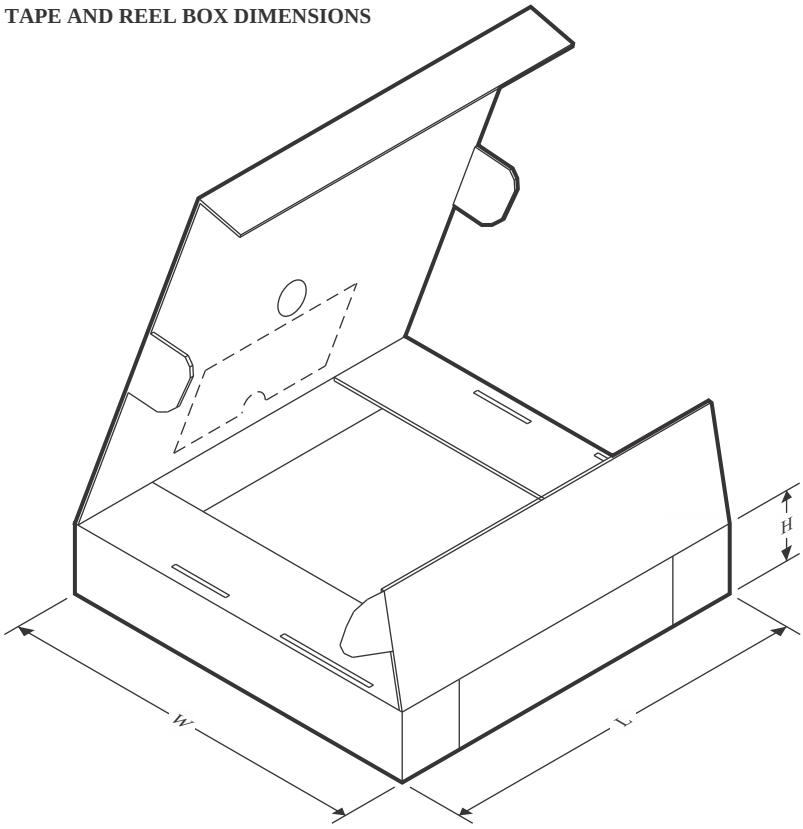
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA6133A2RTJR	QFN	RTJ	20	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPA6133A2RTJR	QFN	RTJ	20	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPA6133A2RTJR	QFN	RTJ	20	3000	330.0	12.4	4.35	4.35	1.1	8.0	12.0	Q2
TPA6133A2RTJT	QFN	RTJ	20	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA6133A2RTJR	QFN	RTJ	20	3000	367.0	367.0	35.0
TPA6133A2RTJR	QFN	RTJ	20	3000	367.0	367.0	35.0
TPA6133A2RTJR	QFN	RTJ	20	3000	338.0	355.0	50.0
TPA6133A2RTJT	QFN	RTJ	20	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

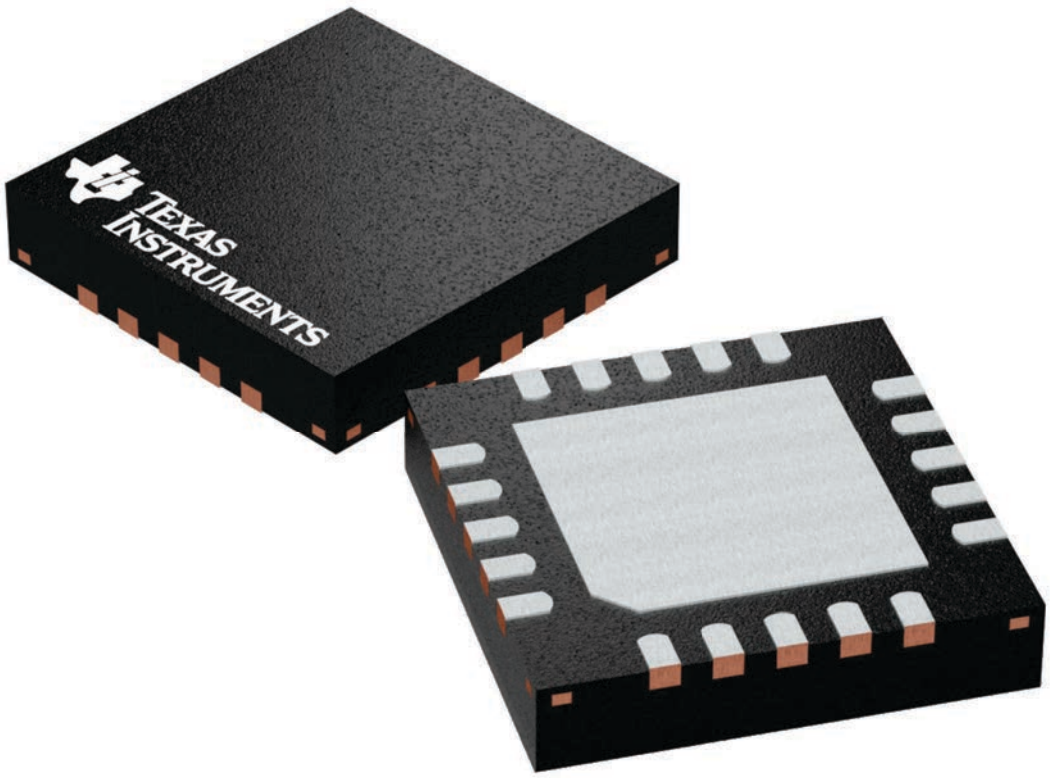
RTJ 20

WQFN - 0.8 mm max height

4 x 4, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224842/A

DATA BOOK
PACKAGE OUTLINE

LEADFRAME EXAMPLE
4222370

DRAFTSMAN: H. DENG	DATE: 09/12/2016		DIMENSIONS IN MILLIMETERS
DESIGNER: H. DENG	DATE: 09/12/2016	TEXAS INSTRUMENTS SEMICONDUCTOR OPERATIONS	CODE IDENTITY NUMBER 01295
CHECKER: V. PAKU & T. LEQUANG	DATE: 09/12/2016	ePOD, RTJ0020D / WQFN, 20 PIN, 0.5 MM PITCH	
ENGINEER: T. TANG	DATE: 09/12/2016		
APPROVED: E. REY & D. CHIN	DATE: 10/06/2016		
RELEASED: WDM	DATE: 10/24/2016		
TEMPLATE INFO: EDGE# 4218519	DATE: 04/07/2016		

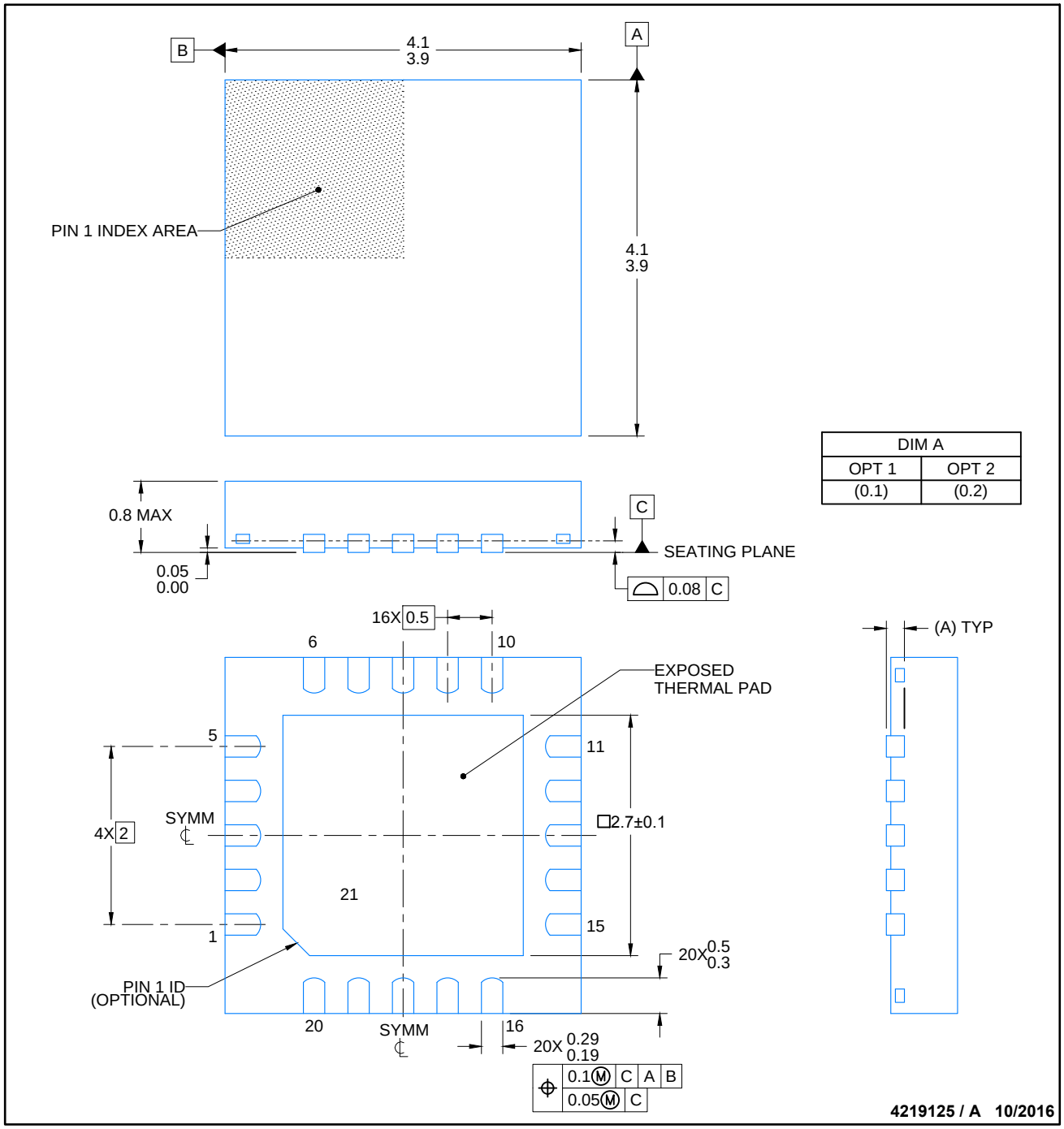
SCALE	SIZE		REV	PAGE
15X	A	4219125	A	1 OF 5

PACKAGE OUTLINE

RTJ0020D

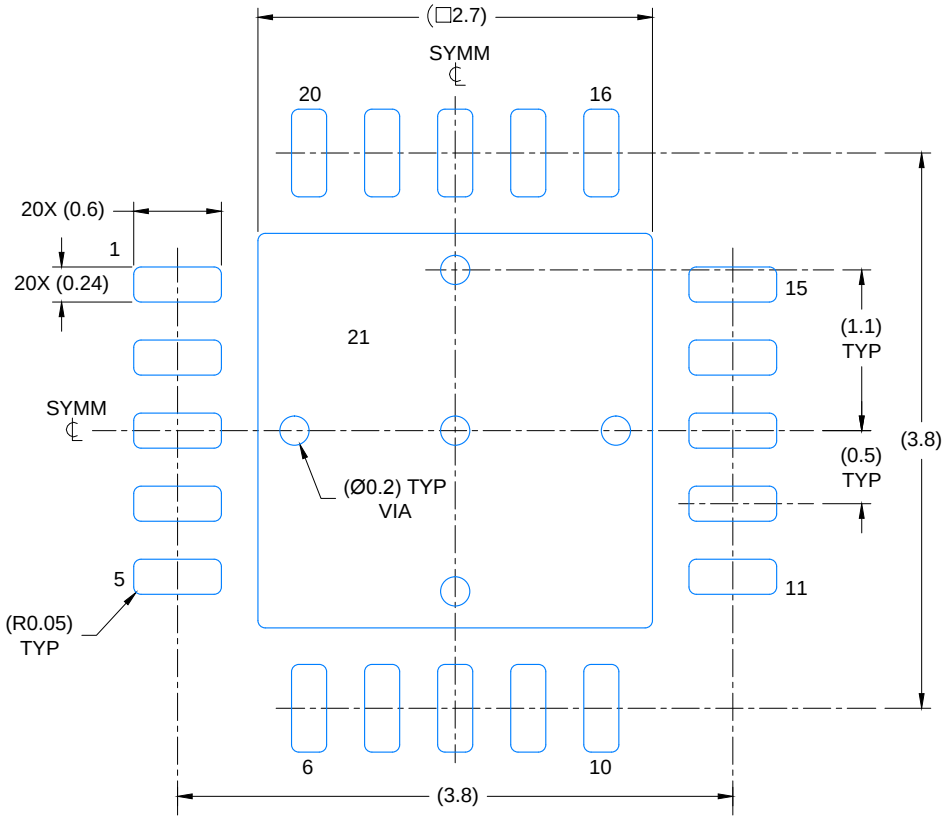
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



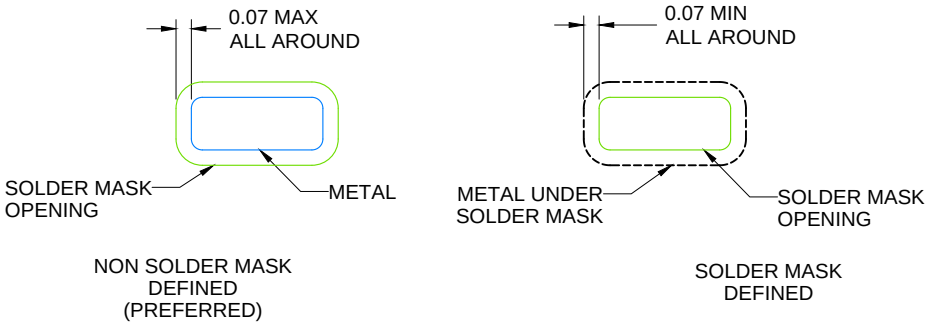
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE

SCALE: 20X

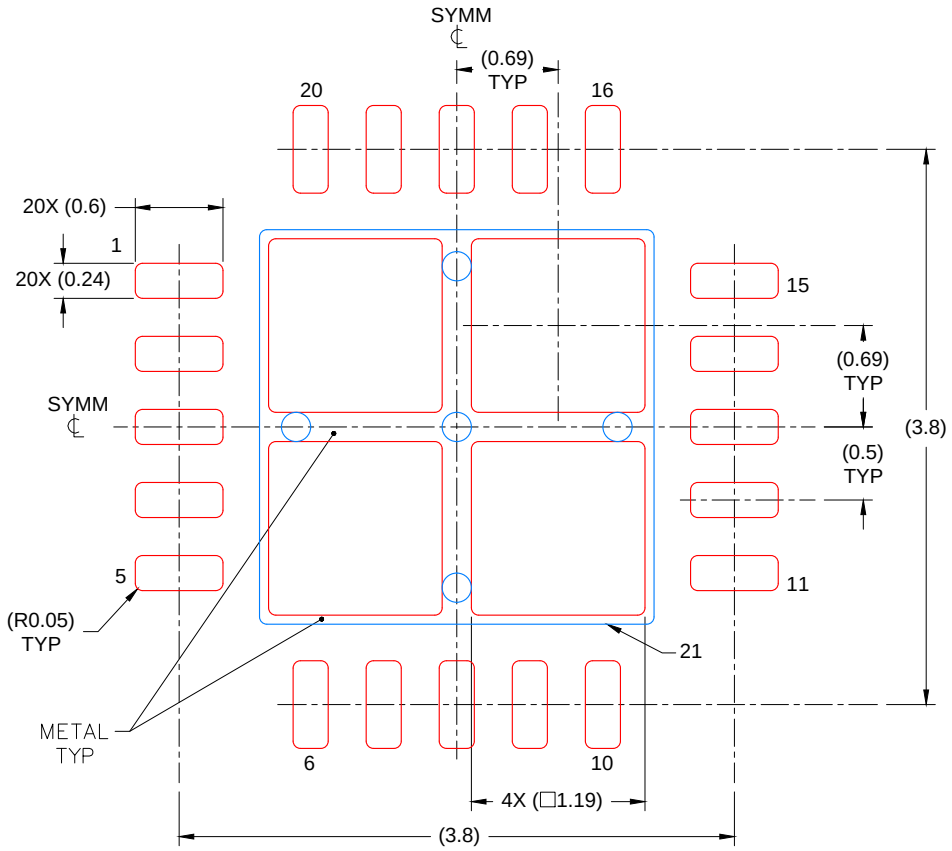


SOLDER MASK DETAILS

4219125 / A 10/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
78% PRINTED COVERAGE BY AREA
SCALE: 20X

4219125 / A 10/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

REVISIONS

REV	DESCRIPTION	ECR	DATE	ENGINEER / DRAFTSMAN
A	RELEASE NEW DRAWING	2160736	10/24/2016	T. TANG / H. DENG

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