TS3USB221 High-speed USB 2.0 (480-Mbps) 1:2 multiplexer – demultiplexer switch with single enable

1 Features

- V_{CC} Operation from 2.3 V and 3.6 V
- $V_{I/O}$ Accepts Signals up to 5.5 V
- 1.8-V Compatible Control-Pin Inputs
- Low-Power Mode When $\overline{OE}$ Is Disabled (1 μA)
- r_{ON} = 6 Ω Maximum
- Δr_{ON} = 0.2 Ω Typical
- $C_{io(on)}$ = 6 pF Maximum
- Low Power Consumption (30 μA Maximum)
- ESD > 2000-V Human-Body Model (HBM)
- High Bandwidth (1.1 GHz Typical)

2 Applications

- Routes Signals for USB 1.0, 1.1, and 2.0
- Mobile Industry Processor Interface (MIPI™) Signal Routing
- MHL 1.0

3 Description

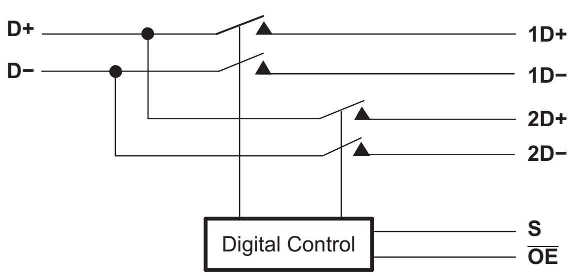
The TS3USB221 is a high-bandwidth switch specially designed for the switching of high-speed USB 2.0 signals in handset and consumer applications, such as cell phones, digital cameras, and notebooks with hubs or controllers with limited USB I/Os. The wide bandwidth (1.1 GHz) of this switch allows signals to pass with minimum edge and phase distortion. The device multiplexes differential outputs from a USB host device to one of two corresponding outputs. The switch is bidirectional and offers little or no attenuation of the high-speed signals at the outputs. The TS3USB221 is designed for low bit-to-bit skew and high channel to channel noise isolation. The TS3USB221 is also compatible with various standards, such as high-speed USB 2.0 (480 Mbps).

Device Information(1)

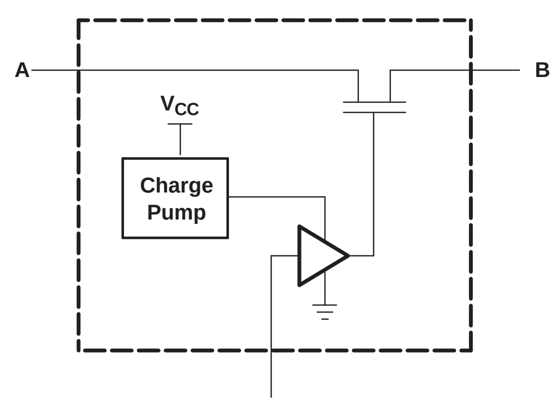
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TS3USB221	VSON (10)	3.00 mm × 3.00 mm
	UQFN (10)	1.50 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Block Diagram



Simplified Schematic, Each FET Switch (SW)



A. EN is the internal enable signal applied to the switch.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

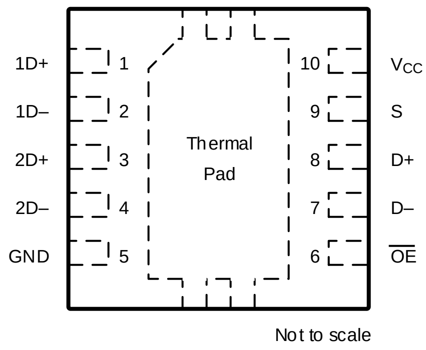
Changes from Revision I (January 2016) to Revision J	Page
• Added CDM value and table notes to the *ESD Ratings*	4

Changes from Revision H (February 2015) to Revision I	Page
• Changed V_{IH} Max from 5.5 to V_{CC} in *Recommended Operating Conditions* table	4

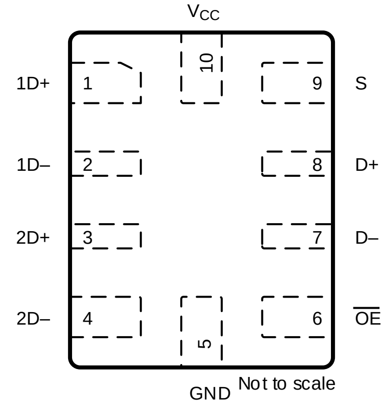
Changes from Revision G (September 2010) to Revision H	Page
• Changed first bullet of the Features FROM: V_{CC} Operation at 2.5 V and 3.3 V TO: V_{CC} Operation at 2.3 V and 3.6 V	1
• Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Removed the *Ordering Information* table	1

5 Pin Configuration and Functions

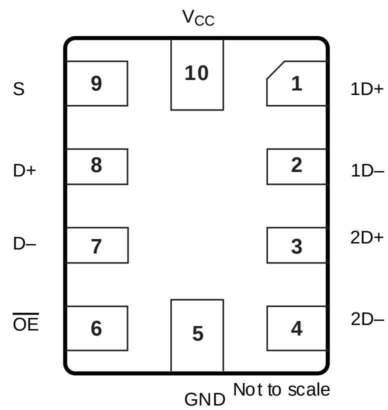
DRC Package
10-Pin VSON
(Top View)



RSE Package
10-Pin UQFN
(Top View)



RSE Package
10-Pin UQFB
(Bottom View)



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
1D+	1	I/O	USB port 1
1D–	2	I/O	
2D+	3	I/O	USB port 2
2D–	4	I/O	
GND	5	—	Ground
$\overline{OE}$	6	I	Bus-switch enable
D–	7	I/O	Common USB port
D+	8	I/O	
S	9	I	Select input
V_{CC}	10	—	Supply voltage

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	4.6	V
V_{IN}	Control input voltage(2) (3)		–0.5	7	V
$V_{I/O}$	Switch I/O voltage(2) (3) (4)		–0.5	7	V
I_{IK}	Control input clamp current	$V_{IN} < 0$		–50	mA
$I_{I/OK}$	I/O port clamp current	$V_{I/O} < 0$		–50	mA
$I_{I/O}$	ON-state switch current(5)			±120	mA
	Continuous current through V_{CC} or GND			±100	mA
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) V_I and V_O are used to denote specific conditions for $V_{I/O}$.
(5) I_I and I_O are used to denote specific conditions for $I_{I/O}$.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

See (1).

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3 V to 2.7 V	$0.46 \times V_{CC}$	V_{CC}	V
		V_{CC} = 2.7 V to 3.6 V			
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V	0	$0.25 \times V_{CC}$	V
		V_{CC} = 2.7 V to 3.6 V			
$V_{I/O}$	Data input/output voltage		0	5.5	V
T_A	Operating free-air temperature		–40	85	°C

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

6.4 Thermal Information

THERMAL METRIC(1)		TS3USB221 DRC (VSON) 10 PINS	TS3USB221 RSE (UQFN) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	57.7	169.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	87.7	84.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	32.6	94.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.2	5.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	32.8	94.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	18.5	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS			MIN	TYP[2]	MAX	UNIT
V_{IK}		V_{CC} = 3.6 V, 2.7 V,	I_I = –18 mA				–1.8	V
I_{IN}	Control inputs	V_{CC} = 3.6 V, 2.7 V, 0 V,	V_{IN} = 0 V to 3.6 V				±1	µA
I_{OZ} [3]		V_{CC} = 3.6 V, 2.7 V, V_O = 0 V to 3.6 V, V_I = 0 V,	V_{IN} = V_{CC} or GND, Switch OFF				±1	µA
I_{OFF}		V_{CC} = 0 V	$V_{I/O}$ = 0 V to 3.6 V				±2	µA
			$V_{I/O}$ = 0 V to 2.7 V				±1	
I_{CC}		V_{CC} = 3.6 V, 2.7 V, V_{IN} = V_{CC} or GND,	$I_{I/O}$ = 0 V, Switch ON or OFF				30	µA
I_{CC} (low power mode)		V_{CC} = 3.6 V, 2.7 V, V_{IN} = V_{CC} or GND	Switch disabled ($\overline{OE}$ in high state)				1	µA
ΔI_{CC} [4]	Control inputs	One input at 1.8 V, Other inputs at V_{CC} or GND	V_{CC} = 3.6 V				20	µA
			V_{CC} = 2.7 V				0.5	
C_{in}	Control inputs	V_{CC} = 3.3 V, 2.5 V,	V_{IN} = 3.3 V or 0 V			1	2	pF
$C_{io(OFF)}$		V_{CC} = 3.3 V, 2.5 V,	$V_{I/O}$ = 3.3 V or 0 V,	Switch OFF		3	4	pF
$C_{io(ON)}$		V_{CC} = 3.3 V, 2.5 V,	$V_{I/O}$ = 3.3 V or 0 V,	Switch ON		5	6	pF
r_{on} [5]		V_{CC} = 3 V, 2.3 V	V_I = 0 V,	I_O = 30 mA			6	Ω
			V_I = 2.4 V,	I_O = –15 mA			6	
Δr_{on}		V_{CC} = 3 V, 2.3 V	V_I = 0 V,	I_O = 30 mA		0.2		Ω
			V_I = 1.7,	I_O = –15 mA		0.2		
$r_{on(flat)}$		V_{CC} = 3 V, 2.3 V	V_I = 0 V,	I_O = 30 mA		1		Ω
			V_I = 1.7,	I_O = –15 mA		1		

(1) V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.
(2) All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.
(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.
(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.
(5) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

6.6 Dynamic Electrical Characteristics, V_{CC} = 3.3 V ± 10%

over operating range, T_A = –40°C to 85°C, V_{CC} = 3.3 V ± 10%, GND = 0 V

PARAMETER		TEST CONDITIONS	TYP(1)	UNIT
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 250 MHz	–40	dB
O_{IRR}	OFF isolation	R_L = 50 Ω, f = 250 MHz	–41	dB
BW	Bandwidth (–3 dB)	R_L = 50 Ω	1.1	GHz

(1) For Maximum or Minimum conditions, use the appropriate value specified under *Electrical Characteristics* for the applicable device type.

6.7 Dynamic Electrical Characteristics, V_{CC} = 2.5 V ± 10%

over operating range, T_A = –40°C to 85°C, V_{CC} = 2.5 V ± 10%, GND = 0 V

PARAMETER		TEST CONDITIONS	TYP(1)	UNIT
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 250 MHz	–39	dB
O_{IRR}	OFF isolation	R_L = 50 Ω, f = 250 MHz	–40	dB
BW	Bandwidth (–3 dB)	R_L = 50 Ω	1.1	GHz

(1) For Maximum or Minimum conditions, use the appropriate value specified under *Electrical Characteristics* for the applicable device type.

6.8 Switching Characteristics, V_{CC} = 3.3 V ± 10%

over operating range, T_A = –40°C to 85°C, V_{CC} = 3.3 V ± 10%, GND = 0 V

PARAMETER			MIN	TYP(1)	MAX	UNIT
t_{pd}	Propagation delay(2) (3)			0.25		ns
t_{ON}	Line enable time	S to D, nD			30	ns
		$\overline{OE}$ to D, nD			17	
t_{OFF}	Line disable time	S to D, nD			12	ns
		$\overline{OE}$ to D, nD			10	
$t_{SK(O)}$	Output skew between center port to any other port(2)			0.1	0.2	ns
$t_{SK(P)}$	Skew between opposite transitions of the same output (t_{PHL} – t_{PLH})(2)			0.1	0.2	ns

(1) For Maximum or Minimum conditions, use the appropriate value specified under *Electrical Characteristics* for the applicable device type.
(2) Specified by design
(3) The bus switch contributes no propagational delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25 ns for 10-pF load. This time constant adds very little propagational delay to the system because it is much smaller than the rise/fall times of typical driving signals. Propagational delay of the bus switch, when used in a system, is determined by the driving circuit on the driving side of the switch and its interactions with the load on the driven side.

6.9 Switching Characteristics, V_{CC} = 2.5 V ± 10%

over operating range, T_A = –40°C to 85°C, V_{CC} = 2.5 V ± 10%, GND = 0 V

PARAMETER			MIN	TYP(1)	MAX	UNIT
t_{pd}	Propagation delay(2) (3)			0.25		ns
t_{ON}	Line enable time	S to D, nD			50	ns
		$\overline{OE}$ to D, nD			32	
t_{OFF}	Line disable time	S to D, nD			23	ns
		$\overline{OE}$ to D, nD			12	
$t_{SK(O)}$	Output skew between center port to any other port(2)			0.1	0.2	ns
$t_{SK(P)}$	Skew between opposite transitions of the same output (t_{PHL} – t_{PLH})(2)			0.1	0.2	ns

(1) For Maximum or Minimum conditions, use the appropriate value specified under *Electrical Characteristics* for the applicable device type.
(2) Specified by design
(3) The bus switch contributes no propagational delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25 ns for 10-pF load. The time constraint adds very little propagational delay to the system because it is much smaller than the rise and fall times of typical driving signals. Propagational delay of the bus switch, when used in a system, is determined by the driving circuit on the driving side of the switch and its interactions with the load on the driven side.

6.10 Typical Characteristics

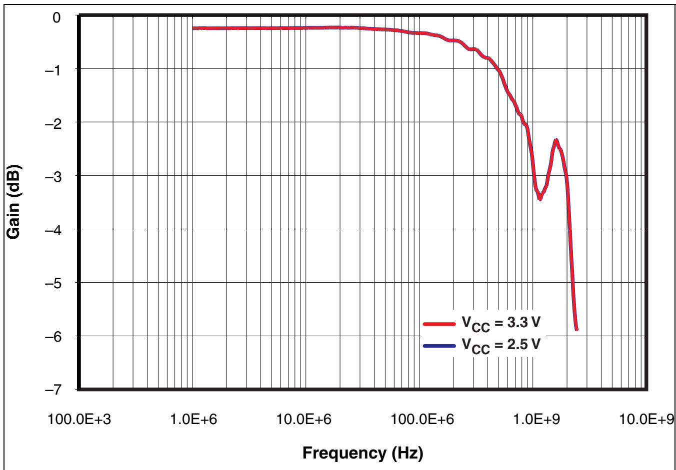


Figure 1. Gain vs Frequency

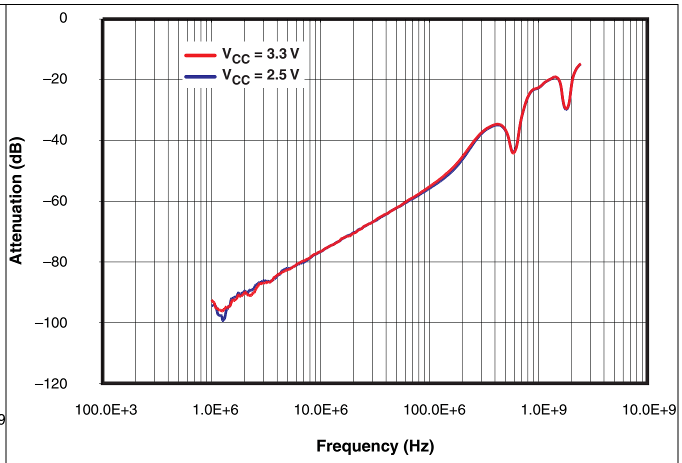


Figure 2. OFF Isolation vs Frequency

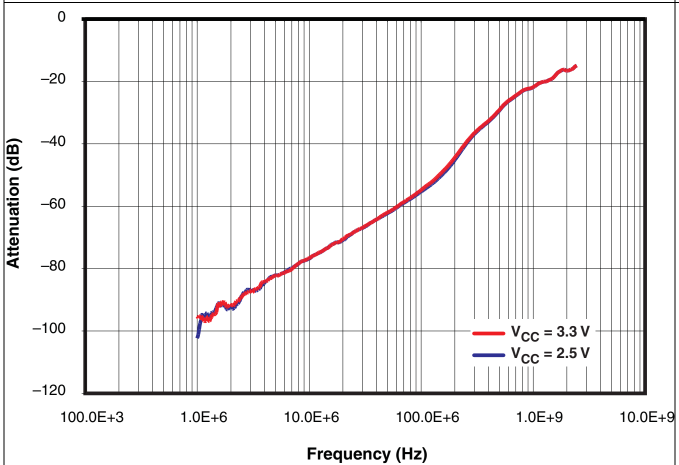


Figure 3. Crosstalk vs Frequency

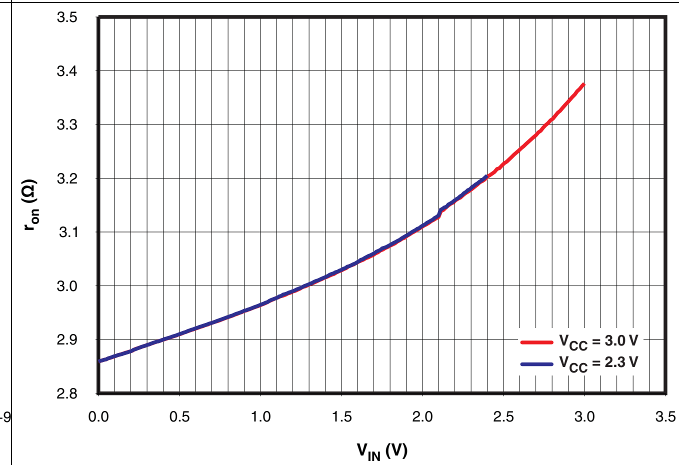


Figure 4. r_{on} vs V_{IN} (I_{OUT} = –15 mA)

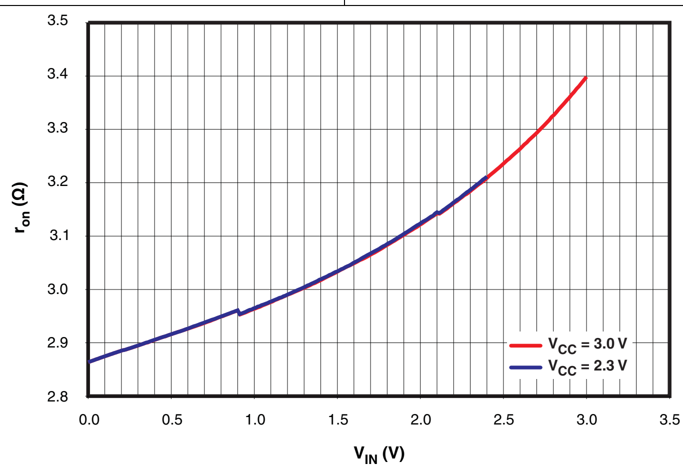
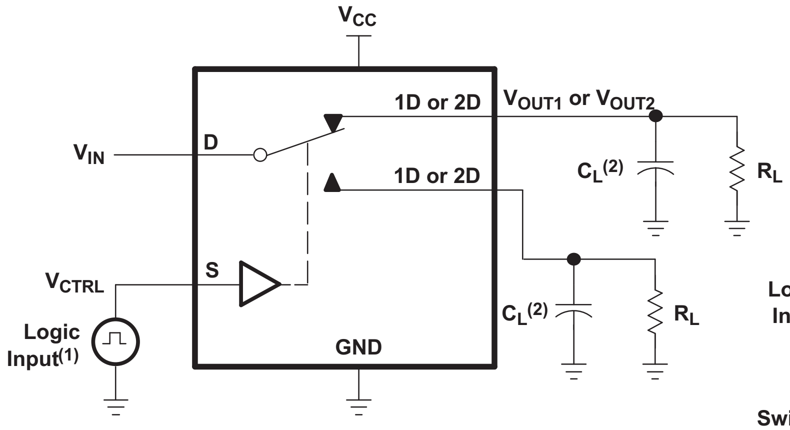
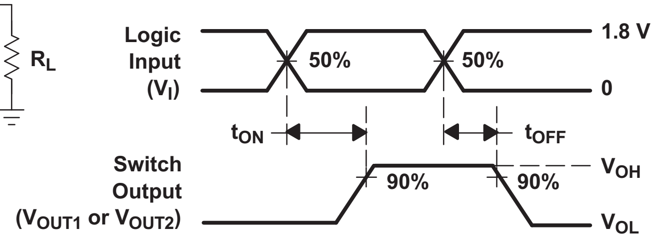


Figure 5. r_{on} vs V_{IN} (I_{OUT} = –30 mA)

7 Parameter Measurement Information

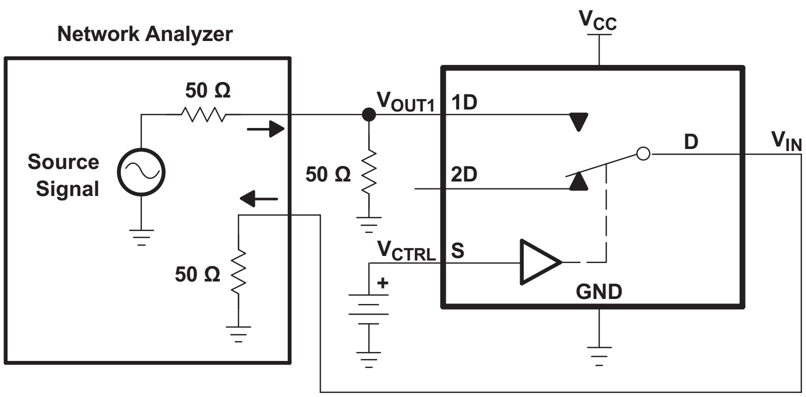


TEST	R_L	C_L	V_{COM}
t_{ON}	500 Ω	50 pF	V_+
t_{OFF}	500 Ω	50 pF	V_+



(1) All input pulses are supplied by generators having the following characteristics: PRR≤ 10 MHz, Z_O = 50Ω, t_r < 5 ns, t_f < 5 ns.
(2) C_L includes probe and jig capacitance.

Figure 6. Turnon (t_{ON}) and Turnoff Time (t_{OFF})



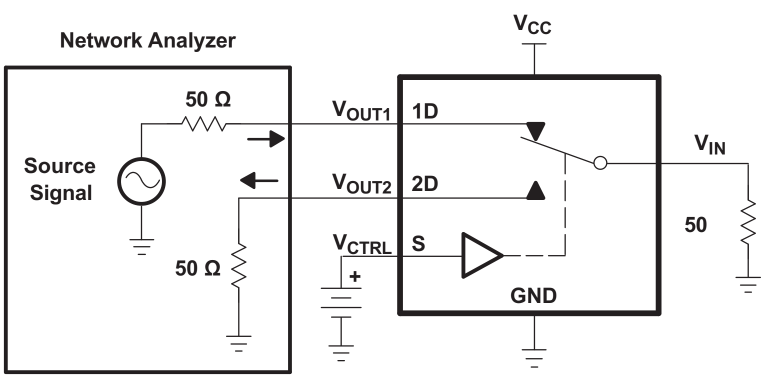
Channel OFF: 1D to D
$V_{CTRL} = V_{CC}$ or GND

<u>Network Analyzer Setup</u>

Source Power = 0 dBm
(632-mV P-P at 50-Ω load)

DC Bias = 350 mV

Figure 7. OFF Isolation (O_{ISO})



Channel ON: 1D to D
Channel OFF: 2D to D
$V_{CTRL} = V_{CC}$ or GND

<u>Network Analyzer Setup</u>

Source Power = 0 dBm
(632-mV P-P at 50-Ω load)

DC Bias = 350 mV

Figure 8. Crosstalk (X_{TALK})

Parameter Measurement Information (continued)

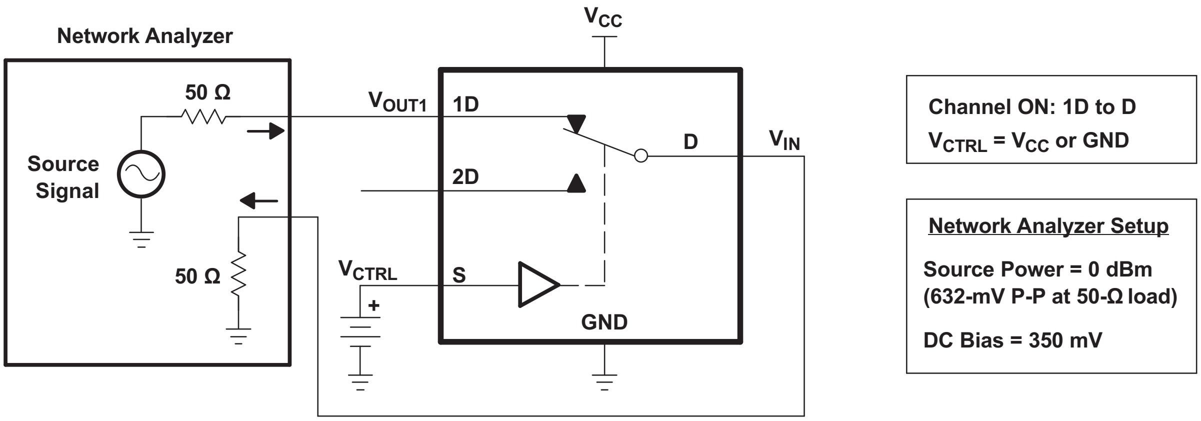


Figure 9. Bandwidth (BW)

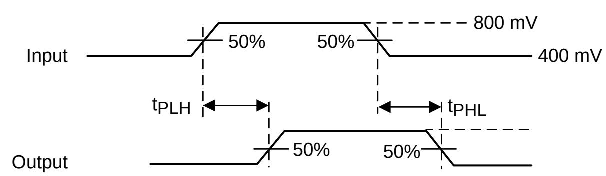


Figure 10. Propagation Delay

Parameter Measurement Information (continued)

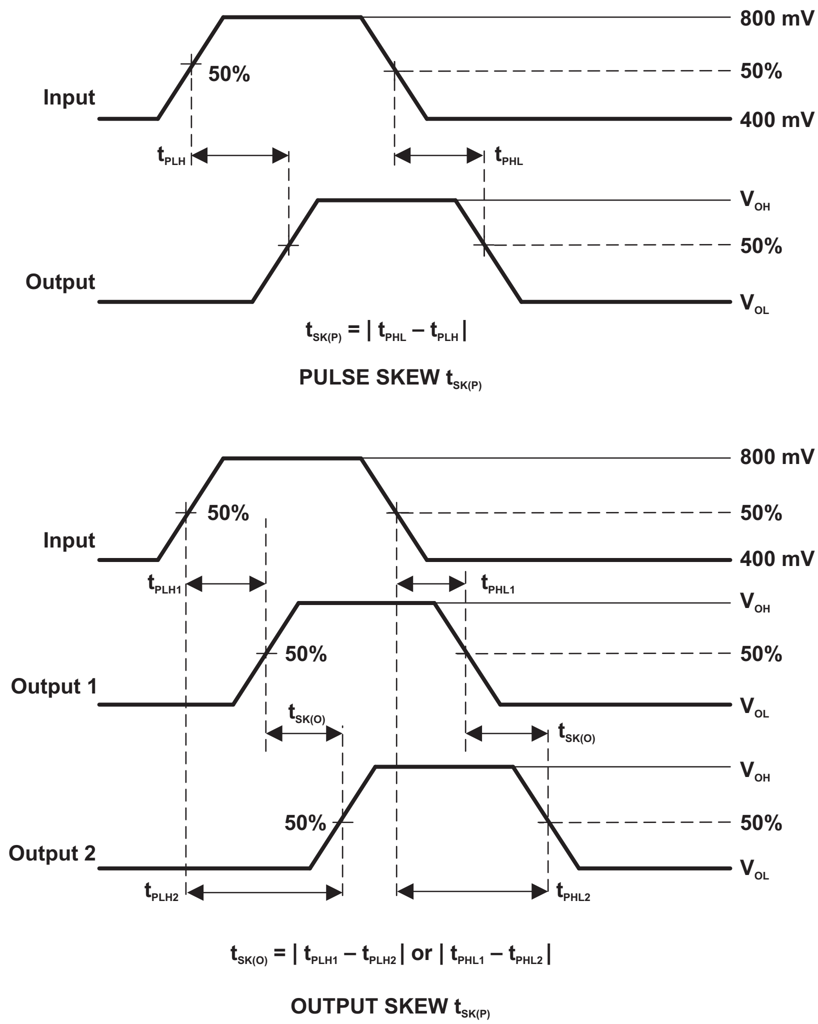


Figure 11. Skew Test

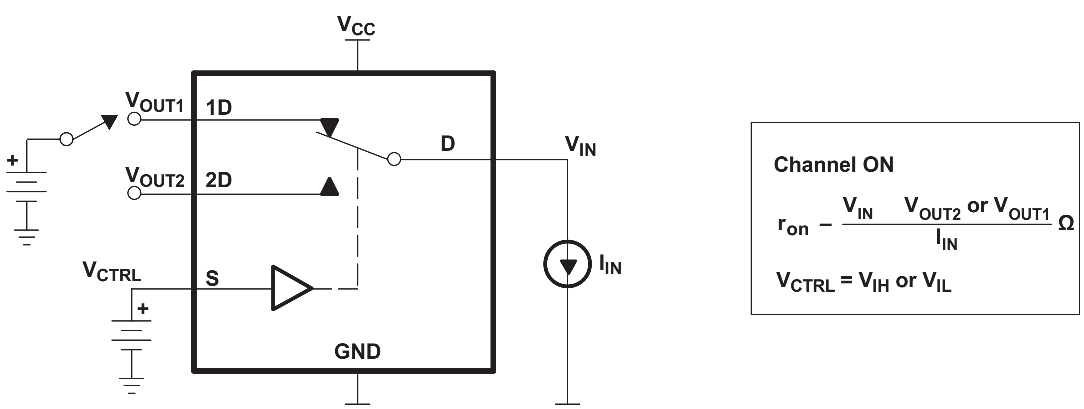


Figure 12. ON-State Resistance (r_{on})

Parameter Measurement Information (continued)

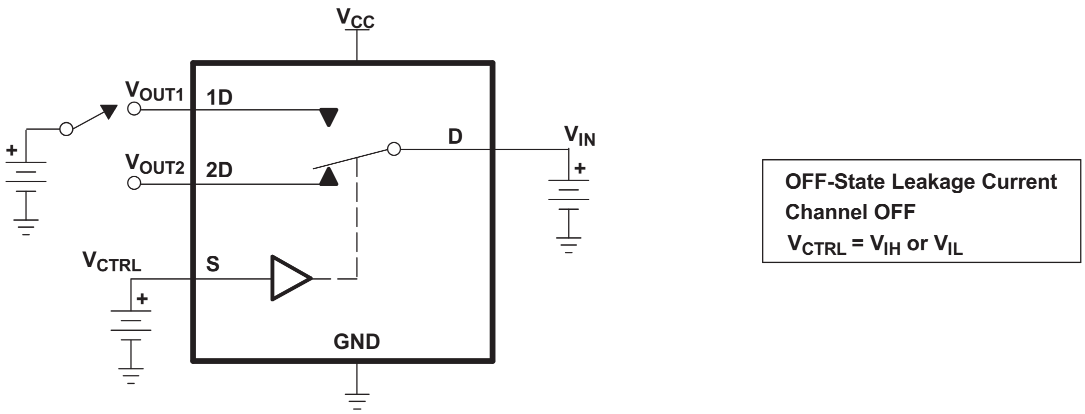


Figure 13. OFF-State Leakage Current

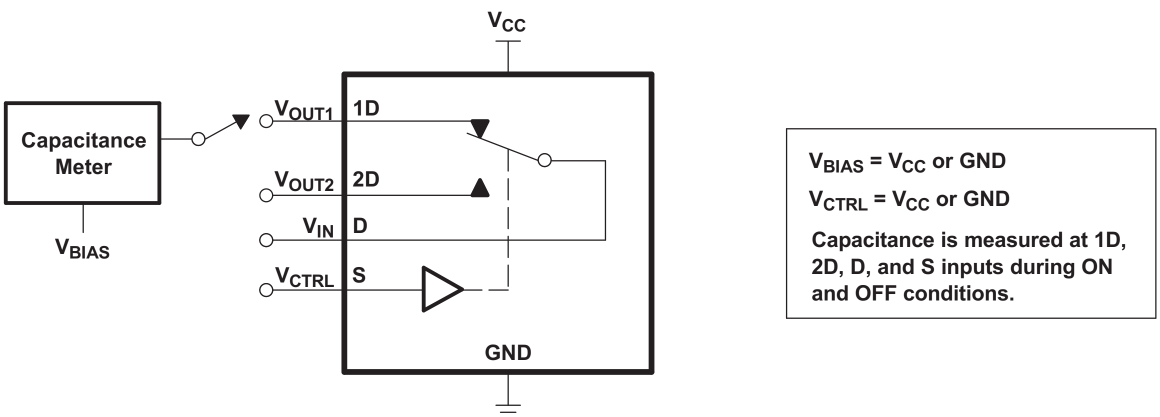


Figure 14. Capacitance

8 Detailed Description

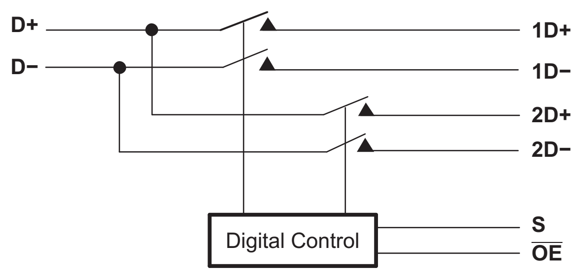
8.1 Overview

The TS3USB221 device is a 2-channel SPDT switch specially designed for the switching of high-speed USB 2.0 signals in handset and consumer applications, such as cell phones, digital cameras, and notebooks with hubs or controllers with limited USB I/Os. The wide bandwidth (1.1 GHz) of this switch allows signals to pass with minimum edge and phase distortion. The device multiplexes differential outputs from a USB host device to one of two corresponding outputs. The switch is bidirectional and offers little or no attenuation of the high-speed signals at the outputs. The device also has a low power mode that reduces the power consumption to 1 μA for portable applications with a battery or limited power budget.

The device is designed for low bit-to-bit skew and high channel-to-channel noise isolation, and is compatible with various standards, such as high-speed USB 2.0 (480 Mbps).

The TS3USB221 device integrates ESD protection cells on all pins, is available in a tiny μQFN package (2 mm × 1.5 mm) and is characterized over the free-air temperature range from –40°C to 85°C.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Low Power Mode

The TS3USB221 has a low power mode that reduces the power consumption to 1 μA when the device is not in use. The bus-switch enable pin $\overline{OE}$ must be supplied with a logic high signal to put the device in low power mode and disable the switch.

8.4 Device Functional Modes

Table 1. Truth Table

S	$\overline{OE}$	FUNCTION
X	H	Disconnect
L	L	D = 1D
H	L	D = 2D

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

There are many USB applications in which the USB hubs or controllers have a limited number of USB I/Os. The TS3USB221 solution can effectively expand the limited USB I/Os by switching between multiple USB buses in order to interface them to a single USB hub or controller. TS3USB221 can also be used to connect a single controller to two USB connectors.

9.2 Typical Application

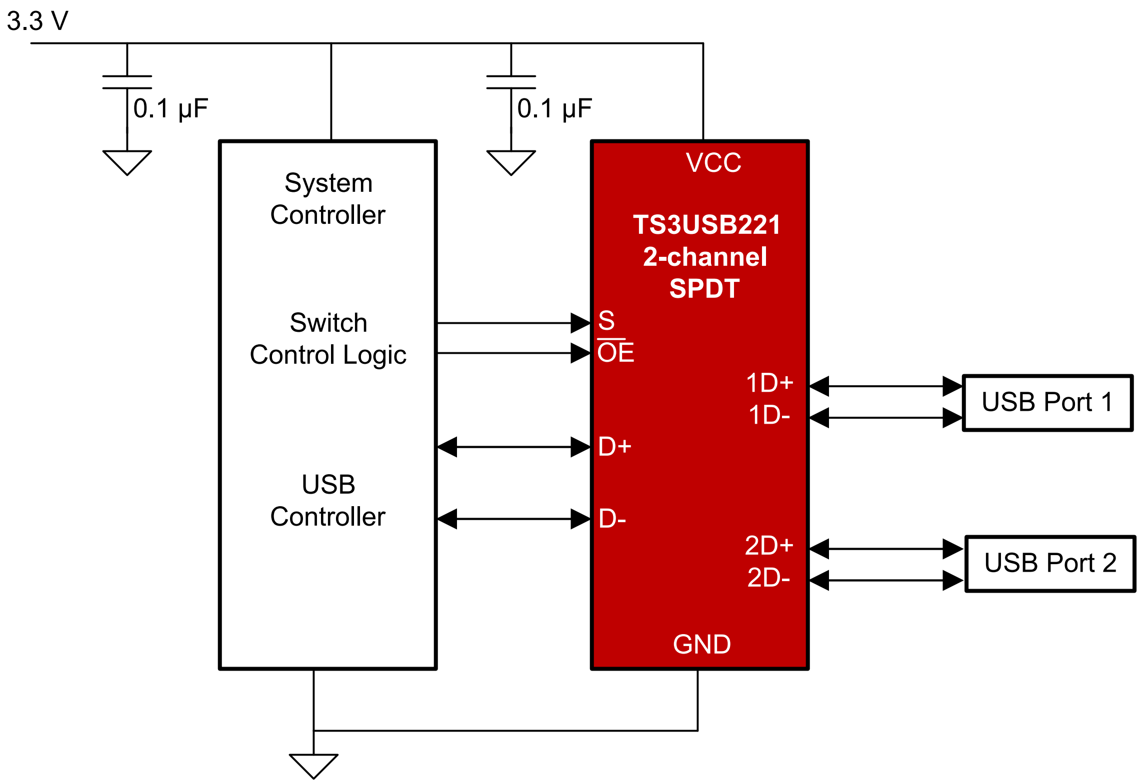


Figure 15. Simplified Schematic

9.2.1 Design Requirements

Design requirements of the USB 1.0, 1.1, and 2.0 standards should be followed.

TI recommends that the digital control pins S and $\overline{OE}$ be pulled up to V_{CC} or down to GND to avoid undesired switch positions that could result from the floating pin.

9.2.2 Detailed Design Procedure

The TS3USB221 may be properly operated without any external components. However, it is recommended that unused pins be connected to ground through a 50-Ω resistor to prevent signal reflections back into the device.

Typical Application (continued)

9.2.3 Application Curves

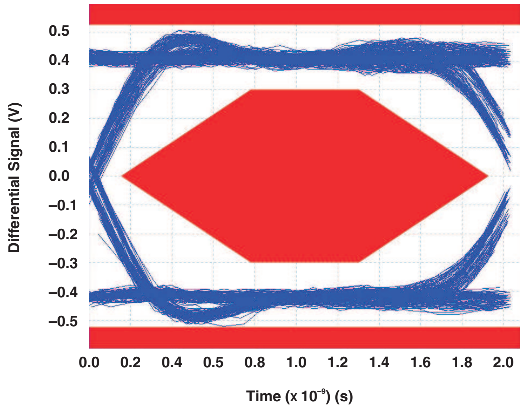


Figure 16. Eye Pattern: 480-Mbps USB Signal With No Switch (Through Path)

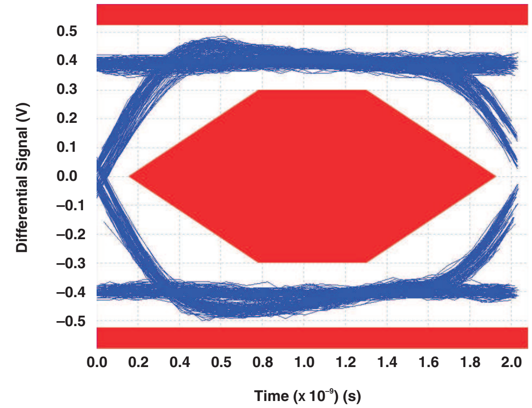


Figure 17. Eye Pattern: 480-Mbps USB Signal With Switch NC Path

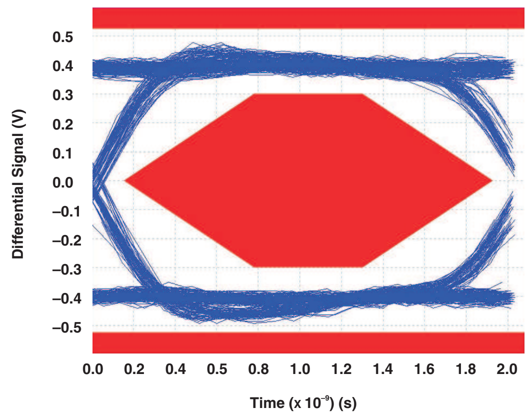


Figure 18. Eye Pattern: 480-Mbps USB Signal With Switch NO Path

10 Power Supply Recommendations

Power to the device is supplied through the V_{CC} pin and should follow the USB 1.0, 1.1, and 2.0 standards. TI recommends placing a bypass capacitor as close as possible to the supply pin V_{CC} to help smooth out lower frequency noise to provide better load regulation across the frequency spectrum.

11 Layout

11.1 Layout Guidelines

Place supply bypass capacitors as close to V_{CC} pin as possible. Avoid placing the bypass caps near the D+/D– traces.

The high-speed D+/D– traces should always be matched lengths and must be no more than 4 inches, otherwise the eye diagram performance may be degraded. A high-speed USB connection is made through a shielded, twisted pair cable with a differential characteristic impedance. In the layout, the impedance of D+ and D– traces should match the cable characteristic differential impedance for optimal performance.

Route the high-speed USB signals using a minimum of vias and corners which will reduce signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points on twisted pair lines; through-hole pins are not recommended.

When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal traces by minimizing impedance discontinuities.

Do not route USB traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or IC's that use or duplicate clock signals.

Avoid stubs on the high-speed USB signals because they cause signal reflections. If a stub is unavoidable, then the stub should be less than 200 mm.

Route all high-speed USB signal traces over continuous planes (V_{CC} or GND), with no interruptions.

Avoid crossing over anti-etch, commonly found with plane splits.

A printed circuit board with at least four layers is recommended because of high frequencies associated with the USB; two signal layers separated by a ground and power layer as shown in Figure 19.

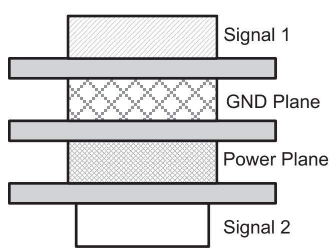


Figure 19. Four-Layer Board Stack-Up

The majority of signal traces should run on a single layer, preferably Signal 1. Immediately next to this layer should be the GND plane, which is solid with no cuts. Avoid running signal traces across a split in the ground or power plane. When running across split planes is unavoidable, sufficient decoupling must be used. Minimizing the number of signal vias reduces EMI by reducing inductance at high frequencies. For more information on layout guidelines, see *High Speed Layout Guidelines* (SCAA082) and *USB 2.0 Board Design and Layout Guidelines* (SPRAAR7).

11.2 Layout Example

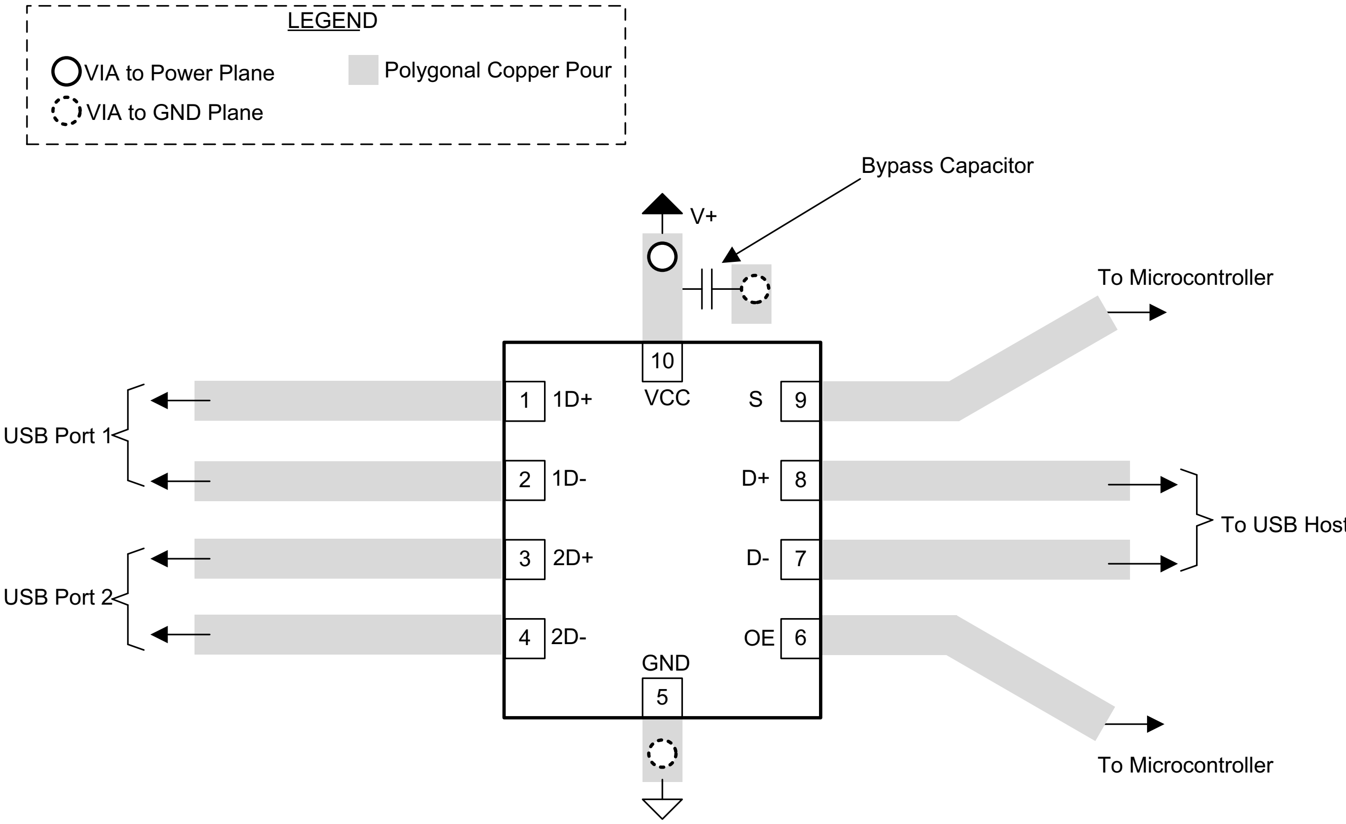


Figure 20. Package Layout Diagram

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- *High Speed Layout Guidelines*, SCAA082
- *USB 2.0 Board Design and Layout Guidelines*, SPRAAR7

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
MIPI is a trademark of Mobile Industry Processor Interface Alliance.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN080104RSER	ACTIVE	UQFN	RSE	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(L57, L5O, L5R, L5 V)	Samples
TS3USB221DRCR	ACTIVE	VSON	DRC	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZWG	Samples
TS3USB221DRCRG4	ACTIVE	VSON	DRC	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZWG	Samples
TS3USB221RSER	ACTIVE	UQFN	RSE	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(L57, L5O, L5R, L5 V)	Samples
TS3USB221RSERG4	ACTIVE	UQFN	RSE	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(L57, L5O, L5R, L5 V)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

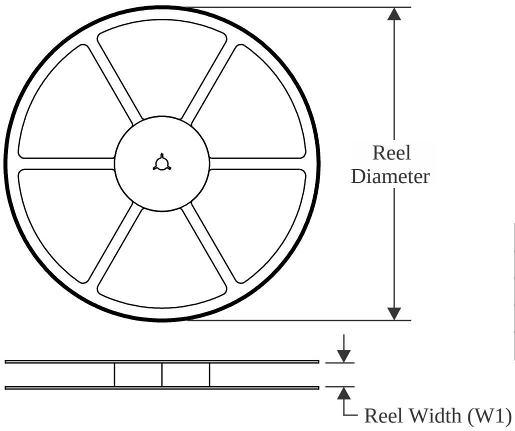
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

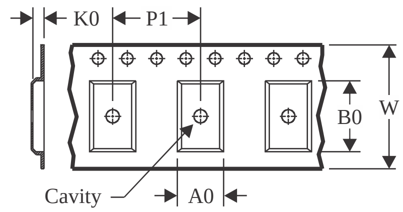
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

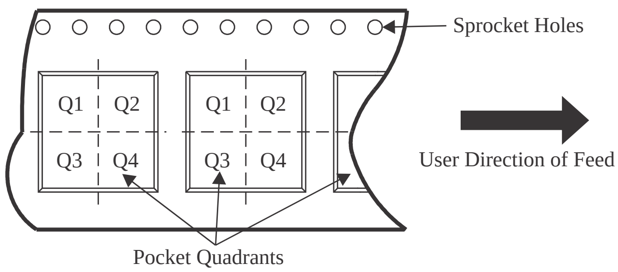


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

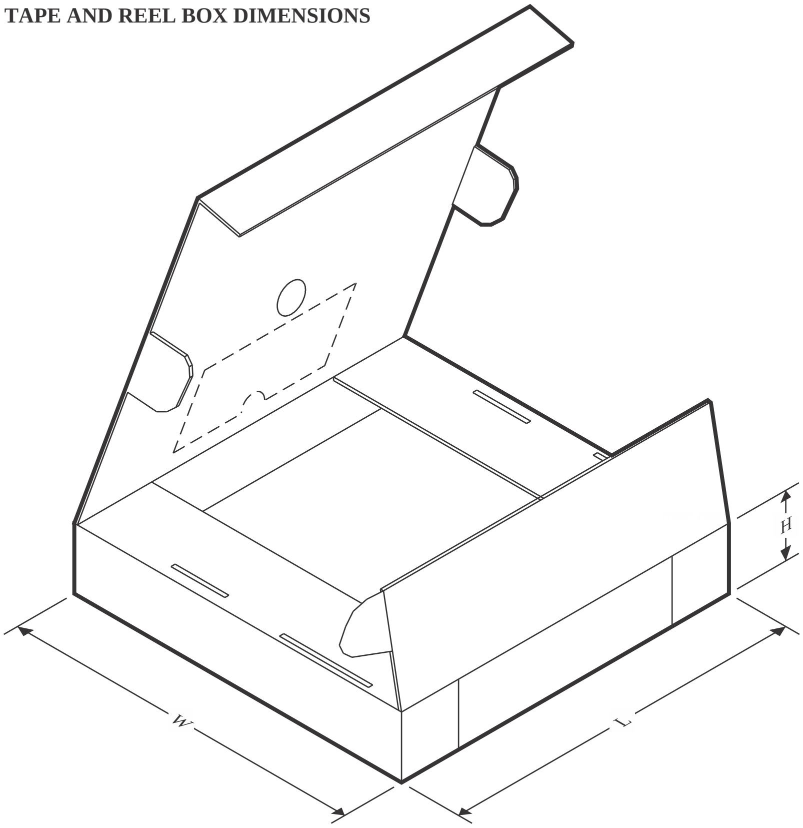
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

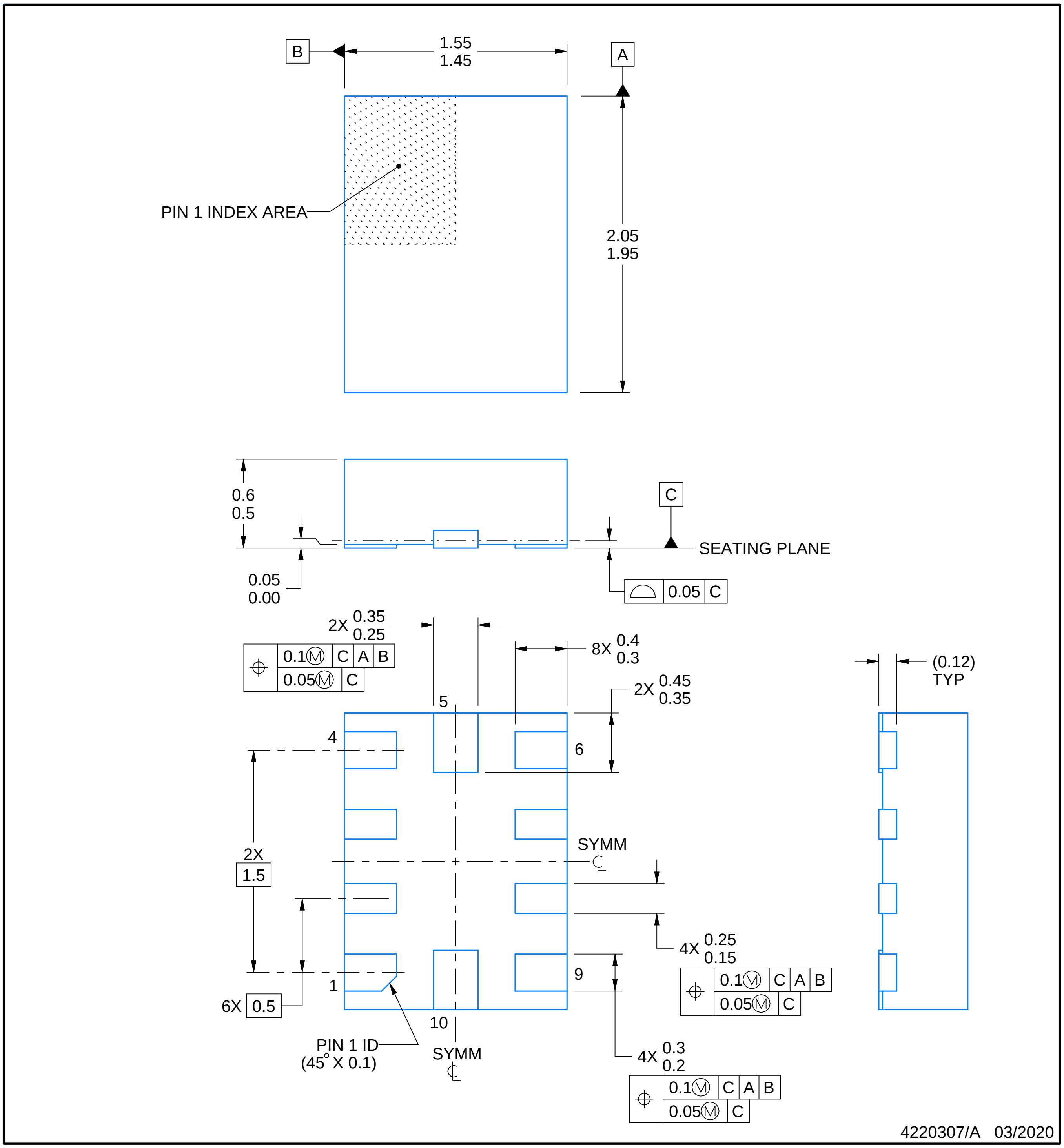
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3USB221DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TS3USB221RSER	UQFN	RSE	10	3000	180.0	9.5	1.7	2.2	0.75	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



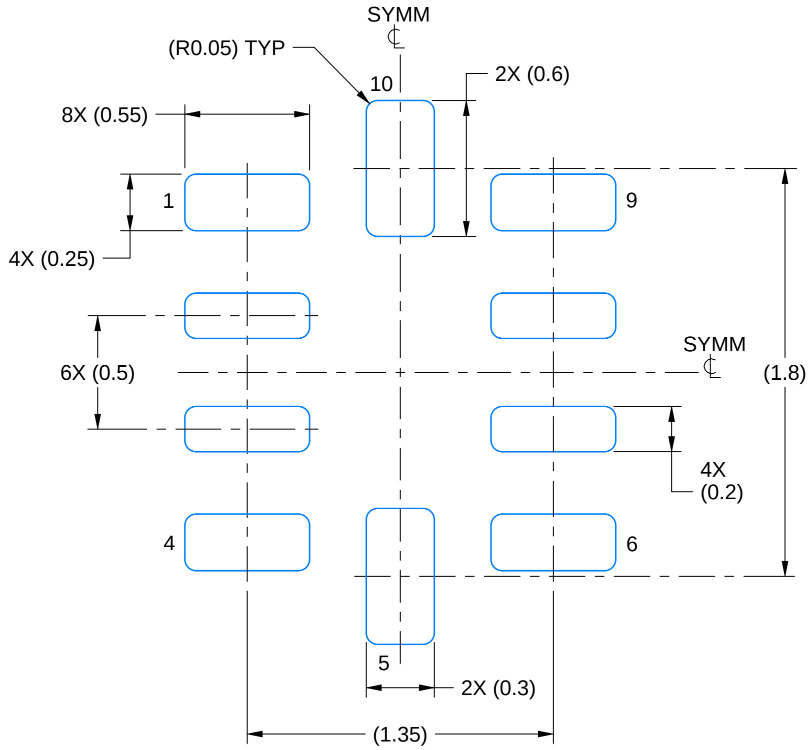
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3USB221DRCR	VSON	DRC	10	3000	356.0	356.0	35.0
TS3USB221RSER	UQFN	RSE	10	3000	189.0	185.0	36.0

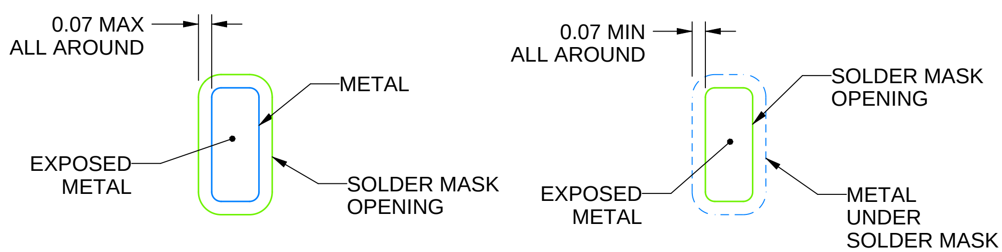


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X



NON SOLDER MASK
DEFINED
(PREFERRED)

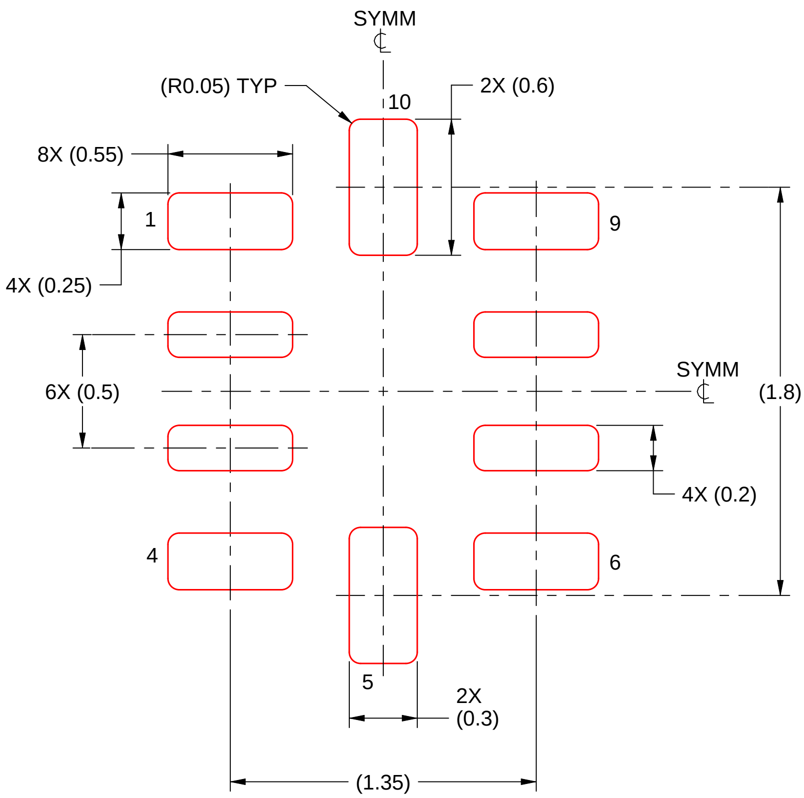
SOLDER MASK
DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

4220307/A 03/2020

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



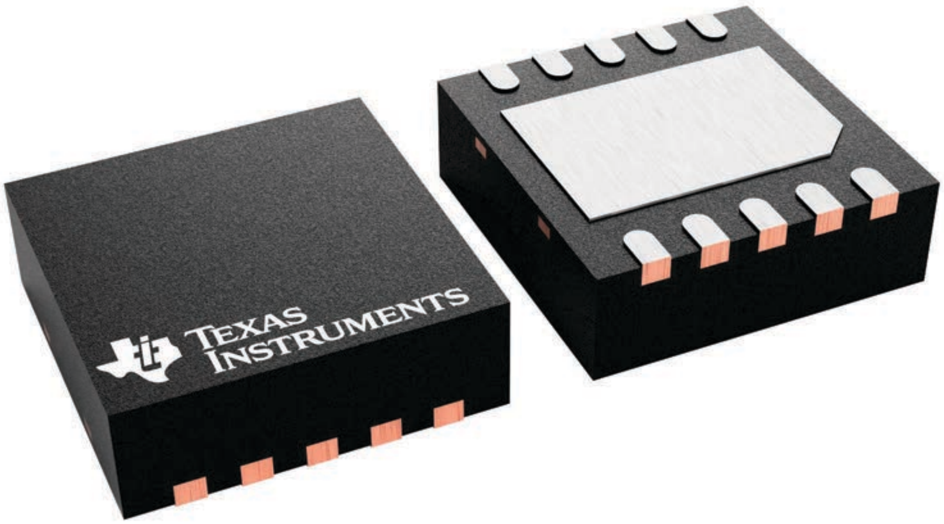
SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICKNESS
SCALE: 30X

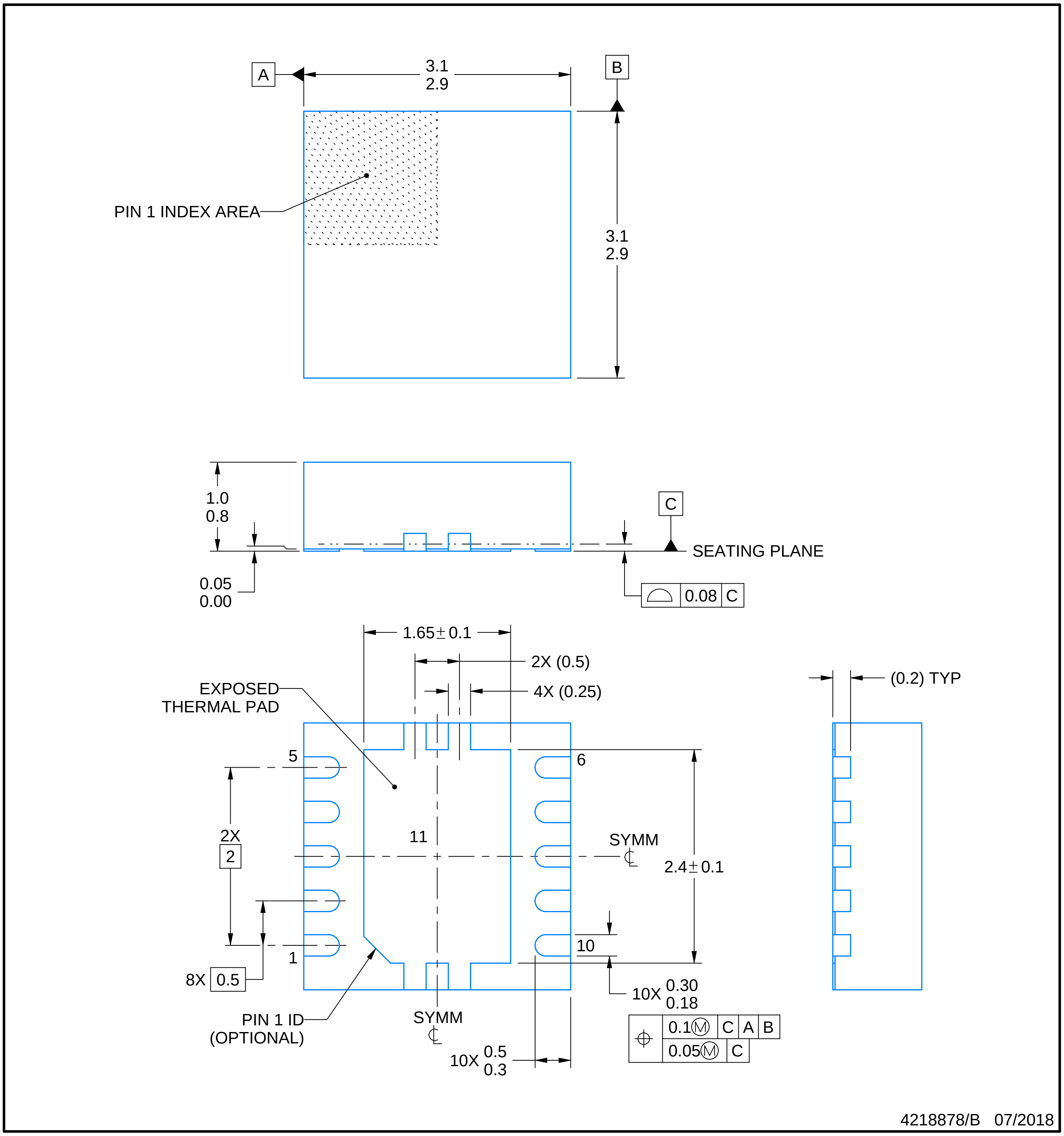
4220307/A 03/2020

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

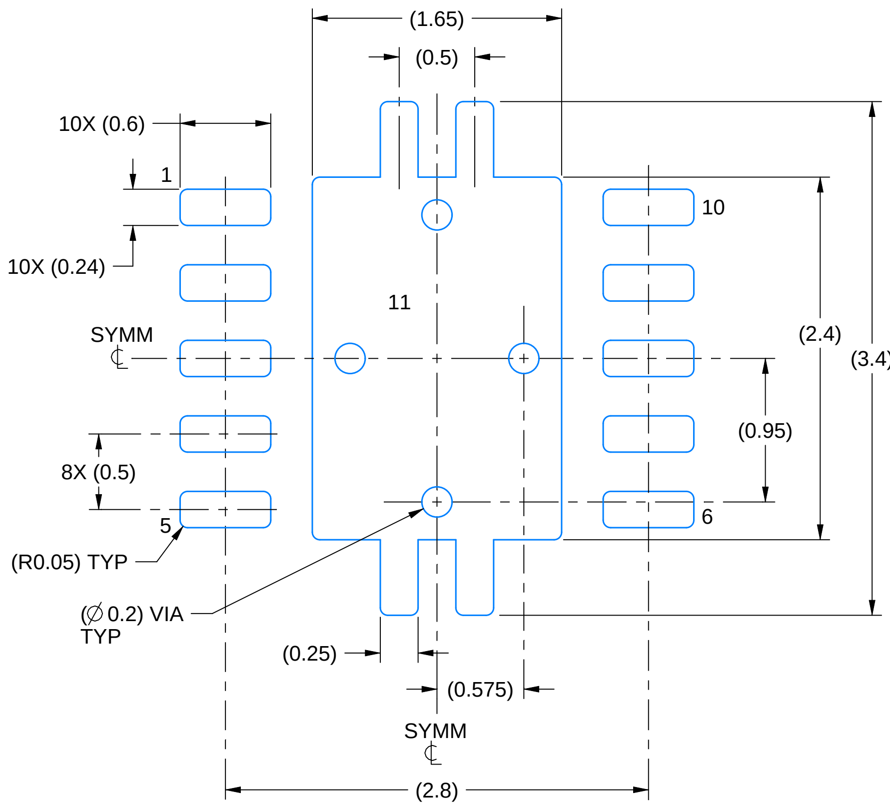
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



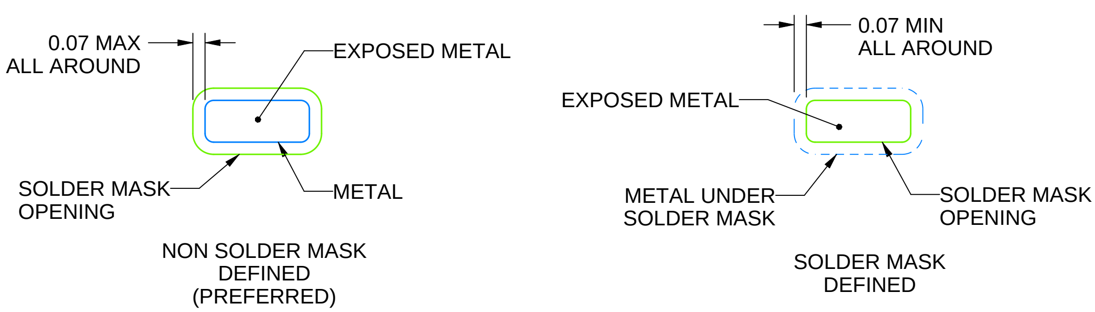


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

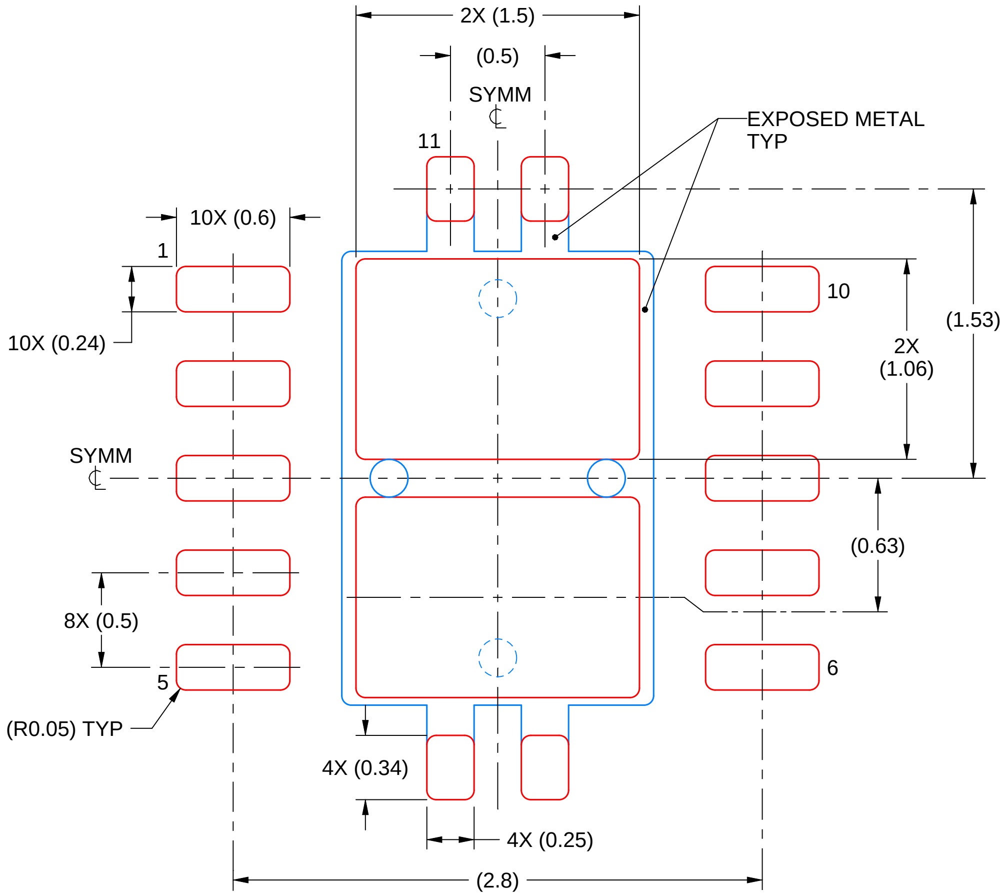


SOLDER MASK DETAILS

4218878/B 07/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218878/B 07/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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