ISO7731B High-Speed, Basic Insulation Triple-Channel Digital Isolator

1 Features

- 100 Mbps Data Rate
- Robust Isolation Barrier:
  - >100-Year Projected Lifetime at 1 kV_{RMS} Working Voltage
  - Up to 5000 V_{RMS} Isolation Rating
  - ±100 kV/µs Typical CMTI
- Wide Supply Range: 2.25 V to 5.5 V
- 2.25-V to 5.5-V Level Translation
- Default Output *High* (ISO7731B) and *Low* (ISO7731FB) Options
- Wide Temperature Range: –55°C to +125°C
- Low Power Consumption, Typical 1.7 mA per Channel at 1 Mbps
- Low Propagation Delay: 11 ns Typical (5-V Supplies)
- Robust Electromagnetic Compatibility (EMC)
  - System-Level ESD, EFT, and Surge Immunity
  - ±8 kV IEC 61000-4-2 Contact Discharge Protection across Isolation Barrier
  - Low Emissions
- Wide-SOIC (DW-16) Package
- Safety-Related Certifications:
  - Basic Insulation per DIN V VDE V 0884-11:2017-01
  - UL 1577 Component Recognition Program
  - CSA Certification per IEC 60950-1 and IEC 62368-1 End Equipment Standards
  - CQC Certification per GB4943.1-2011
  - TUV Certification according to EN 60950-1 and EN 61010-1
  - CQC Certification Planned; All Other Certifications Complete

2 Applications

- Industrial Automation
- Motor Control
- Power Supplies
- Solar Inverters
- Medical Equipment

3 Description

The ISO7731B device is a high-performance, triple-channel digital isolator with 5000 V_{RMS} isolation ratings per UL 1577 and 8000 V_{PK} basic insulation according to VDE.

The ISO7731B device provides high electromagnetic immunity and low emissions at low power consumption, while isolating CMOS or LVCMOS digital I/Os. Each isolation channel has a logic input and output buffer separated by a double capacitive silicon dioxide (SiO_2) insulation barrier. This device comes with enable pins which can be used to put the respective outputs in high impedance for multi-master driving applications and to reduce power consumption. The ISO7731B device has two forward and one reverse-direction channels. If the input power or signal is lost, the default output is *high* for device without suffix F and *low* for device with suffix F. See the *Device Functional Modes* section for further details.

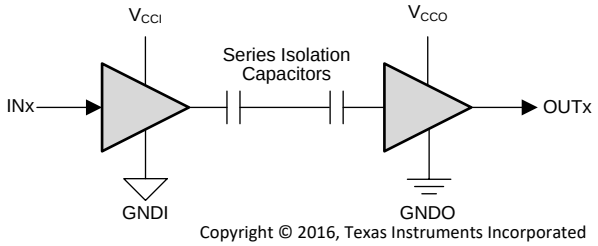
Used in conjunction with isolated power supplies, this device helps prevent noise currents on data buses, such as RS-485, RS-232, and CAN, or other circuits from entering the local ground and interfering with or damaging sensitive circuitry. Through innovative chip design and layout techniques, electromagnetic compatibility of the ISO7731B device has been significantly enhanced to ease system-level ESD, EFT, surge, and emissions compliance. The ISO7731B device is available in 16-pin wide-SOIC package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ISO7731B	SOIC (16)	10.30 mm × 7.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



V_{CCI}=Input V_{CC}, V_{CCO}=Output V_{CC}

GNDI=Input ground, GNDO=Output ground

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4 Revision History

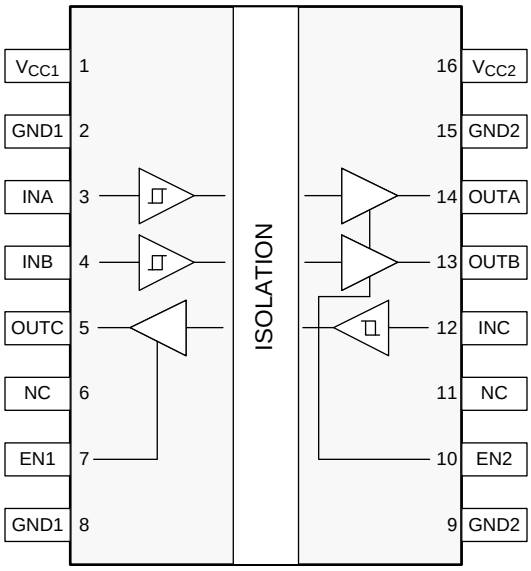
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (April 2018) to Revision A **Page**

- Made editorial and cosmetic changes throughout the document ... 1
- Changed From: "Isolation Barrier Life: >40 Years" To:">100-Year Projected Lifetime at 1 kV_{RMS} Working Voltage" in Features ... 1
- Added "Up to 5000 V_{RMS} Isolation Rating" in Features ... 1
- Added "±8 kV IEC 61000-4-2 Contact Discharge Protection across Isolation Barrier" in Features ... 1
- Changed From: "All Certifications are Planned" To: "CQC Certification Planned; All Other Certifications Complete" in Features ... 1
- Changed Simplified Schematic to show two isolation capacitors in series instead of a single capacitor ... 1
- Added "Contact discharge per IEC 61000-4-2" specification of ±8000 V in ESD Ratings table ... 4
- Added table note to *Data rate* specification in Recommended Operating Conditions table ... 4
- Updated certification information in Safety-Related Certifications table ... 7
- Deleted "EN" from Figure 12 ... 15
- Updated Figure 15 by fixing ground symbols of "Input (Devices with F suffix)" schematic ... 19
- Added "*How to use isolation to improve ESD, EFT and Surge immunity in industrial systems*" application report in Related Documentation section ... 24

5 Pin Configuration and Functions

ISO7731B DW Package
16-Pin SOIC
Top View



Pin Functions

PIN NAME	PIN NO.	I/O	DESCRIPTION
EN1	7	I	Output enable 1. Output pins on side 1 are enabled when EN1 is high or open and in high-impedance state when EN1 is low.
EN2	10	I	Output enable 2. Output pins on side 2 are enabled when EN2 is high or open and in high-impedance state when EN2 is low.
GND1	2, 8	—	Ground connection for V_{CC1}
GND2	9, 15	—	Ground connection for V_{CC2}
INA	3	I	Input, channel A
INB	4	I	Input, channel B
INC	12	I	Input, channel C
NC	6, 11	—	Not connected
OUTA	14	O	Output, channel A
OUTB	13	O	Output, channel B
OUTC	5	O	Output, channel C
V_{CC1}	1	—	Power supply, V_{CC1}
V_{CC2}	16	—	Power supply, V_{CC2}

6 Specifications

6.1 Absolute Maximum Ratings

See (1)

		MIN	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage(2)	–0.5	6	V
V	Voltage at INx, OUTx, ENx	–0.5	V_{CCX} + 0.5(3)	V
I_O	Output current	–15	15	mA
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values.
(3) Maximum voltage must not exceed 6 V.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±6000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	
		Contact discharge per IEC 61000-4-2; Isolation barrier withstand test(3)(4)	±8000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(3) IEC ESD strike is applied across the barrier with all pins on each side tied together creating a two-terminal device.
(4) Testing is carried out in air or oil to determine the intrinsic contact discharge capability of the device.

6.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage		2.25		5.5	V
$V_{CC(UVLO+)}$	UVLO threshold when supply voltage is rising			2	2.25	V
$V_{CC(UVLO–)}$	UVLO threshold when supply voltage is falling		1.7	1.8		V
$V_{HYS(UVLO)}$	Supply voltage UVLO hysteresis		100	200		mV
I_{OH}	High-level output current	V_{CCO}(1) = 5 V	–4			mA
		V_{CCO} = 3.3 V	–2			
		V_{CCO} = 2.5 V	–1			
I_{OL}	Low-level output current	V_{CCO} = 5 V			4	mA
		V_{CCO} = 3.3 V			2	
		V_{CCO} = 2.5 V			1	
V_{IH}	High-level input voltage		0.7 × V_{CCI}(1)		V_{CCI}	V
V_{IL}	Low-level input voltage		0		0.3 × V_{CCI}	V
DR(2)	Data rate		0		100	Mbps
T_A	Ambient temperature		–55	25	125	°C

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}.
(2) 100 Mbps is the maximum specified data rate, although higher data rates are possible.

6.4 Thermal Information

THERMAL METRIC[1]		ISO7731B DW (SOIC) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	81.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	44.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	45.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	28.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	45.5	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case(bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation	$V_{CC1} = V_{CC2} = 5.5$ V, $T_J = 150$°C, $C_L = 15$ pF, input a 50-MHz 50% duty cycle square wave			150	mW
P_{D1}	Maximum power dissipation by side-1	$V_{CC1} = V_{CC2} = 5.5$ V, $T_J = 150$°C, $C_L = 15$ pF, input a 50-MHz 50% duty cycle square wave			50	mW
P_{D2}	Maximum power dissipation by side-2	$V_{CC1} = V_{CC2} = 5.5$ V, $T_J = 150$°C, $C_L = 15$ pF, input a 50-MHz 50% duty cycle square wave			100	mW

6.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
CLR	External clearance (1)	Shortest terminal-to-terminal distance through air	>8	mm
CPG	External creepage (1)	Shortest terminal-to-terminal distance across the package surface	>8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>21	μm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	>600	V
	Material group		I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 150 V_{RMS}	I–IV	
		Rated mains voltage ≤ 300 V_{RMS}	I–IV	
		Rated mains voltage ≤ 600 V_{RMS}	I–IV	
		Rated mains voltage ≤ 1000 V_{RMS}	I–III	
DIN V VDE V 0884-11:2017-01 (2)				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1414	V_{PK}
V_{IOWM}	Maximum working isolation voltage	AC voltage (sine wave); time dependent dielectric breakdown (TDDB) test	1000	V_{RMS}
		DC voltage	1414	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$ = 8000 V_{PK}, t = 60 s (qualification); V_{TEST} = 1.2 × V_{IOTM}= 9600 V_{PK}, t = 1 s (100% production)	8000	V_{PK}
V_{IOSM}	Maximum surge isolation voltage (3)	Test method per IEC 62368-1, 1.2/50 μs waveform, V_{TEST} = 1.3 × V_{IOSM} = 7800 V_{PK} (qualification)	6000	V_{PK}
q_{pd}	Apparent charge (4)	Method a, After I/O safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)}$ = 1.2 × V_{IORM} = 1697 V_{PK}, t_m = 10 s	≤5	pC
		Method a, After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)}$ = 1.2 × V_{IORM} = 1697 V_{PK}, t_m = 10 s	≤5	
		Method b1; At routine test (100% production) and preconditioning (type test) V_{ini} = 1.2 × V_{IOTM}= 9600 V_{PK}, t_{ini} = 1 s; $V_{pd(m)}$ = 1.5 × V_{IORM} = 2121 V_{PK}, t_m = 1 s	≤5	
C_{IO}	Barrier capacitance, input to output (5)	V_{IO} = 0.4 sin (2πft), f = 1 MHz	~0.7	pF
R_{IO}	Isolation resistance (5)	V_{IO} = 500 V, T_A = 25°C	$>10^{12}$	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	$>10^{11}$	
		V_{IO} = 500 V at T_S = 150°C	$>10^{9}$	
	Pollution degree		2	
	Climatic category		55/125/21	
UL 1577				
V_{ISO}	Withstanding isolation voltage	$V_{TEST} = V_{ISO}$ = 5000 V_{RMS} , t = 60 s (qualification), V_{TEST} = 1.2 × V_{ISO} = 6000 V_{RMS}, t = 1 s (100% production)	5000	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.
(2) This coupler is suitable for *basic electrical insulation* only within the maximum operating ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier tied together creating a two-terminal device.

6.7 Safety-Related Certifications

VDE	CSA	UL	CQC	TUV
Certified according to DIN V VDE V 0884-11:2017-01 and DIN EN 61010-1 (VDE 0411-1):2011-07	Certified according to IEC 60950-1 and IEC 62368-1	Recognized under UL 1577 Component Recognition Program	Plan to certify according to GB 4943.1-2011	Certified according to EN 61010-1:2010 (3rd Ed) and EN 60950-1:2006/A2:2013
Basic Insulation; Maximum transient isolation voltage, 8000 V_{PK}; Maximum repetitive peak isolation voltage, 1414 V_{PK}; Maximum surge isolation voltage, 6000 V_{PK}	Basic Insulation; 800 V_{RMS} working voltage per CSA 60950-1-07+A1+A2, IEC 60950-1 2nd Ed. +A1+A2, CSA 62368-1-14 and IEC 62368-1:2014	Single protection, 5000 V_{RMS}	700 V_{RMS} maximum working voltage, Altitude ≤ 5000 m, Tropical Climate	5000 V_{RMS} insulation per EN 61010-1:2010 (3rd Ed) up to working voltage of 600 V_{RMS} 5000 V_{RMS} insulation per EN 60950-1:2006/A2:2013 up to working voltage of 800 V_{RMS}
Certificate number: 40047657	Master contract number: 220991	File number: E181974	Certification planned	Client ID number: 77311

6.8 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current(1)	$R_{\theta JA}$ = 81.4 °C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C, see Figure 1			279	mA
		$R_{\theta JA}$ = 81.4 °C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C, see Figure 1			427	
		$R_{\theta JA}$ = 81.4 °C/W, V_I = 2.75 V, T_J = 150°C, T_A = 25°C, see Figure 1			558	
P_S	Safety input, output, or total power(1)	$R_{\theta JA}$ = 81.4 °C/W, T_J = 150°C, T_A = 25°C, see Figure 2			1536	mW
T_S	Maximum safety temperature(1)				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A.

The junction-to-air thermal resistance, $R_{\theta JA}$, in the *Thermal Information* table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:

$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.

$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature.

$P_S = I_S \times V_I$, where V_I is the maximum input voltage.

6.9 Electrical Characteristics—5-V Supply

V_{CC1} = V_{CC2} = 5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 9	V_{CCO} (1) – 0.4	4.8		V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 9		0.2	0.4	V
$V_{IT+(IN)}$	Rising input voltage threshold			0.6 × V_{CCI}	0.7 × V_{CCI}	V
$V_{IT-(IN)}$	Falling input voltage threshold		0.3 × V_{CCI}	0.4 × V_{CCI}		V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 × V_{CCI}	0.2 × V_{CCI}		V
I_{IH}	High-level input current	V_{IH} = V_{CCI} (1) at INx or ENx			10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx or ENx	–10			µA
$\|CM_H\|$	High-level common-mode transient immunity	V_I = V_{CCI} (2), V_{CM} = 1200 V; see Figure 12	85	100		kV/µs
$\|CM_L\|$	Low-level common-mode transient immunity	V_I = 0 V, V_{CM} = 1200 V; see Figure 12	85	100		kV/µs
C_I	Input Capacitance	V_I = V_{CC} (2) / 2 + 0.4 × sin(2πft), f = 1 MHz, V_{CC} = 5 V		2		pF

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}.
(2) Measured from input pin to ground.

6.10 Supply Current Characteristics—5-V Supply

V_{CC1} = V_{CC2} = 5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
Supply current - disable	EN1 = EN2 = 0 V; V_I = V_{CCI} (1) (ISO7731B); V_I = 0 V (ISO7731B with F suffix)		I_{CC1}		0.8	1.2	mA
			I_{CC2}		0.7	1	mA
	EN1 = EN2 = 0 V; V_I = 0 V (ISO7731B); V_I = V_{CCI} (ISO7731B with F suffix)		I_{CC1}		3	4.3	mA
			I_{CC2}		1.8	2.6	mA
Supply current - DC signal	EN1 = EN2 = V_{CCI}; V_I = V_{CCI} (ISO7731B); V_I = 0 V (ISO7731B with F suffix)		I_{CC1}		1.3	1.7	mA
			I_{CC2}		1.6	2.2	mA
	EN1 = EN2 = V_{CCI}; V_I = 0 V (ISO7731B); V_I = V_{CCI} (ISO7731B with F suffix)		I_{CC1}		3.5	5	mA
			I_{CC2}		2.8	4.1	mA
Supply current - AC signal	EN1 = EN2 = V_{CCI}; All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		2.7	3.4	mA
			I_{CC2}		2.3	3.3	mA
		10 Mbps	I_{CC1}		3	4	mA
			I_{CC2}		3.3	4.4	mA
		100 Mbps	I_{CC1}		8.5	11	mA
			I_{CC2}		13.1	16	mA

(1) V_{CCI} = Input-side V_{CC}

6.11 Electrical Characteristics—3.3-V Supply

V_{CC1} = V_{CC2} = 3.3 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –2 mA; see Figure 9	V_{CCO}(1) – 0.3	3.2		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA; see Figure 9		0.1	0.3	V
$V_{IT+(IN)}$	Rising input voltage threshold			0.6 × V_{CCI}	0.7 × V_{CCI}	V
$V_{IT-(IN)}$	Falling input voltage threshold		0.3 × V_{CCI}	0.4 × V_{CCI}		V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 × V_{CCI}	0.2 × V_{CCI}		V
I_{IH}	High-level input current	V_{IH} = V_{CCI}(1) at INx or ENx			10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx or ENx	–10			µA
$\|CM_H\|$	High-level common-mode transient immunity	V_I = V_{CCI}(1), V_{CM} = 1200 V; see Figure 12	85	100		kV/µs
$\|CM_L\|$	Low-level common-mode transient immunity	V_I = 0 V, V_{CM} = 1200 V; see Figure 12	85	100		kV/µs

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}.

6.12 Supply Current Characteristics—3.3-V Supply

V_{CC1} = V_{CC2} = 3.3 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
Supply current - disable	EN1 = EN2 = 0 V; V_I = V_{CCI}(1) (ISO7731B); V_I = 0 V (ISO7731B with F suffix)		I_{CC1}		0.8	1.2	mA
			I_{CC2}		0.7	1	mA
	EN1 = EN2 = 0 V; V_I = 0 V (ISO7731B); V_I = V_{CCI} (ISO7731B with F suffix)		I_{CC1}		3	4.3	mA
			I_{CC2}		1.8	2.6	mA
Supply current - DC signal	EN1 = EN2 = V_{CCI}; V_I = V_{CCI} (ISO7731B); V_I = 0 V (ISO7731B with F suffix)		I_{CC1}		1.3	1.7	mA
			I_{CC2}		1.6	2.2	mA
	EN1 = EN2 = V_{CCI}; V_I = 0 V (ISO7731B); V_I = V_{CCI} (ISO7731B with F suffix)		I_{CC1}		3.5	5	mA
			I_{CC2}		2.8	4.1	mA
Supply current - AC signal	EN1 = EN2 = V_{CCI}; All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		2.4	3.4	mA
			I_{CC2}		2.2	3.3	mA
		10 Mbps	I_{CC1}		2.8	3.8	mA
			I_{CC2}		2.9	4	mA
		100 Mbps	I_{CC1}		6.7	8.5	mA
			I_{CC2}		10	12.5	mA

(1) V_{CCI} = Input-side V_{CC}

6.13 Electrical Characteristics—2.5-V Supply

V_{CC1} = V_{CC2} = 2.5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –1 mA; see Figure 9	V_{CCO}(1) – 0.2	2.45		V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA; see Figure 9		0.05	0.2	V
$V_{IT+(IN)}$	Rising input voltage threshold			0.6 × V_{CCI}	0.7 × V_{CCI}	V
$V_{IT-(IN)}$	Falling input voltage threshold		0.3 × V_{CCI}	0.4 × V_{CCI}		V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 × V_{CCI}	0.2 × V_{CCI}		V
I_{IH}	High-level input current	V_{IH} = V_{CCI}(1) at INx or ENx			10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx or ENx	–10			µA
$\|CM_H\|$	High-level common-mode transient immunity	V_I = V_{CCI}(1), V_{CM} = 1200 V; see Figure 12	85	100		kV/µs
$\|CM_L\|$	Low-level common-mode transient immunity	V_I = 0 V, V_{CM} = 1200 V; see Figure 12	85	100		kV/µs

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}.

6.14 Supply Current Characteristics—2.5-V Supply

V_{CC1} = V_{CC2} = 2.5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
Supply current - disable	EN1 = EN2 = 0 V; V_I = V_{CCI}(1) (ISO7731B); V_I = 0 V (ISO7731B with F suffix)		I_{CC1}		0.8	1.2	mA
			I_{CC2}		0.7	1	mA
	EN1 = EN2 = 0 V; V_I = 0 V (ISO7731B); V_I = V_{CCI} (ISO7731B with F suffix)		I_{CC1}		3	4.3	mA
			I_{CC2}		1.8	2.6	mA
Supply current - DC signal	EN1 = EN2 = V_{CCI}; V_I = V_{CCI} (ISO7731B); V_I = 0 V (ISO7731B with F suffix)		I_{CC1}		1.3	1.7	mA
			I_{CC2}		1.6	2.2	mA
	EN1 = EN2 = V_{CCI}; V_I = 0 V (ISO7731B); V_I = V_{CCI} (ISO7731B with F suffix)		I_{CC1}		3.5	5	mA
			I_{CC2}		2.8	4.1	mA
Supply current - AC signal	EN1 = EN2 = V_{CCI}; All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		2.4	3.4	mA
			I_{CC2}		2.2	3.2	mA
		10 Mbps	I_{CC1}		2.7	3.7	mA
			I_{CC2}		2.7	3.8	mA
		100 Mbps	I_{CC1}		5.6	7	mA
			I_{CC2}		8	10	mA

(1) V_{CCI} = Input-side V_{CC}

6.15 Switching Characteristics—5-V Supply

V_{CC1} = V_{CC2} = 5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 9	6	11	16	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$			0.6	4.9	ns
$t_{sk(o)}$	Channel-to-channel output skew time(2)	Same-direction channels			4	ns
$t_{sk(pp)}$	Part-to-part skew time(3)				4.5	ns
t_r	Output signal rise time	See Figure 9		1.3	3.9	ns
t_f	Output signal fall time			1.4	3.9	ns
t_{PHZ}	Disable propagation delay, high-to-high impedance output	See Figure 10		8	20	ns
t_{PLZ}	Disable propagation delay, low-to-high impedance output			8	20	ns
t_{PZH}	Enable propagation delay, high impedance-to-high output for ISO7731B			7	20	ns
	Enable propagation delay, high impedance-to-high output for ISO7731B with F suffix			3	8.5	µs
t_{PZL}	Enable propagation delay, high impedance-to-low output for ISO7731B			3	8.5	µs
	Enable propagation delay, high impedance-to-low output for ISO7731B with F suffix			7	20	ns
t_{DO}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7 V. See Figure 11		0.1	0.3	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 100 Mbps		0.6		ns

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.16 Switching Characteristics—3.3-V Supply

V_{CC1} = V_{CC2} = 3.3 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 9	6	11	16	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$			0.1	5	ns
$t_{sk(o)}$	Channel-to-channel output skew time(2)	Same-direction channels			4.1	ns
$t_{sk(pp)}$	Part-to-part skew time(3)				4.5	ns
t_r	Output signal rise time	See Figure 9		1.3	3	ns
t_f	Output signal fall time			1.3	3	ns
t_{PHZ}	Disable propagation delay, high-to-high impedance output	See Figure 10		17	30	ns
t_{PLZ}	Disable propagation delay, low-to-high impedance output			17	30	ns
t_{PZH}	Enable propagation delay, high impedance-to-high output for ISO7731B			17	30	ns
	Enable propagation delay, high impedance-to-high output for ISO7731B with F suffix			3.2	8.5	µs
t_{PZL}	Enable propagation delay, high impedance-to-low output for ISO7731B			3.2	8.5	µs
	Enable propagation delay, high impedance-to-low output for ISO7731B with F suffix			17	30	ns
t_{DO}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7 V. See Figure 11		0.1	0.3	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 100 Mbps		0.6		ns

(1) Also known as Pulse Skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.17 Switching Characteristics—2.5-V Supply

V_{CC1} = V_{CC2} = 2.5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 9	7.5	12	18.5	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$			0.2	5.1	ns
$t_{sk(o)}$	Channel-to-channel output skew time(2)	Same-direction Channels			4.1	ns
$t_{sk(pp)}$	Part-to-part skew time(3)				4.6	ns
t_r	Output signal rise time	See Figure 9		1	3.5	ns
t_f	Output signal fall time			1	3.5	ns
t_{PHZ}	Disable propagation delay, high-to-high impedance output	See Figure 10		22	40	ns
t_{PLZ}	Disable propagation delay, low-to-high impedance output			22	40	ns
t_{PZH}	Enable propagation delay, high impedance-to-high output for ISO7731B			18	40	ns
	Enable propagation delay, high impedance-to-high output for ISO7731B with F suffix			3.3	8.5	µs
t_{PZL}	Enable propagation delay, high impedance-to-low output for ISO7731B			3.3	8.5	µs
	Enable propagation delay, high impedance-to-low output for ISO7731B with F suffix			18	40	ns
t_{DO}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7 V. See Figure 11		0.1	0.3	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 100 Mbps		0.6		ns

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.18 Insulation Characteristics Curves

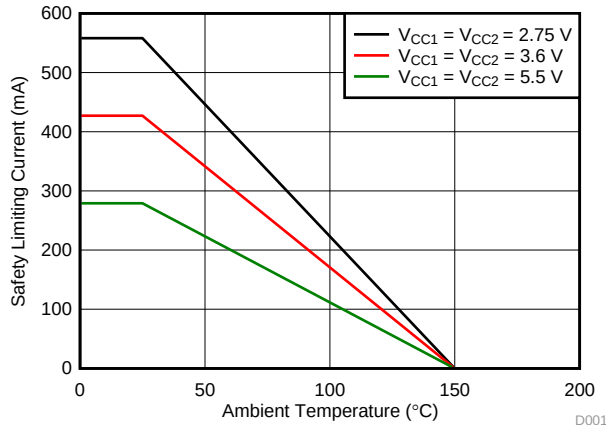


Figure 1. Thermal Derating Curve for Safety Limiting Current per VDE

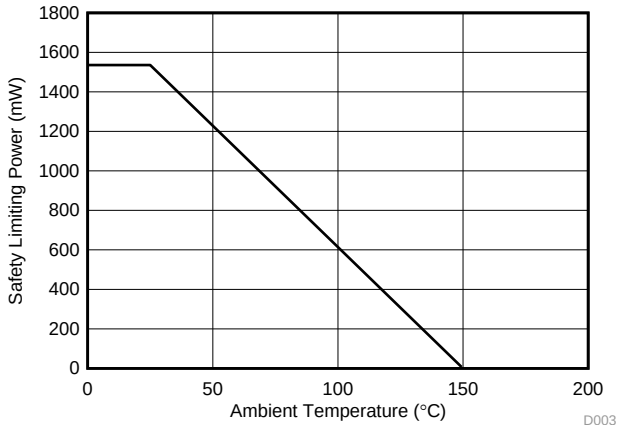
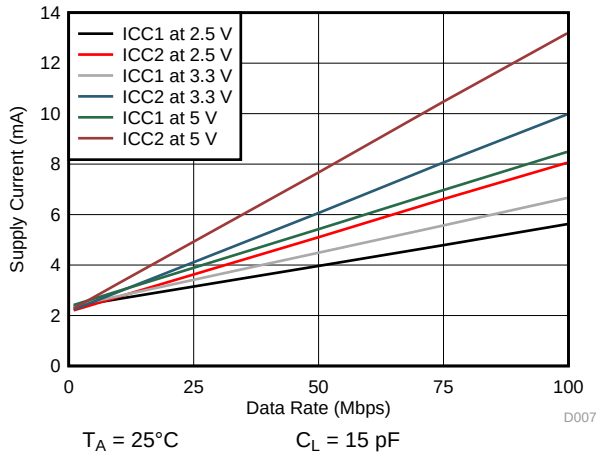


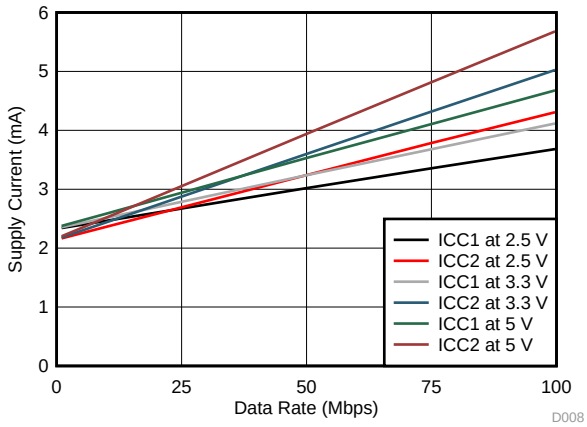
Figure 2. Thermal Derating Curve for Safety Limiting Power per VDE

6.19 Typical Characteristics



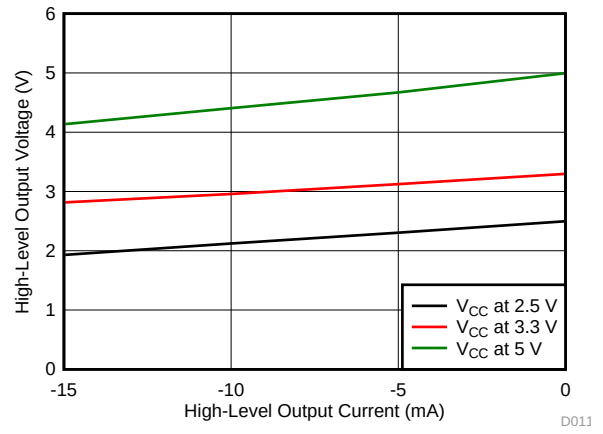
T_A = 25°C C_L = 15 pF

Figure 3. ISO7731B Supply Current vs Data Rate (With 15-pF Load)



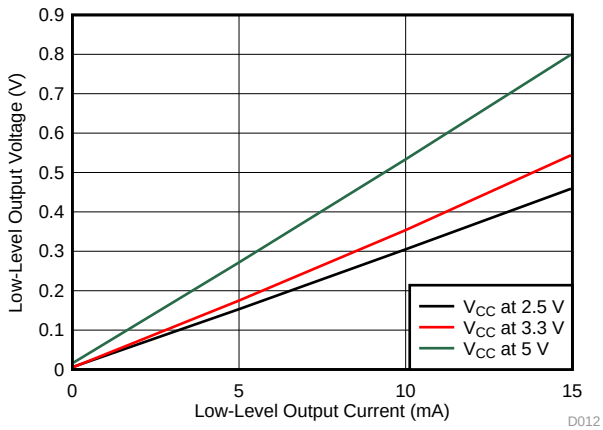
T_A = 25°C C_L = No Load

Figure 4. ISO7731B Supply Current vs Data Rate (With No Load)



T_A = 25°C

Figure 5. High-Level Output Voltage vs High-level Output Current



T_A = 25°C

Figure 6. Low-Level Output Voltage vs Low-Level Output Current

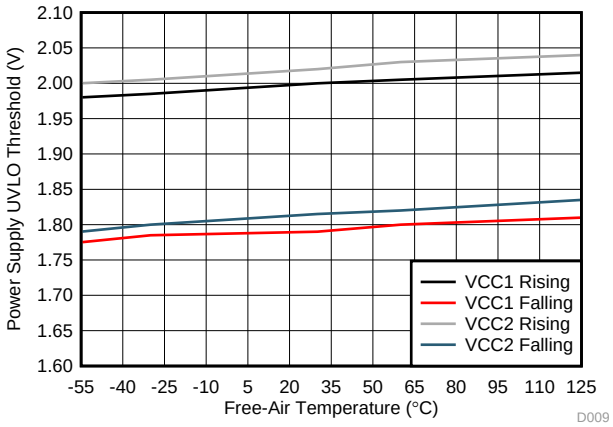


Figure 7. Power Supply Undervoltage Threshold vs Free-Air Temperature

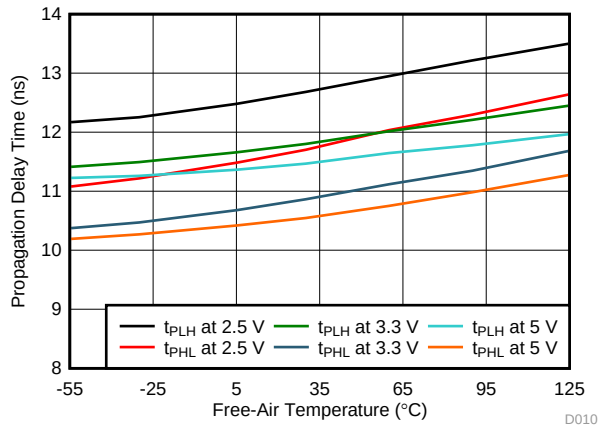
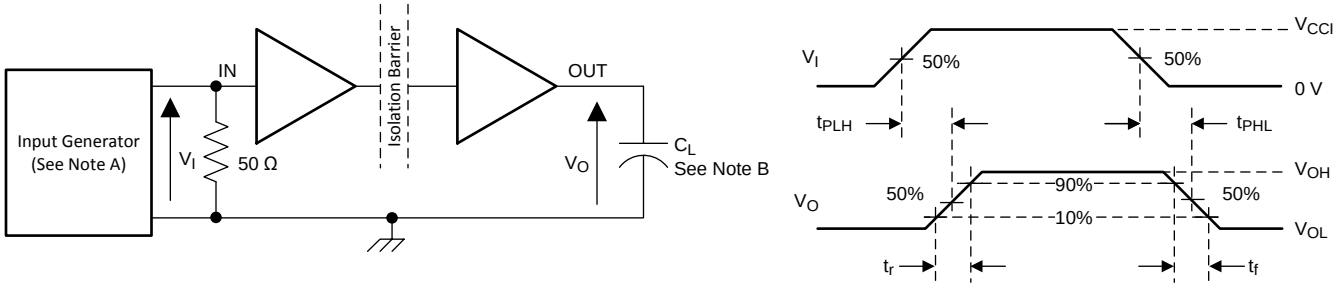


Figure 8. Propagation Delay Time vs Free-Air Temperature

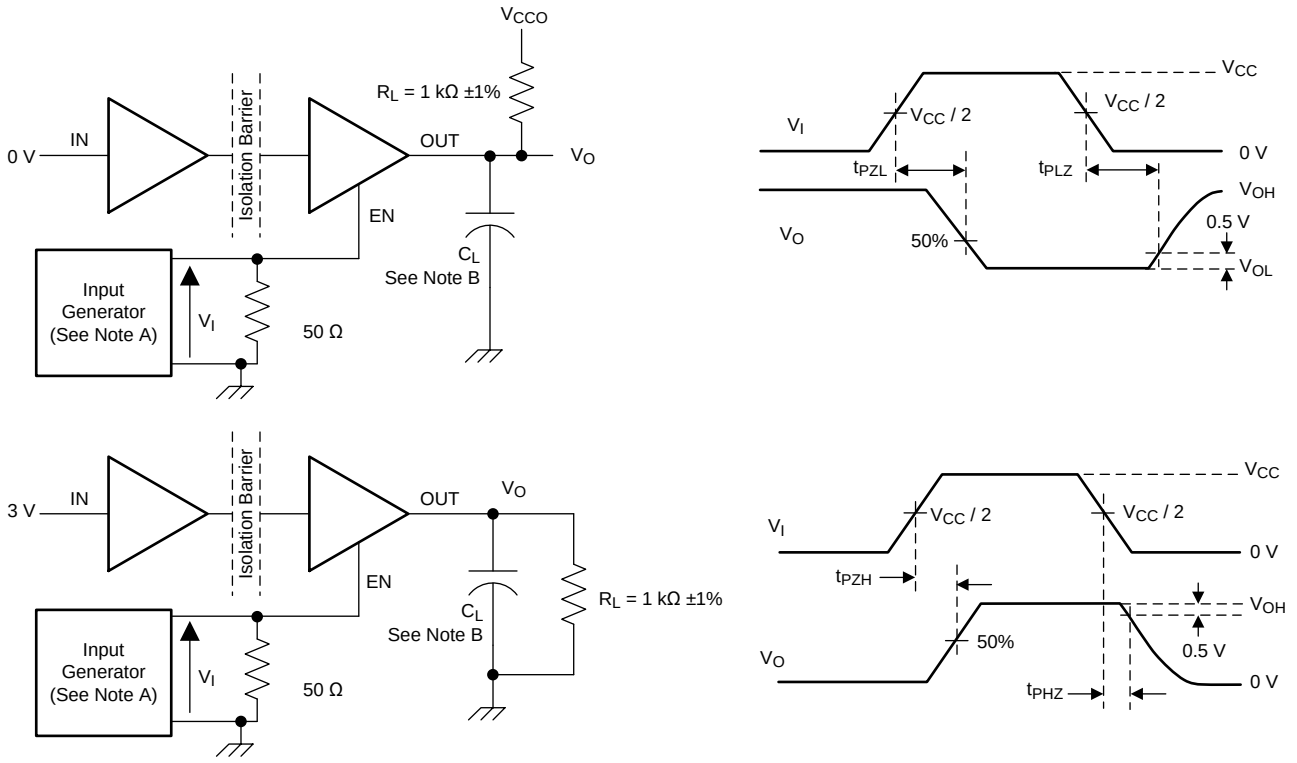
7 Parameter Measurement Information



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3ns, Z_O = 50 Ω. At the input, 50 Ω resistor is required to terminate Input Generator signal. It is not needed in actual application.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 9. Switching Characteristics Test Circuit and Voltage Waveforms

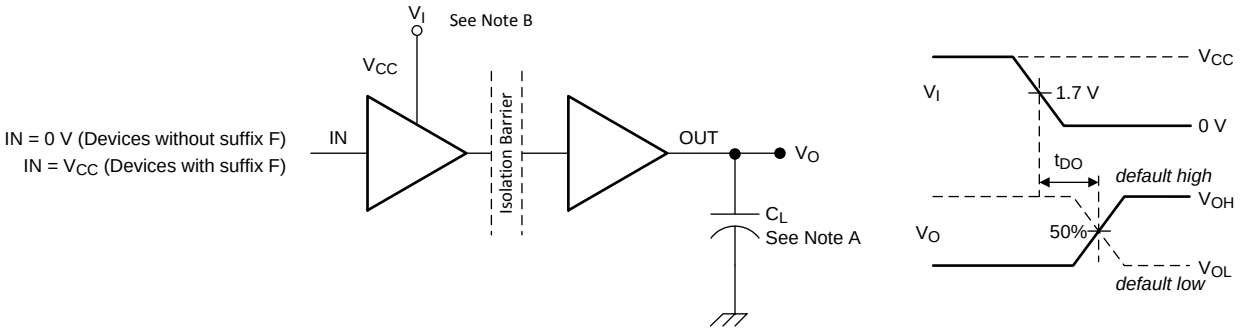


A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 10 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 10. Enable/Disable Propagation Delay Time Test Circuit and Waveform

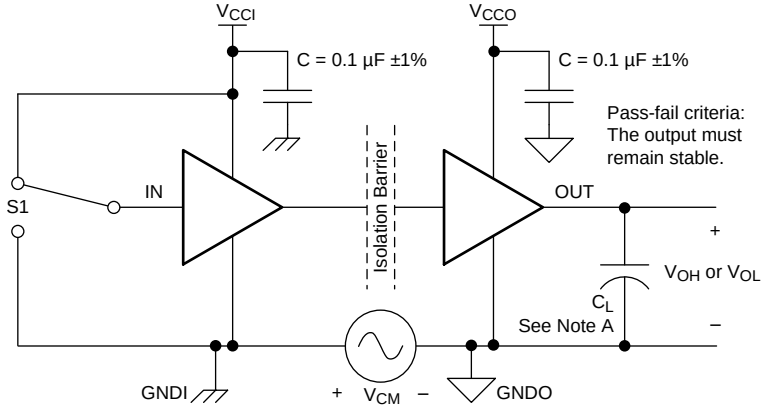
Parameter Measurement Information (continued)



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

B. Power Supply Ramp Rate = 10 mV/ns

Figure 11. Default Output Delay Time Test Circuit and Voltage Waveforms



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 12. Common-Mode Transient Immunity Test Circuit

8 Detailed Description

8.1 Overview

The ISO7731B device has an ON-OFF keying (OOK) modulation scheme to transmit the digital data across a silicon dioxide based isolation barrier. The transmitter sends a high frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal after advanced signal conditioning and produces the output through a buffer stage. If the ENx pin is low then the output goes to high impedance. The ISO7731B device also incorporates advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions because of the high frequency carrier and IO buffer switching. The conceptual block diagram of a digital capacitive isolator, Figure 13, shows a functional block diagram of a typical channel.

8.2 Functional Block Diagram

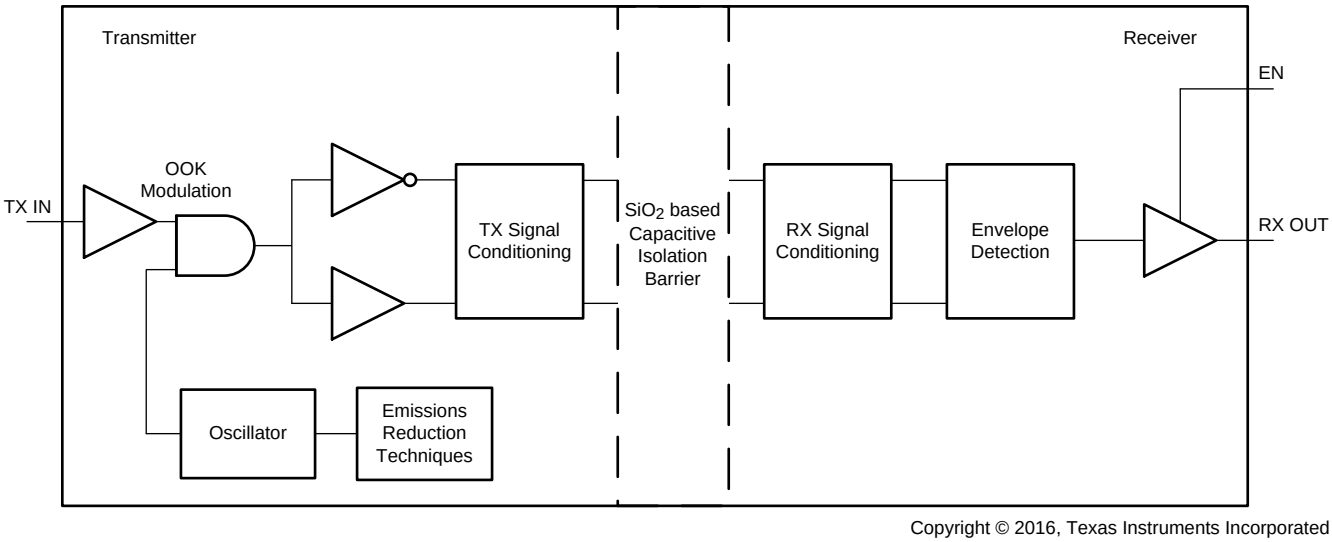


Figure 13. Conceptual Block Diagram of a Digital Capacitive Isolator

Figure 14 shows a conceptual detail of how the ON-OFF keying scheme works.

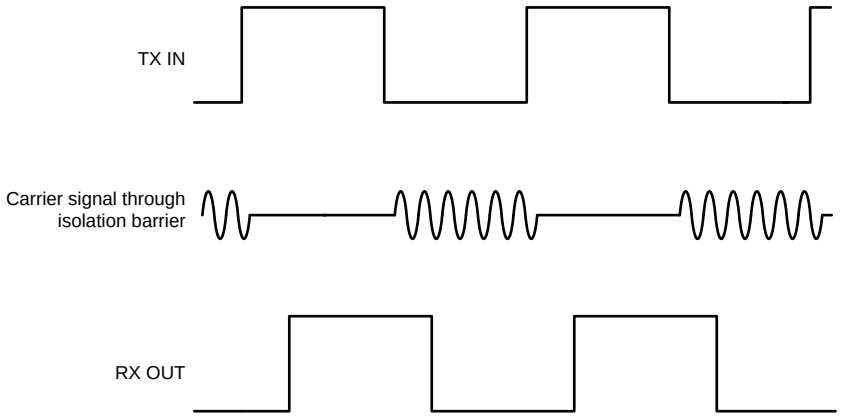


Figure 14. On-Off Keying (OOK) Based Modulation Scheme

8.3 Feature Description

Table 1 provides an overview of the device features.

Table 1. Device Features

PART NUMBER	CHANNEL DIRECTION	MAXIMUM DATA RATE	DEFAULT OUTPUT	ISOLATION RATING(1)
ISO7731B	2 Forward, 1 Reverse	100 Mbps	High	5000 V_{RMS} / 8000 V_{PK}
ISO7731B with F suffix	2 Forward, 1 Reverse	100 Mbps	Low	5000 V_{RMS} / 8000 V_{PK}

(1) See *Safety-Related Certifications* for detailed isolation ratings.

8.3.1 Electromagnetic Compatibility (EMC) Considerations

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x and CISPR 22. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the ISO7731B device incorporates many chip-level design improvements for overall system robustness. Some of these improvements include:

- Robust ESD protection cells for input and output signal pins and inter-chip bond pads.
- Low-resistance connectivity of ESD cells to supply and ground pins.
- Enhanced performance of high voltage isolation capacitor for better tolerance of ESD, EFT and surge events.
- Bigger on-chip decoupling capacitors to bypass undesirable high energy signals through a low impedance path.
- PMOS and NMOS devices isolated from each other by using guard rings to avoid triggering of parasitic SCRs.
- Reduced common mode currents across the isolation barrier by ensuring purely differential internal operation.

8.4 Device Functional Modes

Table 2 lists the functional modes for the ISO7731B device.

Table 2. Function Table(1)

V_{CCI}	V_{CCO}	INPUT (INx)(2)	OUTPUT ENABLE (ENx)	OUTPUT (OUTx)	COMMENTS
PU	PU	H	H or open	H	Normal Operation: A channel output assumes the logic state of its input.
		L	H or open	L	
		Open	H or open	Default	Default mode: When INx is open, the corresponding channel output goes to its default logic state. Default is *High* for ISO7731B and *Low* for ISO7731B with F suffix.
X	PU	X	L	Z	A low value of Output Enable causes the outputs to be high-impedance
PD	PU	X	H or open	Default	Default mode: When V_{CCI} is unpowered, a channel output assumes the logic state based on the selected default option. Default is *High* for IISO7731B and *Low* for ISO7731B with F suffix. When V_{CCI} transitions from unpowered to powered-up, a channel output assumes the logic state of its input. When V_{CCI} transitions from powered-up to unpowered, channel output assumes the selected default state.
X	PD	X	X	Undetermined	When V_{CCO} is unpowered, a channel output is undetermined(3). When V_{CCO} transitions from unpowered to powered-up, a channel output assumes the logic state of its input

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}; PU = Powered up (V_{CC} ≥ 2.25 V); PD = Powered down (V_{CC} ≤ 1.7 V); X = Irrelevant; H = High level; L = Low level ; Z = High Impedance
(2) A strongly driven input signal can weakly power the floating V_{CC} through an internal protection diode and cause undetermined output.
(3) The outputs are in undetermined state when 1.7 V < V_{CCI}, V_{CCO} < 2.25 V.

8.4.1 Device I/O Schematics

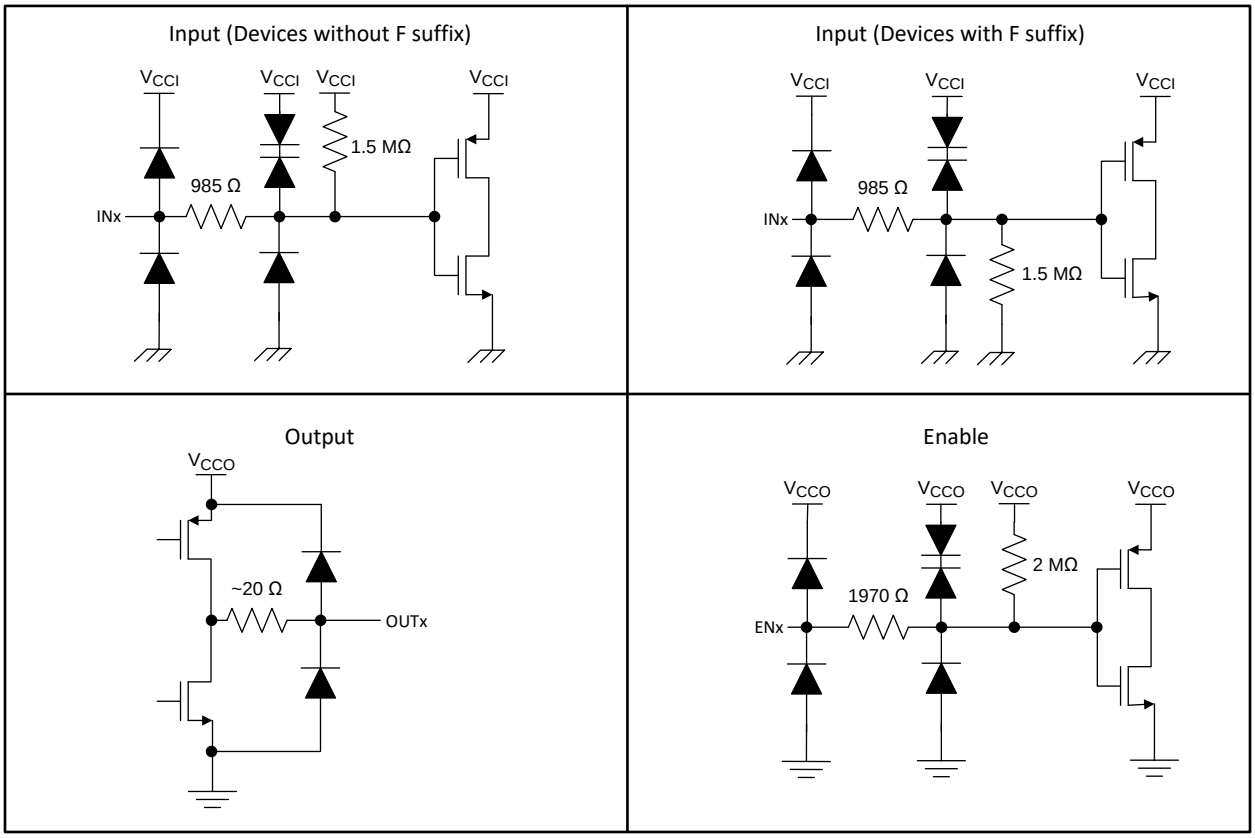


Figure 15. Device I/O Schematics

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The ISO7731B device is a high-performance, triple-channel digital isolator. This device comes with enable pins on each side which can be used to put the respective outputs in high impedance for multi-master driving applications and reduce power consumption. The ISO7731B device uses single-ended CMOS-logic switching technology. The voltage range is from 2.25 V to 5.5 V for both supplies, V_{CC1} and V_{CC2}. When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, μC or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

9.2 Typical Application

The ISO7731B device, combined with Texas Instruments' mixed-signal microcontroller, RS-485 transceiver, transformer driver, and voltage regulator, can create an isolated RS-485 system as shown in Figure 16.

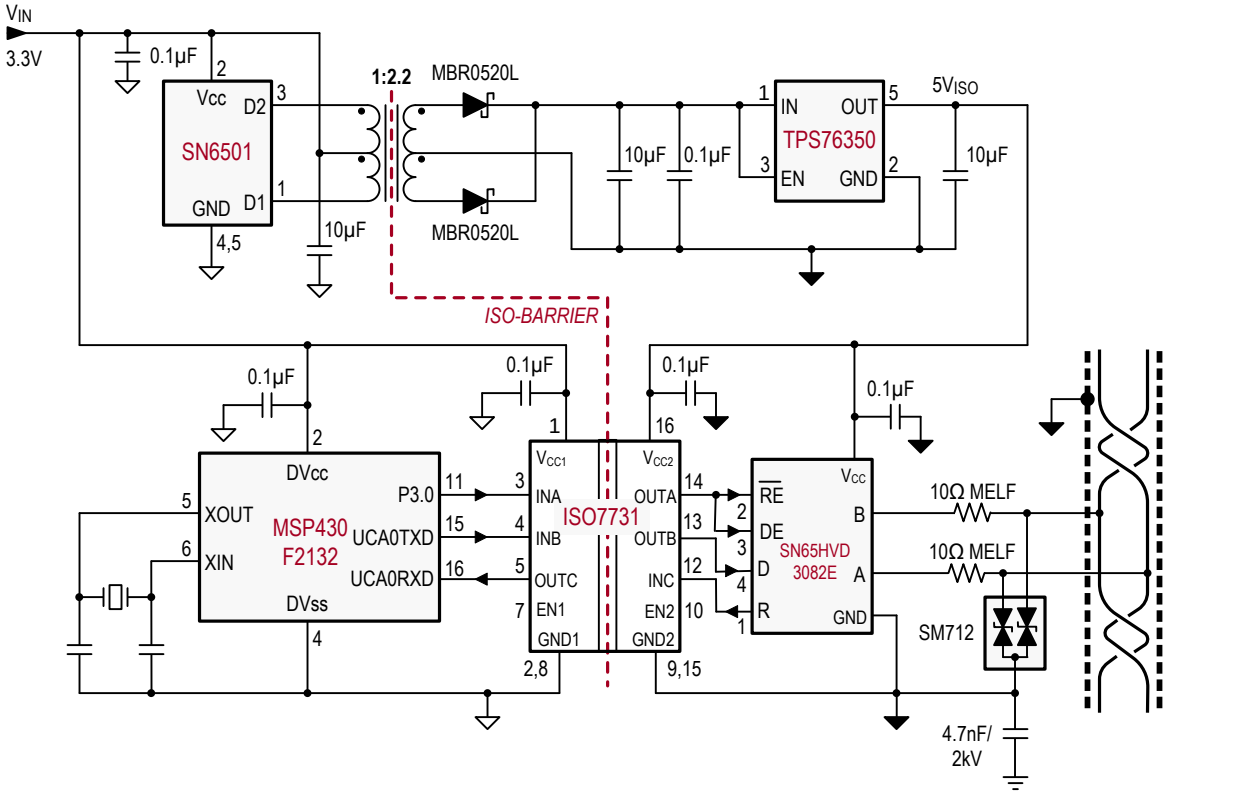


Figure 16. Isolated RS-485 Interface Circuit

Typical Application (continued)

9.2.1 Design Requirements

To design with these devices, use the parameters listed in Table 3.

Table 3. Design Parameters

PARAMETER	VALUE
Supply voltage, V_{CC1} and V_{CC2}	2.25 to 5.5 V
Decoupling capacitor between V_{CC1} and GND1	0.1 µF
Decoupling capacitor from V_{CC2} and GND2	0.1 µF

9.2.2 Detailed Design Procedure

Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the ISO7731B device only requires two external bypass capacitors to operate. Figure 17 shows the typical circuit hook-up for the device.

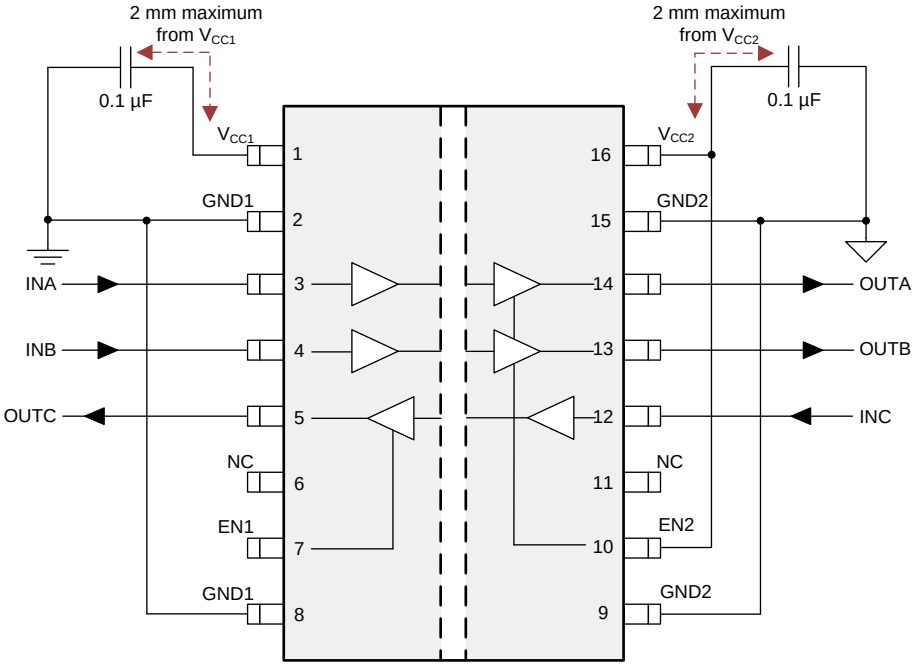


Figure 17. Typical ISO7731B Circuit Hook-Up

9.2.3 Application Curves

The following typical eye diagrams of the ISO7731B device indicates low jitter and wide open eye at the maximum data rate of 100 Mbps.

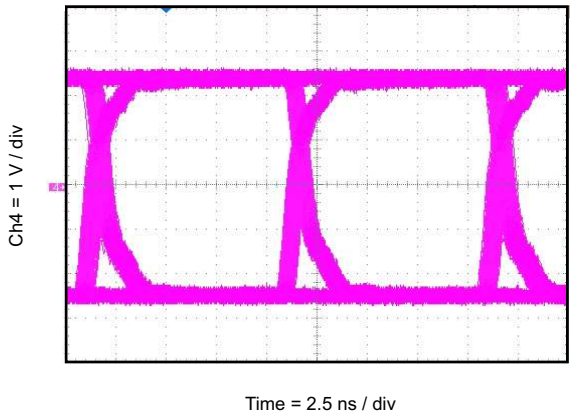


Figure 18. Eye Diagram at 100 Mbps PRBS 2^{16} – 1, 5 V and 25°C

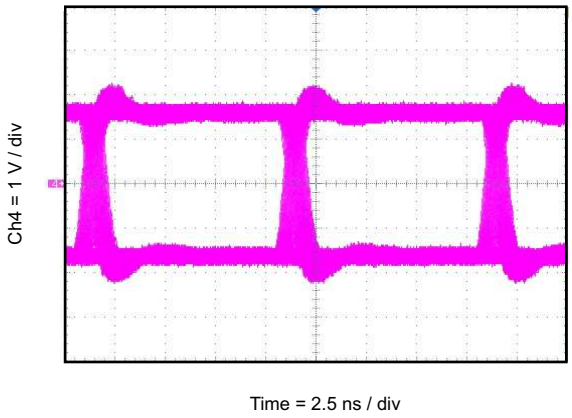


Figure 19. Eye Diagram at 100 Mbps PRBS 2^{16} – 1, 3.3 V and 25°C

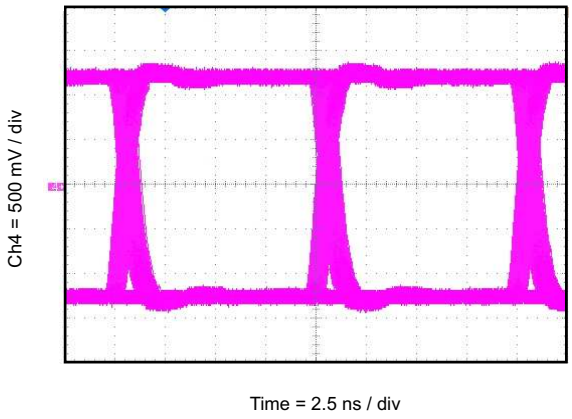


Figure 20. Eye Diagram at 100 Mbps PRBS 2^{16} – 1, 2.5 V and 25°C

10 Power Supply Recommendations

To help ensure reliable operation at data rates and supply voltages, a 0.1-µF bypass capacitor is recommended at the input and output supply pins (V_{CC1} and V_{CC2}). The capacitors should be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments' SN6501 or SN6505A. For such applications, detailed power supply design and transformer selection recommendations are available in the *SN6501 Transformer Driver for Isolated Power Supplies* data sheet or *SN6505A Low-Noise 1-A Transformer Drivers for Isolated Power Supplies* data sheet.

11 Layout

11.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see Figure 21). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/inch^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, refer to the *Digital Isolator Design Guide*.

11.1.1 PCB Material

For digital circuit boards operating below 150 Mbps, (or rise and fall times higher than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit boards. This PCB is preferred over cheaper alternatives due to its lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and self-extinguishing flammability-characteristics.

11.2 Layout Example

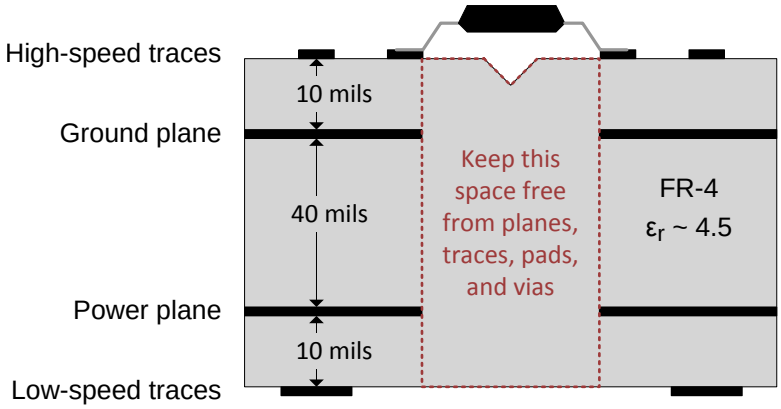


Figure 21. Layout Example Schematic

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Digital Isolator Design Guide*
- Texas Instruments, *Isolation Glossary*
- Texas Instruments, *How to use isolation to improve ESD, EFT and Surge immunity in industrial systems* application report
- Texas Instruments, *SN6501 Transformer Driver for Isolated Power Supplies*
- Texas Instruments, *SNx5HVD308xE Low-Power RS-485 Transceivers, Available in a Small MSOP-8 Package*
- Texas Instruments, TPS76350 *Low-Power 150-mA Low-Dropout Linear Regulators*
- Texas Instruments, MSP430F2132 *Mixed Signal Microcontroller*

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

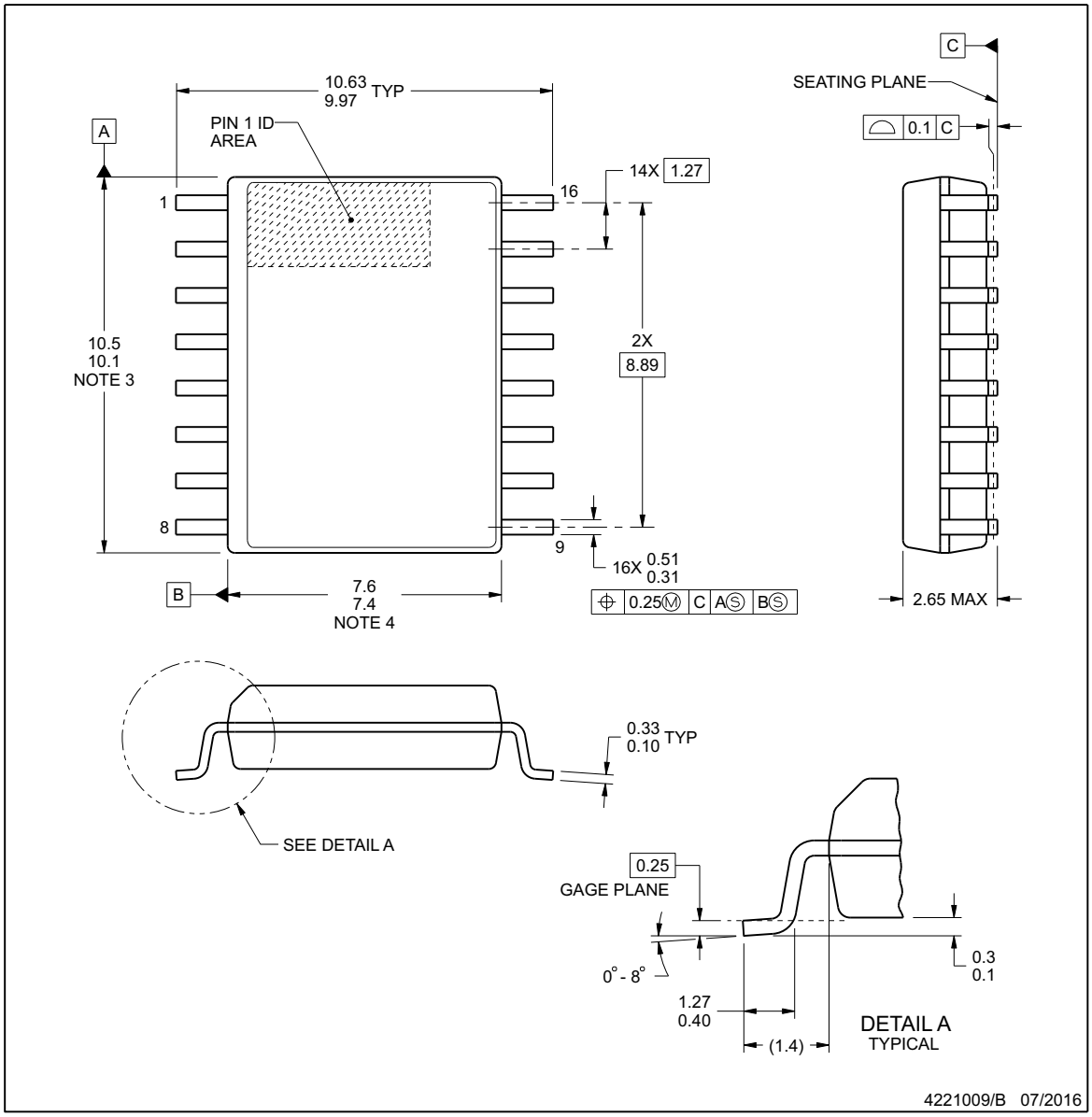
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

DW0016B

SOIC - 2.65 mm max height

SOIC



NOTES:

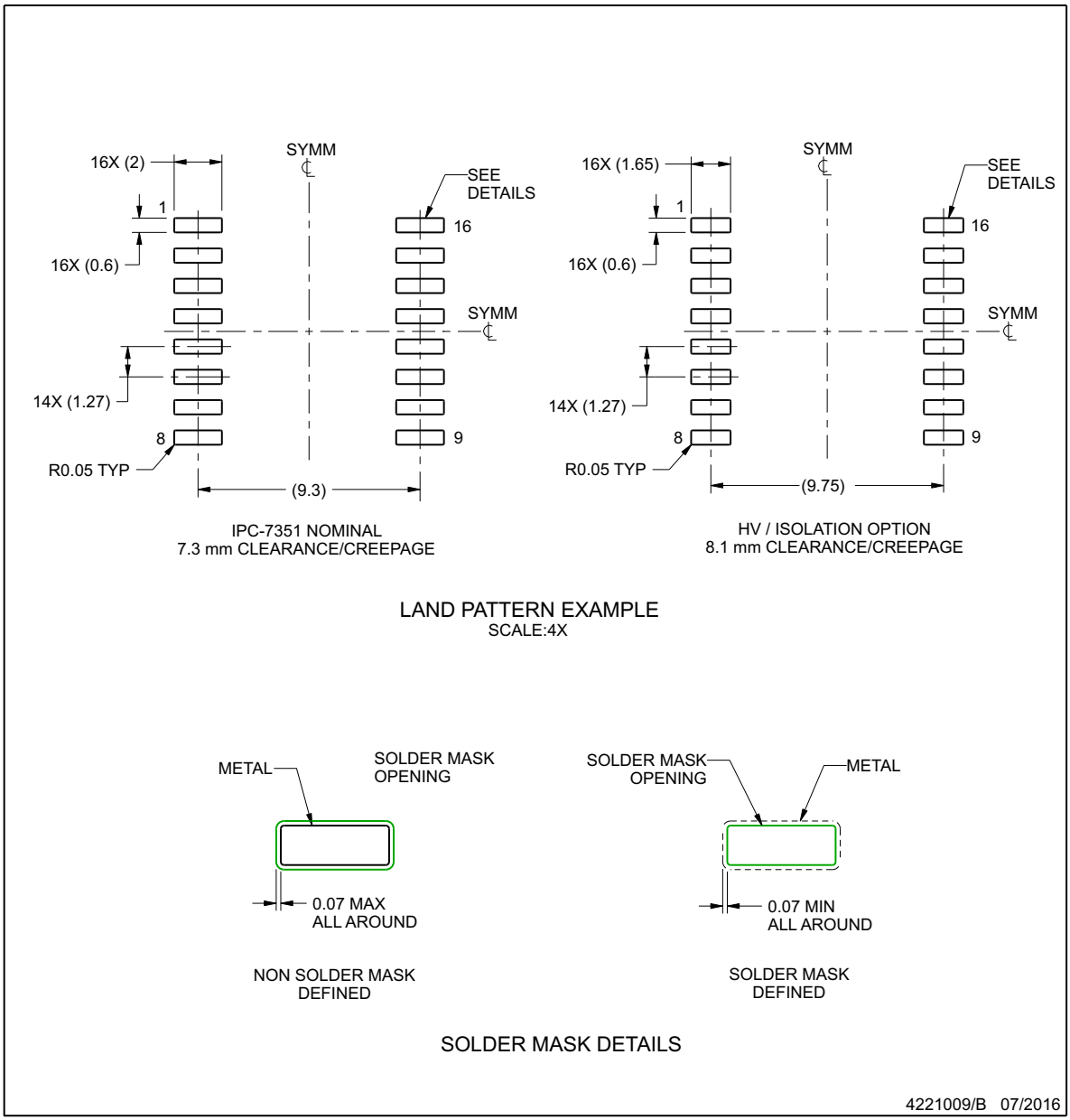
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0016B

SOIC - 2.65 mm max height

SOIC



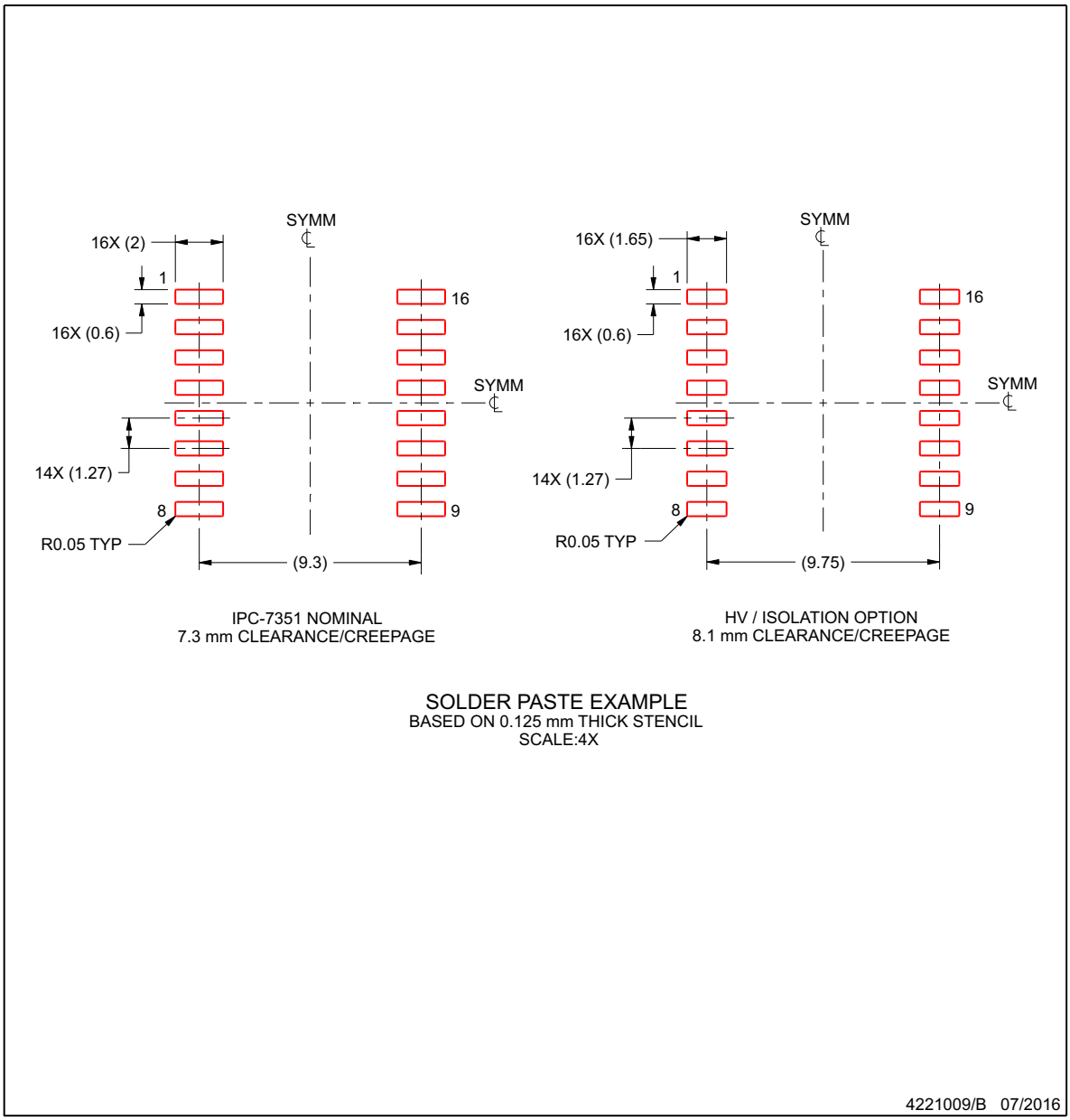
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0016B — **SOIC - 2.65 mm max height**

SOIC



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

13.1 Package Option Addendum

13.1.1 Packaging Information

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (3)	MSL Peak Temp (4)	Op Temp (°C)	Device Marking (5) (6)
ISO7731BDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7731B
ISO7731BDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7731B
ISO7731FBDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7731FB
ISO7731FBDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7731FB

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

(4) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

(6) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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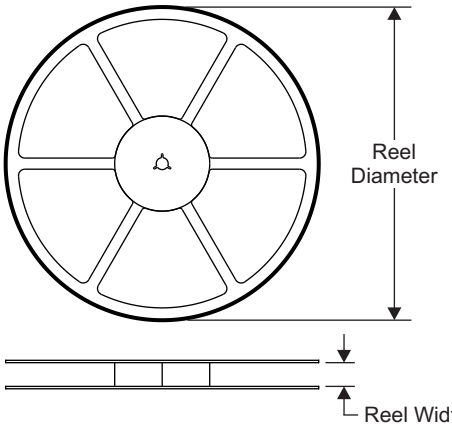
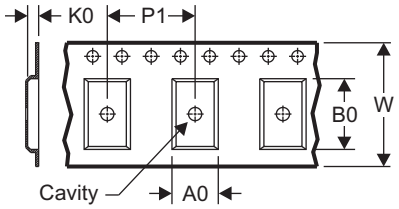
13.1.2 Tape and Reel Information

REEL DIMENSIONS

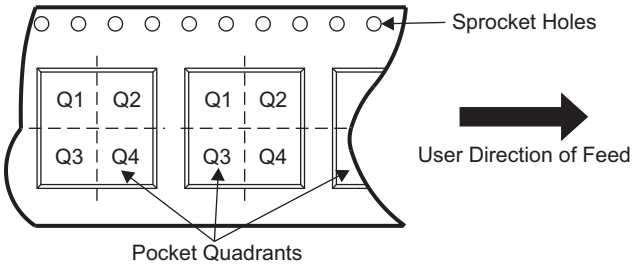


TAPE DIMENSIONS



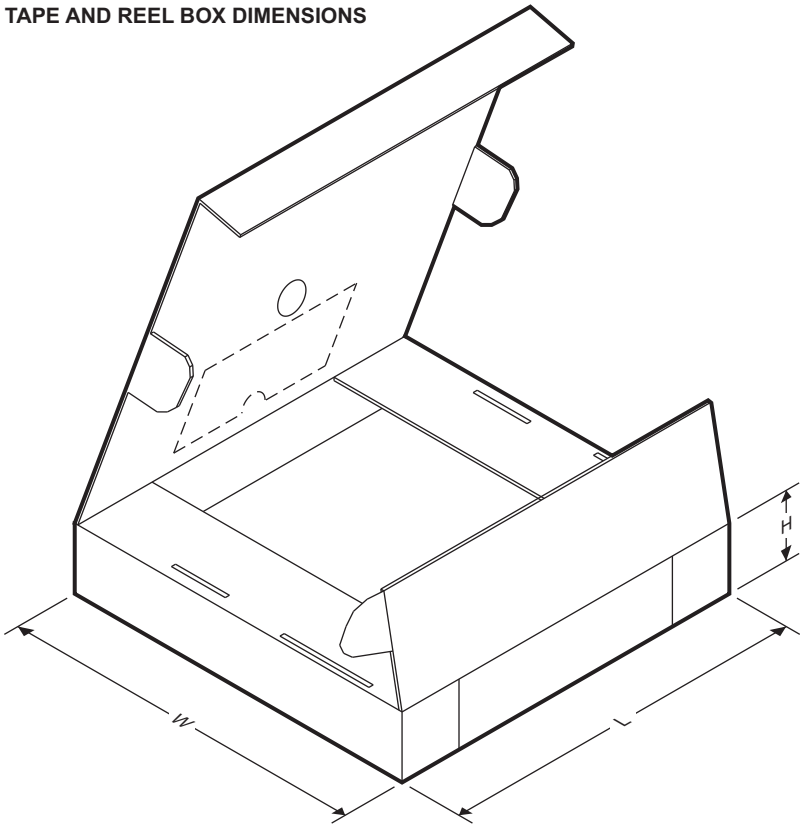
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7731BDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7731FBDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7731BDWR	SOIC	DW	16	2000	367.0	367.0	38.0
ISO7731FBDWR	SOIC	DW	16	2000	367.0	367.0	38.0

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO7731BDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7731B	Samples
ISO7731BDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7731B	Samples
ISO7731FBDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7731FB	Samples
ISO7731FBDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7731FB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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GENERIC PACKAGE VIEW

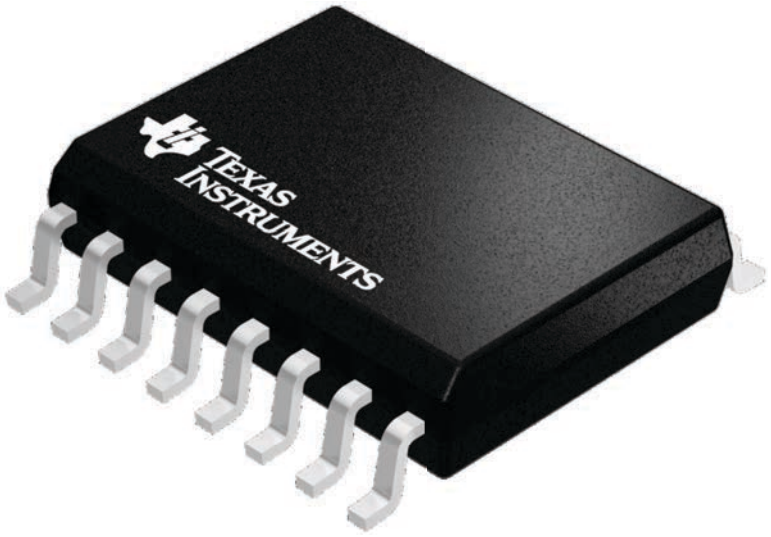
DW 16

SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

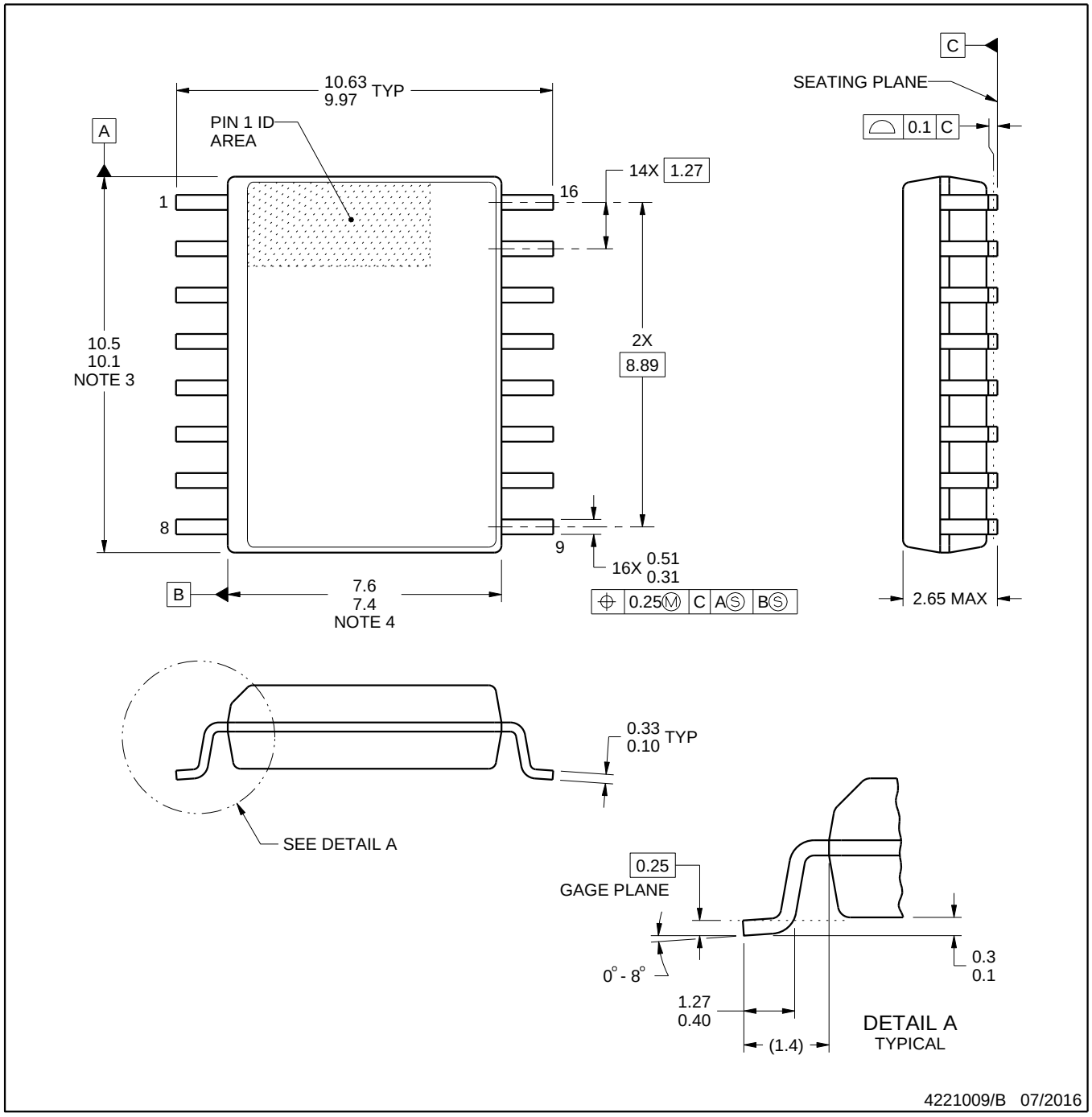
SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



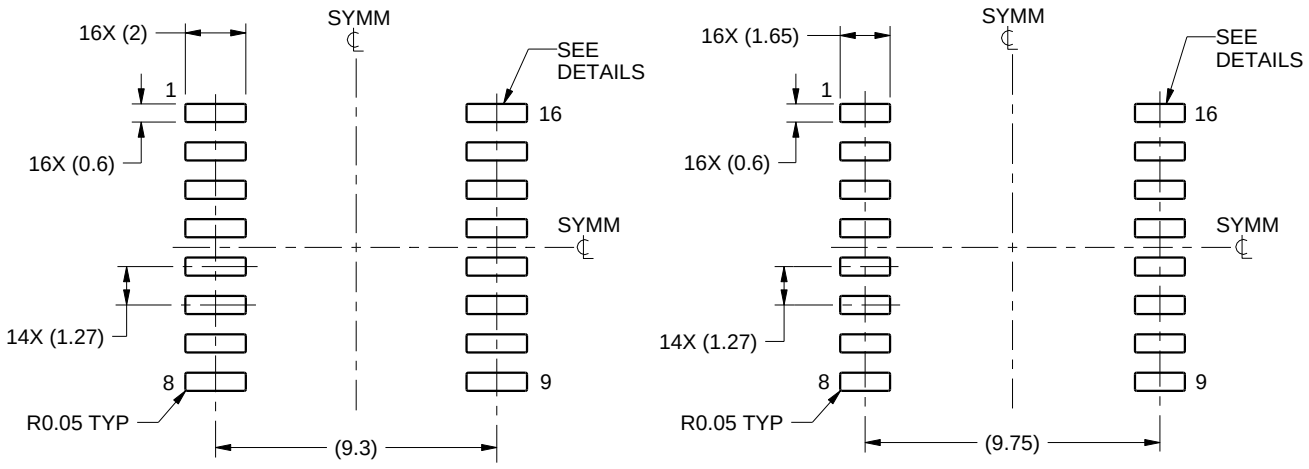
4224780/A

SOIC



NOTES:

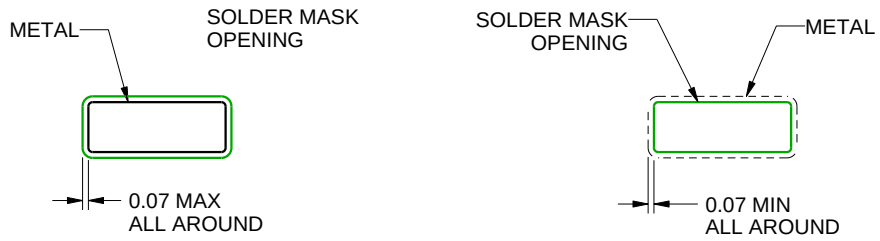
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

LAND PATTERN EXAMPLE
SCALE:4X



NON SOLDER MASK DEFINED

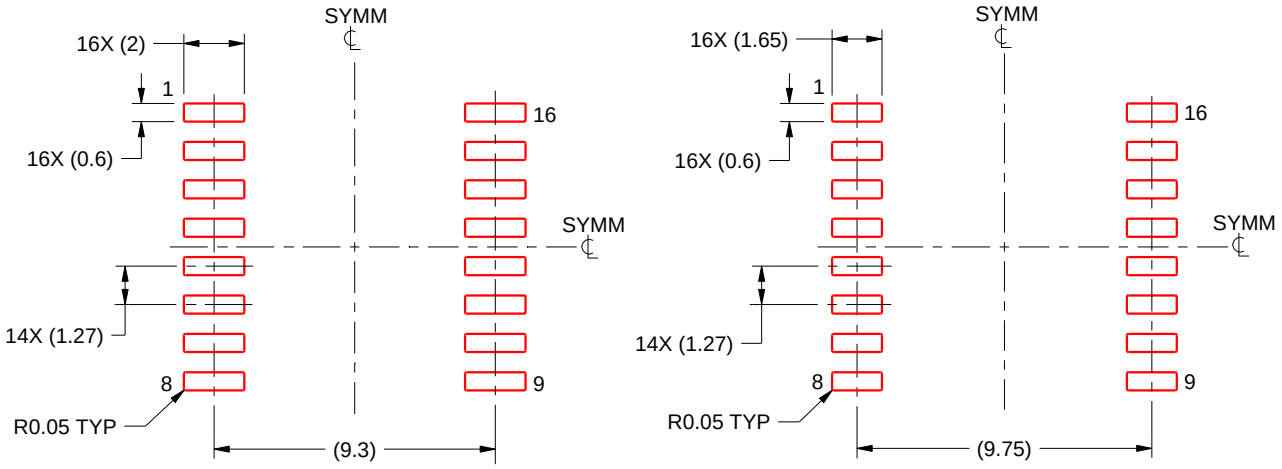
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4221009/B 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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