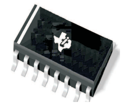


Low-Power 5 KV(rms) Dual Digital Isolators

Check for Samples: ISO7520, ISO7521

FEATURES

- **Highest Signaling Rate: 1 Mbps**
- **Propagation Delay Less Than 20 ns**
- **Low Power Consumption**
- **Wide Ambient Temperature: –40°C to 105°C**
- **Safety and Regulatory Approvals**
  - **5 KV(rms) for 1 minute per UL 1577**
  - **CSA Component Acceptance Notice 5A**
  - **IEC 60747-5-2 (VDE 0884 Rev. 2)**
  - **IEC 60601-1, 60950-1, & 61010-1 End Equipment Standards**
- **50 kV/μs Transient Immunity Typical**
- **Operates From 3.3V or 5V Supply and Logic Levels**

APPLICATIONS

- **Opto-Coupler Replacement in:**
  - **Medical Applications for IEC 60601-1 5KVrms Rated**
  - **Industrial Field-Bus**
    - **ProfiBus**
    - **ModBus**
    - **DeviceNetTM Data Buses**
  - **Servo Control Interface**
  - **Motor Control**
  - **Power Supply**
  - **Battery Packs**

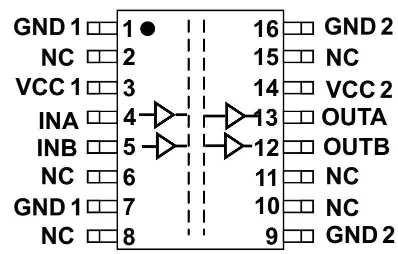
DESCRIPTION

The ISO7520 and ISO7521 provide double galvanic isolation of up to 5KVrms for 1 minute per UL. These digital isolators have two isolated channels with uni-directional (ISO7520) and bi-directional (ISO7521) channel configurations. Each isolation channel has a logic input and output buffer separated by a silicon oxide (SiO_2) insulation barrier. Used in conjunction with isolated power supplies, these devices prevent noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry.

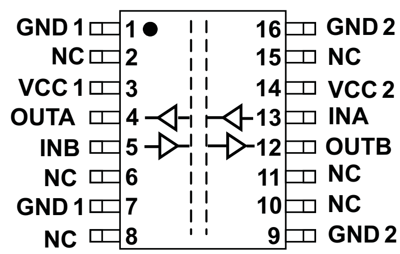
The devices have TTL input thresholds and require two supply voltages, 3.3V or 5V, or any combination. All inputs are 5-V tolerant when supplied from a 3.3-V supply.

Note: The ISO7520 and ISO7521 are specified for signaling rates up to 1 Mbps. Due to their fast response time, under most cases, these devices will also transmit data with much shorter pulse widths. Designers should add external filtering to remove spurious signals with input pulse duration < 20 ns if desired.

ISO 7520



ISO 7521



NC = No Internal Connection

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DEVICE FUNCTION TABLE

INPUT SIDE (VCC)(1)	OUTPUT SIDE (VCC)(1)	INPUT (IN)(1)	OUTPUT (OUT)(1)
PU	PU	H	H
		L	L
		Open	H
PD	PU	X	H

(1) PU = Powered Up (Vcc ≥ 3.15V); PD = Powered Down (Vcc ≤ 2.4V); X = Irrelevant; H = High Level; L = Low Level

AVAILABLE OPTIONS

PRODUCT	RATED T_A	MARKED AS	ORDERING NUMBER
ISO7520C	–40°C to 105°C	ISO7520CDW	ISO7520CDW (rail)
			ISO7520CDWR (reel)
ISO7521C	–40°C to 105°C	ISO7521CDW	ISO7521CDW (rail)
			ISO7521CDWR (reel)

ABSOLUTE MAXIMUM RATINGS(1)

					VALUE	UNIT
V_{CC}	Supply voltage(2), V_{CC1}, V_{CC2}				–0.5 V to 6	V
V_I	Voltage at IN, OUT				–0.5 V to 6	V
I_O	Output Current				±15	mA
ESD	Electrostatic discharge	Human Body Model	JEDEC Standard 22, Test Method A114-C.01	All pins	±4	kV
		Field-Induced-Charged Device Model	JEDEC Standard 22, Test Method C101		±1	kV
		Machine Model	ANSI/ESDS5.2-1996		±200	V
T_J	Maximum junction temperature				150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential I/O bus voltages are with respect to network ground terminal and are peak voltage values.

THERMAL INFORMATION

THERMAL METRIC		ISO752xC DW 16 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(1)	79.9	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(2)	44.6	
θ_{JB}	Junction-to-board thermal resistance(3)	51.2	
ψ_{JT}	Junction-to-top characterization parameter(4)	18.0	
ψ_{JB}	Junction-to-board characterization parameter(5)	42.2	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(6)	n/a	
P_D	Device power dissipation, Vcc1 = Vcc2 = 5.25 V, T_J = 150°C, C_L = 15 pF, Input a 0.5 MHz 50% duty cycle square wave	42	mW

(1) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(2) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(4) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(5) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage - 3.3V Operation	3.15	3.3	3.45	V
	Supply voltage - 5V Operation	4.75	5	5.25	
I_{OH}	High-level output current	–4			mA
I_{OL}	Low-level output current			4	mA
V_{IH}	High-level output voltage	2		V_{CC}	V
V_{IL}	Low-level output voltage	0		0.8	V
T_A	Ambient Temperature	-40		105	°C
T_J(1)	Junction temperature	–40		136	°C
$1/t_{ui}$	Signaling rate	0		1	Mbps
t_{ui}	Input pulse duration	1			us

(1) To maintain the recommended operating conditions for T_J, see the *Package Thermal Characteristics* table and the *Icc Equations* section of this data sheet

ELECTRICAL CHARACTERISTICS

V_{CC1} and V_{CC2} at 5 V ± 5%, T_A = –40°C to 105°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; See Figure 1		V_{CC} –0.8	4.6		V
		I_{OH} = –20 µA; See Figure 1		V_{CC} –0.1	5		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; See Figure 1			0.2	0.4	V
		I_{OL} = 20 µA; See Figure 1			0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				400		mV
I_{IH}	High-level input current	INx at 0 V or V_{CC}				10	µA
I_{IL}	Low-level input current			–10			µA
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V; See Figure 3		25	50		kV/µs
SUPPLY CURRENT (All inputs switching with square wave clock signal for dynamic ICC measurement)							
ISO7520							
I_{CC1}	Supply current for V_{CC1}	DC to 1 Mbps	V_I = V_{CC} or 0 V, 15 pF load		0.4	1	mA
I_{CC2}	Supply current for V_{CC2}	DC to 1 Mbps	V_I = V_{CC} or 0 V, 15 pF load		3	6	mA
ISO7521							
I_{CC1}	Supply current for V_{CC1}	DC to 1 Mbps	V_I = V_{CC} or 0 V, 15 pF load		2	4	mA
I_{CC2}	Supply current for V_{CC2}	DC to 1 Mbps	V_I = V_{CC} or 0 V, 15 pF load		2	4	mA

SWITCHING CHARACTERISTICS

V_{CC1} and V_{CC2} at 5 V ± 5%, T_A = –40°C to 105°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 1		9	14	ns
PWD(1)	Pulse width distortion $\|t_{PHL} – t_{PLH}\|$			0.3	3.5	ns
$t_{sk(pp)}$	Part-to-part skew time				4	ns
$t_{sk(o)}$	Channel-to-channel output skew time				3.6	ns
t_r	Output signal rise time	See Figure 1		1		ns
t_f	Output signal fall time			1		ns
t_{fs}	Fail-safe output delay time from input power loss	See Figure 2		6		ns

(1) Also known as pulse skew.

ELECTRICAL CHARACTERISTICS

V_{CC1} at 5 V ± 5%, V_{CC2} at 3.3 V ± 5%, T_A = –40°C to 105°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; See Figure 1	ISO7521 (5-V side)	V_{CC} –0.8	4.6		V
			ISO7520/7521(3.3-V side)	V_{CC} –0.4	3		
		I_{OH} = –20 µA; See Figure 1		V_{CC} –0.1	V_{CC}		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; See Figure 1			0.2	0.4	V
		I_{OL} = 20 µA; See Figure 1			0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				400		mV
I_{IH}	High-level input current	INx at 0 V or V_{CC}				10	µA
I_{IL}	Low-level input current			–10			µA
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V; See Figure 3		25	40		kV/µs
SUPPLY CURRENT (All inputs switching with square wave clock signal for dynamic ICC measurement)							
	ISO7520						
I_{CC1}	Supply current for V_{CC1}	DC to 1 Mbps	V_I = V_{CC} or 0 V, 15 pF load		0.4	1	mA
I_{CC2}	Supply current for V_{CC2}	DC to 1 Mbps	V_I = V_{CC} or 0 V, 15 pF load		2	4.5	mA
	ISO7521						
I_{CC1}	Supply current for V_{CC1}	DC to 1 Mbps	V_I = V_{CC} or 0 V, 15 pF load		2	4	mA
I_{CC2}	Supply current for V_{CC2}	DC to 1 Mbps	V_I = V_{CC} or 0 V, 15 pF load		1.5	3.5	mA

SWITCHING CHARACTERISTICS

V_{CC1} at 5 V ± 5%, V_{CC2} at 3.3 V ± 5%, T_A = –40°C to 105°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 1		10	17	ns
PWD[(1)]	Pulse width distortion $\|t_{PHL} – t_{PLH}\|$			0.5	4	ns
$t_{sk(pp)}$	Part-to-part skew time				5	ns
$t_{sk(o)}$	Channel-to-channel output skew time				4	ns
t_r	Output signal rise time	See Figure 1		2		ns
t_f	Output signal fall time			2		ns
t_{fs}	Fail-safe output delay time from input power loss	See Figure 2		6		ns

(1) Also known as pulse skew.

ELECTRICAL CHARACTERISTICS

V_{CC1} at 3.3 V ± 5%, V_{CC2} at 5 V ± 5%, T_A = –40°C to 105°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; See Figure 1	ISO7520/7521 (5-V side)	V_{CC} –0.8	4.6		V
			ISO7521 (3.3-V side)	V_{CC} –0.4	3		
		I_{OH} = –20 µA; See Figure 1		V_{CC} –0.1	V_{CC}		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; See Figure 1			0.2	0.4	V
		I_{OL} = 20 µA; See Figure 1			0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				400		mV
I_{IH}	High-level input current	INx at 0 V or V_{CC}				10	µA
I_{IL}	Low-level input current			–10			µA
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V; See Figure 3		25	40		kV/µs
SUPPLY CURRENT (All inputs switching with square wave clock signal for dynamic ICC measurement)							
ISO7520							
I_{CC1}	Supply current for V_{CC1}	DC to 1 Mbps	V_I = V_{CC} or 0 V, 15 pF load		0.2	0.7	mA
I_{CC2}	Supply current for V_{CC2}	DC to 1 Mbps	V_I = V_{CC} or 0 V, 15 pF load		3	6	mA
ISO7521							
I_{CC1}	Supply current for V_{CC1}	DC to 1 Mbps	V_I = V_{CC} or 0 V, 15 pF load		1.5	3.5	mA
I_{CC2}	Supply current for V_{CC2}	DC to 1 Mbps	V_I = V_{CC} or 0 V, 15 pF load		2	4	mA

SWITCHING CHARACTERISTICS

V_{CC1} at 3.3 V ± 5%, V_{CC2} at 5 V ± 5%, T_A = –40°C to 105°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 1		10	17	ns
PWD(1)	Pulse width distortion $\|t_{PHL} – t_{PLH}\|$			0.5	4	ns
$t_{sk(pp)}$	Part-to-part skew time				5	ns
$t_{sk(o)}$	Channel-to-channel output skew time				4	ns
t_r	Output signal rise time	See Figure 1		2		ns
t_f	Output signal fall time			2		ns
t_{fs}	Fail-safe output delay time from input power loss	See Figure 2		6		ns

(1) Also known as pulse skew.

ELECTRICAL CHARACTERISTICS

V_{CC1} and V_{CC2} at 3.3 V ± 5%, T_A = –40°C to 105°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; See Figure 1		V_{CC} –0.4	3		V
		I_{OH} = –20 µA; See Figure 1		V_{CC} –0.1	3.3		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; See Figure 1			0.2	0.4	V
		I_{OL} = 20 µA; See Figure 1			0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				400		mV
I_{IH}	High-level input current	INx at 0 V or V_{CC}					µA
I_{IL}	Low-level input current			–10			µA
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V; See Figure 3		25	40		kV/µs
SUPPLY CURRENT (All inputs switching with square wave clock signal for dynamic ICC measurement)							
	ISO7520						
I_{CC1}	Supply current for V_{CC1}	DC to 1 Mbps	V_I = V_{CC} or 0 V, 15 pF load		0.2	0.7	mA
I_{CC2}	Supply current for V_{CC2}	DC to 1 Mbps	V_I = V_{CC} or 0 V, 15 pF load		2	4.5	mA
	ISO7521						
I_{CC1}	Supply current for V_{CC1}	DC to 1 Mbps	V_I = V_{CC} or 0 V, 15 pF load		1.5	3.5	mA
I_{CC2}	Supply current for V_{CC2}	DC to 1 Mbps	V_I = V_{CC} or 0 V, 15 pF load		1.5	3.5	mA

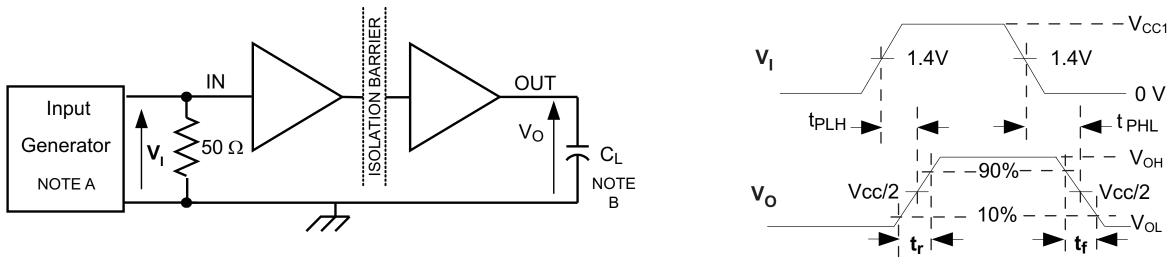
SWITCHING CHARACTERISTICS

V_{CC1} and V_{CC2} at 3.3 V ± 5%, T_A = –40°C to 105°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 1		12	20	ns
PWD[1]	Pulse width distortion $\lvert t_{PHL} – t_{PLH} \rvert$			1	5	ns
$t_{sk(pp)}$	Part-to-part skew time				6	ns
$t_{sk(o)}$	Channel-to-channel output skew time				5.5	ns
t_r	Output signal rise time	See Figure 1		2		ns
t_f	Output signal fall time			2		ns
t_{fs}	Fail-safe output delay time from input power loss	See Figure 2		6		ns

(1) Also known as pulse skew.

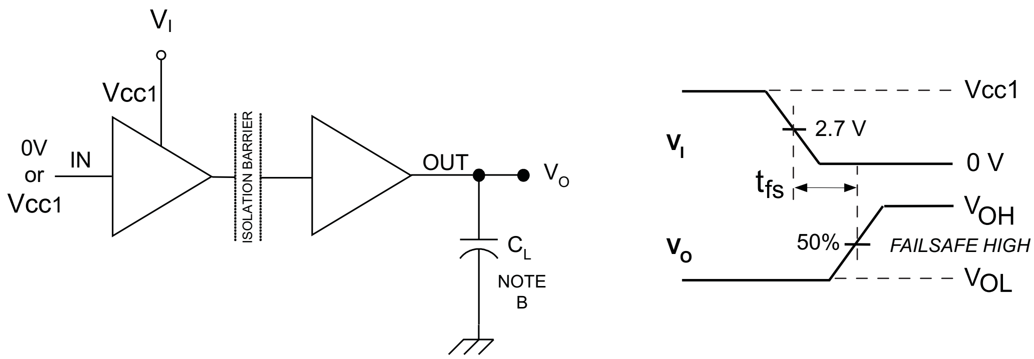
PARAMETER MEASUREMENT INFORMATION



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3ns, t_f ≤ 3ns, Z_O = 50Ω.

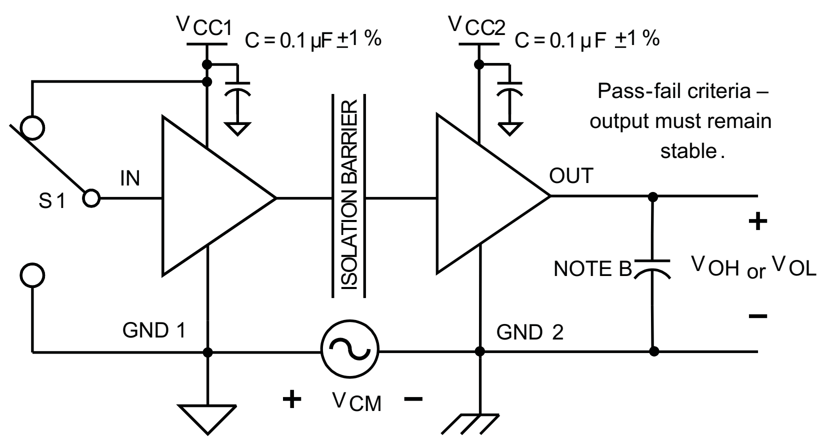
B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 1. Switching Characteristic Test Circuit and Voltage Waveforms



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 2. Failsafe Delay Time Test Circuit and Voltage Waveforms



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 3. Common-Mode Transient Immunity Test Circuit

DEVICE INFORMATION

PACKAGE CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
L(I01)	Minimum air gap (Clearance)	Shortest terminal to terminal distance through air	8.34			mm
L(I02)	Minimum external tracking (Creepage)	Shortest terminal to terminal distance across the package surface	8.1			mm
CTI	Tracking resistance (Comparative Tracking Index)	DIN IEC 60112 / VDE 0303 Part 1	≥400			V
	Minimum internal gap (Internal Clearance)	Distance through the insulation	0.016			mm
R_{IO}	Isolation resistance, input to output(1)	Input to output, V_{IO} = 500 V, all pins on each side of the barrier tied together creating a two-terminal device		$>10^{12}$		Ω
C_{IO}	Barrier capacitance input to output(1)	$V_{IO} = 0.4 \sin(2\pi ft)$, f = 1 MHz		2		pF
C_I	Input capacitance to ground(2)	$V_I = Vcc/2 + 0.4 \sin(2\pi ft)$, f = 1 MHz, Vcc = 5 V		2		pF

(1) All pins on each side of the barrier tied together creating a two-terminal device.
(2) Measured from input pin to ground.

NOTE

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board do not reduce this distance

Creepage and clearance on a printed circuit board become equal according to the measurement techniques shown in the Isolation Glossary. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.

IEC 60664-1 RATINGS TABLE

PARAMETER	TEST CONDITIONS	SPECIFICATION
Basic Isolation Group	Material Group	II
Installation Classification	Rated mains voltages <= 150 Vrms	I - IV
	Rated mains voltages <= 300 Vrms	I - IV
	Rated mains voltages <= 400 Vrms	I - III
	Rated mains voltages <= 600 Vrms	I - III

INSULATION CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SPECIFICATION	UNIT
V_{IORM}	Maximum working insulation voltage	V_{TEST} = 1.875 × V_{IORM}, PD ≤ 5pC, t = 10 sec (qualification) t = 1 sec (100% production)	1300/920	Vpeak/ Vrms
V_{IOTM}	Transient overvoltage	V_{TEST} = V_{IOTM}, t = 60 sec (qualification) t= 1 sec (100% production)	4000/2858	Vpeak/ Vrms
V_{ISO}	Isolation voltage per UL	V_{TEST} = V_{ISO} t = 60 sec (qualification), V_{TEST} = 1.2 × V_{ISO}, t = 1 sec (100% production)	7000/5000 8400/6000	Vpeak/ Vrms
R_S	Insulation resistance	V_{TEST} = 500 V at T_S = 150C	>10^9	Ω
	Pollution degree		2	

REGULATORY INFORMATION

VDE	CSA	UL
Certified according to IEC 60747-5-2	Approved under CSA Component Acceptance Notice	Recognized under 1577 Component Recognition Program
File Number: pending	File Number: pending	File Number: pending

IEC SAFETY LIMITING VALUES

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the IO can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Is	Safety input, output, or supply current	θ_{JA} =79.9 °C/W, V_I = 5.25 V, T_J = 150 °C, T_A = 25 °C			298	mA
		θ_{JA} =79.9 °C/W, V_I = 3.45 V, T_J = 150 °C, T_A = 25 °C			453	
Ts	Maximum Case Temperature				150	°C

The safety-limiting constraint is the absolute maximum junction temperature specified in the absolute maximum ratings table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the Thermal Characteristics table is that of a device installed on a High-K Test Board for Leaded Surface Mount Packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

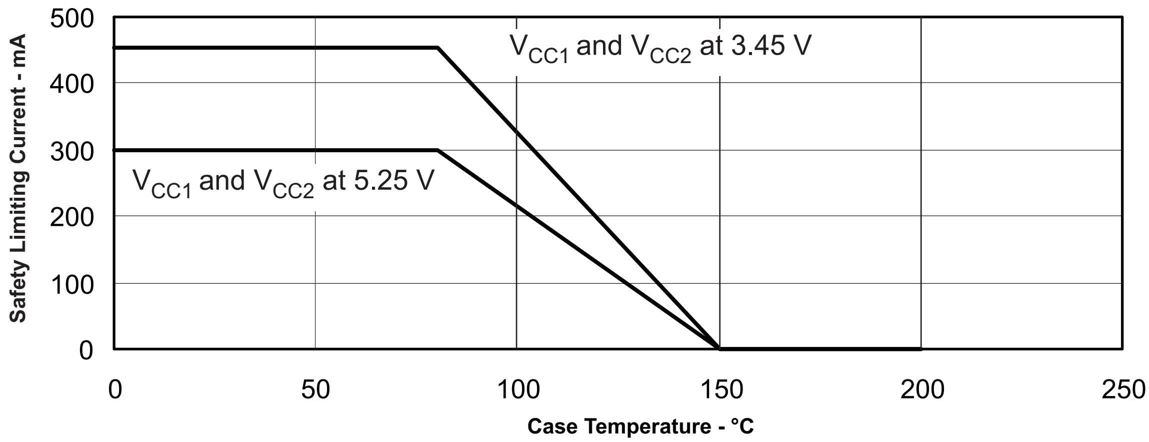


Figure 4. DW-16 Theta-JC Thermal Derating Curve per IEC 60747-5-2

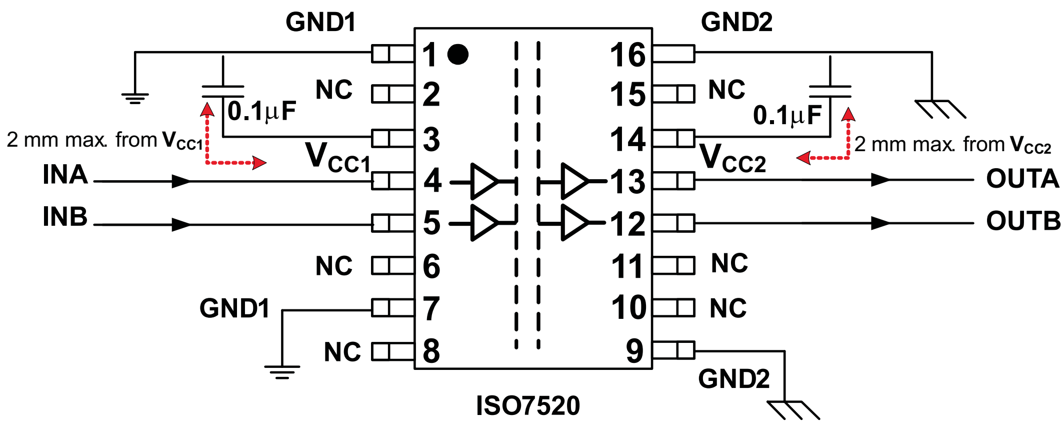


Figure 5. Typical ISO7520 Application Circuit

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

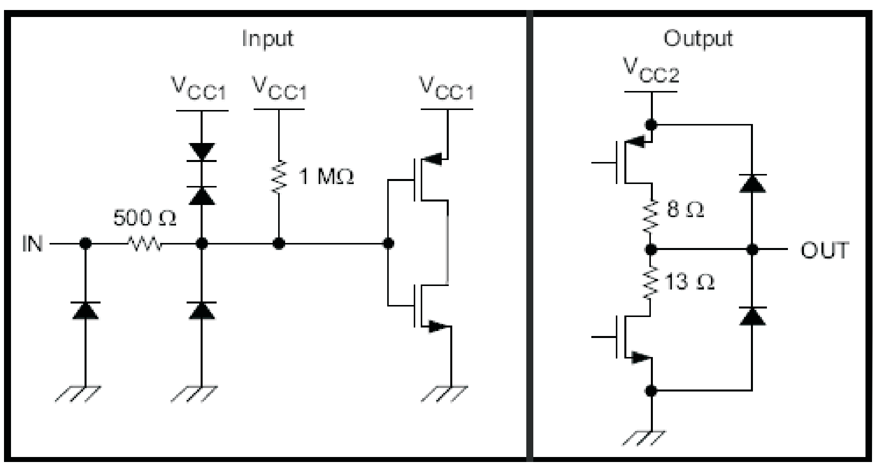


Figure 6. I/O Schematic

TYPICAL CHARACTERISTICS

INPUT VOLTAGE SWITCHING THRESHOLD vs FREE-AIR TEMPERATURE

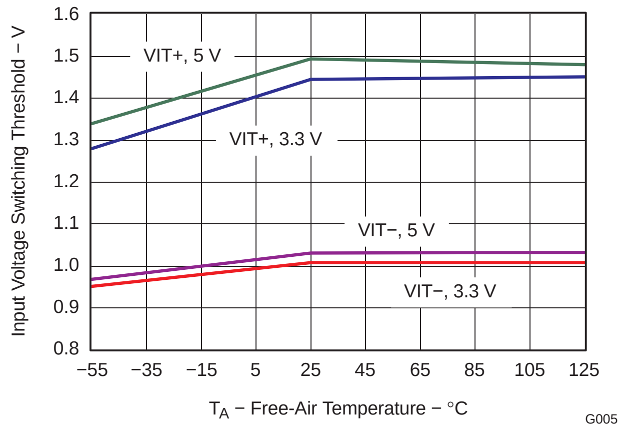


Figure 7.

FAIL-SAFE VOLTAGE THRESHOLD vs FREE-AIR TEMPERATURE

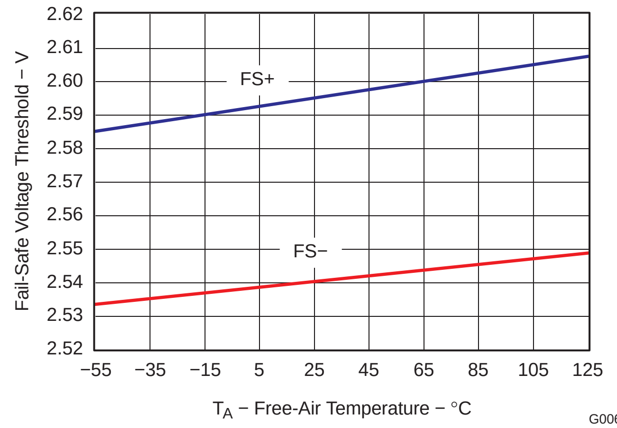


Figure 8.

HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE

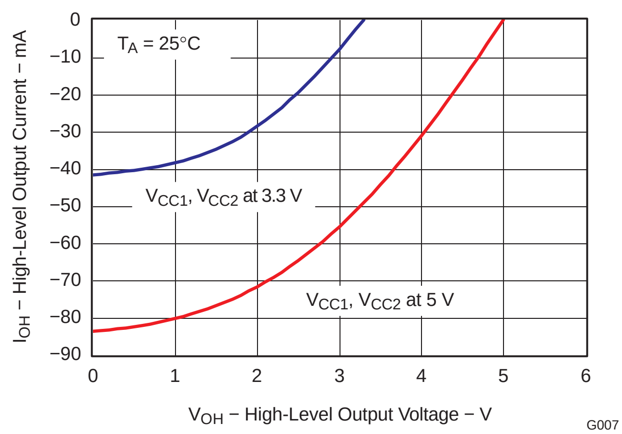


Figure 9.

LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE

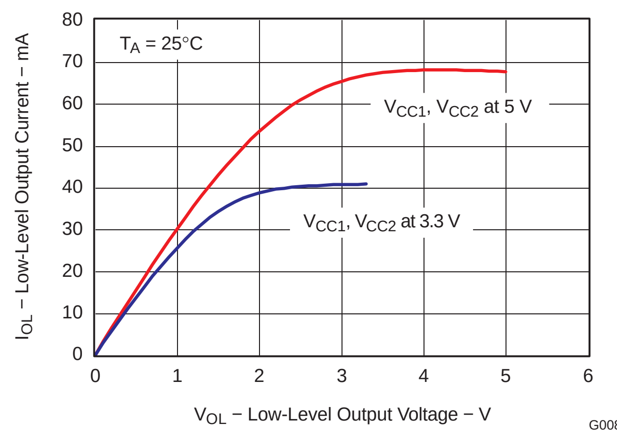


Figure 10.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
ISO7520CDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Purchase Samples
ISO7520CDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Purchase Samples
ISO7521CDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Purchase Samples
ISO7521CDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Purchase Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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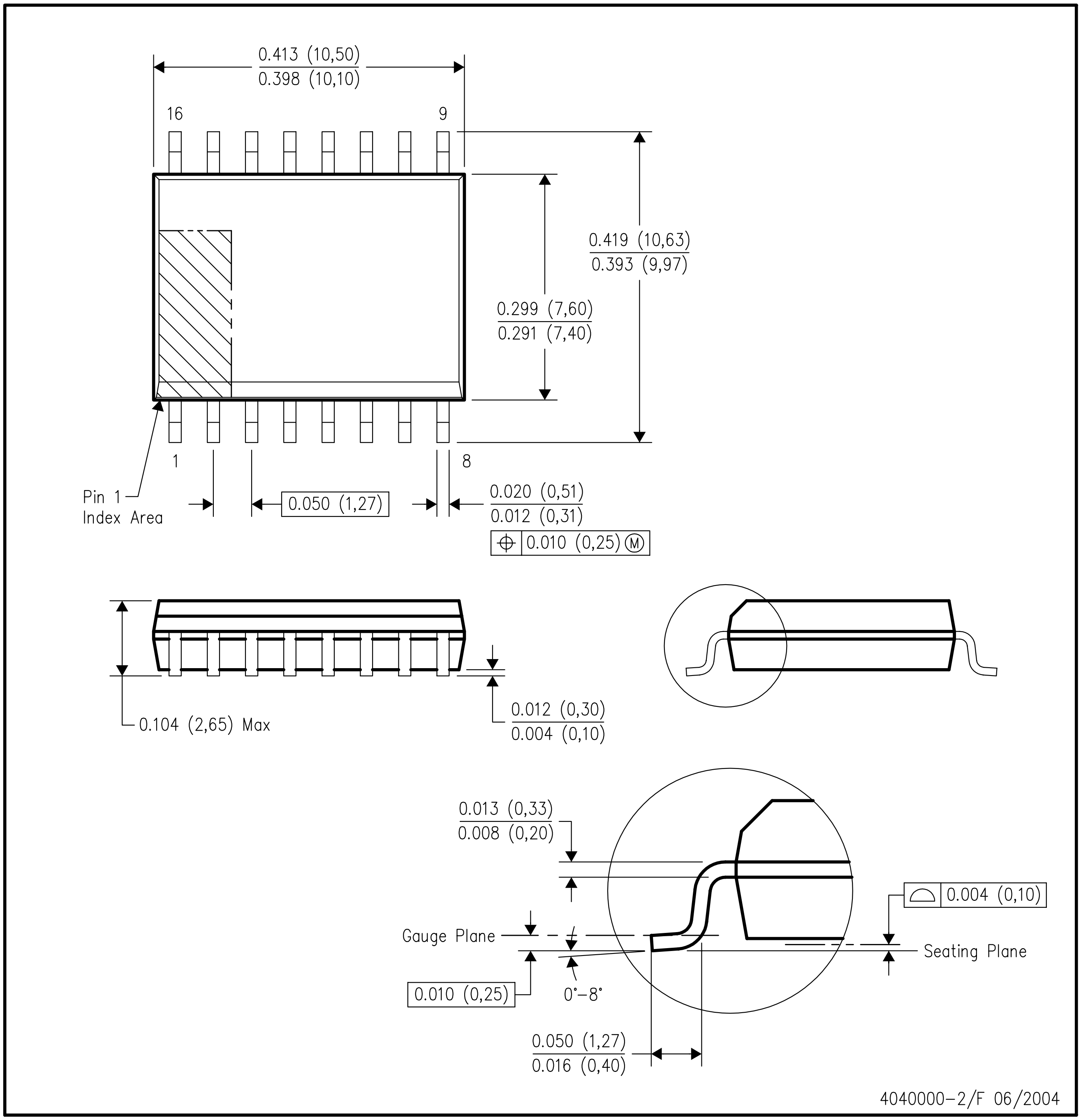
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

DW (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AA.

IMPORTANT NOTICE