

## 40V N-Channel NexFET™ Power MOSFETs

 Check for Samples: [CSD18504Q5A](#)

### FEATURES

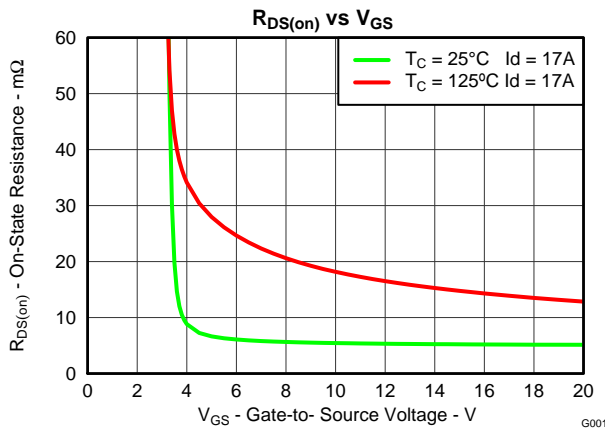
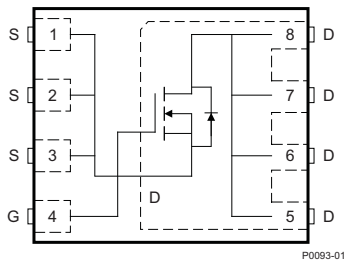
- Ultra Low Qg and Qgd
- Low Thermal Resistance
- Avalanche Rated
- Logic Level
- Pb Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 5-mm x 6-mm Plastic Package

### APPLICATIONS

- DC-DC Conversion
- Secondary Side Synchronous Rectifier
- Battery Motor Control

### DESCRIPTION

The NexFET™ power MOSFET has been designed to minimize losses in power conversion applications.

**Figure 1. Top View**


### PRODUCT SUMMARY

Typical Values at 25°C unless otherwise stated		TYPICAL VALUE		UNIT
V <sub>DS</sub>	Drain to Source Voltage	40		V
Q <sub>g</sub>	Gate Charge Total (4.5V)	7.7		nC
Q <sub>gd</sub>	Gate Charge Gate to Drain	2.4		nC
R <sub>DS(on)</sub>	Drain to Source On Resistance	V <sub>GS</sub> = 4.5V	7.5	mΩ
		V <sub>GS</sub> = 10V	5.3	mΩ
V <sub>GS(th)</sub>	Threshold Voltage	1.9		V

### ORDERING INFORMATION

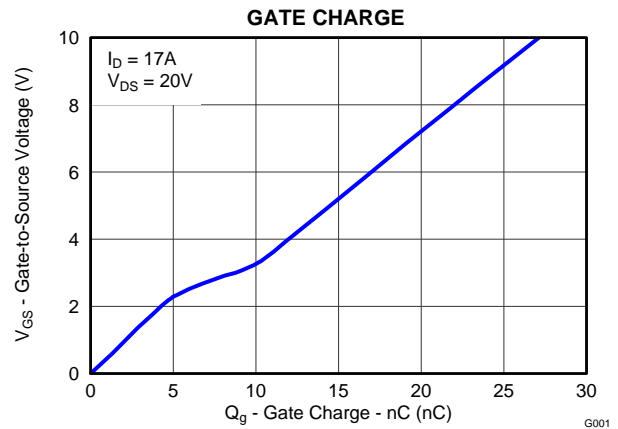
Device	Package	Media	Qty	Ship
CSD18504Q5A	SON 5-mm x 6-mm Plastic Package	13-Inch Reel	2500	Tape and Reel

### ABSOLUTE MAXIMUM RATINGS

T <sub>A</sub> = 25°C unless otherwise stated		VALUE	UNIT
V <sub>DS</sub>	Drain to Source Voltage	40	V
V <sub>GS</sub>	Gate to Source Voltage	±20	V
I <sub>D</sub>	Continuous Drain Current (Package limited), T <sub>C</sub> = 25°C	50	A
	Continuous Drain Current (Silicon limited), T <sub>C</sub> = 25°C	75	
	Continuous Drain Current, T <sub>A</sub> = 25°C <sup>(1)</sup>	15	
I <sub>DM</sub>	Pulsed Drain Current, T <sub>A</sub> = 25°C <sup>(2)</sup>	95	A
P <sub>D</sub>	Power Dissipation <sup>(1)</sup>	3.1	W
T <sub>J</sub> , T <sub>STG</sub>	Operating Junction and Storage Temperature Range	-55 to 150	°C
E <sub>AS</sub>	Avalanche Energy, single pulse I <sub>D</sub> = 43A, L = 0.1mH, R <sub>G</sub> = 25Ω	92	mJ

(1) Typical R<sub>θJA</sub> = 41°C/W on a 1-inch<sup>2</sup>, 2-oz. Cu pad on a 0.06-inch thick FR4 PCB.

(2) Pulse duration ≤300μs, duty cycle ≤2%



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ELECTRICAL CHARACTERISTICS

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

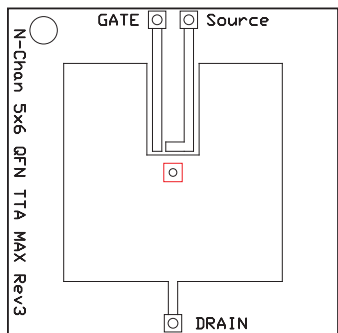
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Static Characteristics</b>						
$BV_{DSS}$	Drain to Source Voltage	$V_{GS} = 0V, I_D = 250\mu A$	40			V
$I_{DSS}$	Drain to Source Leakage Current	$V_{GS} = 0V, V_{DS} = 32V$			1	$\mu A$
$I_{GSS}$	Gate to Source Leakage Current	$V_{DS} = 0V, V_{GS} = 20V$			100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	1.5	1.9	2.4	V
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 4.5V, I_D = 17A$		7.5	9.8	m $\Omega$
		$V_{GS} = 10V, I_D = 17A$		5.3	6.6	m $\Omega$
$g_{fs}$	Transconductance	$V_{DS} = 20V, I_D = 17A$		63		S
<b>Dynamic Characteristics</b>						
$C_{iss}$	Input Capacitance	$V_{GS} = 0V, V_{DS} = 20V, f = 1MHz$		1380	1656	pF
$C_{oss}$	Output Capacitance			310	372	pF
$C_{riss}$	Reverse Transfer Capacitance			8	9.6	pF
$R_G$	Series Gate Resistance			1.4	2.8	$\Omega$
$Q_g$	Gate Charge Total (4.5V)	$V_{DS} = 20V, I_D = 17A$		7.7	9.2	nC
$Q_g$	Gate Charge Total (10V)			16	19	
$Q_{gd}$	Gate Charge Gate to Drain			2.4		nC
$Q_{gs}$	Gate Charge Gate to Source			3.2		nC
$Q_{g(th)}$	Gate Charge at $V_{th}$			2.2		nC
$Q_{oss}$	Output Charge		$V_{DS} = 20V, V_{GS} = 0V$		21	
$t_{d(on)}$	Turn On Delay Time	$V_{DS} = 20V, V_{GS} = 10V,$ $I_{DS} = 17A, R_G = 2\Omega$		3.2		ns
$t_r$	Rise Time			6.8		ns
$t_{d(off)}$	Turn Off Delay Time			12		ns
$t_f$	Fall Time			2		ns
<b>Diode Characteristics</b>						
$V_{SD}$	Diode Forward Voltage	$I_{SD} = 17A, V_{GS} = 0V$		0.8	1	V
$Q_{rr}$	Reverse Recovery Charge	$V_{DS} = 20V, I_F = 17A,$ $di/dt = 300A/\mu s$		18		nC
$t_{rr}$	Reverse Recovery Time			28		ns

## THERMAL CHARACTERISTICS

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

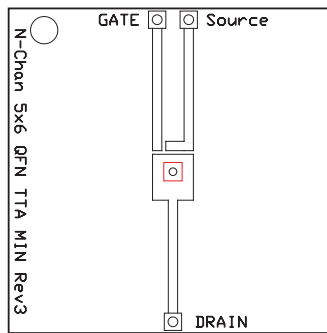
PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal Resistance Junction to Case <sup>(1)</sup>			2	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient <sup>(1)(2)</sup>			51	$^\circ\text{C/W}$

- (1)  $R_{\theta JC}$  is determined with the device mounted on a 1-inch<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch x 1.5-inch (3.81-cm x 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB.  $R_{\theta JC}$  is specified by design, whereas  $R_{\theta JA}$  is determined by the user's board design.
- (2) Device mounted on FR4 material with 1-inch<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz. (0.071-mm thick) Cu.



M0137-01

Max  $R_{\theta JA} = 51^{\circ}\text{C/W}$   
when mounted on  
1 inch<sup>2</sup> (6.45 cm<sup>2</sup>) of 2-  
oz. (0.071-mm thick)  
Cu.



M0137-02

Max  $R_{\theta JA} = 126^{\circ}\text{C/W}$   
when mounted on a  
minimum pad area of  
2-oz. (0.071-mm thick)  
Cu.

### TYPICAL MOSFET CHARACTERISTICS

( $T_A = 25^{\circ}\text{C}$  unless otherwise stated)

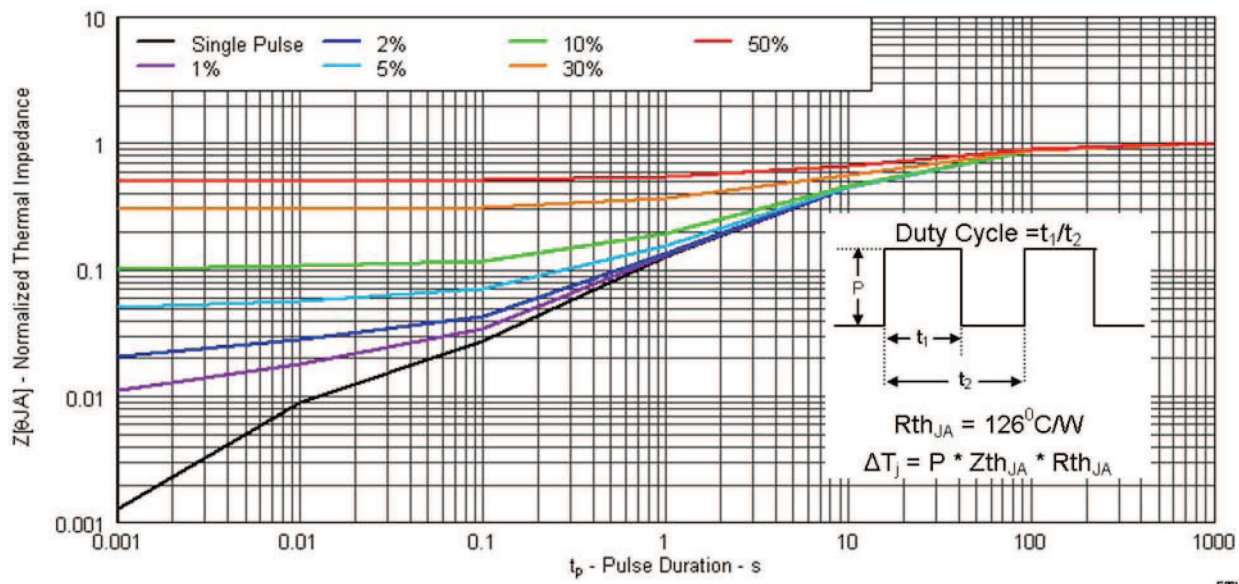
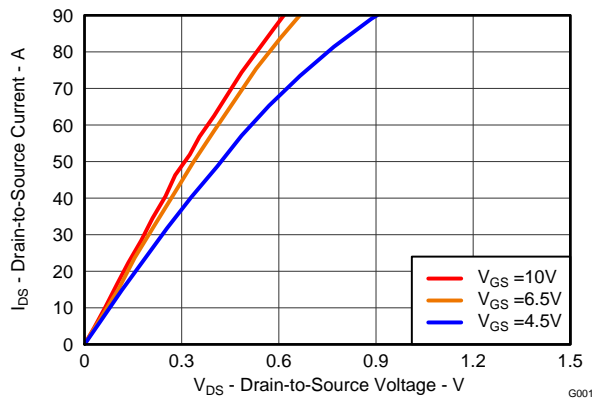


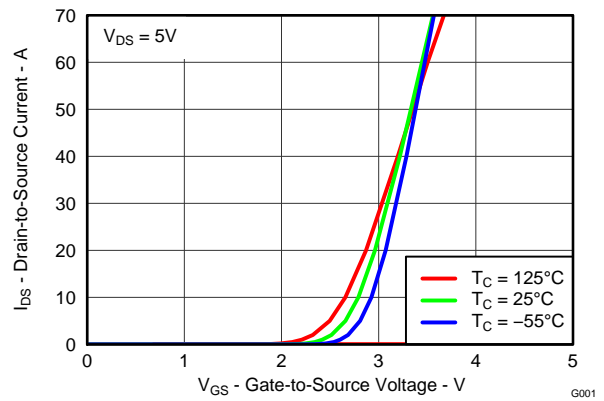
Figure 2. Transient Thermal Impedance

**TYPICAL MOSFET CHARACTERISTICS (continued)**

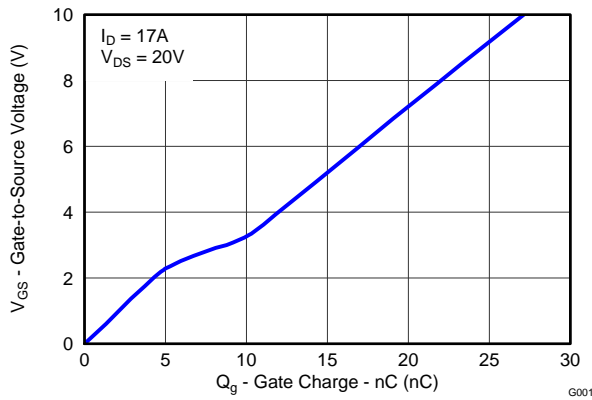
( $T_A = 25^\circ\text{C}$  unless otherwise stated)



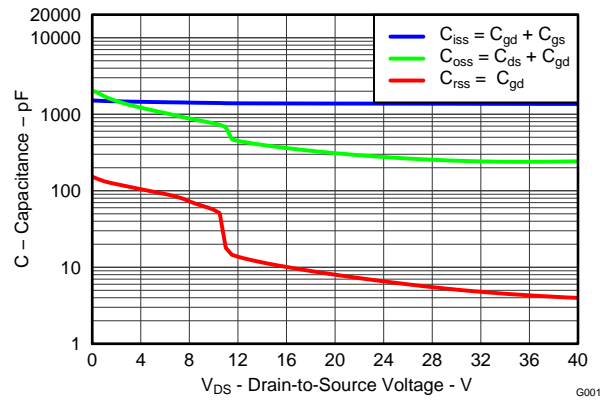
**Figure 3. Saturation Characteristics**



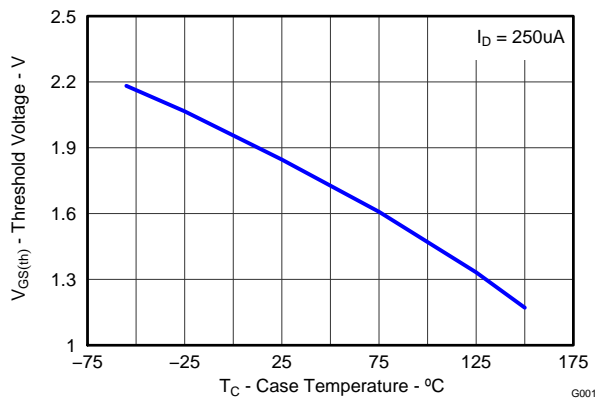
**Figure 4. Transfer Characteristics**



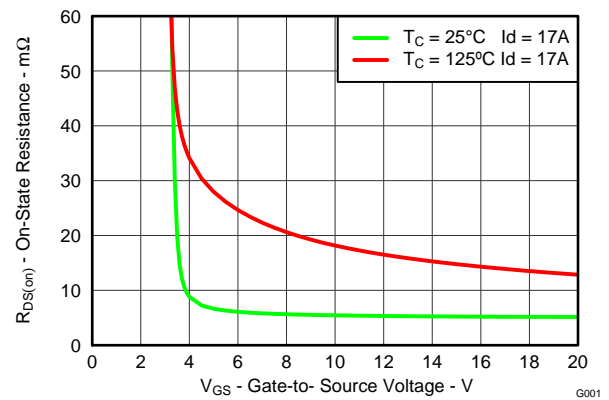
**Figure 5. Gate Charge**



**Figure 6. Capacitance**



**Figure 7. Threshold Voltage vs. Temperature**



**Figure 8. On-State Resistance vs. Gate-to-Source Voltage**

TYPICAL MOSFET CHARACTERISTICS (continued)

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

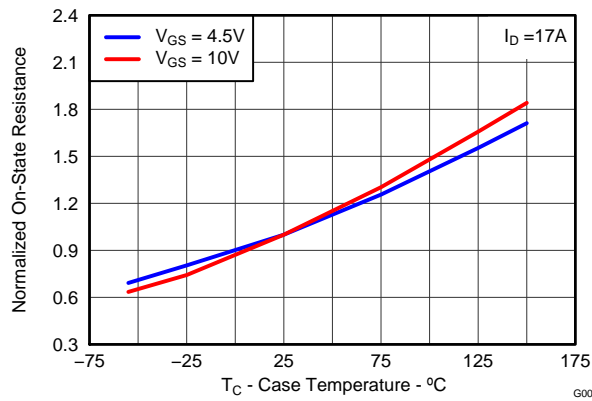


Figure 9. Normalized On-State Resistance vs. Temperature

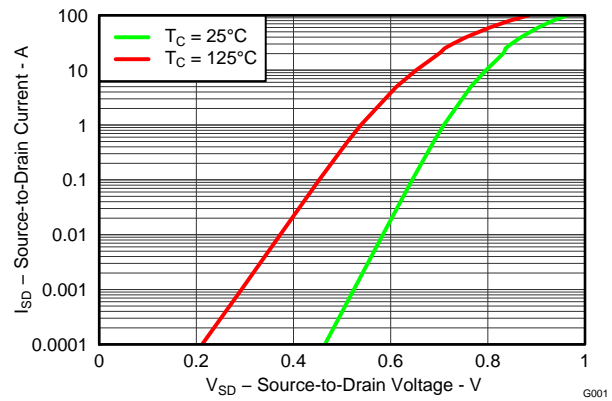


Figure 10. Typical Diode Forward Voltage

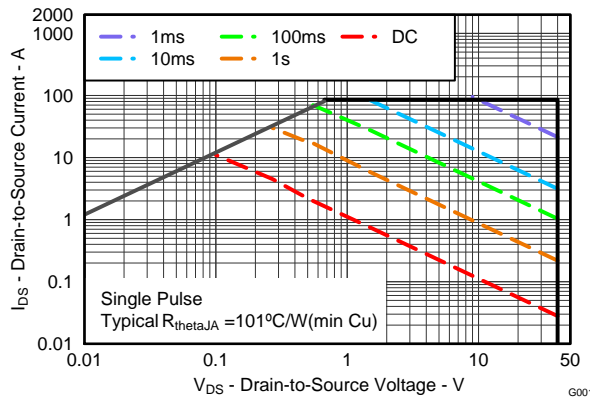


Figure 11. Maximum Safe Operating Area

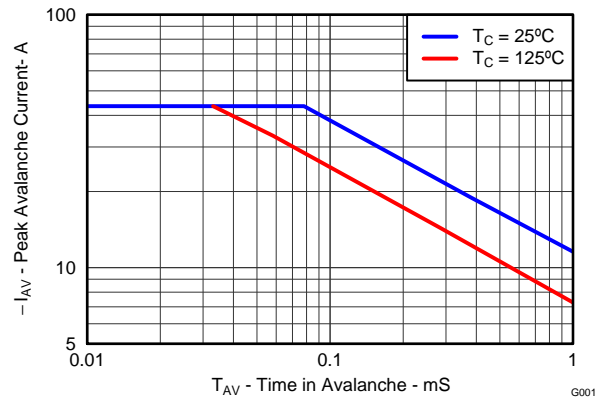


Figure 12. Single Pulse Unclamped Inductive Switching

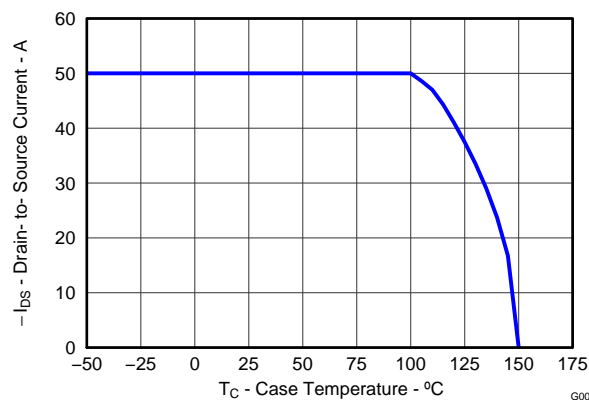
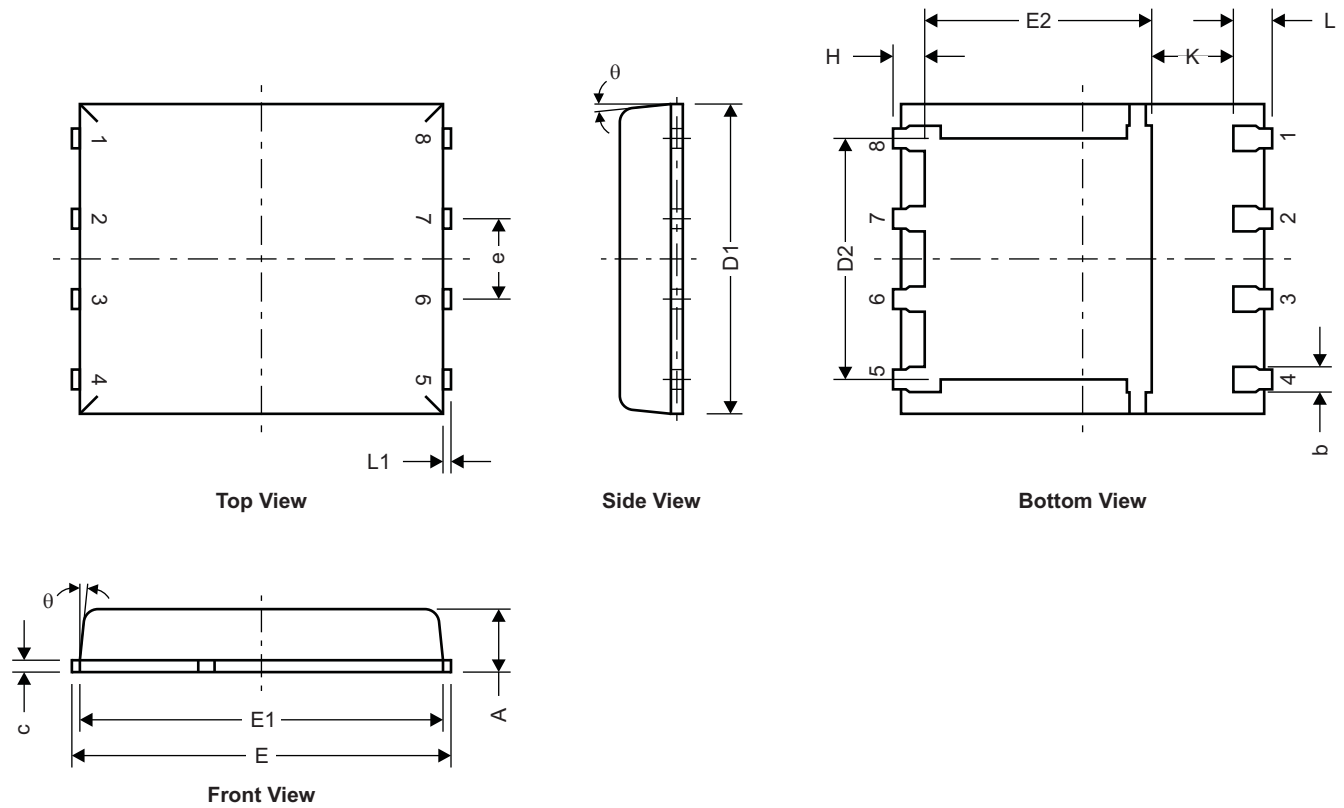


Figure 13. Maximum Drain Current vs. Temperature

**MECHANICAL DATA**

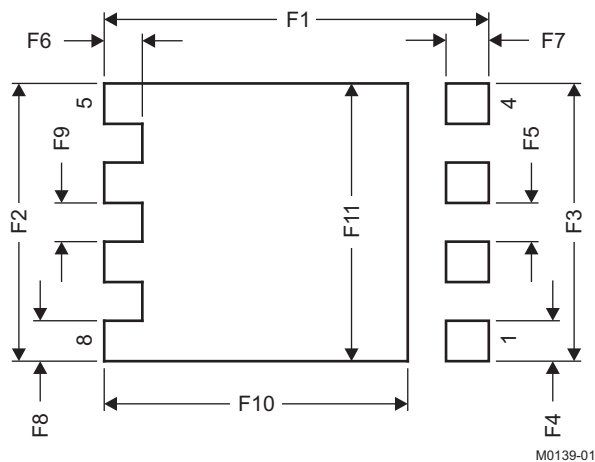
**Q5A Package Dimensions**



M0135-01

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
b	0.33	0.41	0.51
c	0.20	0.25	0.34
D1	4.80	4.90	5.00
D2	3.61	3.81	4.02
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
e	1.17	1.27	1.37
H	0.41	0.56	0.71
K	1.10		
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
$\theta$	0°		12°

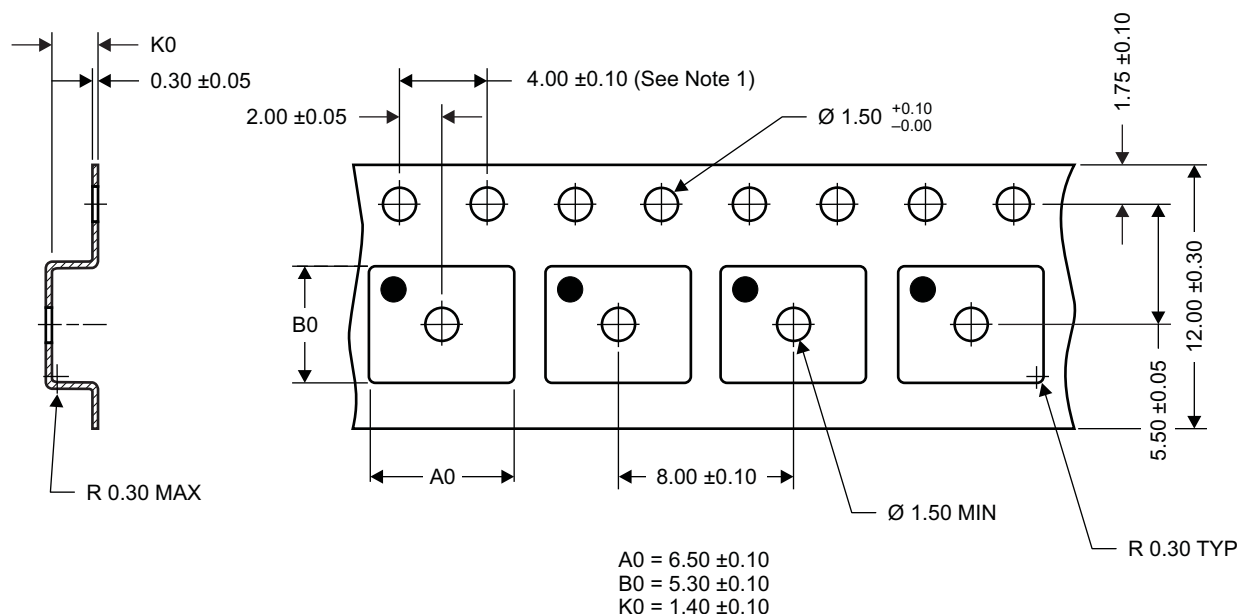
Figure 14. Recommended PCB Pattern



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
F1	6.205	6.305	0.244	0.248
F2	4.46	4.56	0.176	0.18
F3	4.46	4.56	0.176	0.18
F4	0.65	0.7	0.026	0.028
F5	0.62	0.67	0.024	0.026
F6	0.63	0.68	0.025	0.027
F7	0.7	0.8	0.028	0.031
F8	0.65	0.7	0.026	0.028
F9	0.62	0.67	0.024	0.026
F10	4.9	5	0.193	0.197
F11	4.46	4.56	0.176	0.18

For recommended circuit layout for PCB designs, see application note [SLPA005 – Reducing Ringing Through PCB Layout Techniques](#).

### Q5A Tape and Reel Information



M0138-01

### Notes:

- 10-sprocket hole-pitch cumulative tolerance  $\pm 0.2$
- Camber not to exceed 1mm in 100mm, noncumulative over 250mm
- Material: black static-dissipative polystyrene
- All dimensions are in mm (unless otherwise specified)
- A0 and B0 measured on a plane 0.3mm above the bottom of the pocket

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
CSD18504Q5A	ACTIVE	SON	DQJ	8	2500	Pb-Free (RoHS Exempt)	CU SN	Level-1-260C-UNLIM	

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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