

**1.54 inch  
E-paper Display Series**

**BLGDEW0154Z04FL**

## 1 General Description

### 1.1 Overview

The display is a TFT active matrix electrophoretic display, with interface and a reference system design. The 1.54" active area contains 200×200 pixels, and has 1-bit black/white and highlight red full display capabilities. An integrated circuit contains gate buffer, source buffer, interface, timing control logic, oscillator, DC-DC, SRAM, LUT, VCOM, and border are supplied with each panel.

### 1.2 Feature

High contrast  
High reflectance  
Ultra wide viewing angle  
Ultra low power consumption  
Pure reflective mode  
Bi-stable  
Commercial temperature range  
Landscape, portrait mode  
Antiglare hard-coated front-surface  
Low current deep sleep mode  
On chip display RAM  
Serial peripheral interface available  
On-chip oscillator  
On-chip booster and regulator control for generating VCOM, Gate and source driving voltage  
I2C Signal Master Interface to read external temperature sensor  
Available in COG package IC thickness 300um

### 1.3 Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	1.54	Inch	
Display Resolution	200(H)×200(V)	Pixel	Dpi: 184
Active Area	27.6(H)×27.6(V)	mm	
Pixel Pitch	0.138×0.138	mm	
Pixel Configuration	Square		
Outline Dimension	31.8(H)×37.3(V) ×1.05(D)	mm	
Weight	2.18±0.5	g	



## 1.5 Input/Output Terminals

### 1.5-1) Pin out List

Pin #	Type	Single	Description	Remark
1		NC	No connection and do not connect with other NC pins	Keep Open
2	O	GDR	N-Channel MOSFET Gate Drive Control	
3	O	RESE	Current Sense Input for the Control Loop	
4	C	VGL	Negative Gate driving voltage	
5	C	VGH	Positive Gate driving voltage	
6	O	TSCL	I <sup>2</sup> C Interface to digital temperature sensor Clock pin	
7	I/O	TSDA	I <sup>2</sup> C Interface to digital temperature sensor Date pin	
8	I	BS1	Bus selection pin	Note 1-5
9	O	BUSY	Busy state output pin	Note 1-4
10	I	RES #	Reset	Note 1-3
11	I	D/C #	Data /Command control pin	Note 1-2
12	I	CS #	Chip Select input pin	Note 1-1
13	I/O	D0	serial clock pin (SPI)	
14	I/O	D1	serial data pin (SPI)	
15	I	VDDIO	Power for interface logic pins	
16	I	VCI	Power Supply pin for the chip	
17		VSS	Ground	
18	C	VDD	Core logic power pin	
19		NC	No connection and do not connect with other NC pins	Keep Open
20	C	VSH	Positive Source driving voltage	
21	C	PREVGH	Power Supply pin for VGH and VSH	
22	C	VSL	Negative Source driving voltage	
23	C	PREVGL	Power Supply pin for VCOM, VGL and VSL	
24	C	VCOM	VCOM driving voltage	

Note 1-1: This pin (CS#) is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled Low.

Note 1-2: This pin (D/C#) is Data/Command control pin connecting to the MCU.

When the pin is pulled HIGH, the data will be interpreted as data. When the pin is pulled Low, the data will be interpreted as command.

Note 1-3: This pin (RES#) is reset signal input. The Reset is active Low.

Note 1-4: This pin (BUSY) is Busy state output pin. When Busy is Low, the operation of chip should not be interrupted and any commands should not be issued to the module. The driver IC will put Busy pin Low when the driver IC is working such as:

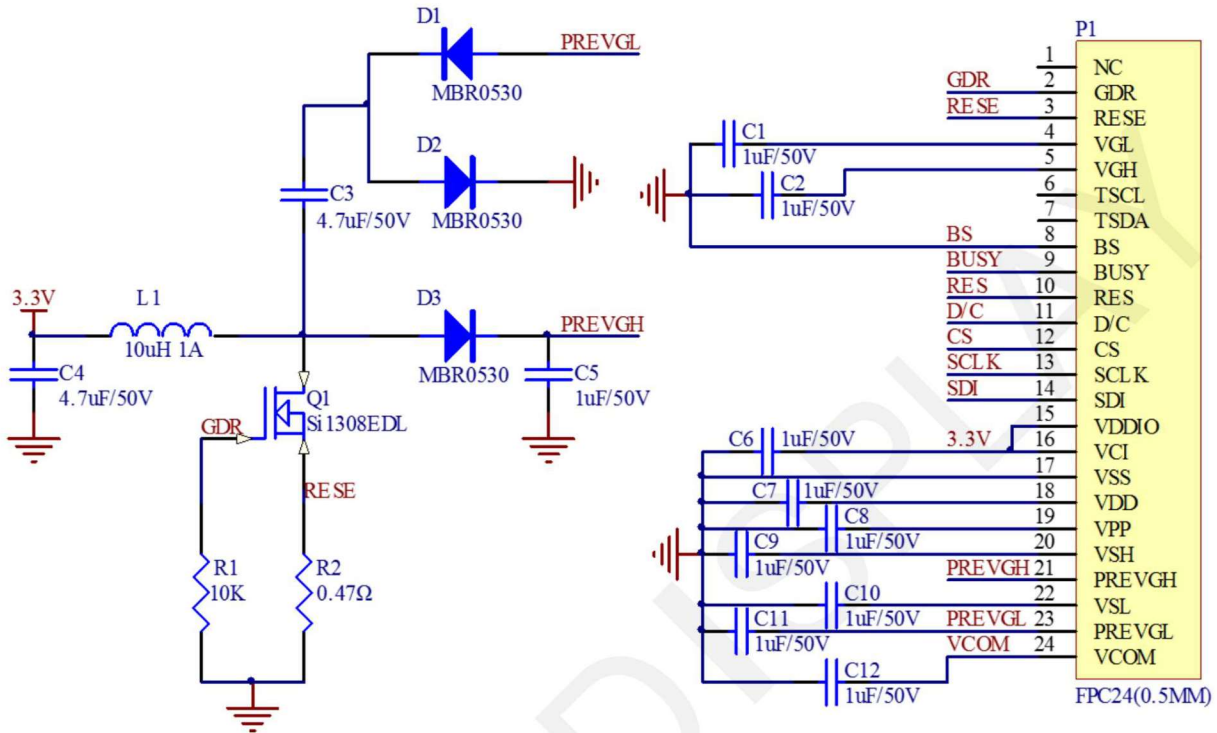
- Outputting display waveform; or
- Communicating with digital temperature sensor

Note 1-5: This pin (BS1) is for 3-line SPI or 4-line SPI selection. When it is "Low", 4-line SPI is selected. When it is "High", 3-line SPI (9 bits SPI) is selected. Please refer to below Table.

**Table: Bus interface selection**

<b>BS1</b>	<b>MPU Interface</b>
L	4-lines serial peripheral interface(SPI)
H	3-lines serial peripheral interface(SPI) – 9 bits SPI

## 1.6 Reference Circuit



### Note :

1. Inductor L1 is wire-wound inductor. There are no special requirements for other parameters.
2. Suggests using Si1304BDL or Si1308EDL TUBE MOS (Q1) , otherwise it may affect the normal boost of the circuit.
3. The default circuit is 4-wire SPI. If the user wants to use 3-wire SPI, the resistor R4 can be removed when users design.
4. Default voltage value of all capacitors is 50V.

## 2. Environmental

### 2.1 Handling, Safety and Environmental Requirements

<b>WARNING</b>
The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

<b>CAUTION</b>
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
Disassembling the display module can cause permanent damage and invalidate the warranty agreements.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

<b>Data sheet status</b>	
Product specification	The data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

<b>Product Environmental certification</b>
RoHS

## 2.2 Reliability test

	TEST	CONDITION	METHOD	REMARK
1	High-Temperature Operation	T = 40°C, RH=30% for 240 hrs	IEC 60 068-2-2Bp	
2	Low-Temperature Operation	T = 0°C for 240 hrs	IEC 60 068-2-2Ab	
3	High-Temperature Storage	T = +60°C, RH=40% for 240 hrs Test in white pattern	IEC 60 068-2-2Bp	
4	Low-Temperature Storage	T = -25°C for 240 hrs Test in white pattern	IEC 60 068-2-2Ab	
5	High Temperature, High-Humidity Operation	T=+40°C, RH=90% for 240 hrs	IEC 60 068-2-3CA	
6	High Temperature, High-Humidity Storage	T=+50°C, RH=80% for 240 hrs Test in white pattern	IEC 60 068-2-3CA	
7	Temperature Cycle	[-25°C 30mins]→[+60°C 30mins], 50cycles Test in white pattern	IEC 60 068-2-14NB	
8	UV exposure Resistance	765 W/m <sup>2</sup> for 168 hrs, 40°C	IEC 60 068-2-5 Sa	
9	Electrostatic discharge	Machine Model: +/-200V 0 OHM 200PF	IEC61000-4-2	
10	Package Vibration	1.04G, Frequency : 10~500Hz Direction : X,Y,Z Duration: 1 hours in each direction	Full packed for shipment	
11	Package Drop Impact	Drop from height of 122 cm on Concrete surface Drop sequence: 1 corner, 3 edges, 6 face One drop for each.	Full packed for shipment	

Actual EMC level to be measured on customer application.

Note: The protective film must be removed before temperature test.



### 3. Electrical Characteristics

#### 3.1 Absolute maximum rating

Parameter	Symbol	Rating	Unit
Logic Supply Voltage	VCI	-0.5 to +3.6	V
Logic Input Voltage	VIN	-0.5 to VCI +0.5	V
Logic Output Voltage	VOUT	-0.5 to VCI +0.5	V
Operating Temp. range	TOPR	0 to +40	°C
Storage Temp. range	TSTG	-25 to +60	°C
Humidity range	-	40~70	%RH

**\*Note: Avoid direct sunlight.**

#### 3.2 Panel DC Characteristics

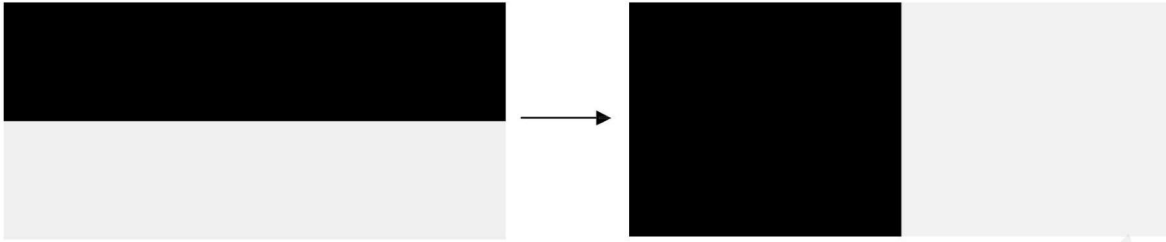
The following specifications apply for : VSS = 0V, VCI = 3.0V, TA = 25°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Single ground	VSS	-	-	0	-	V
Logic Supply Voltage	VCI	-	2.3	3.0	3.6	V
High level input voltage	VIH	-	0.8VCI	-	-	V
Low level input voltage	VIL	-	-	-	0.2VCI	V
High level output voltage	VOH	IOH= -100uA	0.9VCI	-	-	V
Low level output voltage	VOL	IOH= 100uA	-	-	0.1VCI	V
Image update current	I <sub>UPDATE</sub>	-	-	8	10	mA
Standby panel current	I <sub>standby</sub>	-	-	-	5	uA
Power panel (update)	P <sub>UPDATE</sub>	-	-	26.4	40	mW
Standby power panel	P <sub>STBY</sub>	-	-	-	0.0165	mW
Operating temperature	-	-	0	-	40	°C
Storage temperature	-	-	-25	-	60	°C
Image updateTime at 25°C	-	-	-	8	12	Sec
Sleep mode current	VCI	DC/DC off No clock No input load Ram data not retain	-	2	5	uA

- The Typical power consumption is measured with following pattern transition: from horizontal 2 gray scale pattern to vertical 2 gray scale pattern.(Note 3-1)
- The standby power is the consumed power when the panel controller is in standby mode.
- The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by Good Display
- Vcom is recommended to be set in the range of assigned value  $\pm 0.1V$ .

#### Note 3-1

The Typical power consumption



### 3.3 Panel AC Characteristics

#### 3.3-1) MCU Interface

##### 3.3-1-1) MCU Interface Selection

In this module, there are 4-wire SPI and 3-wire SPI that can communicate with MCU. The MCU interface mode can be set by hardware selection on BS1 pins. When it is “Low”, 4-wire SPI is selected. When it is “High”, 3-wire SPI (9 bits SPI) is selected.

Pin Name	Data/Command Interface		Control Signal		
Bus interface	D1	D0	CS#	D/C#	RES#
SPI4	SDin	SCLK	CS#	D/C#	RES#
SPI3	SDin	SCLK	CS#	L	RES#

**Table 3-1: MCU interface assignment under different bus interface mode**

**Note 3-2:** L is connected to VSS

**Note 3-3:** H is connected to VCI

##### 3.3-1-2) MCU Serial Interface (4-wire SPI)

The 4-wire SPI consists of serial clock SCLK, serial data SDIN, D/C#, CS#. In SPI mode, D0 acts as SCLK, D1 acts as SDIN.

Function	CS#	D/C#	SCLK
Write Command	L	L	↑
Write data	L	H	↑

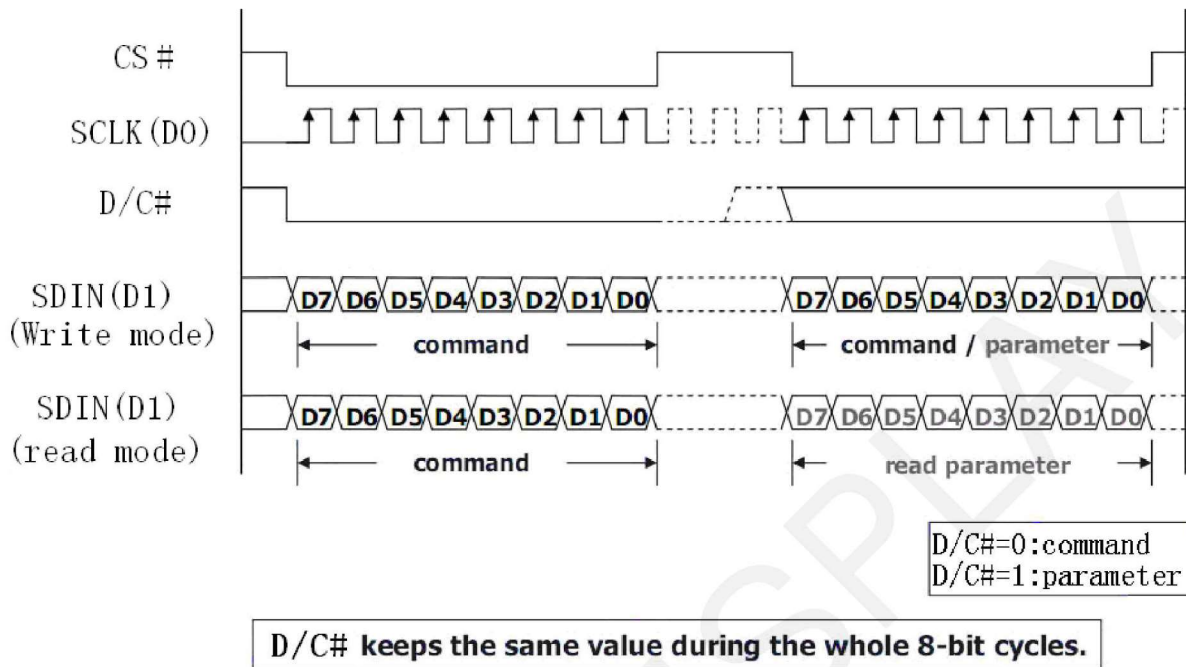
**Table 3-2: Control pins of 4-wire Serial Peripheral interface**

**Note 3-9:** ↑stands for rising edge of signal

SDIN is shifted into an 8-bit shift register in the order of D7, D6, ... D0. The data byte in the shift register is written to the Graphic Display Data RAM (RAM) or command register in the same clock.

Under serial mode, only write operations are allowed.

**Figure 3-1: Write procedure in 4-wire Serial Peripheral Interface mode**



### 3.3-1-3) MCU Serial Interface (3-wire SPI)

The 3-wire serial interface consists of serial clock SCLK, serial data SDIN and CS#.

In 3-wire SPI mode, D0 acts as SCLK, D1 acts as SDIN, The pin D/C# can be connected to an external ground.

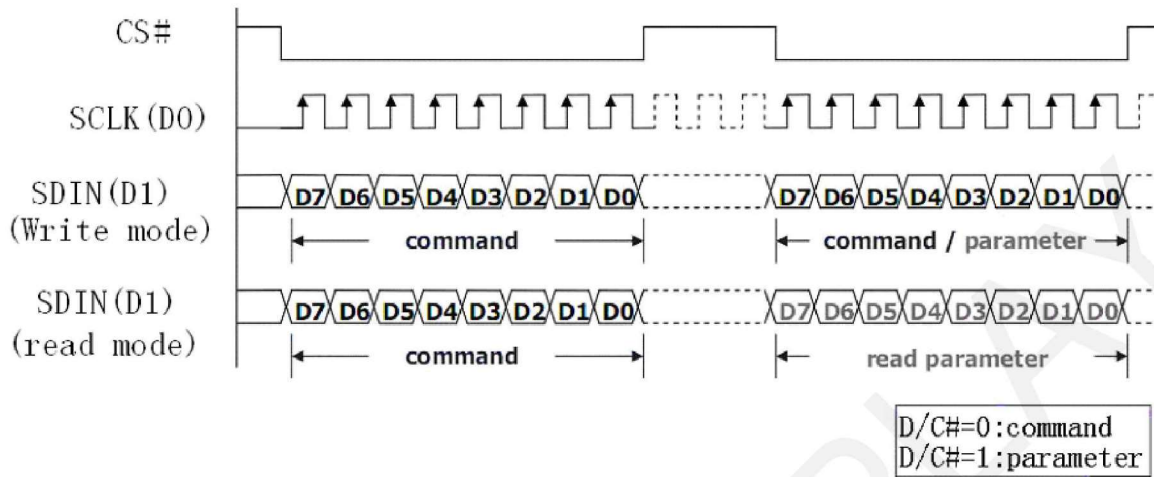
The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C# bit, D7 to D0 bit. The D/C# bit (first bit of the sequential data) will determine the following data byte in shift register is written to the Display Data RAM (D/C# bit= 1) or the command register (D/C# bit = 0). Under serial mode, only write operations are allowed.

Function	CS#	D/C#	SCLK
Write Command	L	Tie LOW	↑
Write data	L	Tie LOW	↑

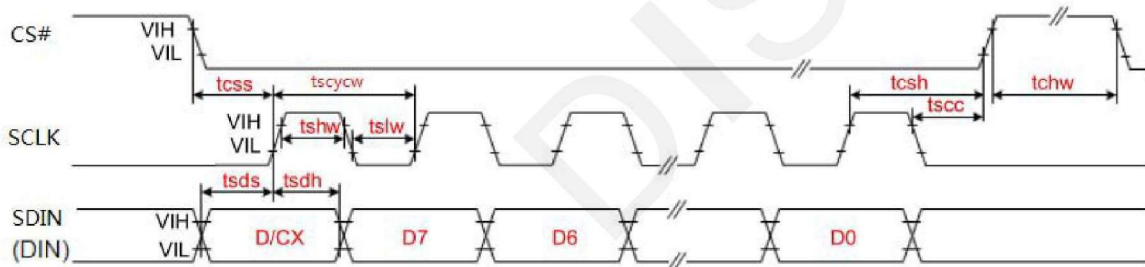
**Table 3-3: Control pins of 3-wire Serial Peripheral Interface**

**Note 3-10:** ↑stands for rising edge of signal

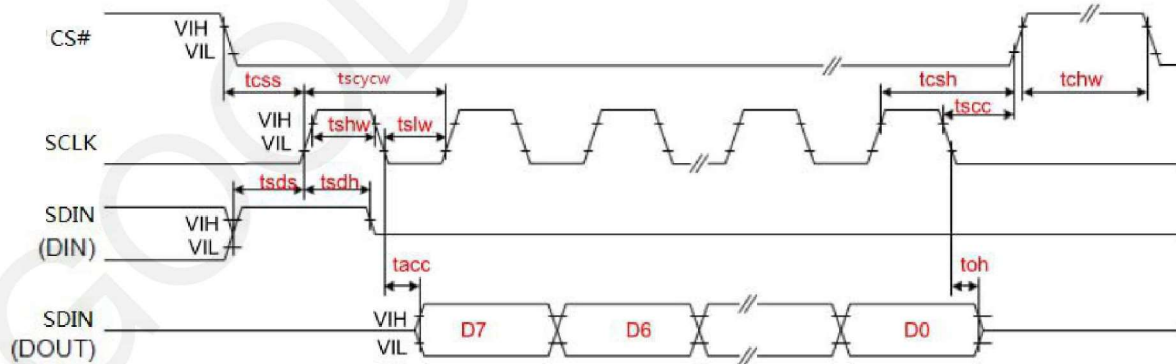
**Figure 3-2: Write procedure in 3-wire Serial Peripheral Interface mode**



**3.3-2) Timing Characteristics of Series Interface**



3-wire Serial Interface – Write



3-wire Serial Interface – Read

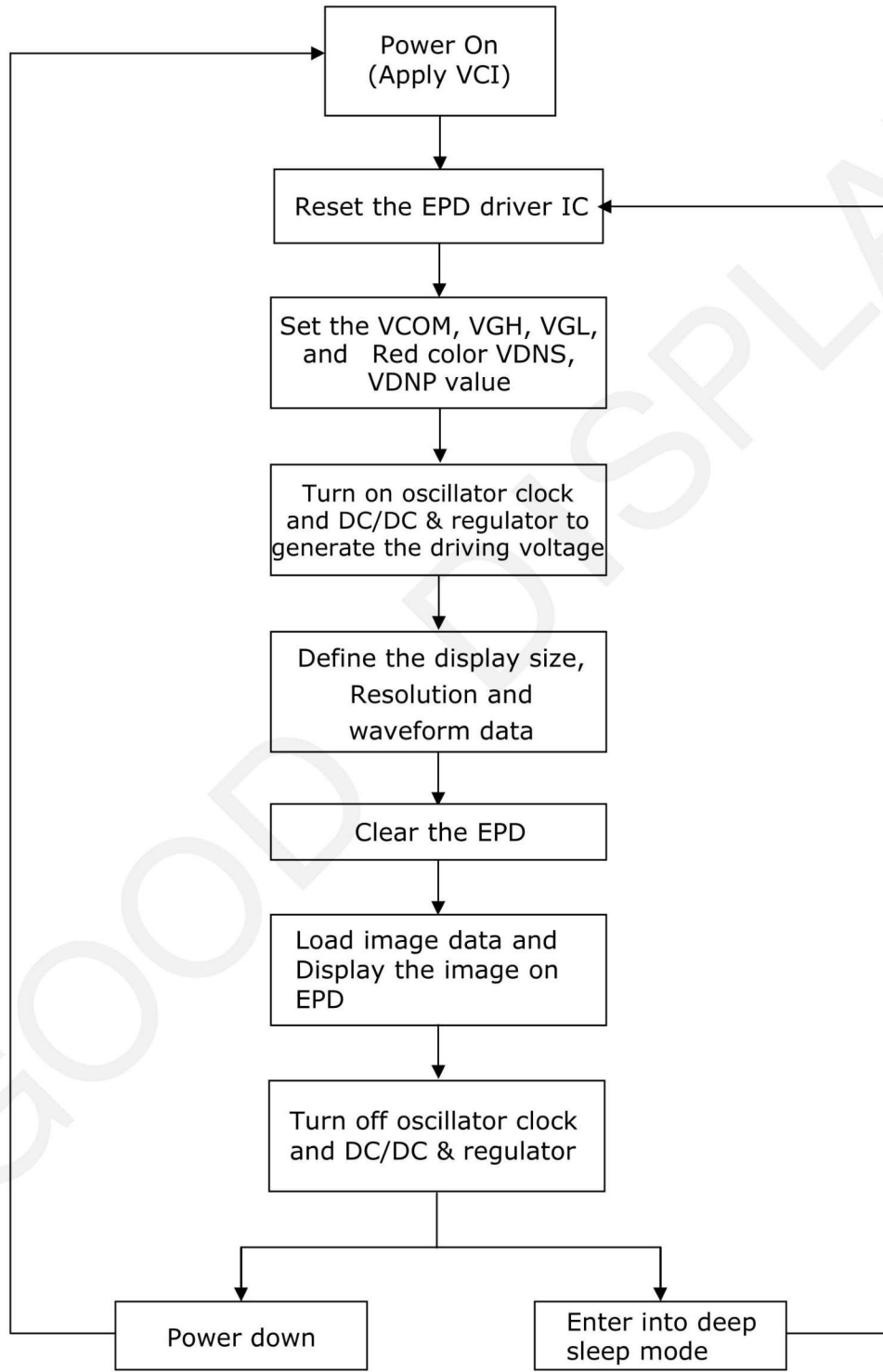
Symbol	Signal	Parameter	Min	Typ	Max	Unit
SERIAL COMMUNICATION						
tcss	CSB	Chip Select Setup Time	60	-	-	ns
tcsH		Chip Select Hold Time	65	-	-	ns
tscC		Chip Select Setup Time	20	-	-	ns
tchW		Chip Select Setup Time	40	-	-	ns
tscycW	SCL	Serial clock cycle (write)	100	-	-	ns
tshW		SCL "H" pulse width (write)	35	-	-	ns
tslW		SCL "L" pulse width (write)	35	-	-	ns
tscycR		Serial clock cycle (Read)	150	-	-	ns
tshR		SCL "H" pulse width (Read)	60	-	-	ns
tslR		SCL "L" pulse width (Read)	60	-	-	ns
tsds	SDIN (DIN) (DOUT)	Data setup time	30	-	-	ns
tsdh		Data hold time	30	-	-	ns
tacc		Access time	10	-	-	ns
toh		Output disable time	15	-	-	ns

### 3.4 Power Consumption

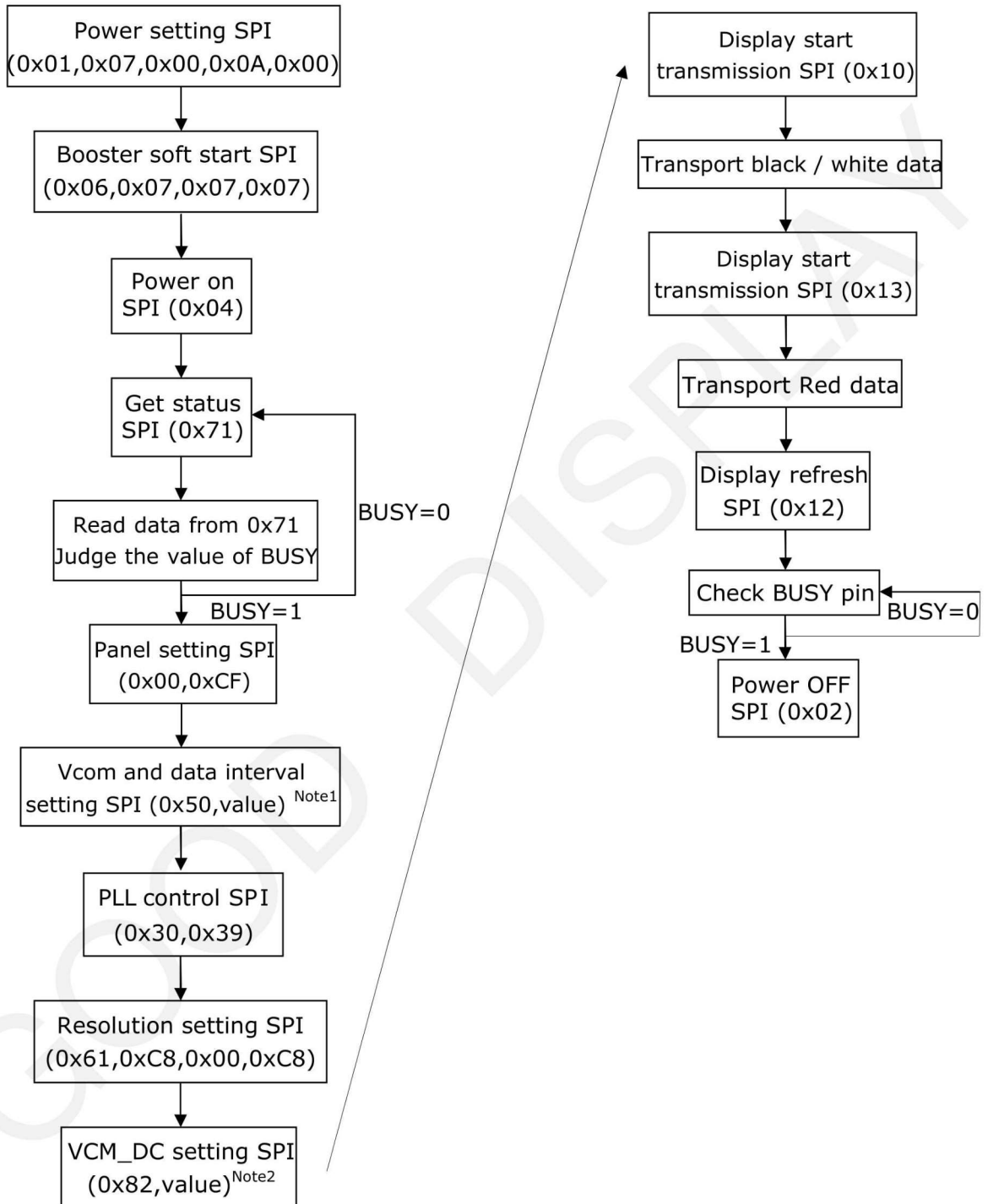
Parameter	Symbol	Condition	TYP	Max	Unit	Remark
Panel power consumption during update	-	25°C	26.4	40	mW	-
Power consumption in standby mode	-	25°C	-	0.0165	mW	-

## 4. Typical Operating Sequence

### 4.1 Normal Operation Flow



## 4.2 Reference Program Code



Note1: When value=0x57, border will be drive to black after refresh. When value=0x17, the border is set to floating.

Note2: Different EPD with different VCOM value, Good Display will provide different values according to different batches of EPD.

## 5. Waveform LUT control software

For every bunch of EPD the waveform data is different, so you may receive the waveform LUT from Good Display. You just need to use the follow sequence to download the waveform into driver IC.

sequence	command	Action Description	remark
1	04	Power on	Send cmd 04
2	20	VCOM LUT Setting	Send cmd 20data lut_vcom0[]
3	21	White LUT Setting	Send cmd 21data lut_w[]
4	22	Black LUT Setting	Send cmd 22data lut_b[]
5	25	RED VCOM LUT Setting	Send cmd 25data lut_vcom1[]
6	26	RED0 LUT Setting	Send cmd 26data lut_red0[]
7	27	RED1 LUT Setting	Send cmd 27data lut_red1[]

Note: To download the waveform into driver ic, you must send command 04 first, then send 20, 21, 22, 25, 26, 27 command.

The data of lut\_vcom0[],lut\_w[],lut\_b[],lut\_vcom1[],lut\_red0[],lut\_red1[],each batch of EPD is different. Good Display will support the data after you receive the EPD.



## 6. Command Table

Code	Inst/Para	R/W	DC	D7	D6	D5	D4	D3	D2	D1	D0	Default
R01H	<b>PWR</b>	W	0	0	0	0	0	0	0	0	0	(01H)
	1 <sup>st</sup> Para	W	1	-	-	-	-	-	-	VDS_EN	VDG_EN	03H
	2 <sup>nd</sup> Para	W	1	-	-	-	-	-	-	0	0	00H
	3 <sup>rd</sup> Para	W	1				VDPS_L V4	VDPS_ LV3	VDPS_L V2	VDPS_ LV1	VDPS_ V0	08H
4 <sup>nd</sup> Para	W	1				VDNS_L V4	VDNS_ LV3	VDNS_L LV2	VDNS_ LV1	VDNS_ LV0	08H	
R02H	<b>POF</b>	W	0	0	0	0	0	0	0	1	0	(02H)
R04H	<b>PON</b>	W	0	0	0	0	0	0	1	0	0	(04H)
R06H	<b>BTST</b>	W	0	1	1	1	0	0	0	1	0	(E2H)
	1 <sup>st</sup> Para	W	1	-	0	0	BT_PH A4	BT_P HA3	1	1	1	0FH
	2 <sup>nd</sup> Para	W	1	-	0	0	BT_PH B4	BT_P HB3	1	1	0	0EH
3 <sup>rd</sup> Para	W	1	-	-	-	BT_PHC 4	BT_P HC3	1	0	1	0DH	
R10H	<b>DTM1</b>	W	0	0	0	1	0	0	0	0	0	(10H)
	1 <sup>st</sup> Para	W	1	KPxI1 [0]	KPxI2[ 1]	KPxI2 [0]	KPxI3[ 1]	KPxI3 [0]	KPxI4[ 1]	KPxI4 [0]	KPxI1[ 1]	00H
	.....	W	1									00H
M <sup>th</sup> Para	W	1	KPxI(N -1)[1]	KPxI(N- 1)[0]	KPxIN [1]	KPxIN[0]						00H
R12H	<b>DRF</b>	W	0	0	0	0	1	0	0	1	0	(12H)
R13H	<b>DTM2</b>	W	0	0	0	1	0	0	0	1	1	(13H)
	1 <sup>st</sup> Para	W	1	PRxI1	PRxI2	PRxI3	PRxI4	PRxI5	PRxI6	PRxI7	PRxI8	00H
	.....	W	1									00H
M <sup>th</sup> Para	W	1	PRxI(N -1)	PRxIN							00H	

Code	Inst/Para	R/W	DC	D7	D6	D5	D4	D3	D2	D1	D0	Default
R30H	<b>PLL</b>	W	0	0	0	1	1	0	0	0	0	(30H)
	1 <sup>st</sup> Para	W	0	-	-	M2	M1	M0	N2	N1	N0	3CH
R40H	<b>TSC</b>	W	0	0	1	0	0	0	0	0	0	(40H)
	1 <sup>st</sup> Para	R	1	D10	D9	D8	D7	D6/TS3	D5/TS2	D4/TS1	D3/TS0	00H
R41H	2 <sup>nd</sup> Para	R	1	D2	D1	D0	-	-	-	-	-	00H
	<b>TSE</b>	W	0	0	1	0	0	0	0	0	1	(41H)
	1 <sup>st</sup> Para	W	1	TSE	-	-	-	-	-	-	-	00H
R42H	<b>TSW</b>	W	0	0	1	0	0	0	0	1	0	(42H)
	1 <sup>st</sup> Para	W	1	WATTR7	WATTR6	WATTR5	WATTR4	WATTR3	WATTR2	WATTR1	WATTR0	00H
	2 <sup>nd</sup> Para	W	1	WMSB7	WMSB6	WMSB5	WMSB4	WMSB3	WMSB2	WMSB1	WMSB0	00H
	3 <sup>rd</sup> Para	W	1	WLSB7	WLSB6	WLSB5	WLSB4	WLSB3	WLSB2	WLSB1	WLSB0	00H
R43H	<b>TSR</b>	W	0	0	1	0	0	0	0	1	1	(43H)
	1 <sup>st</sup> Para	R	1	RMSB7	RMSB6	RMSB5	RMSB4	RMSB3	RMSB2	RMSB1	RMSB0	00H
	2 <sup>nd</sup> Para	R	1	RLSB7	RLSB6	RLSB5	RLSB4	RLSB3	RLSB2	RLSB1	RLSB0	00H
R50H	<b>CDI</b>	W	0	0	1	0	1	0	0	0	0	(50H)
	1 <sup>st</sup> Para	W	1	-	-	-	DDX	CDI3	CDI2	CDI1	CDI0	17H
R61H	<b>TRES</b>	W	0	0	1	1	0	0	0	0	1	(61H)
	1 <sup>st</sup> Para	W	1	HRES7	HRES6	HRES5	HRES4	HRES3	HRES2	HRES1	0	00H
	2 <sup>nd</sup> Para	W	1	-	-	-	-	-	-	-	HRES8	00H
	3 <sup>rd</sup> Para	W	1	VRES7	VRES6	VRES5	VRES4	VRES3	VRES2	VRES1	VRES0	00H
R82H	<b>VDCS</b>	W	0	1	0	0	0	0	0	1	0	(82H)
	1 <sup>st</sup> Para	W	1	-	-	VDCS5	VDCS4	VDCS3	VDCS2	VDCS1	VDCS0	00H

### Power Setting Register

Code	Inst/Para	R/W	DC	D7	D6	D5	D4	D3	D2	D1	D0	Default
R01H	<b>PWR</b>	W	0	0	0	0	0	0	0	0	0	(01H)
	1 <sup>st</sup> Para	W	1	-	-	-	-	-	-	<b>VDS_EN</b>	<b>VDG_EN</b>	03H
	2 <sup>nd</sup> Para	W	1	-	-	-	-	-	-	0	0	00H
	3 <sup>rd</sup> Para	W	1	-	-	-	<b>VDPS_L V4</b>	<b>VDPS_L V3</b>	<b>VDPS_L V2</b>	<b>VDPS_L V1</b>	<b>VDPS_L V0</b>	08H
4 <sup>th</sup> Para	W	1	-	-	-	<b>VDNS_L LV4</b>	<b>VDNS_L V3</b>	<b>VDNS_L V2</b>	<b>VDNS_L V1</b>	<b>VDNS_L V0</b>	08H	

Name	Control	Value	Function Description
VDS_EN	Source Power Selection	0	External positive source voltage from VDH pin and negative source voltage from VDL pin
		1	Internal voltage generation circuit for both VDH/VDL
VDG_EN	Gate Power Selection	0	External positive source voltage from VDH pin and negative source voltage from VDL pin
		1	Internal voltage generation circuit for both VDH/VDL
VDPS_LV[4:0]	Source Voltage-Level(Red)	-	Internal positive source voltage level for red LUT (range: 2.4V ~ 8.0V / step:0.2V)
VDNS_LV[4:0]	Source Voltage-Level(Red)	-	Internal negative source voltage level for red LUT (range: -2.4V ~ -8.0V / step:0.2V)

Note: For this panel the 2<sup>nd</sup> Para must set as 0x00.

### Power OFF

Code	Inst/Para	R/W	DC	D7	D6	D5	D4	D3	D2	D1	D0	Default
R02H	<b>POF</b>	W	0	0	0	0	0	0	0	1	0	(02H)

After the Power Off command, driver will power off based on the power off Sequence, BUSY will become "0". This command will turn off charge pump, T-con, source driver, gate driver, VCOM, and temperature sensor, but register data will be kept until VDD becomes OFF.

SD output and Vcom will base on previous condition. It may have 2 conditions: 0V or floating. This command can be active only when BUSY = "1".

### Power ON / Setting

Code	Inst/Para	R/W	DC	D7	D6	D5	D4	D3	D2	D1	D0	Default
R04H	<b>PON</b>	W	0	0	0	0	0	0	1	0	0	(04H)
R06H	<b>BTST</b>	W	0	1	1	1	0	0	0	1	0	(06H)
	1 <sup>st</sup> Para	W	1	-	0	0	<b>BT_PHA4</b>	<b>BT_PHA3</b>	1	1	1	0FH
	2 <sup>nd</sup> Para	W	1	-	0	0	<b>BT_PHB4</b>	<b>BT_PHB3</b>	1	1	0	0EH
	3 <sup>rd</sup> Para	W	1	-	-	-	<b>BT_PHC4</b>	<b>BT_PHC3</b>	1	0	1	0DH

Name	Control	Value	Description
BT_PHA[4:3] BT_PHB[4:3] BT_PHC[4:3]	Driving Strength	00	1
		01	2
		10	3
		11	4

NOTE: For this panel, You 'd better to set these bits's ( BT\_PHA \BT\_PHB\BT\_PHC) value to 00.

### Data Start Transmission 1 / Data Stop Command (B/W)

Code	Inst/Para	R/W	DC	D7	D6	D5	D4	D3	D2	D1	D0	Default
R10H	<b>DTM1</b>	W	0	0	0	1	0	0	0	0	0	(10H)
	1 <sup>st</sup> Para	W	1	KPixel1[1:0]		KPixel2[1:0]		KPixel3[1:0]		KPixel4[1:0]		00H
		W	1	...		...		...		...		00H
	M <sup>th</sup> Para	W	1	KPixel(n-1)[1:0]		KPixel(n)[1:0]		-	-	-	-	00H

This Command starts transmitting data and write them into SRAM. To complete data transmission, command DSP(Data transmission Stop) must be issued. Then the chip will start to send data/VCOM for panel.

	KPixel(x)[1:0]	LUT
When DDX=0	00	White
	11	Black
When DDX=1	00	Black
	11	White

This command can be active only when BUSY = "1".

### Data Refresh Command

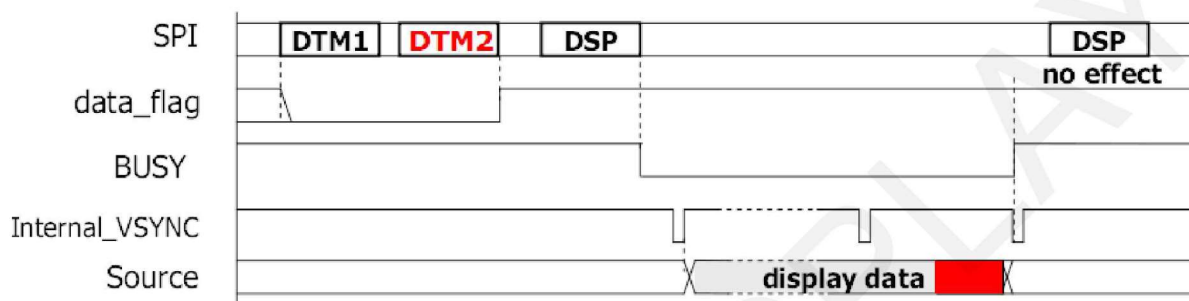
Code	Inst/Para	R/W	DC	D7	D6	D5	D4	D3	D2	D1	D0	Default
R12H	<b>DRF</b>	W	0	0	0	0	1	0	0	1	0	(12H)

While user sent this command, driver will refresh display (data/VCOM) according to SRAM data and LUT.

This command can be active only when BUSY = "1". After display refresh command, BUSY signal will become "0".

### Data Start Transmission 1&2 / Data Stop Command(B/W/Red)

Code	Inst/Par	R/W	DC	D7	D6	D5	D4	D3	D2	D1	D0	Default
R13H	<b>DTM2</b>	W	0	0	0	1	0	0	0	1	1	(13H)
	1 <sup>st</sup> Para	W	1	PRxI1	PRxI2	PRxI3	PRxI4	PRxI5	PRxI6	PRxI7	PRxI8	00H
	.....	W	1									00H
	M <sup>th</sup> Para	W	1	PRxI(N-1)	PRxIN							00H



1. <data\_flag>=1 while writing both DTM1 and DTM2 parameters fully (B/W/Red)
2. SEG/BG/VCOM change based on internal frame clock

### PLL Control

Code	Inst/Para	R/W	DC	D7	D6	D5	D4	D3	D2	D1	D0	Default
R30H	<b>PLL</b>	W	0	0	0	1	1	0	0	0	0	(30H)
	1 <sup>st</sup> Para	W	0	-	-	M2	M1	M0	N2	N1	N0	3CH

Note: For this panel the R30H Must be set as follow:

- When Temperature  $\geq 30$  value=0x39;  
 When Temperature  $< 30$  value=0x2A.

### Temperature Sensor Command

Code	Inst/Para	R/W	DC	D7	D6	D5	D4	D3	D2	D1	D0	Default
R40H	TSC	W	0	0	1	0	0	0	0	0	0	(40H)
	1 <sup>st</sup> Para	R	1	D10	D9	D8	D7	D6/TS3	D5/TS2	D4/TS1	D3/TS0	00H
	2 <sup>nd</sup> Para	R	1	D2	D1	D0	-	-	-	-	-	00H

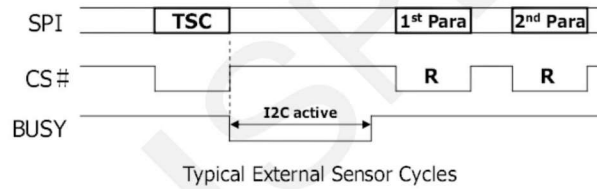
### Internal Sensor Mapping

TS[3:0]	temperature
0000	0 °C
0001	5 °C
0010	10 °C
0011	15 °C
0100	20 °C
0101	25 °C
0110	30 °C
0111	35 °C
1000	40 °C
1001	45 °C
1010	50 °C

### External LM75 Sensor Mapping (D10~D0)

Table 10. Temp register value

11-bit binary (2's complement)	Hexadecimal value	Decimal value	Value
011 1111 1000	3F8	1016	+127.000 °C
011 1111 0111	3F7	1015	+126.875 °C
011 1111 0001	3F1	1009	+126.125 °C
011 1110 1000	3E8	1000	+125.000 °C
000 1100 1000	0C8	200	+25.000 °C
000 0000 0001	001	1	+0.125 °C
000 0000 0000	000	0	0.000 °C
111 1111 1111	7FF	-1	-0.125 °C
111 0011 1000	738	-200	-25.000 °C
110 0100 1001	649	-439	-54.875 °C
110 0100 1000	648	-440	-55.000 °C



### Temperature Sensor Setting

Code	Inst/Para	R/W	DC	D7	D6	D5	D4	D3	D2	D1	D0	Default
R41H	TSE	W	0	0	1	0	0	0	0	0	1	(41H)
	1 <sup>st</sup> Para	W	1	TSE	0	0	0	0	0	0	0	00H

Name	Control	Value	Description
TSE	Temperature Sensor Selection	0	Internal temperature sensor
		1	External temperature sensor

### VCOM and Data Interval Setting Command

Code	Inst/Para	R/W	DC	D7	D6	D5	D4	D3	D2	D1	D0	Default
R50H	CDI	W	0	0	1	0	1	0	0	0	0	(50H)
	1 <sup>st</sup> Para	W	1	-	-	-	DDX	CDI3	CDI2	CDI1	CDI0	17H

Note: For this panel the R50H Must be set as 0x17.

### Resolution Setting Command

Code	Inst/Para	R/W	DC	D7	D6	D5	D4	D3	D2	D1	D0	Default
R61H	<b>TRES</b>	W	0	0	1	1	0	0	0	0	1	(61H)
	1st Para	W	1	HRES7	HRES6	HRES5	HRES4	HRES3	HRES2	HRES1	0	00H
	2nd Para	W	1	-	-	-	-	-	-	-	HRES8	00H
	3rd Para	W	1	VRES7	VRES6	VRES5	VRES4	VRES3	VRES2	VRES1	VRES0	00H

Name	Control	Description
HRES[7:0]	Horizontal Resolution	(1) Horizontal resolution setting (HRES[0] is forced to '0') (2) Minimum active SD channel = S0 (3) Maximum active SD channel = min_active SD + HRES[7:0] - 1
VRES[8:0]	Vertical Resolution	(1) Vertical resolution setting (2) Minimum active GD channel = G0 (3) Maximum active GD channel = min_active GD + VRES[8:0] - 1

Resolution setting(R61H) has higher priority than RES[1:0](R00H).

Note : For this panel R61H 's value must be 0xC8, 0x00, 0xC8.

### VCOM-DC Setting

Code	Inst/Para	R/W	DC	D7	D6	D5	D4	D3	D2	D1	D0	Default
R82H	<b>VDCS</b>	W	0	1	0	0	0	0	0	0	1	(82H)
	1st Para	W	1	-	-	VDCS5	VDCS4	VDCS3	VDCS2	VDCS1	VDCS0	0CH

VDCS[5:0]	VCOM Value	VDCS[5:0]	VCOM Value
000000	0v	.....	.....
000001	-0.1v	011011	-2.7v
000010	-0.2v	011100	-2.8v
000011	-0.3v	011101	-2.9v
000100	-0.4v	011110	-3.0v
000101	-0.5v	.....	
000110	-0.6v	111111	

## 7. Optical characteristics

### 7.1 Specifications

Measurements are made with that the illumination is under an angle of 45 degrees, the detection is perpendicular unless otherwise specified.

T=25°C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYPE	MAX	UNIT	Note
R	Reflectance	White	30	35	-	%	Note 7-1
RS_a	Red State a value	Red	30	35	45		
Gn	2Grey Level	-	-	$DS+(WS-DS) \times n(m-1)$	-	L*	-
CR	Contrast Ratio	indoor	8		-	-	-
Panel's life		0°C~40°C		1000000 times or 5 years		7	Note 10-2

WS: White state, DS: Dark state

Gray state from Dark to White : DS、WS

m: 2

Note 7-1: Luminance meter: Eye – One Pro Spectrophotometer

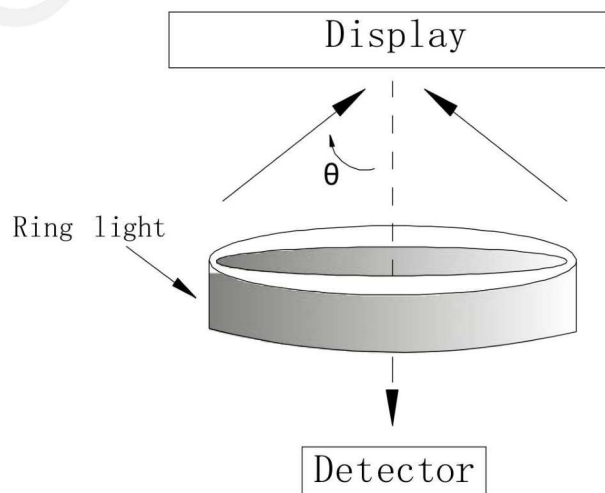
Note 7-2: When work in temperature below 0 degree or above 40 degree, we do not recommend because the panel's life will not be guaranteed. Each update interval time should be minimum at 180 seconds.

### 7.2 Definition of contrast ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (R1) and the reflectance in a dark area (Rd) :

R1: white reflectance      Rd: dark reflectance

$$CR = R1/Rd$$



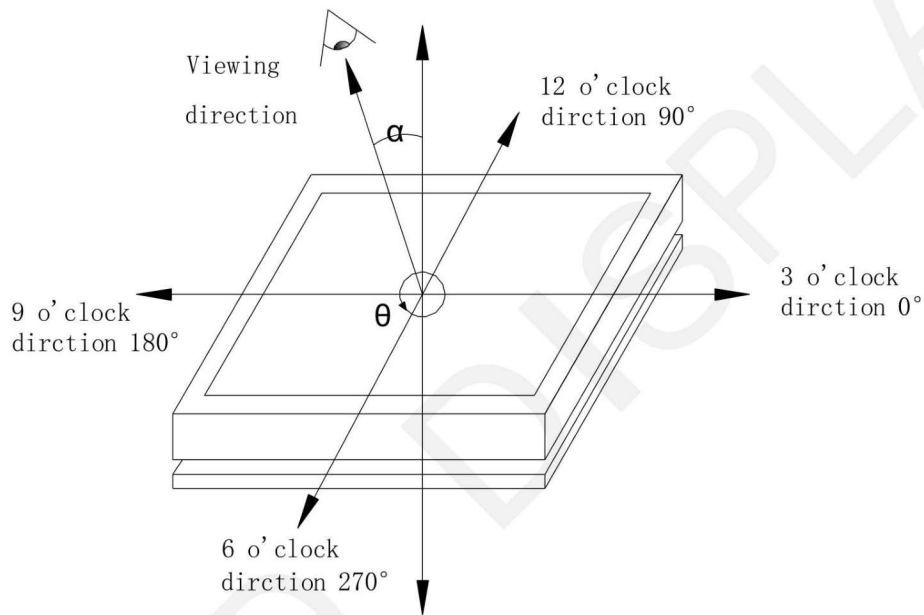


### 7.3 Reflection Ratio

The reflection ratio is expressed as :

$$R = \text{Reflectance Factor}_{\text{white board}} \times (L_{\text{center}} / L_{\text{white board}})$$

$L_{\text{center}}$  is the luminance measured at center in a white area ( $R=G=B=1$ ).  $L_{\text{white board}}$  is the luminance of a standard white board. Both are measured with equivalent illumination source. The viewing angle shall be no more than 2 degrees.



## 8. Point and line standard

### Shipment Inseption Standard

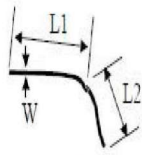
Equipment: Electrical test fixture, Point gauge

Outline demension:

31.8(H) ×37.32(V) ×1.05(D)

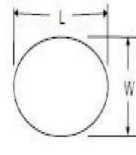
Unit: mm

Environment	Temperature	Humidity	Illuminance	Distance	Time	Angle
	23±2°C	55±5%RH	1200~1500Lux	300 mm	35Sec	
appearance standard	Defet type	Defect size			Part-A	Note
	Dot Defect	D ≤ 0.25mm			Ignore	The defect is below protection film
		0.25mm < D ≤ 0.52mm			4	
		0.52mm < D ≤ 0.65mm			1	
		0.65mm < D			0	
	1.Edge glue lost 2.Burr 3.AI-I film over EPD 4.Edge dent 5.Edge protrusion 6.Dimension	Distance from edge ≤ 0.2mm			Ignore	
	Edge dot defect (Microcup Damage)	Distance from edge ≤ 0.75mm			Ignore	
	Diffusion length of wiping solution	Distance from edge ≤ 0.5mm			Ignore	
	Microcup residue (at Vcom pad)	Distance from edge ≤ 0.5mm			Ignore	
	Display unwork	Electric Display	Not Allow			
	Display error	Electric Display	Not Allow			
	PS PET warping	Vsual	cannot beyond 1/2 of the border			
	Protector hurt	Vsual	L≤2 mm, W≤0.05 mm, Ignore;			
			L>2 mm, W>0.05 mm, Not Allow;			
Adhesive coating	Vsual	Bubble:D≤0.65 & N≤2				
Packing	Vsual	cannot be dirty and breakdown;must be marked and identified				
Remark	1.Cannot be defect&failure cause by appearance defect;					
	2.Cannot be larger size cause by appearance defect;					



$$L = L1 + L2$$

Line Defect



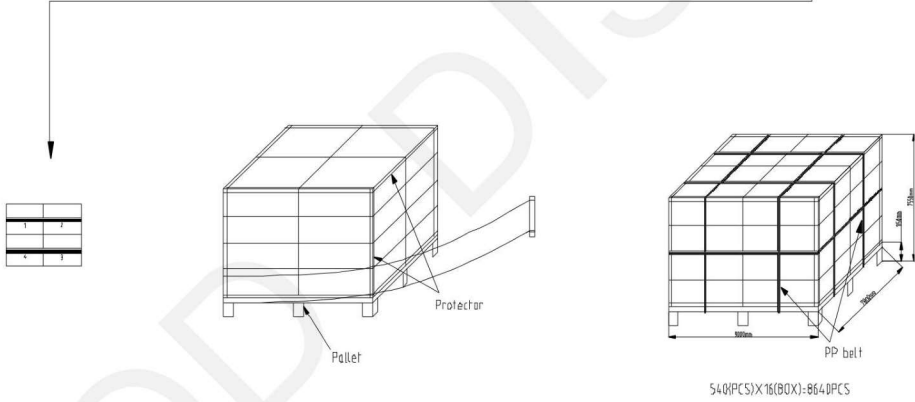
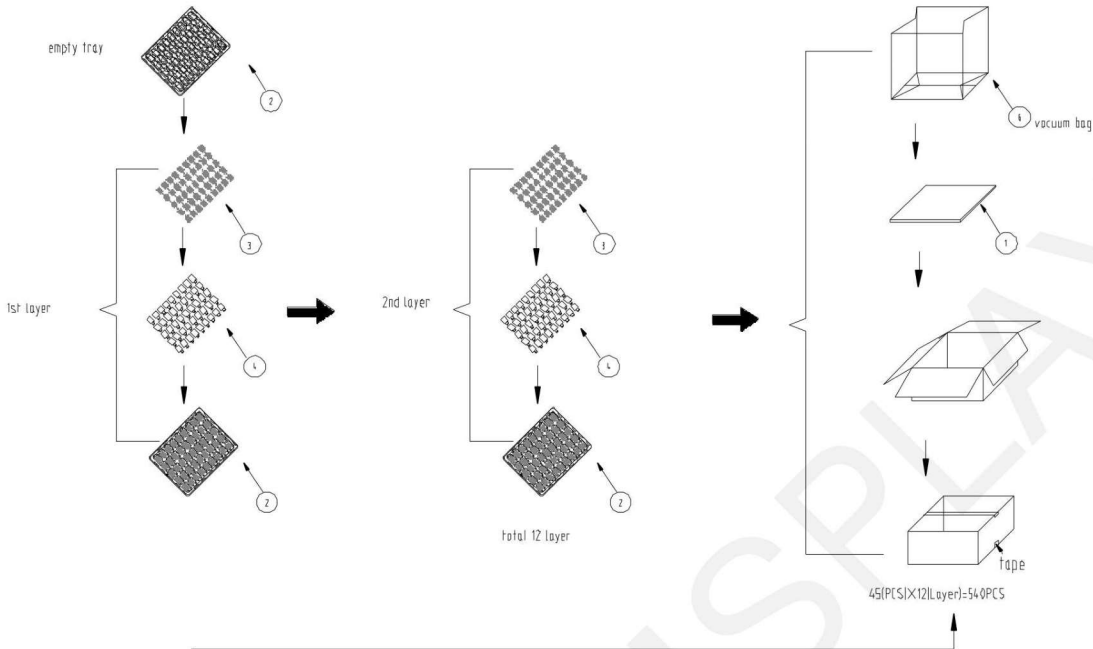
$$D = (L + W) / 2$$

Spot Defect

L=long    W=wide    D=point size

Edition	Content	Date
1	New edition	Sep.30.2013

# 9. Packing



## 10. Precautions

- (1) Do not apply pressure to the EPD panel in order to prevent damaging it.
- (2) Do not connect or disconnect the interface connector while the EPD panel is in operation.
- (3) Do not touch IC bonding area. It may scratch TFT lead or damage IC function.
- (4) Please be mindful of moisture to avoid its penetration into the EPD panel, which may cause damage during operation.
- (5) If the EPD Panel / Module is not refreshed every 24 hours, a phenomena known as “Ghosting” or “Image Sticking” may occur. It is recommended to refreshed the ESL / EPD Tag every 24 hours in use case. It is recommended that customer ships or stores the ESL / EPD Tag with a completely white image to avoid this issue
- (6) High temperature, high humidity, sunlight or fluorescent light may degrade the EPD panel’s performance. Please do not expose the unprotected EPD panel to high temperature, high humidity, sunlight, or fluorescent for long periods of time.