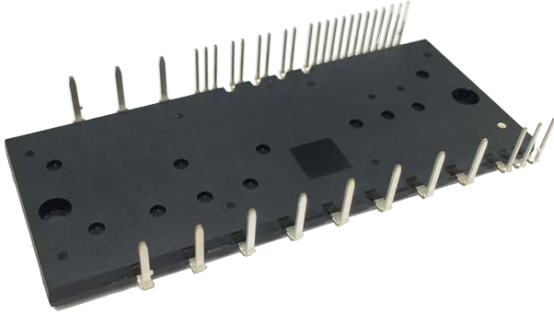


< Dual-In-Line Package Intelligent Power Module >

# PSS50NC1F6

TRANSFER MOLDING TYPE  
INSULATED TYPE

## OUTLINE



## MAIN FUNCTION

CI(Converter + Inverter) type IPM

- 3-phase Inverter
- 3-phase Converter

## RATING

- Inverter part : 50A/600V (CSTBT)

## APPLICATION

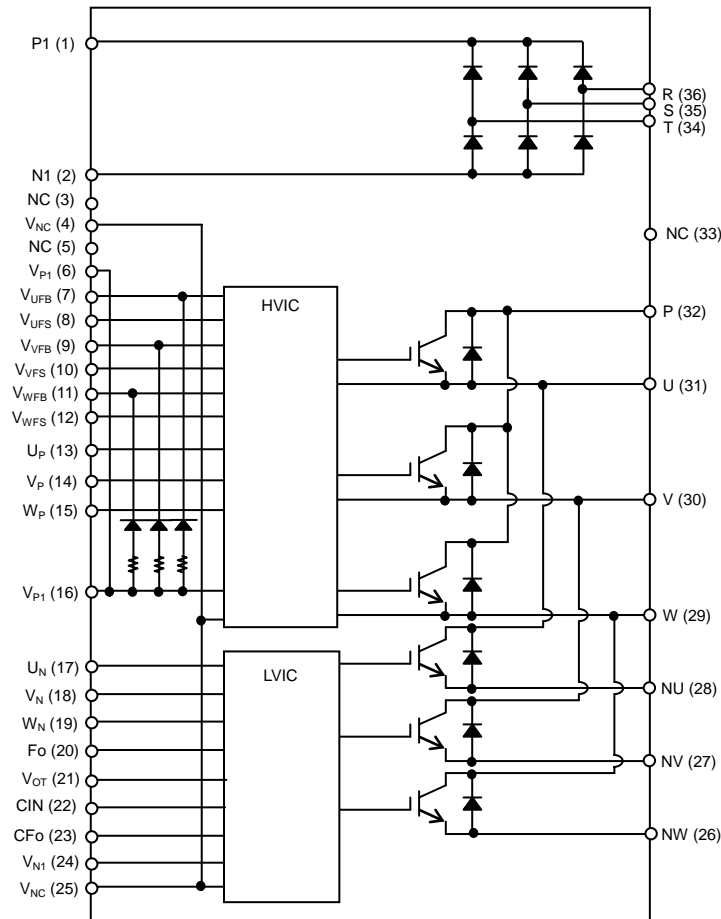
- AC200V three phase motor inverter drive

\* With brake circuit type 'PSS50MC1F6' is also available.

## INTEGRATED DRIVE, PROTECTION AND SYSTEM CONTROL FUNCTIONS

- For P-side : Drive circuit, High voltage high-speed level shifting, Control supply under-voltage protection (UV) without fault signal output  
Built-in discrete bootstrap diode chips with current limiting resistor
- For N-side : Drive circuit, Control supply under-voltage protection (UV), Short circuit protection (SC) by detecting voltage of external shunt resistor
- Fault signaling : Corresponding to SC fault (N-side IGBT) and UV fault (N-side supply)
- Temperature monitoring : Outputting LVIC temperature by analog signal (No self over temperature protection)
- Input interface : 5V high active logic
- UL Recognized : UL1557 File E323585

## INTERNAL CIRCUIT



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**MAXIMUM RATINGS** ( $T_j = 25^\circ\text{C}$ , unless otherwise noted)

**INVERTER PART**

Symbol	Parameter	Condition	Ratings	Unit
$V_{CC}$	Supply voltage	Applied between P-NU,NV,NW	450	V
$V_{CC(surge)}$	Supply voltage (surge)	Applied between P-NU,NV,NW	500	V
$V_{CES}$	Collector-emitter voltage		600	V
$\pm I_C$	Each IGBT collector current	$T_C = 25^\circ\text{C}$ (Note 1)	50	A
$\pm I_{CP}$	Each IGBT collector current (peak)	$T_C = 25^\circ\text{C}$ , less than 1ms	100	A
$T_j$	Junction temperature		-30~+150	$^\circ\text{C}$

Note1: Pulse width and period are limited due to junction temperature.

**CONVERTER PART**

Symbol	Parameter	Condition	Ratings	Unit
$V_{RRM}$	Repetitive peak reverse voltage		800	V
$I_O$	DC output current	3-phase full wave rectification	50	A
$I_{FSM}$	Surge forward current	Peak value of half cycle at 60Hz, Non-repetitive	350	A
$I^2t$	$I^2t$ capability	Value for 1 cycle of surge current	510	$\text{A}^2\text{s}$
$T_j$	Junction temperature		-30~+150	$^\circ\text{C}$

**CONTROL (PROTECTION) PART**

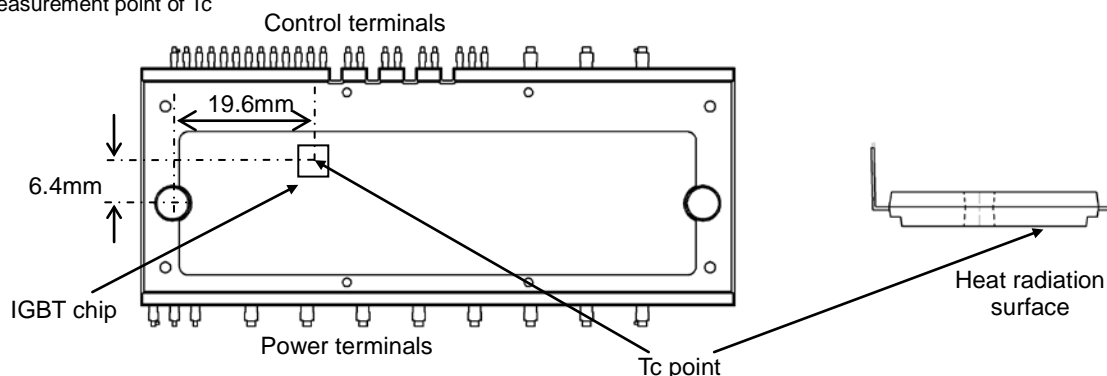
Symbol	Parameter	Condition	Ratings	Unit
$V_D$	Control supply voltage	Applied between $V_{P1}-V_{NC}$ , $V_{N1}-V_{NC}$	20	V
$V_{DB}$	Control supply voltage	Applied between $V_{UFB}-V_{UFS}$ , $V_{VFB}-V_{VFS}$ , $V_{WFB}-V_{WFS}$	20	V
$V_{IN}$	Input voltage	Applied between $U_P, V_P, W_P, U_N, V_N, W_N-V_{NC}$	-0.5- $V_D$ +0.5	V
$V_{FO}$	Fault output supply voltage	Applied between $F_O-V_{NC}$	-0.5- $V_D$ +0.5	V
$I_{FO}$	Fault output current	Sink current at $F_O$ terminal	5	mA
$V_{SC}$	Current sensing input voltage	Applied between $CIN-V_{NC}$	-0.5- $V_D$ +0.5	V

**TOTAL SYSTEM**

Symbol	Parameter	Condition	Ratings	Unit
$V_{CC(prot)}$	Self protection supply voltage limit (Short circuit protection capability)	$V_D = 13.5\sim 16.5\text{V}$ , Inverter Part $T_j = 125^\circ\text{C}$ , non-repetitive, less than $2\mu\text{s}$	400	V
$T_C$	Module case operation temperature	(Note 2)	-30~+125	$^\circ\text{C}$
$T_{stg}$	Storage temperature		-40~+125	$^\circ\text{C}$
$V_{iso}$	Isolation voltage	60Hz, Sinusoidal, AC 1min, between connected all pins and heat sink plate	2500	$V_{rms}$

Note2: Measurement point of  $T_c$  is described in Fig.1.

Fig. 1 Measurement point of  $T_c$



**THERMAL RESISTANCE**

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
$R_{th(j-c)Q}$	Junction to case thermal resistance (Note 3)	Inverter IGBT part (per 1/6 module)	-	-	0.95	K/W
$R_{th(j-c)F}$		Inverter FWD part (per 1/6 module)	-	-	1.20	
$R_{th(j-c)R}$		Converter part (per 1/6 module)	-	-	1.10	

Note 3: Grease with good thermal conductivity and long-term endurance should be applied evenly with about  $+100\mu\text{m}\sim +200\mu\text{m}$  on the contacting surface of DIPIPM and heat sink. The contacting thermal resistance between DIPIPM case and heat sink  $R_{th(c-f)}$  is determined by the thickness and the thermal conductivity of the applied grease. For reference,  $R_{th(c-f)}$  is about 0.25K/W (per 1 chip, grease thickness:  $20\mu\text{m}$ , thermal conductivity:  $1.0\text{W/m}\cdot\text{K}$ ).

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## ELECTRICAL CHARACTERISTICS (T<sub>j</sub> = 25°C, unless otherwise noted)

### INVERTER PART

Symbol	Parameter	Condition	Limits			Unit	
			Min.	Typ.	Max.		
V <sub>CE(sat)</sub>	Collector-emitter saturation voltage	V <sub>D</sub> =V <sub>DB</sub> = 15V, V <sub>IN</sub> = 5V	I <sub>C</sub> = 50A, T <sub>j</sub> = 25°C	-	1.25	1.60	V
			I <sub>C</sub> = 50A, T <sub>j</sub> = 125°C	-	1.30	1.75	
V <sub>EC</sub>	FWDi forward voltage	V <sub>IN</sub> = 0V, -I <sub>C</sub> = 50A	-	1.60	2.10	V	
t <sub>on</sub>	Switching times	V <sub>CC</sub> = 300V, V <sub>D</sub> = V <sub>DB</sub> = 15V I <sub>C</sub> = 50A, T <sub>j</sub> = 125°C, V <sub>IN</sub> = 0→5V Inductive Load (upper-lower arm)		1.20	1.80	2.50	μs
t <sub>C(on)</sub>				-	0.50	0.90	μs
t <sub>off</sub>				-	2.60	3.60	μs
t <sub>C(off)</sub>				-	0.35	0.90	μs
t <sub>rr</sub>				-	0.40	-	μs
I <sub>CES</sub>	Collector-emitter cut-off current	V <sub>CE</sub> =V <sub>CES</sub>	T <sub>j</sub> = 25°C	-	-	1	mA
			T <sub>j</sub> = 125°C	-	-	10	

### CONVERTER PART

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
I <sub>RRM</sub>	Repetitive reverse current	V <sub>R</sub> =V <sub>RRM</sub> , T <sub>j</sub> =125°C	-	-	7.0	mA
V <sub>F</sub>	Forward voltage drop	I <sub>F</sub> =50A	-	1.2	1.6	V

### CONTROL (PROTECTION) PART

Symbol	Parameter	Condition	Limits			Unit	
			Min.	Typ.	Max.		
I <sub>D</sub>	Circuit current	Total of V <sub>P1</sub> -V <sub>NC</sub> , V <sub>N1</sub> -V <sub>NC</sub>	V <sub>D</sub> =15V, V <sub>IN</sub> =0V	-	-	4.70	mA
			V <sub>D</sub> =15V, V <sub>IN</sub> =5V	-	-	4.70	
I <sub>DB</sub>		Each part of V <sub>UFB</sub> -V <sub>UFS</sub> , V <sub>VFB</sub> -V <sub>VFS</sub> , V <sub>WFB</sub> -V <sub>WFS</sub>	V <sub>D</sub> =V <sub>DB</sub> =15V, V <sub>IN</sub> =0V	-	-	0.55	
			V <sub>D</sub> =V <sub>DB</sub> =15V, V <sub>IN</sub> =5V	-	-	0.55	
V <sub>SC(ref)</sub>	Short circuit trip level	V <sub>D</sub> = 15V (Note 4)	0.455	0.480	0.505	V	
UV <sub>DBt</sub>	Control supply under-voltage protection(UV) for P-side of inverter part		Trip level	10.0	-	12.0	V
UV <sub>DBr</sub>			Reset level	10.5	-	12.5	V
UV <sub>Dt</sub>	Control supply under-voltage protection(UV) for N-side of inverter part		Trip level	10.3	-	12.5	V
UV <sub>Dr</sub>			Reset level	10.8	-	13.0	V
V <sub>OT</sub>	Temperature Output	Pull down R=5.1kΩ, LVIC Temperature=100°C (Note 5)	2.89	3.02	3.14	V	
V <sub>FOH</sub>	Fault output voltage	V <sub>SC</sub> = 0V, F <sub>O</sub> terminal pulled up to 5V by 10kΩ	4.9	-	-	V	
V <sub>FOL</sub>		V <sub>SC</sub> = 1V, I <sub>F0</sub> = 1mA	-	-	0.95	V	
t <sub>F0</sub>	Fault output pulse width	In case of C <sub>F0</sub> =22nF (Note 6,7)	1.6	2.4	-	ms	
I <sub>IN</sub>	Input current	V <sub>IN</sub> = 5V	0.70	1.00	1.50	mA	
V <sub>th(on)</sub>	ON threshold voltage	Applied between U <sub>P</sub> , V <sub>P</sub> , W <sub>P</sub> , U <sub>N</sub> , V <sub>N</sub> , W <sub>N</sub> -V <sub>NC</sub>	-	-	3.5	V	
V <sub>th(off)</sub>	OFF threshold voltage		0.8	-	-		
V <sub>F</sub>	Bootstrap Di forward voltage	I <sub>F</sub> =10mA including voltage drop by limiting resistor (Note 8)	-	0.9	1.3	V	
R	Built-in limiting resistance	Included in bootstrap Di	16	20	24	Ω	

Note 4 : SC protection works only for N-side IGBT in inverter part. Please select the external shunt resistance such that the SC trip-level is less than 1.7 times of the current rating.

5 : DIPIPM don't shutdown IGBTs and output fault signal automatically when temperature rises excessively. When temperature exceeds the protective level that user defined, controller (MCU) should stop the DIPIPM. Temperature of LVIC vs. V<sub>OT</sub> output characteristics is described in Fig. 3.

6 : Fault signal Fo outputs when SC or UV protection works for N-side IGBT in inverter part. The fault output pulse-width t<sub>F0</sub> is depended on the capacitance value of C<sub>F0</sub> (C<sub>F0</sub> = t<sub>F0</sub> × 9.1 × 10<sup>6</sup> [F]).

7 : UV protection also works for P-side IGBT in inverter part without fault signal Fo.

8 : The characteristics of bootstrap Di is described in Fig.2.

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Fig. 2 Characteristics of Bootstrap Di  $V_F$ - $I_F$  curve (@ $T_a=25^\circ\text{C}$ ) Including Voltage Drop by Limiting Resistor (Right chart is enlarged chart.)

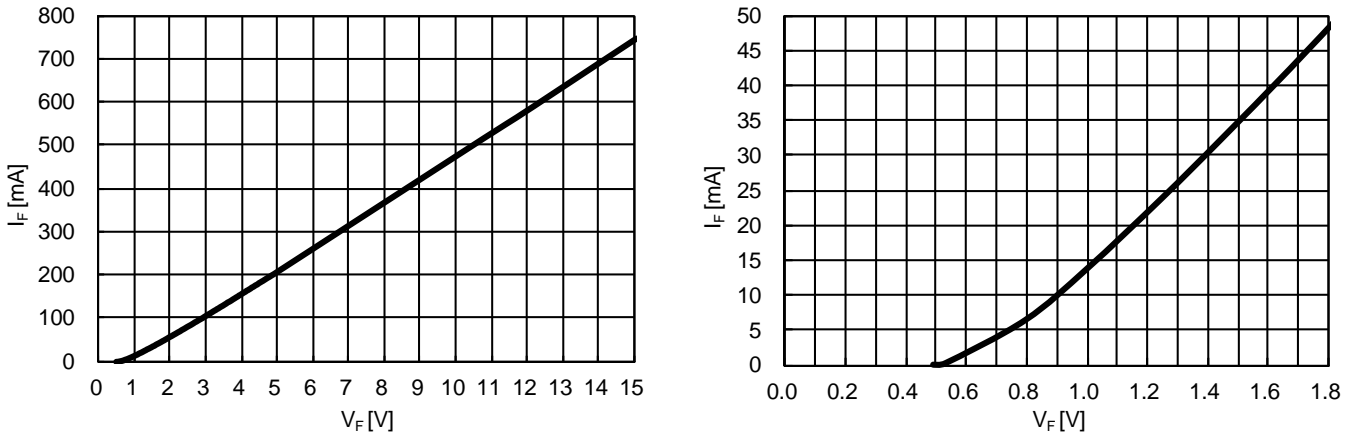
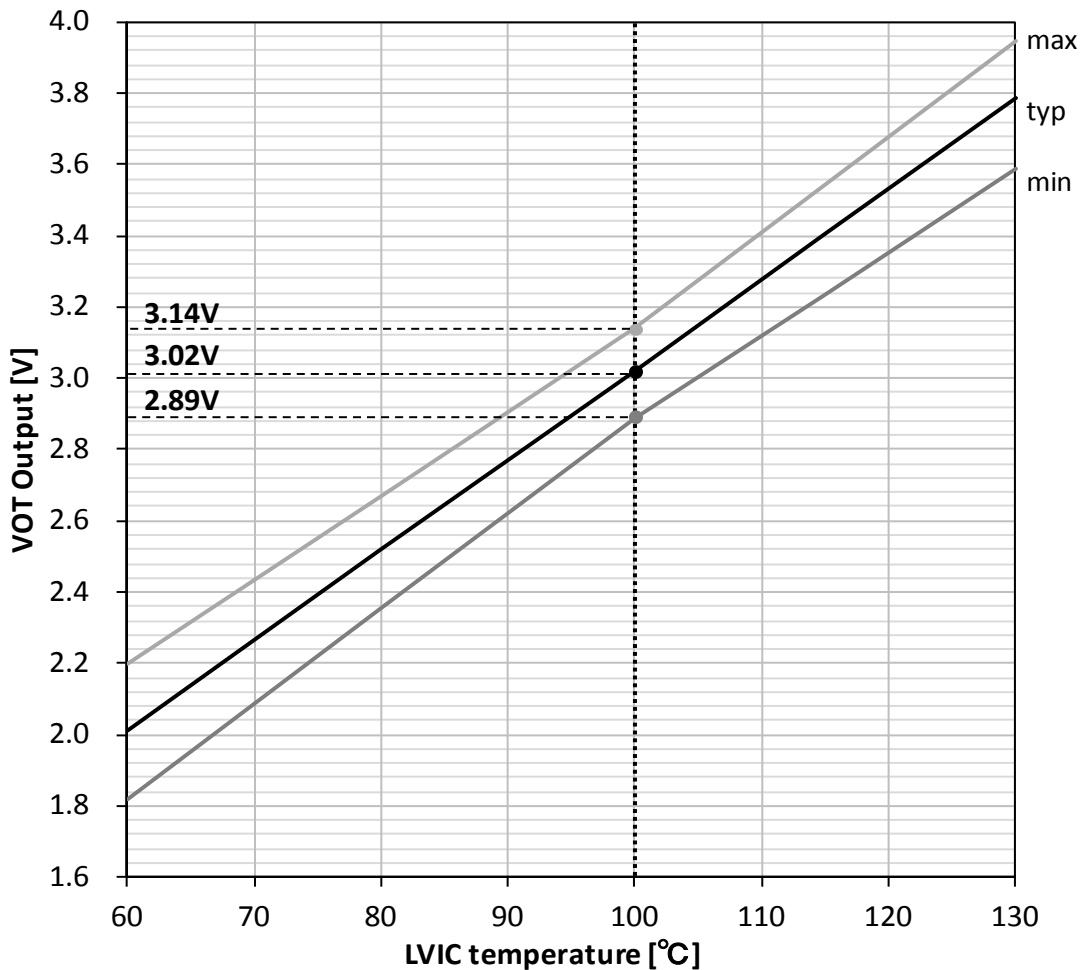


Fig. 3 Temperature of LVIC vs.  $V_{OT}$  Output Characteristics



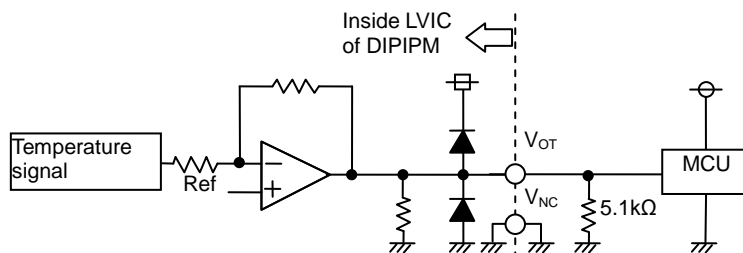
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Fig. 4 Pattern Wiring Around the Analog Voltage Output Circuit [V<sub>OT</sub> terminal]



- (1) V<sub>OT</sub> outputs the analog signal that is amplified signal of temperature detecting element on LVIC by inverting amplifier.
- (2) It is recommended to insert 5kΩ (5.1kΩ is recommended) pull down resistor for getting linear output characteristics at low temperature below room temperature. When the pull down resistor is inserted between V<sub>OT</sub> and V<sub>NC</sub>(control GND), the extra circuit current, which is calculated approximately by V<sub>OT</sub> output voltage divided by pull down resistance, flows as LVIC circuit current continuously. In the case of using V<sub>OT</sub> for detecting high temperature over room temperature only, it is unnecessary to insert the pull down resistor.
- (3) In the case of not using V<sub>OT</sub>, leave V<sub>OT</sub> output NC (No Connection).

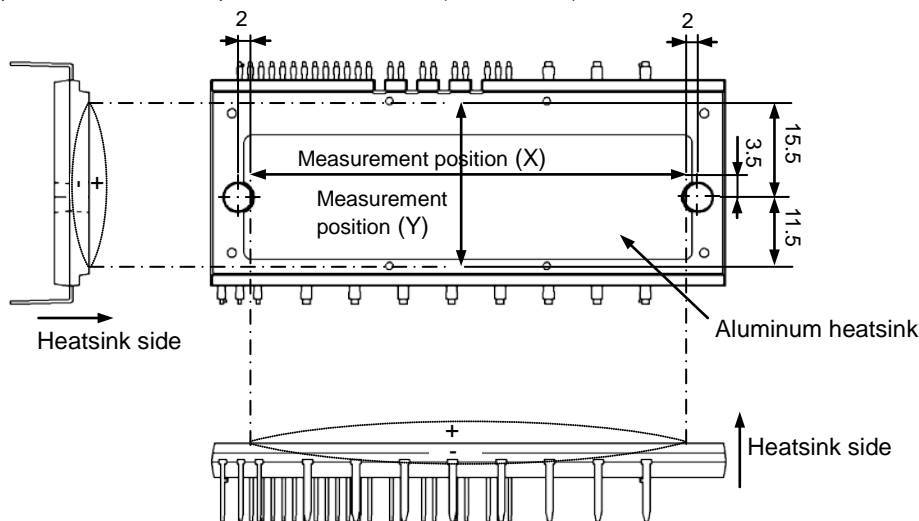
Please also refer the application note for DIIPM+ series about the usage of V<sub>OT</sub>.

**MECHANICAL CHARACTERISTICS AND RATINGS**

Parameter	Condition		Limits			Unit
			Min.	Typ.	Max.	
Mounting torque	Mounting screw : M4 (Note 9)	Recommended 1.18N·m	0.98	1.18	1.47	N·m
Terminal pulling strength	20N load	JEITA-ED-4701	10	-	-	s
Terminal bending strength	90deg bending with 10N load	JEITA-ED-4701	2	-	-	times
Weight			-	40	-	g
Heat radiation part flatness		(Note 10)	-50	-	+100	μm

Note 9: Plain washers (ISO 7089~7094) are recommended.

Note 10: Measurement positions of heat radiation part flatness are as below. (Dimension:mm)



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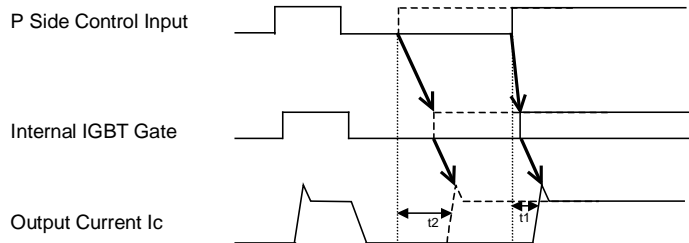
**RECOMMENDED OPERATION CONDITIONS**

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
$V_{CC}$	Supply voltage	Applied between P-NU, NV, NW	0	300	400	V
$V_D$	Control supply voltage	Applied between $V_{P1}-V_{NC}, V_{N1}-V_{NC}$	13.5	15.0	16.5	V
$V_{DB}$	Control supply voltage	Applied between $V_{UFB}-V_{UFS}, V_{VFB}-V_{VFS}, V_{WFB}-V_{WFS}$	13.0	15.0	18.5	V
$\Delta V_D, \Delta V_{DB}$	Control supply variation		-1	-	1	V/ $\mu$ s
$t_{dead}$	Arm shoot-through blocking time	For each input signal	3.0	-	-	$\mu$ s
$f_{PWM}$	PWM input frequency	$T_C \leq 100^\circ\text{C}, T_j \leq 125^\circ\text{C}$	-	-	20	kHz
PWIN(on)	Minimum input pulse width	$I_C \leq 1.7$ times of rated current (Note 11)	1.5	-	-	$\mu$ s
PWIN(off)		$0 \leq V_{CC} \leq 350\text{V}, 13.5 \leq V_D \leq 16.5\text{V},$ $13.0 \leq V_{DB} \leq 18.5\text{V}, -20 \leq T_C \leq 100^\circ\text{C},$ N line wiring inductance less than 10nH (Note 12)	Less than rated current From rated current to 1.7 times of rated current	3.0	-	
$V_{NC}$	$V_{NC}$ variation	Between $V_{NC}$ - NU, NV, NW (including surge)	-5.0	-	+5.0	V
$T_j$	Junction temperature		-20	-	125	$^\circ\text{C}$

Note 11: DIPIPM might not make response if the input signal pulse width is less than PWIN(on).

Note 12: DIPIPM might make no response or delayed response (P-side IGBT only) for the input signal with off pulse width less than PWIN(off). Please refer below figure about delayed response.

About Delayed Response Against Shorter Input Off Signal Than PWIN(off) (P side only)



Real line···off pulse width>PWIN(off); turn on time t1  
 Broken line···off pulse width<PWIN(off); turn on time t2

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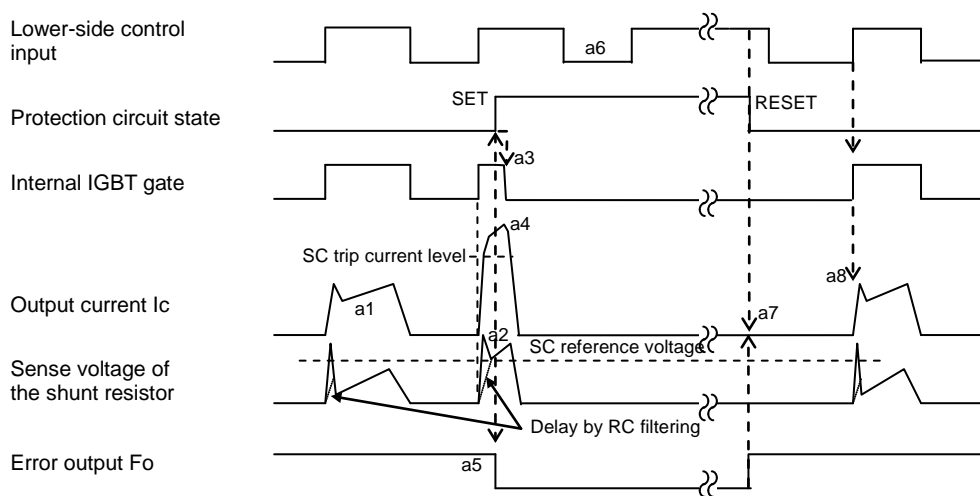
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Fig. 5 Timing Charts of The DIIPM Protective Functions

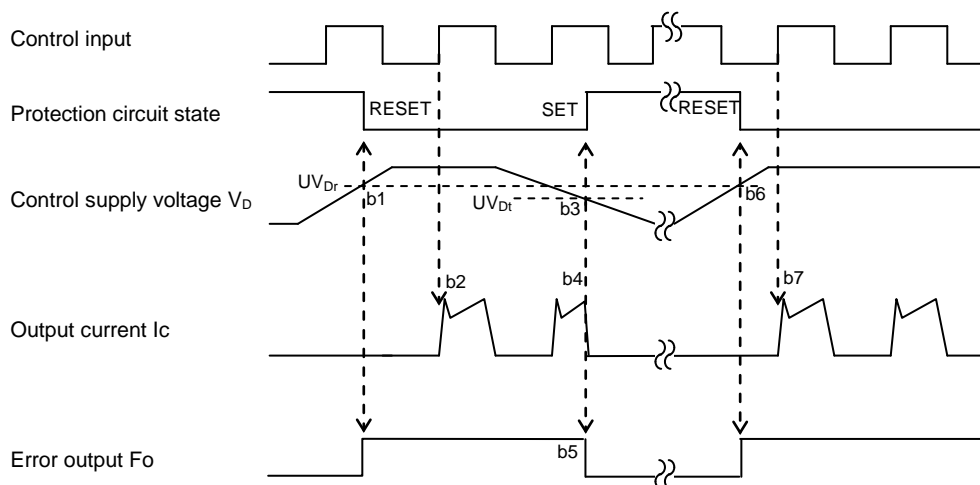
[A] Short-Circuit Protection (N-side only with the external shunt resistor and RC filter)

- a1. Normal operation: IGBT ON and outputs current.
- a2. Short circuit current detection (SC trigger)  
(It is recommended to set RC time constant 1.5~2.0 $\mu$ s so that IGBT shut down within 2.0 $\mu$ s when SC.)
- a3. All N-side IGBT's gates are hard interrupted.
- a4. All N-side IGBTs turn OFF.
- a5. LVIC starts outputting fault signal (fault signal output time is controlled by external capacitor  $C_{FO}$ )
- a6. Input = "L": IGBT OFF
- a7. Fo finishes output, but IGBTs don't turn on until inputting next ON signal (L $\rightarrow$ H).
- (IGBT of each phase can return to normal state by inputting ON signal to each phase.)
- a8. Normal operation: IGBT ON and outputs current.



[B] Under-Voltage Protection (N-side,  $UV_D$ )

- b1. Control supply voltage  $V_D$  exceeds under voltage reset level ( $UV_{Dr}$ ), but IGBT turns ON by next ON signal (L $\rightarrow$ H).  
(IGBT of each phase can return to normal state by inputting ON signal to each phase.)
- b2. Normal operation: IGBT ON and outputs current.
- b3.  $V_D$  level drops to under voltage trip level. ( $UV_{Dt}$ ).
- b4. All N-side IGBTs turn OFF in spite of control input condition.
- b5. Fo outputs for the period set by external capacitor  $C_{FO}$ , but output is extended during  $V_D$  keeps below  $UV_{Dt}$ .
- b6.  $V_D$  level reaches  $UV_{Dr}$ .
- b7. Normal operation: IGBT ON and outputs current.



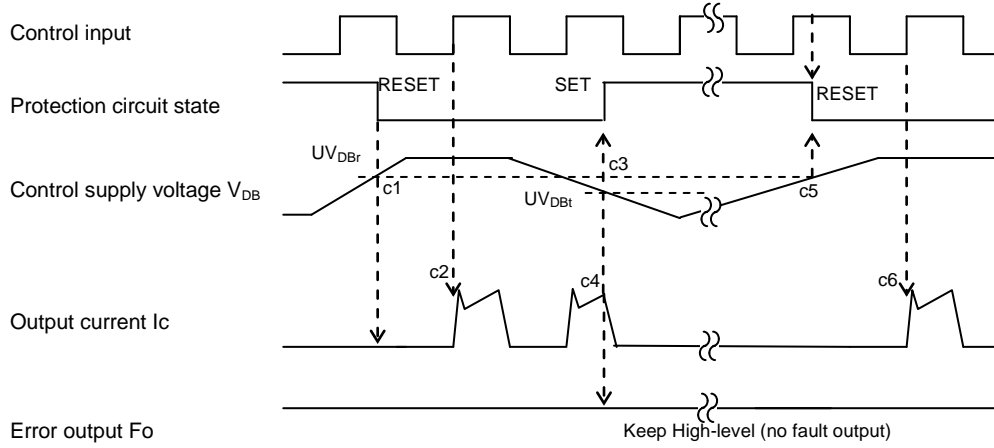
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## [C] Under-Voltage Protection (P-side, $UV_{DB}$ )

- c1. Control supply voltage  $V_{DB}$  rises. After the voltage reaches under voltage reset level  $UV_{DBr}$ , IGBT turns on by next ON signal (L→H).
- c2. Normal operation: IGBT ON and outputs current.
- c3.  $V_{DB}$  level drops to under voltage trip level ( $UV_{DBt}$ ).
- c4. IGBT of the correspond phase only turns OFF in spite of control input signal level, but there is no  $F_o$  signal output.
- c5.  $V_{DB}$  level reaches  $UV_{DBr}$ .
- c6. Normal operation: IGBT ON and outputs current.

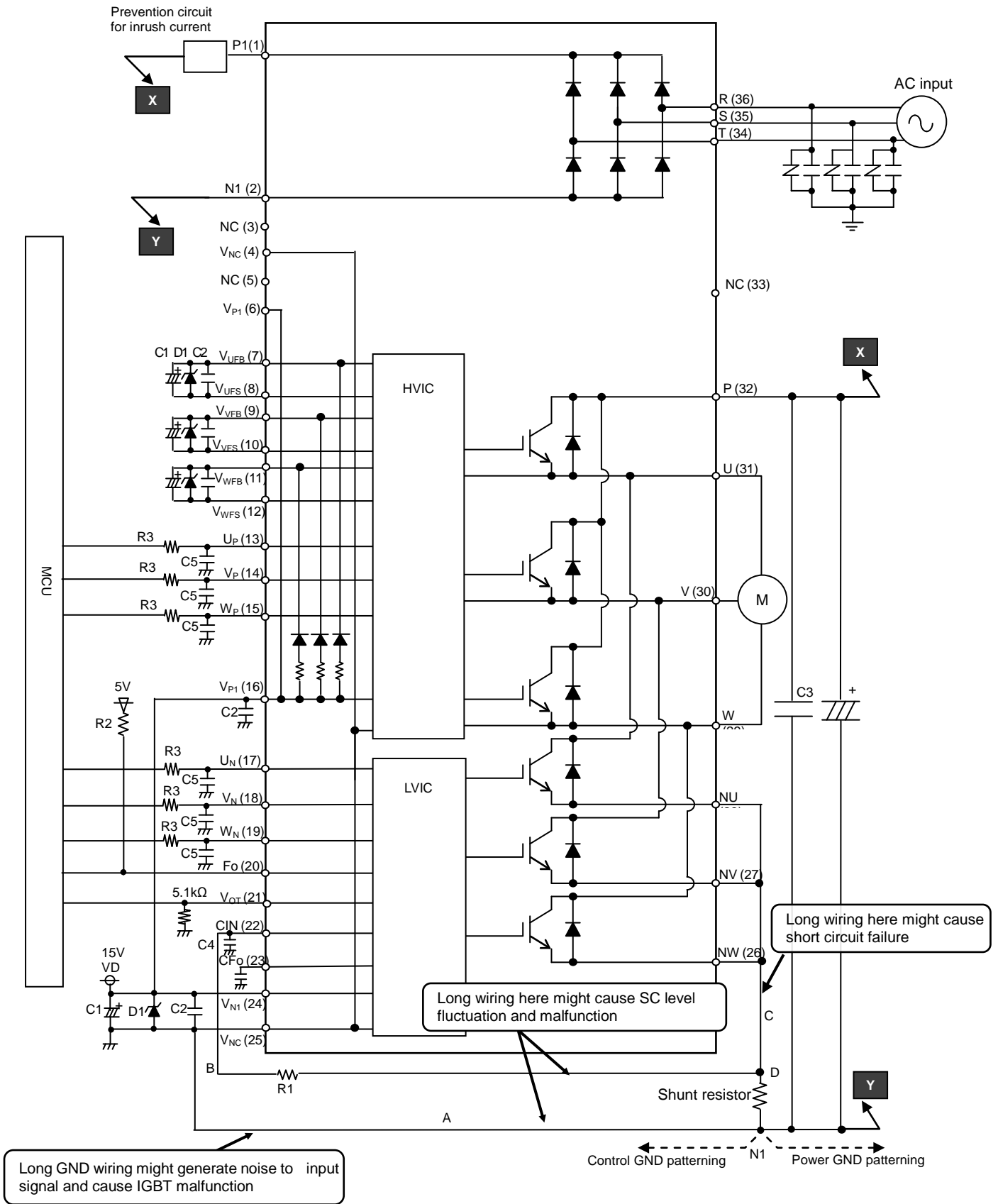




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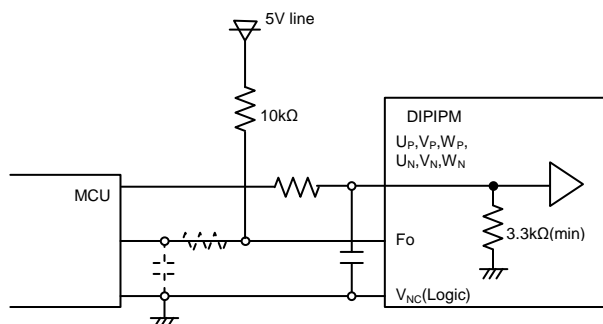
Fig. 6 Example of Application Circuit



Note for the previous application circuit

- (1) If control GND is connected with power GND by common broad pattern, it may cause malfunction by power GND fluctuation. It is recommended to connect control GND and power GND at only a point N1 (near the terminal of shunt resistor).
- (2) It is recommended to insert a Zener diode D1(24V/1W) between each pair of control supply terminals to prevent surge destruction.
- (3) To prevent surge destruction, the wiring between the smoothing capacitor and the P, N1 terminals should be as short as possible. Generally a 0.1-0.22μF snubber capacitor C3 between the P-N1 terminals is recommended.
- (4) R1, C4 of RC filter for preventing protection circuit malfunction is recommended to select tight tolerance, temp-compensated type. The time constant R1C4 should be set so that SC current is shut down within 2μs. (1.5μs~2μs is recommended generally.) SC interrupting time might vary with the wiring pattern, so the enough evaluation on the real system is necessary.
- (5) To prevent malfunction, the wiring of A, B, C should be as short as possible.
- (6) The point D at which the wiring to CIN filter is divided should be near the terminal of shunt resistor. NU, NV, NW terminals should be connected each other at near those three terminals when it is used by one shunt operation. Low inductance SMD type with tight tolerance, temp-compensated type is recommended for shunt resistor.
- (7) All capacitors should be mounted as close to the terminals as possible. (C1: good temperature, frequency characteristic electrolytic type and C2:0.01μ-2μF, good temperature, frequency and DC bias characteristic ceramic type are recommended.)
- (8) Input logic is High-active. There is a 3.3kΩ(min.) pull-down resistor in the input circuit of IC. To prevent malfunction, the input wiring should be as short as possible. When using RC coupling, make the input signal level meet the turn-on and turn-off threshold voltage.
- (9) Fo output is open drain type. Fo output will be max 0.95V(@I<sub>FO</sub>=1mA,25°C), so it should be pulled up to MCU or control power supply (e.g. 5V,15V) by a resistor that makes I<sub>FO</sub> up to 1mA. (In the case of pulled up to 5V, 10kΩ is recommended.) About driving opto coupler by Fo output, please refer the application note of this series.
- (10) Fo pulse width can be set by the capacitor connected to CFO terminal. C<sub>FO</sub>(F) = 9.1 × 10<sup>-6</sup> × t<sub>FO</sub> (Required Fo pulse width).
- (11) If high frequency noise superimposed to the control supply line, IC malfunction might happen and cause DIPIPM erroneous operation. To avoid such problem, line ripple voltage should meet dV/dt ≤ +/-1V/μs, V<sub>ripple</sub> ≤ 2Vp-p.
- (12) For DIPIPM, it isn't recommended to drive same load by parallel connection with other phase IGBT or other DIPIPM.
- (13) No.4 and No.25 V<sub>NC</sub> terminals (GND terminal for control supply) are connected mutually inside of DIPIPM+ and also No.6 and No.16 V<sub>P1</sub> terminals are connected mutually inside, please connect either No.4 or No.25 terminal to GND and also connect either No.6 or No.16 terminal to supply and make the unused terminal leave no connection.

Fig. 7 MCU I/O Interface Circuit

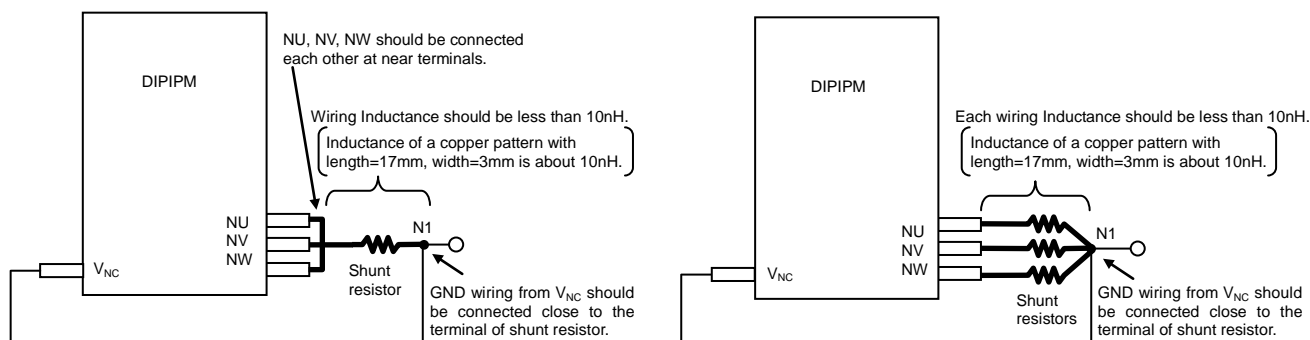


Note)

Design for input RC filter depends on the PWM control scheme used in the application and the wiring impedance of the printed circuit board. The DIPIPM input signal interface integrates a min. 3.3kΩ pull-down resistor. Therefore, when using RC filter, be careful to satisfy turn-on threshold voltage requirement.

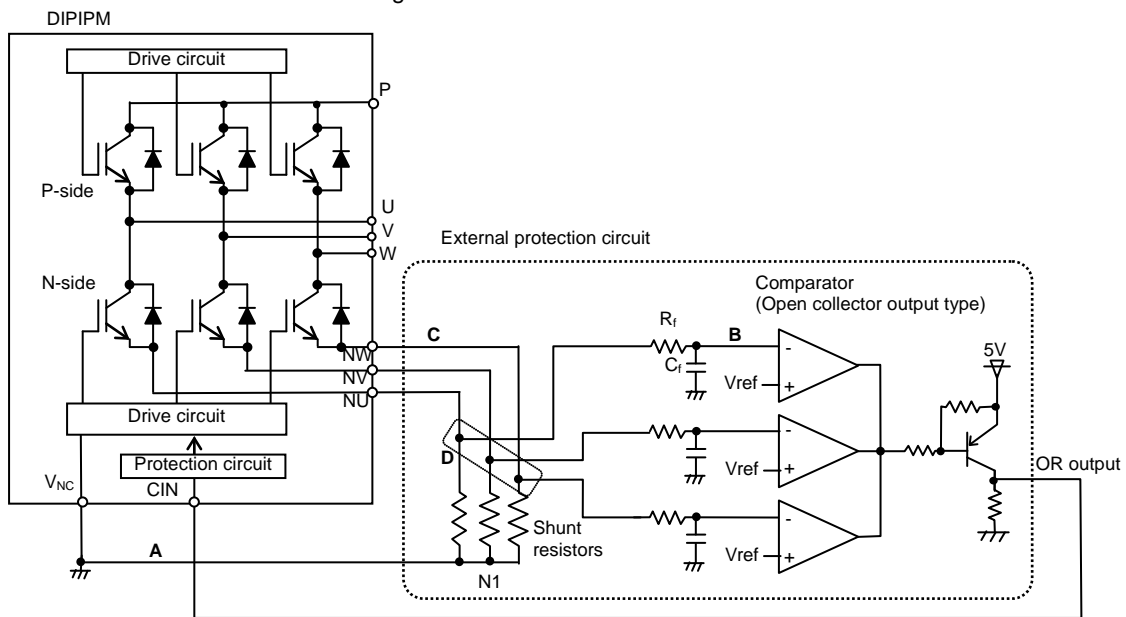
Fo output is open drain type. It should be pulled up to the positive side of 5V or 15V power supply with the resistor that limits Fo sink current I<sub>FO</sub> under 1mA. In the case of pulling up to 5V supply, over 5.1kΩ is needed. (10kΩ is recommended.)

Fig. 8 Pattern Wiring Around the Shunt Resistor



Low inductance shunt resistor like surface mounted (SMD) type is recommended.

Fig. 9 External SC Protection Circuit with Using Three Shunt Resistors



- (1) It is necessary to set the time constant  $R_i C_f$  of external comparator input so that IGBT stop within  $2\mu s$  when short circuit occurs. SC interrupting time might vary with the wiring pattern, comparator speed and so on.
- (2) The threshold voltage  $V_{ref}$  should be set up the same rating of short circuit trip level ( $V_{sc(ref)}$  typ. 0.48V).
- (3) Select the external shunt resistance so that SC trip-level is less than specified value.
- (4) To avoid malfunction, the wiring A, B, C should be as short as possible.
- (5) The point D at which the wiring to comparator is divided should be near the terminal of shunt resistor.
- (6) OR output high level should be over 0.505V (=maximum  $V_{sc(ref)}$ ).
- (7) GND of Comparator, Vref circuit and  $C_f$  should be not connected to noisy power GND but to control GND wiring.

< Dual-In-Line Package Intelligent Power Module >

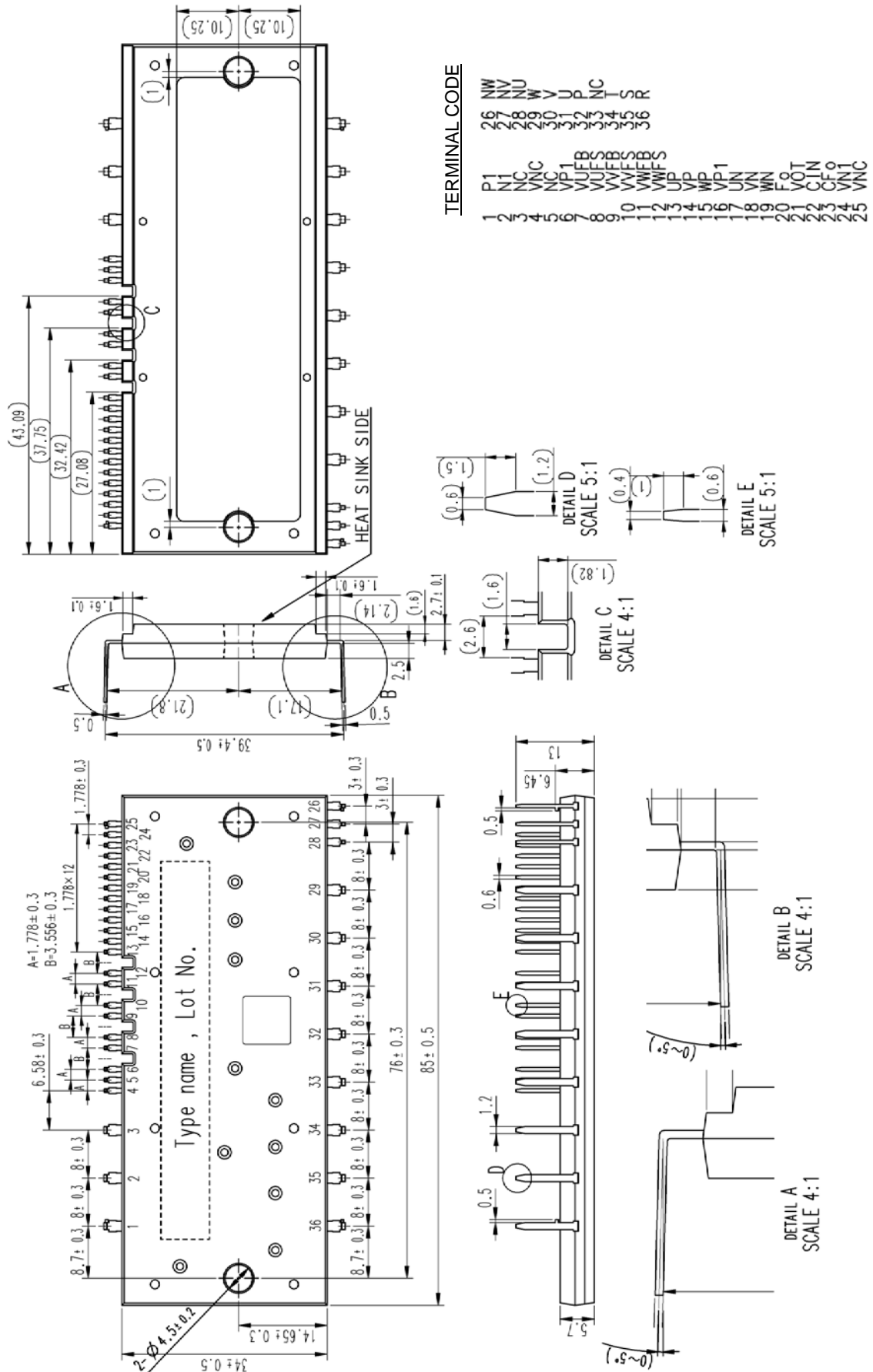
**PSS50NC1F6**

TRANSFER MOLDING TYPE

INSULATED TYPE

Fig. 10 Package Outlines

Dimensions in mm



< Dual-In-Line Package Intelligent Power Module >

# PSS50NC1F6

TRANSFER MOLDING TYPE

INSULATED TYPE

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## Revision Record

Rev.	Date	Page	Revised contents
1	12/09/2016	-	New

## PSS50NC1F6

TRANSFER MOLDING TYPE

INSULATED TYPE

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