**SPECIFICATION:** 

**BLGDEW080T5** 

#### 1. Over View

The display is a TFT active matrix electrophoretic display, with associated interface and control logic, and a reference system design . The 8" active area contains  $768 \times 1024$  pixels, and has 1-4 bit full display capabilities. An integrated circuit contains interface, timing control logic are supplied with each panel.

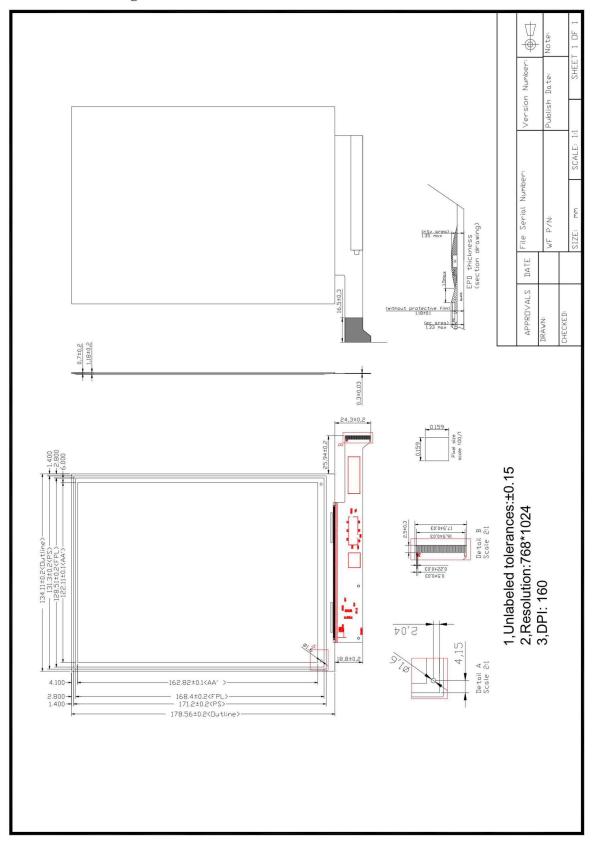
#### 2. Features

- High contrast TFT electrophoretic
- High reflectance
- Ultra wide viewing angle
- Ultra low power consumption
- Pure reflective mode
- Bi-stable
- Commercial temperature range
- Landscape, portrait mode
- Antiglare hard-coated front-surface

### 3. Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	8	Inch	
Display Resolution	768(H)×1024(V)	Pixel	Dpi:160
Active Area	122.11 (H)×162.82 (V)	mm	
Pixel Pitch	0.159×0.159	mm	
Pixel Configuration	Rectangle		
Outline Dimension	134.11(H)×178.56(V) ×1.18(D)	mm	
Weight	57±5	g	

## 4. Mechanical Drawing of EPD module



# 5. Input/Output Terminals

## 5-1) Pin out List

Pin#	Single	Description
1	VNEG	Negative power supply source driver
2	VEE	Negative power supply gate driver
3	VSS	Ground
4	NC	No connection
5	NC	No connection
6	VDD	Digital power supply drivers
7	VSS	Ground
8	CKH	Clock source driver
9	VSS	Ground
10	LEH	Latch enable source driver
11	OEH	Output enable source driver
12	STH	Start pulse gate driver
13	D0	Data signal source driver
14	D1	Data signal source driver
15	D2	Data signal source driver
16	D3	Data signal source driver
17	D4	Data signal source driver
18	D5	Data signal source driver
19	D6	Data signal source driver
20	D7	Data signal source driver
21	VCOM	Common voltage control
22	NC	NO Connection
23	NC	NO Connection
24	NC	NO Connection
25	NC	NO Connection
26	VSS	Ground
27	MODE1	Output mode selection gate driver
28	CKV	Clock gate driver
29	STV	Start pulse gate driver
30	NC	NO Connection
31	BORDER	Border connection
32	VSS	Ground
33	VPOS	Positive power supply source driver
34	VGG	Positive power supply gate driver

## 6. Electrical Characteristics

## 6-1) Absolute maximum rating

Parameter	Symbol	Rating	Unit
Logic Supply Voltage	VDD	-0.3 to +7	V
Positive Supply Voltage	$V_{POS}$	-0.3 to +18	V
Negative Supply Voltage	$V_{ m NEG}$	-0.3 to -18	V
Max .Drive Voltage Range	$V_{POS}$ - $V_{NEG}$	36	V
Supply Voltage	VGG	-0.3 to +45	V
Supply Voltage	VEE	-25.0 to +0.3	V
Supply Range	VGG-VEE	-0.3 to +45	V
Operating Temp. range	$T_{OPR}$	0 to +50	$^{\circ}$
Storage Temp. range	$T_{STG}$	-25 to +70	$^{\circ}$

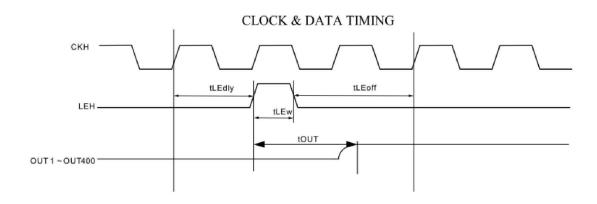
## 6-2) Panel DC Characteristics

Parameter	Symbol	Conditions	Min	Тур	Max	Unit
Single ground	$V_{SS}$		-	0	-	V
Lagia Cymply Valtaga	$V_{DD}$		3.0	3.3	3.6	V
Logic Supply Voltage	$I_{VDD}$	$V_{DD}=3.3V$	-	1.5	-	mA
Gate Negative Supply	$V_{EE}$		-21	-20	-19	V
Gate Negative Supply	$I_{\rm EE}$	$V_{EE}$ =-20 $V$	-	3.0	-	mA
Gate Positive Supply	$V_{GG}$		21	22	23	V
Gate Positive Supply	$I_{\rm EE}$	$V_{GG}=22V$	-	0.6	-	mA
Source Negative Supply	V <sub>NEG</sub>		-15.4	-15	-14.6	V
Source Negative Suppry	I <sub>NEG</sub>	$V_{NEG} = -15V$	-	37.6	75.2	mA
Cormon Donitivo Cremity	V <sub>POS</sub>		14.6	15	15.4	V
Source Positive Supply	I <sub>POS</sub>	$V_{POS} = 15V$	-	30	-	mA
Border Supply	V	$V_{POS}=15V$	14.6	15	15.4	V
Border Supply	V <sub>Border</sub>	$V_{NEG}=-15V$	-15.4	-15	-14.6	V
Asymmetry Source	V <sub>ASYM</sub>	$V_{POS} + V_{NEG} \\$	-800	0	800	mV
Common voltage	$V_{COM}$		-2.5	Adjusted	-0.5	V
Common voltage	$I_{COM}$		-	0.2	-	mA
Maximum power panel	P <sub>MAX</sub>		-	-	TBD	mW
Standby power panel	P <sub>STBY</sub>		-	-	TBD	mW
Typical power panel	P <sub>TYP</sub>		-	TBD	( <del>-</del> )	mW
Operating temperature			0	-	50	$^{\circ}\mathbb{C}$
Storage temperature			-25	-	70	$^{\circ}$ C
Image update time at 25 °C	-	-	-	1	-	Sec

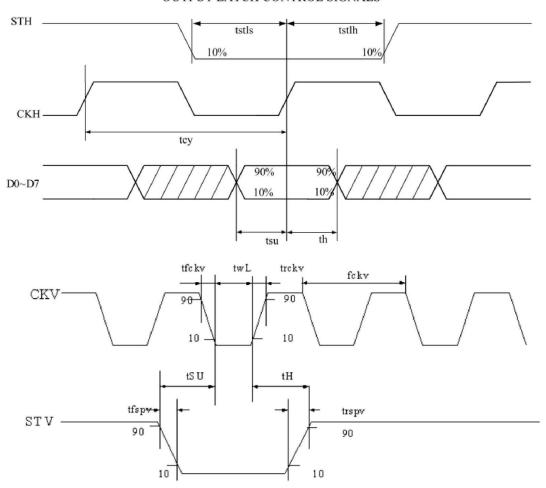
## 6-3) Panel AC Characteristics

VDD=3.0V to 3.6V, unless otherwise specified.

Parameter	Symbol	Min.	Тур.	Max.	unit
Clock frequency	fckv	-	-	200	kHz
Minimum "L"clock pulse width	twL	0.5	-	-	us
Clock rise time	trckv	-	-	100	ns
Clock fall time	tfckv	-	-	100	ns
Data setup time	tSU	100	-	.=	ns
Data hold time	tH	300	-	-	ns
Pulse rise time	trspv	-	-	100	ns
Pulse fall time	tfspv	-	-	100	ns
Clock CKH cycle time	tcy	40	-	DC	ns
D0D7setup time	tsu	8	-	-	ns
D0D7 hold time	th	8	-	-	ns
STH setup time	tstls	100	-	-	ns
STH hold time	tstls	10	-	-	
LEH on delay time	tLEdly	40	-	-	ns
LEH high-level pulse width	tLEW	40	-	-	ns
LEH off delay time	tLEoff	40	-	-	ns
Output setting time to +/-30mV (V <sub>load</sub> =200pF)	tout	-	-	12	us



### OUTPUT LATCH CONTROL SIGNALS



## 6-4) Power Consumption

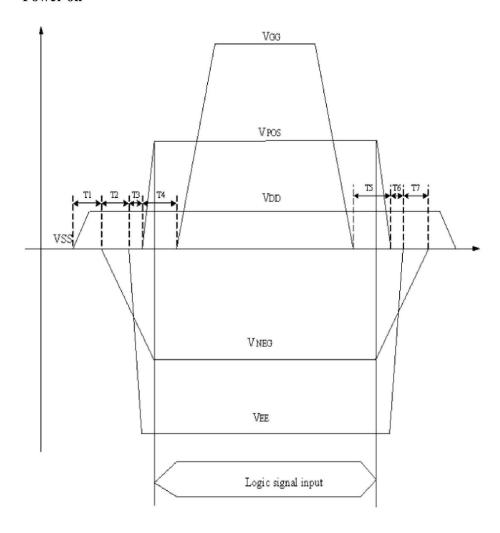
Parameter	Symbol	Conditions	TYP	Max	Unit	Remark
Maximum Panel power consumption	-	-	-	TBD	mW	-
Power consumption in standby mode	-	-	-	TBD	mW	ī
Panel power consumption during update	-	-	TBD	-	mW	-

## 7. Power on sequence

Power Rails must be sequenced in following order:

- 1. VSS→VDD→VNEG→VPOS (Source driver)
- 2. VEE→VGG (Gate drive)

### Power on



T1: 100us (min)

T2: 0us (min)

T3: 1000us (min)

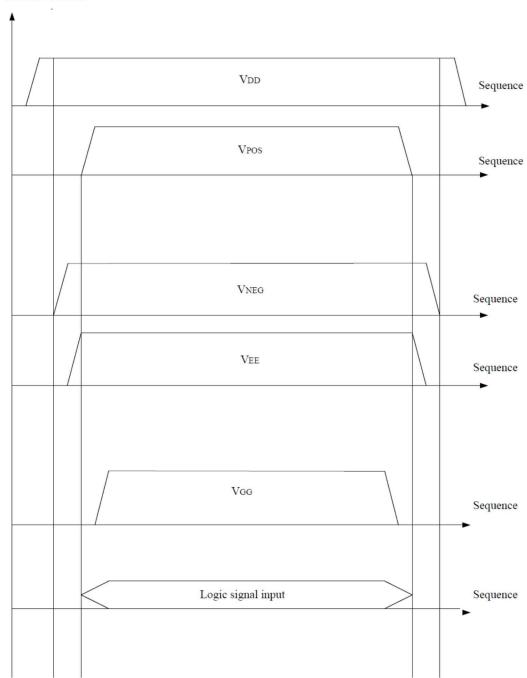
T4: 0us (min)

T5: 0us (min)

T6: 0us (min)

T7: 0us (min)

### **Power Down**



### 8. Optical characteristics

#### 8-1) Specifications

Measurements are made with that the illumination is under an angle of 45 degrees, the detection is perpendicular unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYPE	MAX	UNIT	Note
R	Reflectance	White	30	35		0/	Note
K	Reflectance	w mie	30	33	-	%	8-1
Gn	N <sub>th</sub> Grey Level	-	-	$DS+(WS-DS) \times n/(m-1)$	-	L*	-
CR	Contrast Ratio	indoor	8		-	-	-
$T_{update}$	Update time	25℃	-	1	-	Sec	-
Panel's life		0°C~50°C		1000000 times or 5 years			Note
ranei sine		0 0~30 0		1000000 times or 5 years	-	-	8-2

WS: White state; DS: Dark state, Gray state from Dark to White: DS, G1, G2..., Gn..., Gm-2, WS m:4,8,16 when 2,3,4 bit mode.

Note 8-1: Luminance meter: Eye – One Pro Spectrophotometer

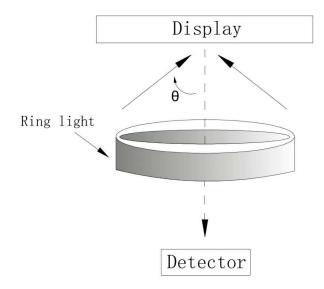
Note 8-2: Panel life will not guaranteed when work in temperature below 0 degree or above 50 degree. Each update interval time should be minimum at 180 seconds.

### 8-2) Definition of contrast ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (R1) and the reflectance in a dark area (Rd)():

R1: white reflectance Rd: dark reflectance

CR = R1/Rd

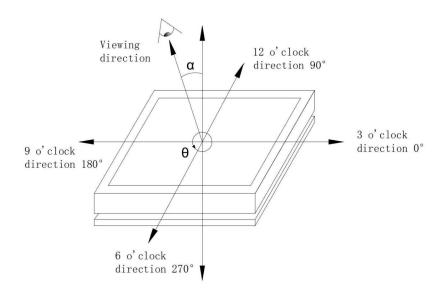


### 8-3) Reflection Ratio

The reflection ratio is expressed as:

 $R = Reflectance Factor_{white board} x (L_{center} / L_{white board})$ 

 $L_{center}$  is the luminance measured at center in a white area (R=G=B=1).  $L_{white\ board}$  is the luminance of a standard white board. Both are measured with equivalent illumination source. The viewing angle shall be no more than 2 degrees.



### 8-4) Bi-stability

1. The value of Contrast ratio in different time as follows:

Bi-stability	Result
250 hours	CR >8
500 hours	CR >8
750 hours	CR >7.5
1000 hours	CR >7

### 9. HANDLING, SAFETY AND ENVIROMENTAL REQUIREMENTS

#### WARNING

The display glass may break when it is dropped or bumped on a hard surface. Handle with care.

Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

#### **CAUTION**

The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.

Disassembling the display module can cause permanent damage and invalidate the warranty agreements.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

Data sheet status					
Product specification	The data sheet contains final product specifications.				
Limiting values					

Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134).

Stress above one or more of the limiting values may cause permanent damage to the device.

These are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

#### **Application information**

Where application information is given, it is advisory and dose not form part of the specification.

Product Environmental certification	
ROHS	

# 10. Reliability test

	TEST	CONDITION	METHOD	REMARK
1	High-Temperatu re Operation	T = 50°C, RH=35% for 240 hrs	When the experimental cycle finished, the EPD samples will be taken out from the high temperature environmental chamber and set aside for a few minutes. As EPDs return to room temperature, testers will observe the appearance, and test electrical and optical performance based on standard # IEC 60 068-2-2Bp.	When experiment finished, the EPD must meet electrical and optical performance standards.
2	Low-Temperatu re Operation	T = 0°C for 240 hrs	When the experimental cycle finished, the EPD samples will be taken out from the low temperature environmental chamber and set aside for a few minutes. As EPDs return room temperature, testers will observe the appearance, and test electrical and optical performance based on standard # IEC 60 068-2-2Ab.	When experiment finished, the EPD must meet electrical and optical performance standards.
3	High-Temperatu re Storage	T = +70°C, RH=35% for 240 hrs Test in white pattern	When the experimental cycle finished, the EPD samples will be taken out from the high temperature environmental chamber and set aside for a few minutes. As EPDs return to room temperature, testers will observe the appearance, and test electrical and optical performance based on standard # IEC 60 068-2-2Bp.	When experiment finished, the EPD must meet electrical and optical performance standards.
4	Low-Temperatu re Storage	T = -25°C for 240 hrs Test in white pattern	When the experimental cycle finished, the EPD samples will be taken out from the low temperature environmental chamber and set aside for a few minutes. As EPDs return to room temperature, testers will observe the appearance, and test electrical and optical performance based on standard # IEC 60 068-2-2Ab	When experiment finished, the EPD must meet electrical and optical performance standards.
5	High Temperature, High- Humidity Operation	T=+40°C, RH=80% for240hrs	When the experimental cycle finished, the EPD samples will be taken out from the environmental chamber and set aside for a few minutes. As EPDs return to room temperature, testers will observe the appearance, and test electrical and optical performance based on standard # IEC 60 068-2-3CA.	When experiment finished, the EPD must meet electrical and optical performance standards.
6	High Temperature, High- Humidity Storage	T=+60°C, RH=80% for240hrs Test in white pattern	When the experimental cycle finished, the EPD samples will be taken out from the environmental chamber and set aside for a few minutes. As EPDs return to room temperature, testers will observe the appearance, and test electrical and optical performance based on standard # IEC 60 068-2-3CA.	When experiment finished, the EPD must meet electrical performance standards.
7	Temperature Cycle	[-25°C 30mins]→ [+70°C, RH=35% 30mins], 70cycles, Test in white	1. Samples are put in the Temp & Humid. Environmental Chamber. Temperature cycle starts with -25°C, storage period 30 minutes. After 30 minutes, it needs 30min to let temperature rise to 70°C. After 30min, temperature will be adjusted to 70°C, RH=35% and storage period	When experiment finished, the EPD must meet electrical and optical performance

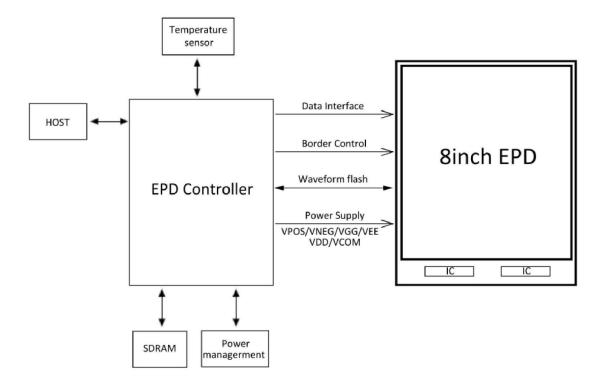
		pattern	is 30 minutes. After 30 minutes, it needs 30min to let	standards.
			temperature rise to -25°C. One temperature cycle	
			(2hrs) is complete.	
			2. Temperature cycle repeats 70 times.	
			3. When 70 cycles finished, the samples will be taken out	
			from experiment chamber and set aside a few minutes.	
			As EPDs return to room temperature, tests will	
			observe the appearance, and test electrical and optical	
			performance based on standard # IEC 60 068-2-14NB.	
8	UV exposure	765 W/m <sup>2</sup> for 168	Standard # IEC 60 068-2-5 Sa	
8	Resistance	hrs,40°C	Standard # IEC 60 008-2-3 Sa	
	Electrostatic	Machine model:		
9		discharge +/-250V,	Standard # IEC61000-4-2	
	discharge	0Ω,200pF		
		1.04G,Frequency:		
	Package	10~500Hz		
10	Vibration	Direction : X,Y,Z	Full packed for shipment	
	vibration	Duration:1hours		
		in each direction		
		Drop from height		
		of 122 cm on		
		Concrete surface		
11	Package Drop	Drop sequence:1	Full packed for shipmont	
11	Impact	corner, 3edges,	Full packed for shipment	
		6face		
		One drop for		
		each.		

Actual EMC level to be measured on customer application.

Note: (1) The protective film must be removed before temperature test.

(2) In order to make sure the display module can provide the best display quality, the update should be made after putting the display module in stable temperature environment for 4 hours at  $25^{\circ}$ C.

## 11. Block Diagram



#### 12. Point and line standard

#### **Shipment Inseption Standard**

Part-A: Active area Part-B: Border area

Equipment: Electrical test fixture, Point gauge

Outline dimension:

134.11(H)×178.56(V)×1.18(D)

Unit: mm

Environment	Temperature	Humidity	Illuminan	ce Distance	Time	Angle	
	23±2℃	55±	1200~	300 mm	35 Sec		
		5%RH	1500Lux				
Name	Causes	Spot size			Part-A	Part-B	
Spot	B/W spot in glass or protection sheet, foreign mat. Pin hole	D ≤ 0.25mm			Ignore	Ignore	
		$0.25$ mm $< D \leqslant 0.4$ mm			4		
		$0.4$ mm $< D \leqslant 0.5$ mm			1		
		0.5mm < D			0		
Scratch or line defect	Scratch on glass or	Leng	gth	Width	Part-A		
	Scratch on FPL or	L ≤2.0mm		W≤0.2 mm	Ignore	T	
	Particle is Protection	2.0 mm < L	≤ 8.0mm	0.2 mm <w≤ 0.5mm<="" td=""><td>2</td><td colspan="2">Ignore</td></w≤>	2	Ignore	
	sheet.	8.0 mn	n < L	0.5mm < W	0		
Air bubble	Air bubble	D1, D2 ≤ 0.25 mm			Ignore	Ignore	
		0.25 mm < D1,D2 ≤ 0.4mm			4		
		0.4mm < D1, D2			0		
Side Fragment	X X						
	X≤6mm, Y≤1mm & display is ok, Ignore						

Remarks: Spot define: That only can be seen under WS or DS defects.

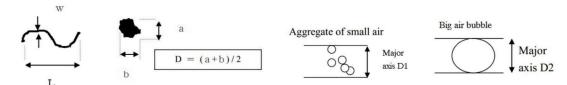
Any defect which is visible under gray pattern or transition process but invisible under black and white is disregarded.

Here is definition of the "Spot" and "Scratch or line defect".

Spot: W > 1/4L Scratch or line defect:  $W \le 1/4L$ 

Definition for L/W and D (major axis)

FPC bonding area pad doesn't allowed visual inspection.



Note: AQL = 0.4

# 13. Packing

