3.71 inch
E-paper Display Series

BLGDEW0371W7

1. Over View

The display is a TFT active matrix electrophoretic display, with interface and a reference system design. The 3.71" active area contains 416×240 pixels, and has 1-bit white/black full display capabilities. An integrated circuit contains gate buffer, source buffer, interface, timing control logic, oscillator, DC-DC, SRAM, LUT, VCOM, and border are supplied with each panel.

2. Features

- High contrast
- High reflectance
- Ultra wide viewing angle
- Ultra low power consumption
- Pure reflective mode
- Bi-stable
- Commercial temperature range
- Landscape, portrait mode
- Antiglare hard-coated front-surface
- Low current deep sleep mode
- On chip display RAM
- Waveform stored in On-chip OTP
- Serial peripheral interface available
- On-chip oscillator
- On-chip booster and regulator control for generating VCOM, Gate and source driving voltage
- I^2C Signal Master Interface to read external temperature sensor
- Available in COG package IC thickness 300um

3. Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	3.71	Inch	
Display Resolution	416(H)×240(V)	Pixel	Dpi: 130
Active Area	81.536(H)×47.04(V)	mm	
Pixel Pitch	0.196×0.196	mm	
Pixel Configuration	Square		
Outline Dimension	92.99(H)×53(V) ×1.18(D)	mm	
Weight	TBD	g	

5. Input/Output Terminals

5-1) Pin out List

Pin #	Type	Single	Description	Remark
1		NC	No connection and do not connect with other NC pins	Keep Open
2	O	GDR	N-MOS gate control	
3	P	RESE	Current Sense Input for Control Loop	
4		NC	No connection and do not connect with other NC pins	Keep Open
5	I/O	VDHR	Positive source driver voltage for Red	
6	O	TSCL	I^2C Interface to digital temperature sensor Clock pin	
7	I/O	TSDA	I^2C Interface to digital temperature sensor Date pin	
8	I	BS1	Bus selection pin	Note 5-5
9	O	BUSY	Busy state output pin	Note 5-4
10	I	RES #	Reset	Note 5-3
11	I	D/C #	Data /Command control pin	Note 5-2
12	I	CS #	Chip Select input pin	Note 5-1
13	I	SCL	Serial clock pin (SPI)	
14	I/O	SDA	Serial data pin (SPI)	
15	I	VCI	Power Supply pin for the chip	
16	PWR	VDDIO	IO power	
17	PWR	GND	Digital Ground	
18	PWR	VDD	Digital power	
19	PWR	VPP	OTP program power (7.75V)	
20	I/O	VSH	Positive source driver voltage	
21	I/O	VGH	Positive Gate voltage	
22	I/O	VSL	Negative Source driving voltage	
23	I/O	VGL	Negative Gate voltage	
24	O	VCOM	VCOM output	

Note 5-1: This pin (CS#) is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled Low.

Note 5-2: This pin (D/C#) is Data/Command control pin connecting to the MCU. When the pin is pulled HIGH, the data will be

interpreted as data. When the pin is pulled Low, the data will be interpreted as command.

Note 5-3: This pin (RES#) is reset signal input. The Reset is active Low.

Note 5-4: This pin (BUSY) is Busy state output pin. When Busy is low, the operation of chip should not be interrupted and any commands should not be issued to the module. The driver IC will put Busy pin low when the driver IC is working such as:

- Outputting display waveform; or
- Programming with OTP
- Communicating with digital temperature sensor

Note 5-5: This pin (BS1) is for 3-line SPI or 4-line SPI selection. When it is "Low", 4-line SPI is selected. When it is "High", 3-line SPI (9 bits SPI) is selected. Please refer to below Table.

Table: Bus interface selection

BS1	MPU Interface
L	4-lines serial peripheral interface (SPI)
H	3-lines serial peripheral interface (SPI) – 9 bits SPI

6. Command Table

W/R: 0: Write cycle 1: Read cycle C/D: 0: Command 1: Data D7~D0: -: Don't care #: Valid Data

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
1	Panel Setting (PSR)	0	0	0	0	0	0	0	0	0	0		00h
		0	1	--	--	#	#	#	#	#	#	REG, KW/R, UD, SHL, SHD_N, RST_N	0Fh
2	Power Setting (PWR)	0	0	0	0	0	0	0	0	0	1		01h
		0	1	--	--	--	--	--	#	#	#	VSR_EN, VS_EN, VG_EN	03h
		0	1	--	--	--	--	#	#	#	#	VCOM_HV, VG_LVL[2:0]	00h
		0	1	--	--	#	#	#	#	#	#	VDH_LVL[5:0]	26h
		0	1	--	--	#	#	#	#	#	#	VDL_LVL[5:0]	26h
		0	1	--	--	#	#	#	#	#	#	VDHR_LVL[5:0]	03h
3	Power OFF (POF)	0	0	0	0	0	0	0	0	1	0		02h
4	Power OFF Sequence Setting (PFS)	0	0	0	0	0	0	0	0	1	1		03h
		0	1	--	--	#	#	--	--	--	--	T_VDS_OFF[1:0]	00h
5	Power ON (PON)	0	0	0	0	0	0	0	1	0	0		04h
6	Power ON Measure (PMES)	0	0	0	0	0	0	0	1	0	1		05h
7	Booster Soft Start (BTST)	0	0	0	0	0	0	0	1	1	0		06h
		0	1	#	#	#	#	#	#	#	#	BT_PHA[7:0]	17h
		0	1	#	#	#	#	#	#	#	#	BT_PHB[7:0]	17h
		0	1	--	--	#	#	#	#	#	#	BT_PHC[5:0]	17h
8	Deep sleep (DSLP)	0	0	0	0	0	0	0	1	1	1		07h
		0	1	1	0	1	0	0	1	0	1	Check code	A5h
9	Display Start Transmission 1 (DTM1, White/Black Data) (x-byte command)	0	0	0	0	0	1	0	0	0	0	K/W or OLD Pixel Data (240x512):	10h
		0	1	#	#	#	#	#	#	#	#	KPXL[1:8]	-
		0	1	:	:	:	:	:	:	:	:	:	:
		0	1	#	#	#	#	#	#	#	#	KPXL[n-7:n]	-
10	Data Stop (DSP)	0	0	0	0	0	1	0	0	0	1		11h
		1	1	#	--	--	--	--	--	--	--		00h
11	Display Refresh (DRF)	0	0	0	0	0	1	0	0	1	0		12h
12	Display Start transmission 2 (DTM2, Red Data) (x-byte command)	0	0	0	0	0	1	0	0	1	1	Red or NEW Pixel Data (240X512):	13h
		0	1	#	#	#	#	#	#	#	#	RPXL[1:8]	-
		0	1	:	:	:	:	:	:	:	:	:	:
		0	1	#	#	#	#	#	#	#	#	RPXL[n-7:n]	-
13	Auto Sequence (AUTO)	0	0	0	0	0	1	0	1	1	1		17h
		0	1	1	0	1	0	0	1	0	1	Check code	A5h
14	VCOM LUT (LUTC) (61-byte command, structure of bytes 2~7 repeated 10 times)	0	0	0	0	1	0	0	0	0	0		20h

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
15	W2W LUT (LUTWW) (43-byte command, structure of bytes 2~7 repeated 7 times)	0	0	0	0	1	0	0	0	0	1		21h
16	K2W LUT (LUTKW / LUTR) (61-byte command, structure of bytes 2~7 repeated 10 times)	0	0	0	0	1	0	0	0	1	0		22h
17	W2K LUT (LUTWK / LUTW) (61-byte command, structure of bytes 2~7 repeated 10 times)	0	0	0	0	1	0	0	0	1	1		23h
18	K2K LUT (LUTKK / LUTK) (61-byte command, structure of bytes 2~7 repeated 10 times)	0	0	0	0	1	0	0	1	0	0		24h
19	Border LUT (43-byte command, structure of bytes 2~7 repeated 7 times)	0	0	0	0	1	0	0	1	0	1		25h
20	LUT option (LUTOPT)	0	0	0	0	1	0	1	0	1	0		2Ah
		0	1	#	#	--	--	--	--	--	--	STATE_XON[9:8]	00h
		0	1	#	#	#	#	#	#	#	#	STATE_XON[7:0]	00h
21	KW LUT option (KWOPT)	0	0	0	0	1	0	1	0	1	1		2Bh
		0	1	--	--	--	--	--	--	#	#	ATRED, NORED	00h
		0	1	#	#	--	--	--	--	--	--	KWE[9:8]	00h
		0	1	#	#	#	#	#	#	#	#	KWE[7:0]	00h
22	PLL control (PLL)	0	0	0	0	1	1	0	0	0	0		30h
		0	1	--	--	--	--	#	#	#	#	FRS[3:0]	04h
23	Temperature Sensor Calibration (TSC)	0	0	0	1	0	0	0	0	0	0		40h
		1	1	#	#	#	#	#	#	#	#	D[10:3] / TS[7:0]	00h
		1	1	#	#	#	--	--	--	--	--	D[2:0] / -	00h
24	Temperature Sensor Selection (TSE)	0	0	0	1	0	0	0	0	0	1		41h
		0	1	#	--	--	--	#	#	#	#	TSE,TO[3:0]	00h
25	Temperature Sensor Write (TSW)	0	0	0	1	0	0	0	0	1	0		42h
		0	1	#	#	#	#	#	#	#	#	WATTR[7:0]	00h
		0	1	#	#	#	#	#	#	#	#	WMSB[7:0]	00h
		0	1	#	#	#	#	#	#	#	#	WLSB[7:0]	00h
26	Temperature Sensor Read (TSR)	0	0	0	1	0	0	0	0	1	1		43h
		1	1	#	#	#	#	#	#	#	#	RMSB[7:0]	00h
		1	1	#	#	#	#	#	#	#	#	RLSB[7:0]	00h

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
27	Panel Break Check (PBC)	0	0	0	1	0	0	0	1	0	0		44h
		1	1	--	--	--	--	--	--	--	#	PSTA	00h
28	VCOM and data interval setting (CDI)	0	0	0	1	0	1	0	0	0	0		50h
		0	1	#	--	#	#	--	--	#	#	BDZ, BDV[1:0], DDX[1:0]	31h
		0	1	--	--	--	--	#	#	#	#	CDI[3:0]	07H
29	Lower Power Detection (LPD)	0	0	0	1	0	1	0	0	0	1		51h
		1	1	--	--	--	--	--	--	--	#	LPD	01h
30	End Voltage Setting (EVS)	0	0	0	1	0	1	0	0	1	0		52h
		0	1	--	--	--	--	#	--	#	#	VCEND, BDEND[1:0]	02h
31	TCON setting (TCON)	0	0	0	1	1	0	0	0	0	0		60h
		0	1	#	#	#	#	#	#	#	#	S2G[3:0], G2S[3:0]	22h
32	Resolution setting (TRES)	0	0	0	1	1	0	0	0	0	1		61h
		0	1	#	#	#	#	#	0	0	0	HRES[7:3]	F0h
		0	1	--	--	--	--	--	--	#	#	VRES[9:0]	02h
		0	1	#	#	#	#	#	#	#	#		00h
33	Gate/Source Start setting (GSST)	0	0	0	1	1	0	0	1	0	1		65h
		0	1	#	#	#	#	#	0	0	0	HST[7:3]	00h
		0	1	--	--	--	--	--	--	--	#	VST[8:0]	00h
		0	1	#	#	#	#	#	#	#	#		00h
34	Revision (REV)	0	0	0	1	1	1	0	0	0	0		70h
		1	1	#	#	#	#	#	#	#	#	LUT_REV[7:0]	FFh
		1	1	--	--	--	--	#	#	#	#	CHIP_REV[3:0]	0Ch
35	Get Status (FLG)	0	0	0	1	1	1	0	0	0	1		71h
		1	1	--	#	#	#	#	#	#	#	PTL_FLAG ,I2C_ERR, I2C_BUSYN, DATA_FLAG, PON, POF, BUSY_N	13h
36	Auto Measurement VCOM (AMV)	0	0	1	0	0	0	0	0	0	0		80h
		0	1	--	--	#	#	#	#	#	#	AMVT[1:0], XON,AMVS, AMV, AMVE	10h
37	Read VCOM Value (VV)	0	0	1	0	0	0	0	0	0	1		81h
		1	1	--	--	#	#	#	#	#	#	VV[5:0]	00h
38	VCOM_DC Setting (VDCS)	0	0	1	0	0	0	0	0	1	0		82h
		0	1	--	--	#	#	#	#	#	#	VDCS[5:0]	00h
39	Partial Window (PTL)	0	0	1	0	0	1	0	0	0	0		90h
		0	1	#	#	#	#	#	0	0	0	HRST[7:3]	00h
		0	1	#	#	#	#	#	1	1	1	HRED[7:3]	EFh
		0	1	--	--	--	--	--	--	--	#	VRST[8:0]	00h
		0	1	#	#	#	#	#	#	#	#		00h
		0	1	--	--	--	--	--	--	--	#	VRED[8:0]	01h
		0	1	#	#	#	#	#	#	#	#		FFh
		0	1	--	--	--	--	--	--	--	#	PT_SCAN	01h

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
40	Partial In (PTIN)	0	0	1	0	0	1	0	0	0	1		91h
41	Partial Out (PTOUT)	0	0	1	0	0	1	0	0	1	0		92h
42	Program Mode (PGM)	0	0	1	0	1	0	0	0	0	0		A0h
43	Active Programming (APG)	0	0	1	0	1	0	0	0	0	1		A1h
44	Read OTP (ROTP)	0	0	1	0	1	0	0	0	1	0		A2h
		1	1	--	--	--	--	--	--	--	--	Read Dummy	N/A
		1	1	#	#	#	#	#	#	#	#	Data of Address = 000h	N/A
		1	1	:	:	:	:	:	:	:	:	:	N/A
		1	1	#	#	#	#	#	#	#	#	Data of Address = n	N/A
45	Cascade Setting (CCSET)	0	0	1	1	1	0	0	0	0	0		E0h
		0	1	--	--	--	--	--	--	#	#	TSFIX, CCEN	00h
46	Power Saving (PWS)	0	0	1	1	1	0	0	0	1	1		E3h
		0	1	#	#	#	#	#	#	#	#	VCOM_W[3:0], SD_W[3:0]	00h
47	LVD Voltage Select (LVSEL)	0	0	1	1	1	0	0	1	0	0		E4h
		0	1	--	--	--	--	--	--	#	#	LVD_SEL[1:0]	03h
48	Force Temperature (TSSET)	0	0	1	1	1	0	0	1	0	1		E5h
		0	1	#	#	#	#	#	#	#	#	TS_SET[7:0]	00h

(1) Panel Setting (PSR) (Register: R00H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Setting the panel	0	0	0	0	0	0	0	0	0	0
	0	1	-	-	REG-	KW/R	UD	SHL	SHD_N	RST_N

REG: LUT selection

0: LUT from OTP. (Default)

1: LUT from register.

KW/R: Black / White / Red

0: Pixel with Black/White/Red, KWR mode. (Default)

1: Pixel with Black/White, KW mode.

UD: Gate Scan Direction

0: Scan down. First line to last line: Gn-1 → Gn-2 → Gn-3 → … → G0

1: Scan up. (default) First line to last line: G0 → G1 → G2 → … → Gn-1

SHL: Source Shift direction

0: Shift left First data to last data: Sn-1 → Sn-2 → Sn-3 → … → S0

1: Shift right. (default) First data to last data: S0 → S1 → S2 → … → Sn-1

SHD_N: Booster Switch

0: Booster OFF, register data are kept, and SEG/BG/VCOM are kept 0V or floating.

1: Booster ON (Default)

When SHD_N become LOW, charge pump will be turned OFF, register and SRAM data will keep until VDD OFF, And Source/Gate/Border/VCOM will be released to floating.

RST_N: Soft Reset

0: Reset. Booster OFF, Register data are set to their default values, all drivers will be reset, and all functions will be disabled. Source/Gate/Border/VCOM will be released to floating.

1: No effect (Default).

(2) Power Setting (PWR) (R01H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Selecting Internal/External Power	0	0	0	0	0	0	0	0	0	1
	0	1	-	-	-	-	-	VSR_EN	VS_EN	VG_EN
	0	1	-	-	-	-	VCOM_HV	VG_LV[2:0]		
	0	1	-	-	VDH_LVL[5:0]					
	0	1	-	-	VDL_LVL[5:0]					
	0	1	-	-	VDHR_LVL[5:0]					

VSR_EN: Source LV power selection

0 : External source power from VDHR pins

1 : Internal DC/DC function for generating VDHR. (Default)

VS_EN: Source power selection

0 : External source power from VDH/VDL pins

1 : Internal DC/DC function for generating VDH/VDL. (Default)

VG_EN: Gate power selection

0 : External gate power from VGH/VGL pins

1 : Internal DC/DC function for generating VGH/VGL. (Default)

VCOM_HV: VCOM Voltage Level

0 : VCOMH=VDH+VCOM_DC, VCOML=VDL+VCOM_DC. (Default)

1 : VCOMH=VGH, VCOML=VGL

VG_LVL[2:0]: VGH / VGL Voltage Level selection.

VG_LVL[2:0]	VGH/VGL Voltage Level
000	VGH=9V, VGL= -9V
001	VGH=10V, VGL= -10V
010	VGH=11V, VGL= -11V
011	VGH=12V, VGL= -12V
100	VGH=17V, VGL= -17V
101	VGH=18V, VGL= -18V
110	VGH=19V, VGL= -19V
111 (Default)	VGH=20V, VGL= -20V

VDH_LVL[5:0]: Internal VDH power selection for K/W pixel.(Default value: 100110b)

VDH_LVL	Voltage	VDH_LVL	Voltage	VDH_LVL	Voltage	VDH_LVL	Voltage
000000	2.4 V	010001	5.8 V	100010	9.2 V	110011	12.6 V
000001	2.6 V	010010	6.0 V	100011	9.4 V	110100	12.8 V
000010	2.8 V	010011	6.2 V	100100	9.6 V	110101	13.0 V
000011	3.0 V	010100	6.4 V	100101	9.8 V	110110	13.2 V
000100	3.2 V	010101	6.6 V	100110	10.0 V	110111	13.4 V
000101	3.4 V	010110	6.8 V	100111	10.2 V	111000	13.6 V
000110	3.6 V	010111	7.0 V	101000	10.4 V	111001	13.8 V
000111	3.8 V	011000	7.2 V	101001	10.6 V	111010	14.0 V
001000	4.0 V	011001	7.4 V	101010	10.8 V	111011	14.2 V
001001	4.2 V	011010	7.6 V	101011	11.0 V	111100	14.4 V
001010	4.4 V	011011	7.8 V	101100	11.2 V	111101	14.6 V
001011	4.6 V	011100	8.0 V	101101	11.4 V	111110	14.8 V
001100	4.8 V	011101	8.2 V	101110	11.6 V	111111	15.0 V
001101	5.0 V	011110	8.4 V	101111	11.8 V		
001110	5.2 V	011111	8.6 V	110000	12.0 V		
001111	5.4 V	100000	8.8 V	110001	12.2 V		
010000	5.6 V	100001	9.0 V	110010	12.4 V		

VDL_LVL[5:0]: Internal VDL power selection for K/W pixel. (Default value: 100110b)

VDL_LVL	Voltage	VDL_LVL	Voltage	VDL_LVL	Voltage	VDL_LVL	Voltage
000000	-2.4 V	010001	-5.8 V	100010	-9.2 V	110011	-12.6 V
000001	-2.6 V	010010	-6.0 V	100011	-9.4 V	110100	-12.8 V
000010	-2.8 V	010011	-6.2 V	100100	-9.6 V	110101	-13.0 V
000011	-3.0 V	010100	-6.4 V	100101	-9.8 V	110110	-13.2 V
000100	-3.2 V	010101	-6.6 V	100110	-10.0 V	110111	-13.4 V
000101	-3.4 V	010110	-6.8 V	100111	-10.2 V	111000	-13.6 V
000110	-3.6 V	010111	-7.0 V	101000	-10.4 V	111001	-13.8 V
000111	-3.8 V	011000	-7.2 V	101001	-10.6 V	111010	-14.0 V
001000	-4.0 V	011001	-7.4 V	101010	-10.8 V	111011	-14.2 V
001001	-4.2 V	011010	-7.6 V	101011	-11.0 V	111100	-14.4 V
001010	-4.4 V	011011	-7.8 V	101100	-11.2 V	111101	-14.6 V
001011	-4.6 V	011100	-8.0 V	101101	-11.4 V	111110	-14.8 V
001100	-4.8 V	011101	-8.2 V	101110	-11.6 V	111111	-15.0 V
001101	-5.0 V	011110	-8.4 V	101111	-11.8 V		
001110	-5.2 V	011111	-8.6 V	110000	-12.0 V		
001111	-5.4 V	100000	-8.8 V	110001	-12.2 V		
010000	-5.6 V	100001	-9.0 V	110010	-12.4 V		

VDHR_LVL[5:0]: Internal VDHR power selection for Red pixel. (Default value: 000011b)

VDHR_LVL	Voltage	VDHR_LVL	Voltage	VDHR_LVL	Voltage	VDHR_LVL	Voltage
000000	2.4 V	010001	5.8 V	100010	9.2 V	110011	12.6 V
000001	2.6 V	010010	6.0 V	100011	9.4 V	110100	12.8 V
000010	2.8 V	010011	6.2 V	100100	9.6 V	110101	13.0 V
000011	3.0 V	010100	6.4 V	100101	9.8 V	110110	13.2 V
000100	3.2 V	010101	6.6 V	100110	10.0 V	110111	13.4 V
000101	3.4 V	010110	6.8 V	100111	10.2 V	111000	13.6 V
000110	3.6 V	010111	7.0 V	101000	10.4 V	111001	13.8 V
000111	3.8 V	011000	7.2 V	101001	10.6 V	111010	14.0 V
001000	4.0 V	011001	7.4 V	101010	10.8 V	111011	14.2 V
001001	4.2 V	011010	7.6 V	101011	11.0 V	111100	14.4 V
001010	4.4 V	011011	7.8 V	101100	11.2 V	111101	14.6 V
001011	4.6 V	011100	8.0 V	101101	11.4 V	111110	14.8 V
001100	4.8 V	011101	8.2 V	101110	11.6 V	111111	15.0 V
001101	5.0 V	011110	8.4 V	101111	11.8 V		
001110	5.2 V	011111	8.6 V	110000	12.0 V		
001111	5.4 V	100000	8.8 V	110001	12.2 V		
010000	5.6 V	100001	9.0 V	110010	12.4 V		

(3) Power OFF (PWR) (R02H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Turning OFF the power	0	0	0	0	0	0	0	0	1	0

After the Power OFF command, the driver will be powered OFF. Refer to the POWER MANAGEMENT section for the sequence.

This command will turn off booster, controller, source driver, gate driver, VCOM, and temperature sensor, but register data will be kept until VDD turned OFF or Deep Sleep Mode. Source/Gate/Border/VCOM will be released to floating.

(4) Power off sequence setting (PFS) (R03H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Setting Power OFF sequence	0	0	0	0	0	0	0	0	1	1
	0	1	-	-	T_VDS_OFF[1:0]		-	-	-	-

T_VDS_OFF[1:0]: Power OFF Sequence of VDH and VDL.

00b: 1frame (Default) 01b: 2 frames 10b: 3frames 11b:4 frame

(5) Power ON (PON) (R04H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Turning ON the Power	0	0	0	0	0	0	0	1	0	0

After the Power ON command, the driver will be powered ON. Refer to the POWER MANAGEMENT section for the sequence.

This command will turn on booster, controller, regulators, and temperature sensor will be activated for one-time sensing before enabling booster. When all voltages are ready, the BUSY signal will return to high.

(6) Power ON Measure (PMES) (R05H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
	0	0	0	0	0	0	0	1	0	1

This command enables the internal bandgap, which will be cleared by the next POF.

(7) Booster Soft Start (BTST) (R06H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Starting data transmission	0	0	0	0	0	0	0	1	1	0
	0	1	BT_PHA7	BT_PHA6	BT_PHA5	BT_PHA4	BT_PHA3	BT_PHA2	BT_PHA1	BT_PHA0
	0	1	BT_PHB7	BT_PHB6	BT_PHB5	BT_PHB4	BT_PHB3	BT_PHB2	BT_PHB1	BT_PHB0
	0	1	-	-	BT_PHC5	BT_PHC4	BT_PHC3	BT_PHC2	BT_PHC1	BT_PHC0

BTPHA[7:6]: Soft start period of phase A.

00b: 10mS 01b: 20mS 10b: 30mS 11b: 40mS

BTPHA[5:3]: Driving strength of phase A

000b: strength 1 001b: strength 2 **010b: strength 3** 011b: strength 4

100b: strength 5 101b: strength 6 110b: strength 7 111b: strength 8 (strongest)

BTPHA[2:0]: Minimum OFF time setting of GDR in phase B

000b: 0.27uS 001b: 0.34uS 010b: 0.40uS 011b: 0.54uS

100b: 0.80uS 101b: 1.54uS 110b: 3.34uS **111b: 6.58uS**

BTPHB[7:6]: Soft start period of phase B.

00b: 10mS 01b: 20mS 10b: 30mS 11b: 40mS

BTPHB[5:3]: Driving strength of phase B

	000b: strength 1	001b: strength 2	**010b: strength 3**	011b: strength 4
	100b: strength 5	101b: strength 6	110b: strength 7	111b: strength 8 (strongest)

BTPHB[2:0]: Minimum OFF time setting of GDR in phase B

000b: 0.27uS	001b: 0.34uS	010b: 0.40uS	011b: 0.54uS
100b: 0.80uS	101b: 1.54uS	110b: 3.34uS	**111b: 6.58uS**

BTPHC[5:3]: Driving strength of phase C

000b: strength 1	001b: strength 2	**010b: strength 3**	011b: strength 4
100b: strength 5	101b: strength 6	110b: strength 7	111b: strength 8 (strongest)

BTPHC[2:0]: Minimum OFF time setting of GDR in phase C

000b: 0.27uS	001b: 0.34uS	010b: 0.40uS	011b: 0.54uS
100b: 0.80uS	101b: 1.54uS	110b: 3.34uS	**111b: 6.58uS**

(8) Deep Sleep (DSLP) (R07H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Deep Sleep	0	0	0	0	0	0	0	1	1	1
	0	1	1	0	1	0	0	1	0	1

After this command is transmitted, the chip would enter the deep-sleep mode to save power. Deep Sleep Mode will return to Standby Mode by hardware reset. The only one parameter is a check code, the command would be executed if check code = 0xA5.

(9) Data Start Transmission 1 (DTM1) (R10H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Starting data transmission	0	0	0	0	0	1	0	0	0	0
	0	1	Pixel1	Pixel2	Pixel3	Pixel4	Pixel5	Pixel6	Pixel7	Pixel8
	0	1	..	..	..	..	..	..	..	..
	0	1	Pixel(n-7)	Pixel(n-6)	Pixel(n-5)	Pixel(n-4)	Pixel(n-3)	Pixel(n-2)	Pixel(n-1)	Pixel(n)

This command starts transmitting data and write them into SRAM.

In KW mode, this command writes “OLD” data to SRAM.

In KWR mode, this command writes “K/W” data to SRAM.

In Program mode, this command writes “OTP” data to SRAM for programming.

(10) Data Stop (DSP) (R11H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Stopping data transmission	0	0	0	0	0	1	0	0	0	1
	1	1	Data_flag	-	-	-	-	-	-	-

Check the completeness of data. If data is complete, start to refresh display.

Data_flag: Data flag of receiving user data.

0: Driver didn’t receive all the data.

1: Driver has already received all the one-frame data (DTM1 and DTM2).

After “Data Start” (R10h) or “Data Stop” (R11h) commands and when data_flag=1, the refreshing of panel starts and BUSY_N signal will become “0”.

(11) Display Refresh (DRF) (R12H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Refreshing the display	0	0	0	0	0	1	0	0	1	0

While user sent this command, driver will refresh display (data/VCOM) according to SRAM data and LUT.

After Display Refresh command, BUSY signal will become "0" and the refreshing of panel starts.

(12) Data Start Transmission 2 (DTM2) (R13H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Starting data transmission	0	0	0	0	0	1	0	0	1	1
	0	1	Pixel1	Pixel2	Pixel3	Pixel4	Pixel5	Pixel6	Pixel7	Pixel8
	0	1	..	..	..	..	..	..	..	..
	0	1	Pixel(n-7)	Pixel(n-6)	Pixel(n-5)	Pixel(n-4)	Pixel(n-3)	Pixel(n-2)	Pixel(n-1)	Pixel(n)

This command starts transmitting data and write them into SRAM.

In KW mode, this command writes "NEW" data to SRAM.

In KWR mode, this command writes "RED" data to SRAM.

(13) Auto Sequence (AUTO) (R17H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Auto sequence	0	0	0	0	0	1	0	1	1	1
	0	1	1	0	1	0	0	1	0	1

The command can enable the internal sequence to execute several commands continuously. The successive execution can minimize idle time to avoid unnecessary power consumption and reduce the complexity of host's control procedure. The sequence contains several operations, including PON, DRF, POF, DSLP.

AUTO (0x17) + Code(0xA5) = (PON → DRF → POF)

AUTO (0x17) + Code(0xA7) = (PON → DRF → POF → DSLP)

(14) VCOM LUT (LUTC) (R20H)

This command builds Look-up Table for VCOM

(15) W2W LUT (LUTWW) (R21H)

This command builds Look-up Table for White-to-White.

(16) K2W LUT (LUTKW/LUTR) (R22H)

This command builds Look-up Table for Black-to-White or Red.

(17) W2K LUT (LUTWK/LUTW) (R23H)

This command builds Look-up Table for White - to- Black.

(18) K2K LUT (LUTKK / LUTK) (R24H)

This command builds Look-up Table for Black - to- Black.

(19) Border LUT (LUTBD) (R25H)

This command builds Look-up Table for Border.

(20) LUT Option (LUTOPT) (R2AH)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
LUT Option	0	0	0	0	1	0	1	0	1	0
	0	1	STATE XON[9:8]		-	-	-	-	-	-
	0	1	STATE XON[7:0]							

This command sets XON control enable.

STATE_XON[9:0]:

All Gate ON (Each bit controls one state, STATE_XON [0] for state-1, STATE_XON [1] for state-2 …..)

00 0000 0000b: no All-Gate-ON

00 0000 0001b: State-1 All-Gate-ON

00 0000 0011b: State-1 and State2 All-Gate-ON

: :

(21) KW LUT Option (KWOPT) (R2BH)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
KW LUT Option	0	0	0	0	1	0	1	0	1	1
	0	1	-	-	-	-	-	-	ATRED	NORED
	0	1	KWE[9:8]		-	-	-	-	-	-
	0	1	KWE[7:0]							

This command sets KW LUT mechanism option in KWR mode's LUT and only valid in K/W/R mode.

{ATRED, NORED}: KW LUT or KWR LUT selection control

ATRED	NORED	Description
0	0	KWR LUT always
0	1	KW LUT only
1	0	Auto detect by red data
1	1	KW LUT only

KWE[9:0]:

KW LUT enable control bits. Each bit controls one state, KWE[0] for state-1, KWE[1] for state-2 …..

At least 1 Enable Control bit should be set when KW LUT only is selected in KWR mode.

00 0000 0001b: KW LUT enable in State-1

00 0000 0011b: KW LUT enable in State-1 and State2

00 0000 1011b: KW LUT enable in State-1, State2 and State-4

(22) PLL Control (PLL) (R30H)

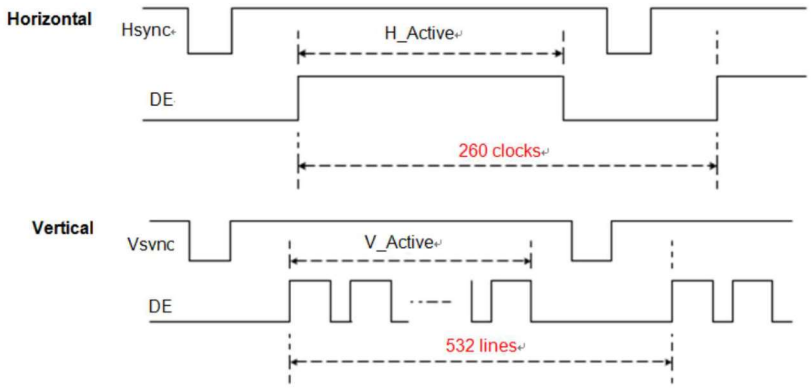
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Controlling PLL	0	0	0	0	1	1	0	0	0	0
	0	1	-	-	-	-	FRS[3:0]			

The command controls the PLL clock frequency. The PLL structure must support the following frame rates:

FMR[3:0]:Frame rate setting

FRS	Frame rate
0000	10Hz
0001	20Hz
0010	30Hz
0011	40Hz
0100	**50Hz**
0101	60Hz
0110	70Hz
0111	80Hz

FRS	Frame rate
1000	90Hz
1001	100Hz
1010	110Hz
1011	120Hz
1100	130Hz
1101	140Hz
1110	150Hz
1111	200Hz



(23) Temperature Sensor Calibration (TSC) (R40H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Sensing Temperature	0	0	0	1	0	0	0	0	0	0
	1	1	D10/TS7	D9/TS6	D8/TS5	D7/TS4	D6/TS3	D5/TS2	D4/TS1	D3/TS0
	1	1	D2	D1	D0	-	-	-	-	-

This command enables internal or external temperature sensor, and reads the result.

TS[7:0]: When TSE (R41h) is set to 0, this command reads internal temperature sensor value.

D[10:0]: When TSE (R41h) is set to 1, this command reads external LM75 temperature sensor value.

TS[7:0]/D[10:3]	Temperature (℃)	TS[7:0]/D[10:3]	Temperature (℃)	TS[7:0]/D[10:3]	Temperature (℃)
1110_0111	-25	0000_0000	0	0001_1001	25
1110_1000	-24	0000_0001	1	0001_1010	26
1110_1001	-23	0000_0010	2	0001_1011	27
1110_1010	-22	0000_0011	3	0001_1100	28
1110_1011	-21	0000_0100	4	0001_1101	29
1110_1100	-20	0000_0101	5	0001_1110	30
1110_1101	-19	0000_0110	6	0001_1111	31
1110_1110	-18	0000_0111	7	0010_0000	32

1110_1111	-17	0000_1000	8	0010_0001	33
1111_0000	-16	0000_1001	9	0010_0010	34
1111_0001	-15	0000_1010	10	0010_0011	35
1111_0010	-14	0000_1011	11	0010_0100	36
1111_0011	-13	0000_1100	12	0010_0101	37
1111_0100	-12	0000_1101	13	0010_0110	38
1111_0101	-11	0000_1110	14	0010_0111	39
1111_0110	-10	0000_1111	15	0010_1000	40
1111_0111	-9	0001_0000	16	0010_1001	41
1111_1000	-8	0001_0001	17	0010_1010	42
1111_1001	-7	0001_0010	18	0010_1011	43
1111_1010	-6	0001_0011	19	0010_1100	44
1111_1011	-5	0001_0100	20	0010_1101	45
1111_1100	-4	0001_0101	21	0010_1110	46
1111_1101	-3	0001_0110	22	0010_1111	47
1111_1110	-2	0001_0111	23	0011_0000	48
1111_1111	-1	0001_1000	24	0011_0001	49

(24) Temperature Sensor Enable (TSE) (R41H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Enable Temperature	0	0	0	1	0	0	0	0	0	1
Sensor/Offset	0	1	TSE	-	-	-	TO[3:0]			

This command selects Internal or External temperature sensor.

TSE: Internal temperature sensor switch

0: Enable (Default) 1: Disable; using external sensor.

TO[3:0]: Temperature offset.

TO[3:0]	Calculation	TO[3:0]	Calculation
0000 b	0	1000	-8
0001	1	1001	-7
0010	2	1010	-6
…	…	…	…
0110	6	1110	-2
0111	7	1111	-1

(25) Temperature Sensor Write (TSW) (R42H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Write External Temperature Sensor	0	0	0	1	0	0	0	0	1	0
	0	1	WATTR[7:0]							
	0	1	WMSB[7:0]							
	0	0	WLSB[7:0]							

This command reads the temperature sensed by the temperature sensor.

WATTR: D[7:6]: I^2C Write Byte Number

00b : 1 byte (head byte only)

01b : 2 bytes (head byte + pointer)

10b : 3 bytes (head byte + pointer + 1st parameter)

11b : 4 bytes (head byte + pointer + 1st parameter + 2nd parameter)

D[5:3]: User-defined address bits (A2, A1, A0)

D[2:0]: Pointer setting

WMSB[7:0]: MSByte of write-data to external temperature sensor.

WLSB[7:0]: LSByte of write-data to external temperature sensor.

(26) Temperature Sensor Read (TSR) (R43H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Read External Temperature Sensor	0	0	0	1	0	0	0	0	1	1
	1	1	RMSB[7:0]							
	1	1	RLSB[7:0]							

This command reads the temperature sensed by the temperature sensor.

RMSB[7:0]: MSByte read data from external temperature sensor

RLSB[7:0]: LSByte read data from external temperature sensor

(27) Panel Glass check (PBC) (R44H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Check Panel Glass	0	0	0	1	0	0	0	1	0	0
	1	1	-	-	-	-	--	-	-	PSTA

This command is used to enable panel check, and to disable after reading result.

PSTA: 0: Panel check fail (panel broken) 1: Panel check pass

(28) VCOM And Data Interval Setting (CDI) (R50H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set Interval Between Vcom and Data	0	0	0	1	0	1	0	0	0	0
	0	1	BDZ	-	BDV[1:0]		N2OCP	-	DDX[1:0]	
	0	1	-	-	-	-	CDI[3:0]			

This command indicates the interval of VCOM and data output. When setting the vertical back porch, the total blanking will be kept (20 Hsync).

BDZ: Border Hi-Z control

0: Border output Hi-Z disabled (default) 1: Border output Hi-Z enabled

BDV[1:0]: Border LUT selection

KWR mode (KW/R=0)

DDX[0]	BDV[1:0]	LUT
0	00	LUTBD
	01	LUTR
	10	LUTW
	11	LUTK
1	00	LUTK

(Default)	01	LUTW
	10	LUTR
	11	LUTBD

KW mode (KW/R=1)

DDX[0]	BDV[1:0]	LUT
0	00	LUTBD
	01	LUTKW (1 → 0)
	10	LUTWK (0 → 1)
	11	LUTKK (0 → 0)
1 (Default)	00	LUTKK (0 → 0)
	01	LUTWK (1 → 0)
	10	LUTKW (0 → 1)
	11	LUTBD

N2OCP: Copy frame data from NEW data to OLD data enable control after display refresh with NEW/OLD in KW mode.

0: Copy NEW data to OLD data disabled (default) 1: Copy NEW data to OLD data enabled

DDX[1:0]: Data polality

Under KWR mode (KW/R=0):

DDX[1] is for RED data.

DDX[0] is for K/W data,

DDX[1:0]	Data {Red, K/W}	LUT
00	00	LUTW
	01	LUTK
	10	LUTR
	11	LUTR
01 (Default)	00	LUTK
	01	LUTW
	10	LUTR
	11	LUTR

DDX[1:0]	Data {Red, K/W}	LUT
10	00	LUTR
	01	LUTR
	10	LUTW
	11	LUTK
11	00	LUTR
	01	LUTR
	10	LUTK
	11	LUTW

Under KW mode (KW/R=1):

DDX[1]=0 is for KW mode with NEW/OLD,

DDX[1]=1 is for KW mode without NEW/OLD.

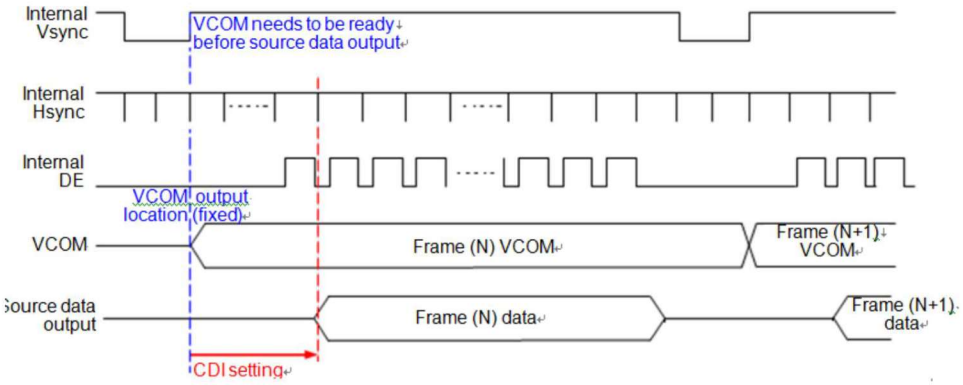
DDX[1:0]	Data {NEW, OLD}	LUT
00	00	LUTWW (0 → 0)
	01	LUTKW (1 → 0)
	10	LUTWK (0 → 1)
	11	LUTKK (1 → 1)
01 (Default)	00	LUTKK (0 → 0)
	01	LUTWK (1 → 0)
	10	LUTKW (0 → 1)
	11	LUTWW (1 → 1)

DDX[1:0]	Data {NEW}	LUT
10	0	LUTKW (1 → 0)
	1	LUTWK (0 → 1)
11	0	LUTWK (1 → 0)
	1	LUTKW (0 → 1)

CDI[3:0]: VCOM and data interval

CDI[3:0]	VCOM and Data Interval
0000 b	17 hsync
0001	16
0010	15
0011	14
0100	13
0101	12
0110	11
0111	**10 (Default)**

CDI[3:0]	VCOM and Data Interval
1000	9
1001	8
1010	7
1011	6
1100	5
1101	4
1110	3
1111	2



(29) Low Power Detection (LPD) (R51H)

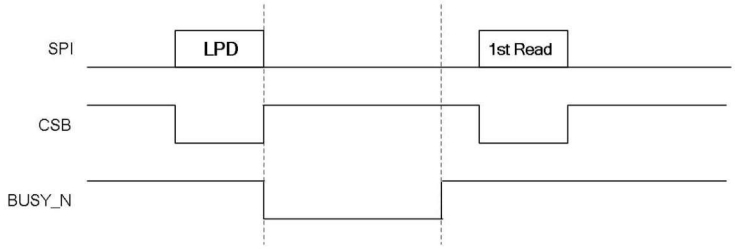
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Detect Low Power	0	0	0	1	0	1	0	0	0	1
	1	1	-	-	-	-	-	-	-	LPD

This command indicates the input power condition. Host can read this flag to learn the battery condition.

LPD: Internal Low Power Detection Flag

0: Low power input (Vdd < 2.5V, 2.4V, 2.3V, or 2.2V, selected by LVD_SEL[1:0] in command LVSEL)

1: Normal status (default)



(30) END voltage setting (EVS) (R52H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
End voltage setting	0	0	0	1	0	1	0	0	1	0
	0	1	-	-	-	-	VCEND	-	BDEND[1:0]	

This command selects source end voltage and border end voltage after LUTs are finished.

VCEND: VCOM end voltage selection

0b: VCOM_DC 1b: floating

BDEND[1:0]: Border end voltage selection

00b: 0V 01b: 0V 10b: VCOM_DC 11b: floating

(31) TCON Setting (TCON) (R60H)

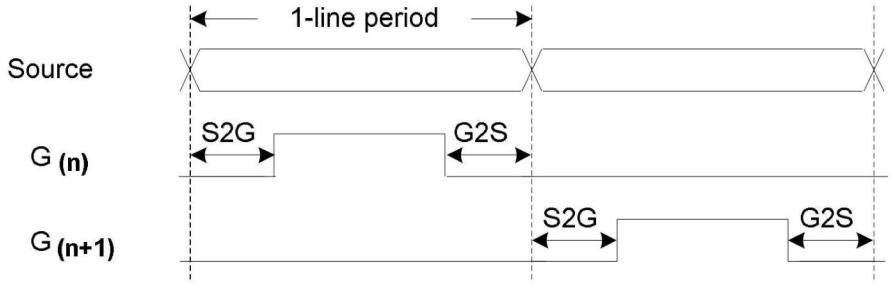
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set Gate/Source Non-overlap Period	0	0	0	1	1	0	0	0	0	0
	0	1	S2G[3:0]				G2S[3:0]			

This command defines non-overlap period of Gate and Source.

S2G[3:0] or G2S[3:0]: Source to Gate / Gate to Source Non-overlap period

S2G[3:0] or G2S[3:0]	Period		S2G[3:0] or G2S[3:0]	Period
0000b	4		…	…
0001	8		1011	48
0010	12(Default)		1100	52
0011	16		1101	56
0100	20		1110	60
0101	24		1111	64

Period = 667 nS.



(32) Resolution Setting (TRES) (R61H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set Display Resolution	0	0	0	1	1	0	0	0	0	1
	0	1	HRES[7:3]					0	0	0
	0	1	-	-	-	-	-	-	VRES[9]	VRES[8]
	0	0	VRES[7:0]							

This command defines resolution setting.

HRES[7:3]: Horizontal Display Resolution (Value range: 01h ~ 1Eh)

VRES[9:0]: Vertical Display Resolution (Value range: 01h ~ 200h)

Active channel calculation, assuming HST[7:0]=0, VST[8:0]=0:

Gate: First active gate = G0;

Last active gate = VRES[9:0] – 1

Source: First active source = S0;

Last active source = HRES[7:3]*8 – 1

(33) Gate/Status Start setting (GSST) (R65H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set Gate/Source Start	0	0	0	1	1	0	0	1	0	1
	0	1	HST[7:3]					0	0	0
	0	1	-	-	-	-	-	-	-	VST[8]
	0	1	VST[7:0]							

This command defines resolution start gate/source position.

HST[7:3]: Horizontal Display Start Position (Source). (Value range: 00h ~ 1Dh)

VST[8:0]: Vertical Display Start Position (Gate). (Value range: 000h ~ 1FFh)

Example : For 128(Source) x 240(Gate)

HST[7:3] = 4 (HST[7:0] = 4*8 = 32),

VST[8:0] = 32

Gate: First active gate = G32 (VST[8:0] = 32),

Last active gate = G271 (VRES[8:0] = 240, VST[8:0] = 32, 240-1+32=271)

Source: First active source = S32 (HST[7:0]= 32),

Last active source = S239 (HRES[8:0] = 128, HST[7:0] = 32, 128-1+32=239)

(34) Revision (REV) (R70H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Chip Revision	0	0	0	1	1	1	0	0	0	0
	1	1	LUT_REV							

The LUT_REV is read from OTP address = 0x001 or 0xC01.

(35) Get Status (FLG) (R71H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Read Flags	0	0	0	1	1	1	0	0	0	1
	1	1	-	PTL_flag	I^2C_ERR	I^2C_ BUSY	data_ flag	PON	POF	BUSY

This command reads the IC status.

PTL_FLAG Partial display status (high: partial mode)

I^2C_ERR: I^2C master error status

I^2C_BUSY: I^2C master busy status (low active)

data_flag: Driver has already received all the one frame data

PON: Power ON status

POF: Power OFF status

BUSY: Driver busy status (low active)

(36) Auto Measure Vcom (AMV) (R80H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Automatically measure Vcom	0	0	1	0	0	0	0	0	0	0
	0	1	-	-	AMVT[1:0]		XON	AMVS	AMV	AMVE

This command reads the IC status.

AMVT[1:0]: Auto Measure Vcom Time

00b: 3s 01b: 5s (Default)

10b: 8s 11b: 10s

XON: All Gate ON of AMV

0: Gate normally scan during Auto Measure VCOM period. (default)

1: All Gate ON during Auto Measure VCOM period.

AMVS: Source output of AMV

0: Source output 0V during Auto Measure VCOM period. (default)

1: Source output VDHR during Auto Measure VCOM period.

AMV: Analog signal

0: Get Vcom value with the VV command (R81h) (default)

1: Get Vcom value in analog signal. (External analog to digital converter)

AMVE: Auto Measure Vcom Enable (/Disable)

0: No effect

1: Trigger auto Vcom sensing.

(37) Vcom Value (VV) (R81H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Automatically measure Vcom	0	0	1	0	0	0	0	0	0	1
	1	1	-	-	VV[5:0]					

This command gets the Vcom value.

VV[5:0]: Vcom Value Output

VV[5:0]	Vcom value
00 0000b	-0.10 V
00 0001b	-0.15 V
00 0010b	-0.20 V
:	:
11 1010b	-3.00 V
11 1011b	-3.05 V

(38) VCM_DC Setting (VDCS) (R82H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set VCM_DC	0	0	1	0	0	0	0	0	1	0
	0	1	-	-	VDCS[5:0]					

This command sets VCOM_DC value

VDCS[5:0]: VCOM_DC Setting

VDCS[5:0]	Vcom value
00 0000b	-0.10 V

00 0001b	-0.15 V
00 0010b	-0.20 V
:	:
11 1010b	-3.00 V
Others	-3.00 V

(39) Partial Window(PTL) (R90H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set Partial Window	0	0	1	0	0	1	0	0	0	0
	0	1	HRST[7:3]					0	0	0
	0	1	HRED[7:3]					1	1	1
	0	1	-	-	-	-	-	-	-	VRST[8]
	0	1	VRST[7:0]							
	0	1	-	-	-	-	-	-	-	VRED[8]
	0	1	VRED[7:0]							
	0	1	-	-	-	-	-	-	-	PT_SCAN

This command sets partial window.

HRST[7:3]: Horizontal start channel bank. (value 00h~1Dh)

HRED[7:3]: Horizontal end channel bank. (value 00h~1Dh). HRED must be greater than HRST.

VRST[8:0]: Vertical start line. (value 000h~1FFh)

VRED[8:0]: Vertical end line. (value 000h~1FFh). VRED must be greater than VRST.

PT_SCAN: 0: Gates scan only inside of the partial window.

1: Gates scan both inside and outside of the partial window. (default)

(40) Partial In (PTIN) (R91H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Partial In	0	0	1	0	0	1	0	0	0	1

This command makes the display enter partial mode.

(41) Partial Out (PTOUT) (R92H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Partial In	0	0	1	0	0	1	0	0	1	0

This command makes the display exit partial mode and enter normal mode.

(42) Program Mode (PGM) (RA0H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Enter Program Mode	0	0	1	0	1	0	0	0	0	0

After this command is issued, the chip would enter the program mode.

After the programming procedure completed, a hardware reset is necessary for leaving program mode.

(43) Active Program (APG) (RA1H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Active Program OTP	0	0	1	0	1	0	0	0	0	1

After this command is transmitted, the programming state machine would be activated.

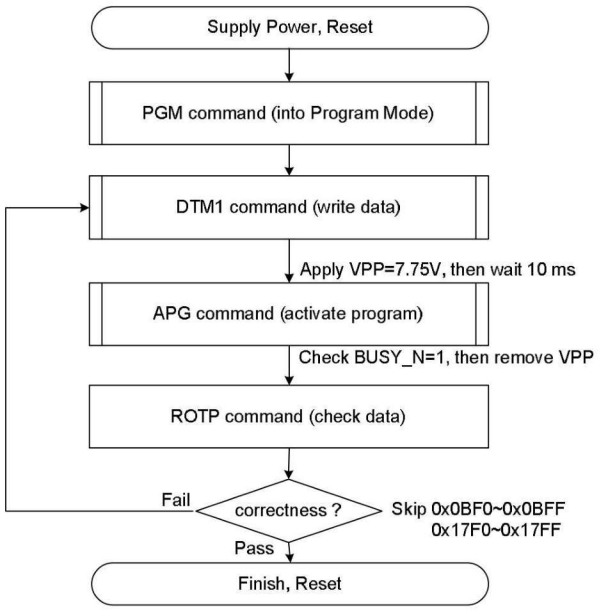
The BUSY flag would fall to 0 until the programming is completed.

(44) Read OTP Data (ROTP) (RA2H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Read OTP data for check	0	0	1	0	1	0	0	0	1	0
	1	1	Dummy							
	1	1	The data of address 0x000 in the OTP							
	1	1	The data of address 0x001 in the OTP							
	1	1	..							
	1	1	The data of address (n-1) in the OTP							
	1	1	The data of address (n) in the OTP							

The command is used for reading the content of OTP for checking the data of programming.

The value of (n) is depending on the amount of programmed data, tha max address = 0x17FF.



The sequence of programming OTP

(45) Cascade setting (CCSET) (RE0H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set cascade option	0	0	1	1	1	0	0	0	0	0
	0	1	-	-	-	-	-	-	TSFIX	CCEN

This command is used for cascade.

TSFIX: Let the value of slave's temperature is same as the master's.

0: Temperature value is defined by internal temperature sensor / external LM75. (default)

1: Temperature value is defined by TS_SET[7:0] registers.

CCEN: Output clock enable/disable.

0: Output 0V at CL pin. (default)

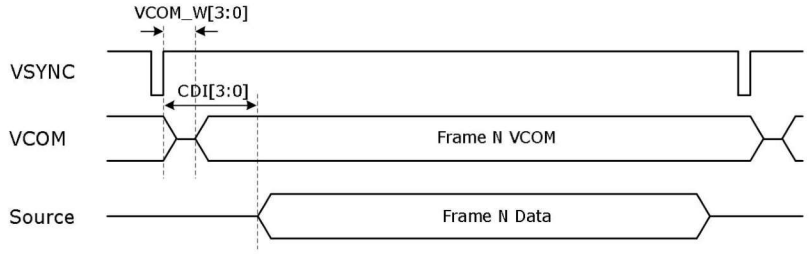
1: Output clock at CL pin to slave chip.

(46) Power Saving (PWS) (RE3H)

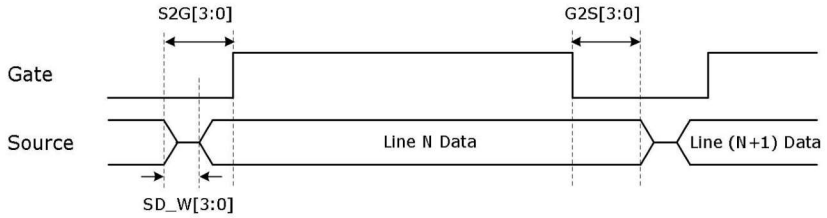
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Power Saving for	0	0	1	1	1	0	0	0	1	1
Vcom &Source	0	1	VCOM W[3:0]				SD W[3:0]			

This command is set for saving power during fresh period. If the output voltage of VCOM / Source is from negative to positive or from positive to negative, the power saving mechanism will be activated. The active period width is defined by the following two parameters.

VCOM_W[3:0]: VCOM power saving width (unit = line period)



SD_W[3:0]: Source power saving width (unit = 660nS)



(47) Power Saving (PWS) (RE4H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Power LVD voltage	0	0	1	1	1	0	0	1	0	0
	0	1	-	-	-	-	-	-	LVD_SEL[1:0]	

LVD_SEL[1:0]: Low Power Voltage selection

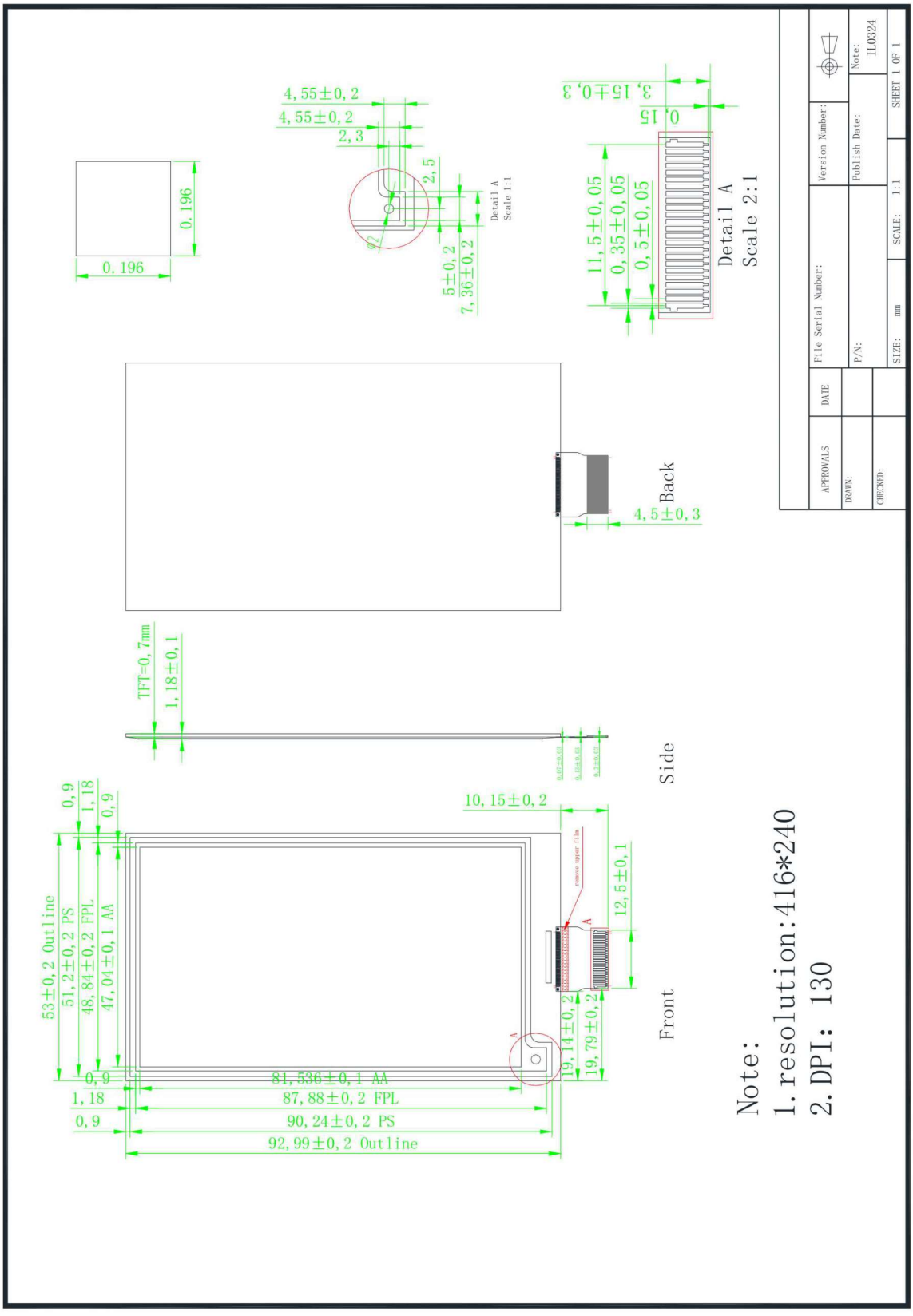
LVD_SEL[1:0]	D4
00	< 2.2 V
01	< 2.3 V
10	< 2.4 V
11	< 2.5 V (default)

(48) Power Saving (PWS) (RE5H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Power LVD voltage	0	0	1	1	1	0	0	1	0	1
	0	1	TS_SET[7:0]							

This command is used for cascade to fix the temperature value of master and slave chip.

4. Mechanical Drawing of EPD module



7. Electrical Characteristics

7-1) Absolute maximum rating

Parameter	Symbol	Rating	Unit
Logic Supply Voltage	V_{CI}	-0.3 to +6.0	V
Digital Input Voltage	V_{IN}	-0.3 to V_{DDIO}+0.3	V
Operating Temp. range	T_{OPR}	0 to +50	℃
Storage Temp. range	T_{STG}	-25 to +70	℃
Humidity range	-	40~70	%RH

***Note: Avoid direct sunlight.**

7-2) Panel DC Characteristics

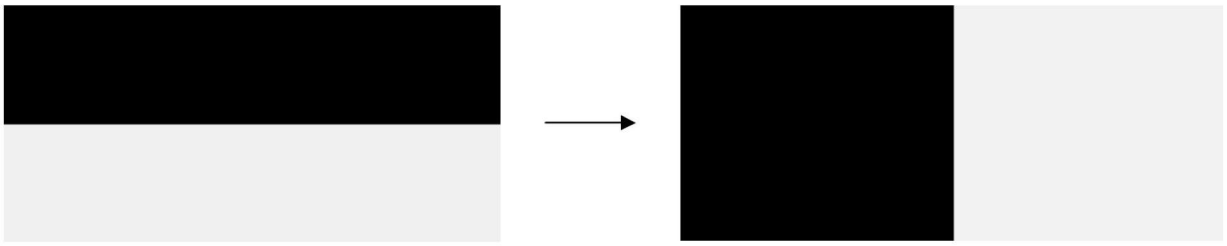
The following specifications apply for: VSS = 0V, TA = 25℃

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Single ground	V_{SS}	-	-	0	-	V
IO supply voltage	V_{DDIO}	-	2.3	3.3	3.6	V
High level input voltage	VIH	Digital input pins	0.7 V_{DDIO}	-	V_{DDIO}	V
Low level input voltage	VIL	Digital input pins	0	-	0.3 V_{DDIO}	V
High level output voltage	VOH	Digital input pins , IOH= 400uA	V_{DDIO} -0.4	-	-	V
Low level output voltage	VOL	Digital input pins , IOL= -400uA	0	-	0.4	V
Image update current	I_{UPDATE}	-	-	8	10	mA
Standby panel current	Istandby	-	-	-	25	uA
Power panel（update）	P_{UPDATE}	-	-	26.4	40	mW
Standby power panel	P_{STBY}	-	-	-	0.09	mW
Operating temperature	-	-	0	-	50	℃
Storage temperature	-	-	-25	-	70	℃
Image update Time at 25 ℃	-	-	-	6	8	Sec
Deep sleep mode current	I_{VCI}	DC/DC off No clock No input load Ram data not retain	-	2	5	uA
Sleep mode current	I_{VCI}	DC/DC off No clock No input load Ram data retain	-	35	50	uA

- The Typical power consumption is measured with following pattern transition: from horizontal 2 gray scale pattern to vertical 2 gray scale pattern.(Note 7-1)
- The standby power is the consumed power when the panel controller is in standby mode.
- The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by GOOD DISPLAY
- Vcom is recommended to be set in the range of assigned value ± 0.1V.

Note 7-1

The Typical power consumption



7-3) Panel AC Characteristics

7-3-1) Oscillator frequency

The following specifications apply for : VSS = 0V, VCI = 3.3V, T_A = 25℃

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Internal Oscillator frequency	Fosc	VCI=2.3 to 3.6V	-	1.625	-	MHz

7-3-2) MCU Interface

7-3-2-1) MCU Interface Selection

In this module, there are 4-wire SPI and 3-wire SPI that can communicate with MCU. The MCU interface mode can be set by hardware selection on BS1 pins. When it is “Low”, 4-wire SPI is selected. When it is “High”, 3-wire SPI (9 bits SPI) is selected.

Pin Name	Data/Command Interface		Control Signal		
Bus interface	D1	D0	CS#	D/C#	RES#
SPI4	SDIN	SCLK	CS#	D/C#	RES#
SPI3	SDIN	SCLK	CS#	L	RES#

Table 7-1: MCU interface assignment under different bus interface mode

Note 7-2: L is connected to VSS

Note 7-3: H is connected to VCI

7-3-2-2) MCU Serial Interface (4-wire SPI)

The 4-wire SPI consists of serial clock SCLK, serial data SDIN, D/C#, CS#. In SPI mode, D0 acts as SCLK, D1 acts as SDIN.

Function	CS#	D/C#	SCLK
Write Command	L	L	↑
Write data	L	H	↑

Table 7-2: Control pins of 4-wire Serial Peripheral interface

Note 7-4: ↑stands for rising edge of signal

SDIN is shifted into an 8-bit shift register in the order of D7, D6, ... D0. The data byte in the shift register is written to the Graphic Display Data RAM (RAM) or command register in the same clock. Under serial mode, only write operations are allowed.

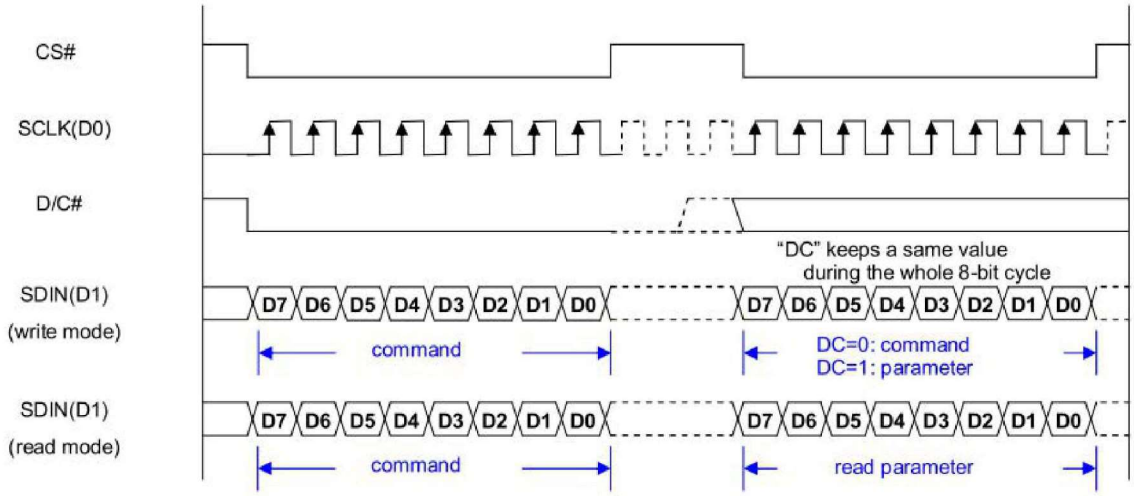


Figure 7-1: Write procedure in 4-wire Serial Peripheral Interface mode

7-3-2-3) MCU Serial Interface (3-wire SPI)

The 3-wire serial interface consists of serial clock SCLK, serial data ADIN and CS#.

In 3-wire SPI mode, D0 acts as SCLK, D1 acts as SDIN, The pin D/C# can be connected to an external ground.

The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C# bit, D7 to D0 bit. The D/C# bit (first bit of the sequential data) will determine the following data byte in shift register is written to the Display Data RAM (D/C# bit = 1) or the command register (D/C# bit = 0).Under serial mode, only write operations are allowed.

Function	CS#	D/C#	SCLK
Write Command	L	Tie LOW	↑
Write data	L	Tie LOW	↑

Table 7-3: Control pins of 3-wire Serial Peripheral Interface

Note 7-5: ↑stands for rising edge of signal

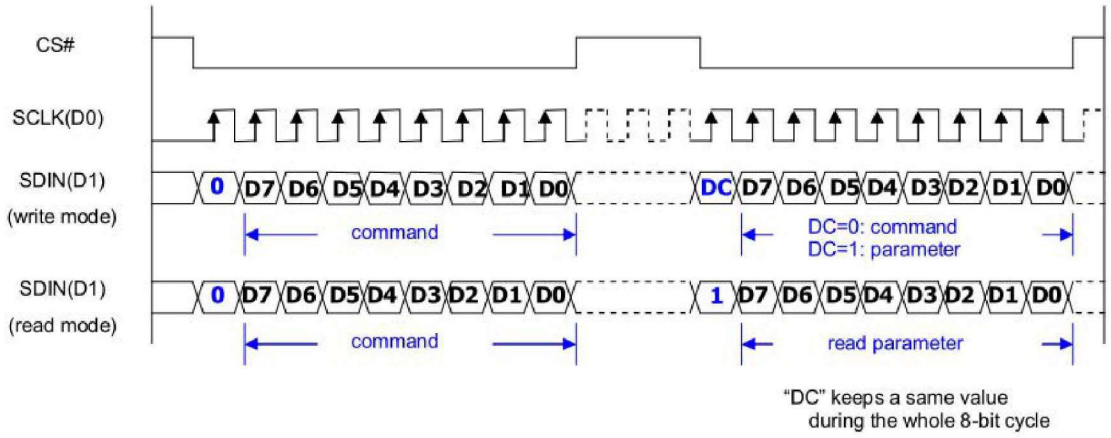


Figure 7-2: Write procedure in 3-wire Serial Peripheral Interface mode

7-3-3) Timing Characteristics of Series Interface

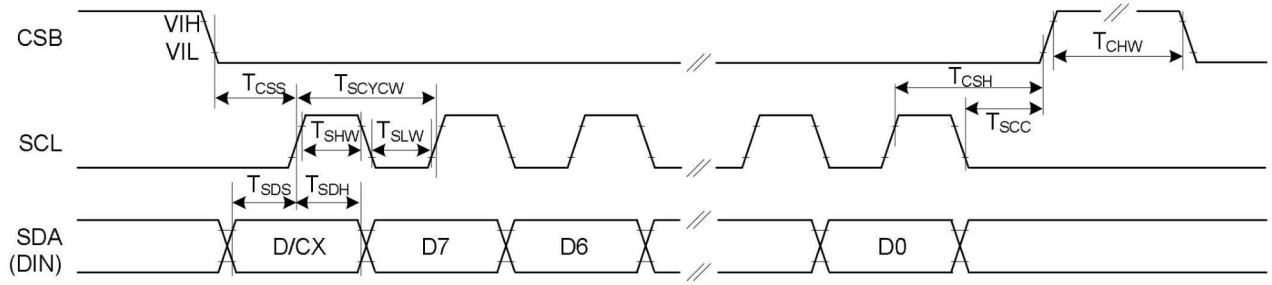


Figure: 3-wire Serial Interface Characteristics (Write mode)

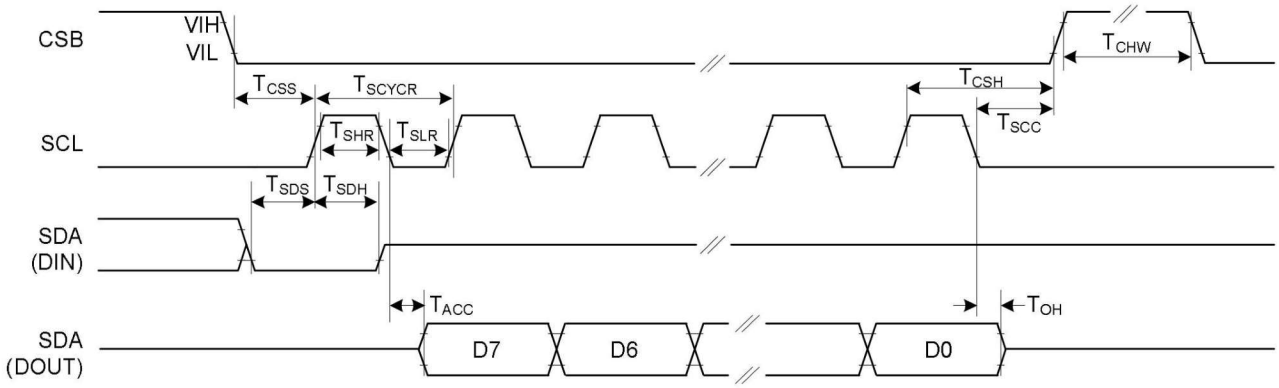


Figure: 3-wire Serial Interface Characteristics (Read mode)

Symbol	Signal	Parameter	Min	Typ	Max	Unit
tcss	CS#	Chip Select Setup Time	60	-	-	ns
tcsh		Chip Select Hold Time	65	-	-	ns
tscc		Chip Select Setup Time	20	-	-	ns
tchw		Chip Select Setup Time	40	-	-	ns
tscycw	SCLK	Serial clock cycle (write)	100	-	-	ns
tshw		SCL “H” pulse width (write)	35	-	-	ns
tslw		SCL“L” pulse width (write)	35	-	-	ns
tscycr		Serial clock cycle (Read)	150	-	-	ns
tshr		SCL “H” pulse width (Read)	60	-	-	ns
tslr		SCL “L” pulse width (Read)	60	-	-	ns
tsds	SDIN (DIN) (DOUT)	Data setup time	30	-	-	ns
tsdh		Data hold time	30	-	-	ns
tacc		Access time	-	-	50	ns
toh		Output disable time	15	-	-	ns

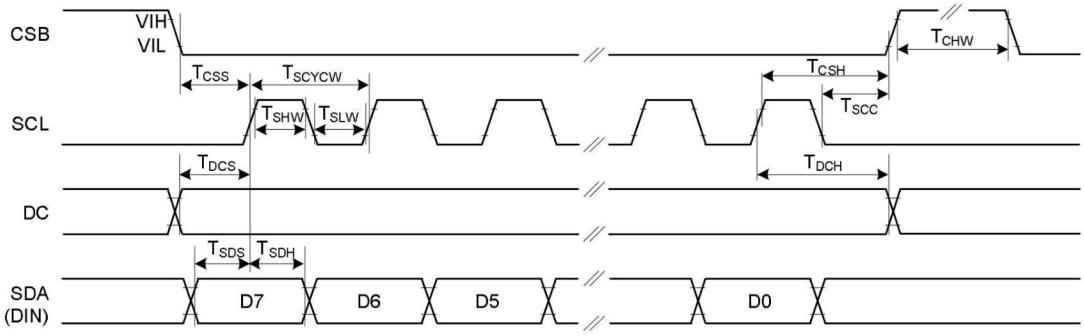


Figure: 4-wire Serial Interface Characteristics (Write mode)

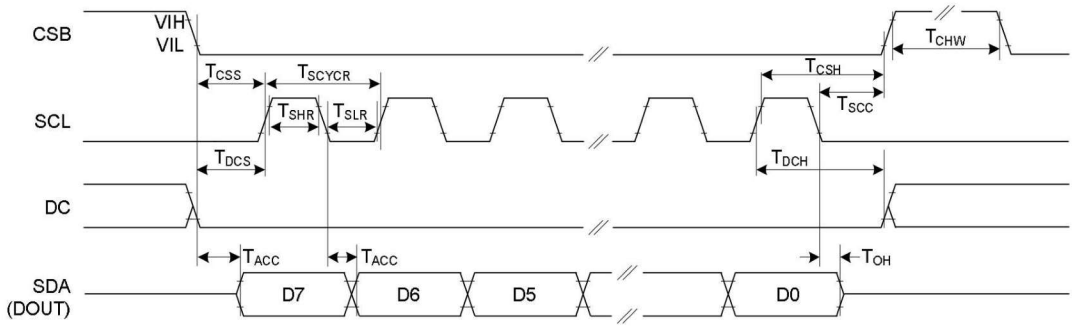


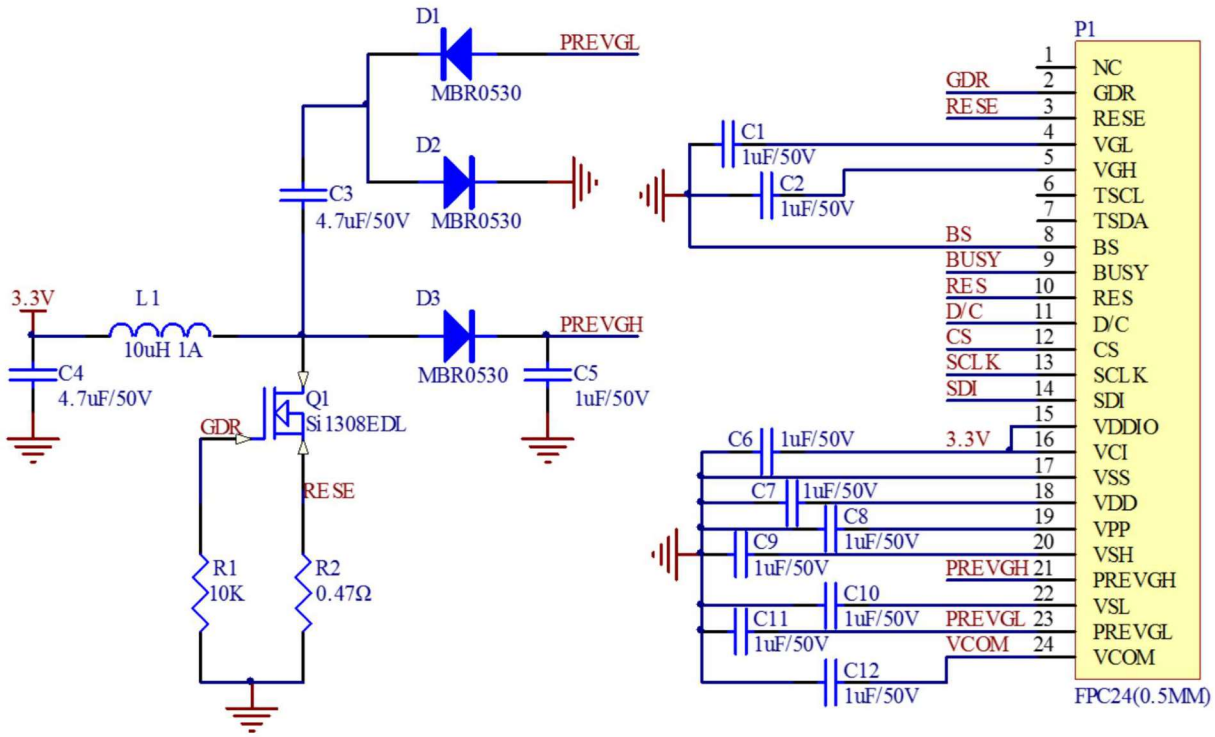
Figure: 4-wire Serial Interface Characteristics (Read mode)

Symbol	Signal	Parameter	Min	Typ	Max	Unit
tcss	CS#	Chip Select Setup Time	60	-	-	ns
tcsh		Chip Select Hold Time	65	-	-	ns
tscc		Chip Select Setup Time	20	-	-	ns
tchw		Chip Select Setup Time	40	-	-	ns
tscycw	SCLK	Serial clock cycle (write)	100	-	-	ns
tshw		SCL “H” pulse width (write)	35	-	-	ns
tslw		SCL“L” pulse width (write)	35	-	-	ns
tscycr		Serial clock cycle (Read)	150	-	-	ns
tshr		SCL “H” pulse width (Read)	60	-	-	ns
tslr		SCL “L” pulse width (Read)	60	-	-	ns
tdcs	DC#	DC setup time	30	-	-	ns
tdch		DC hold time	30	-	-	ns
tsds	SDIN (DIN) (DOUT)	Data setup time	30	-	-	ns
tsdh		Data hold time	30	-	-	ns
tacc		Access time	-	-	50	ns
toh		Output disable time	15	-	-	ns

7-4) Power Consumption

Parameter	Symbol	Conditions	TYP	Max	Unit	Remark
Panel power consumption during update	-	25℃	26.4	40	mW	-
Power consumption in standby mode	-	25℃	-	0.0165	mW	-

7-5) Reference Circuit



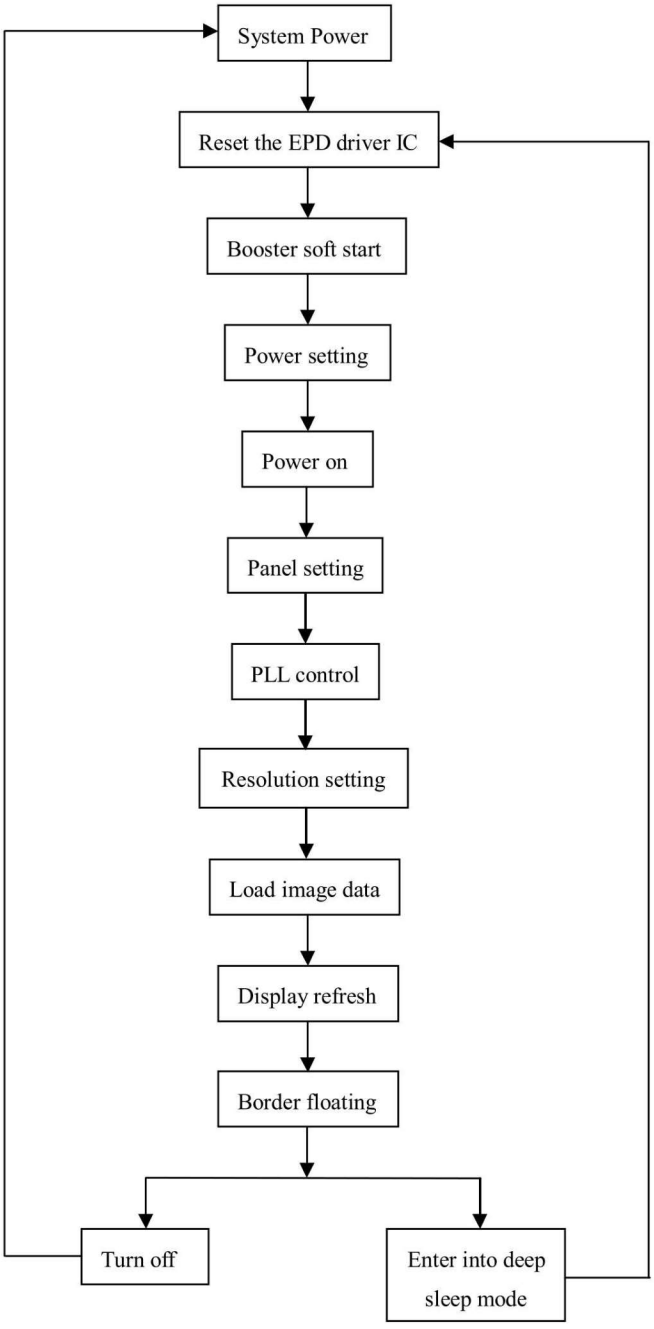
Note >

1. Inductor L1 is wire-wound inductor. There are no special requirements for other parameters.
2. Suggests using Si1304BDL or Si1308EDL TUBE MOS (Q1) , otherwise it may affect the normal boost of the circuit.
3. The default circuit is 4-wire SPI. If the user wants to use 3-wire SPI, the resistor R4 can be removed when users design.
4. Default voltage value of all capacitors is 50V.

8. Typical Operating Sequence

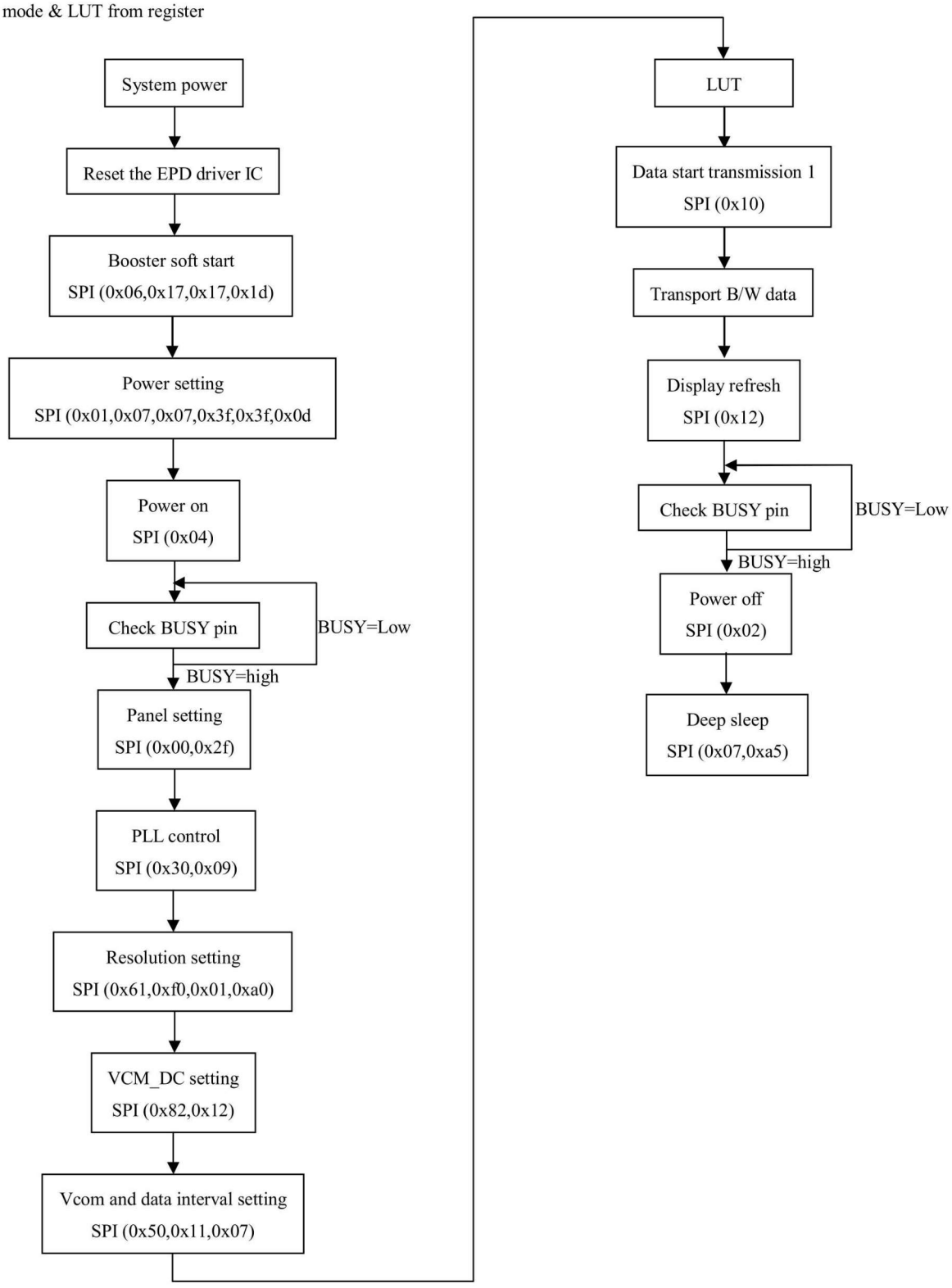
8.1) Normal Operation Flow

1. BW mode & LUT form Register



8.2) Reference Program Code

1. BW mode & LUT from register



Note1: Set border to floating.

9. Optical characteristics

9-1) Specifications

Measurements are made with that the illumination is under an angle of 45 degrees, the detection is perpendicular unless otherwise specified.

T=25℃

SYMBOL	PARAMETER	CONDITIONS	MIN	TYPE	MAX	UNIT	Note
R	Reflectance	White	30	35	-	%	Note 9-1
Gn	2Grey Level	-	-	DS＋(WS-DS)×n(m-1)	-	L*	-
CR	Contrast Ratio	indoor	8		-	-	-
Panel's life		0℃~50℃		1000000 times or 5 years			Note 9-2

WS: White state, DS: Dark state

Gray state from Dark to White : DS、WS

m: 2

Note 9-1: Luminance meter: Eye – One Pro Spectrophotometer

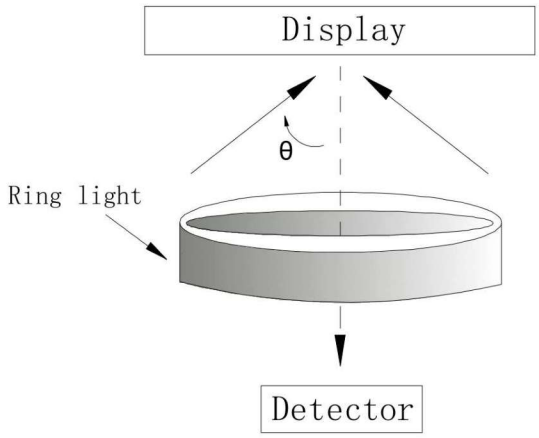
Note 9-2: Panel life will not guaranteed when work in temperature below 0 degree or above 50 degree. Each update interval time should be minimum at 180 seconds.

9-2) Definition of contrast ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (R1) and the reflectance in a dark area (Rd)() :

R1: white reflectance Rd: dark reflectance

CR = R1/Rd

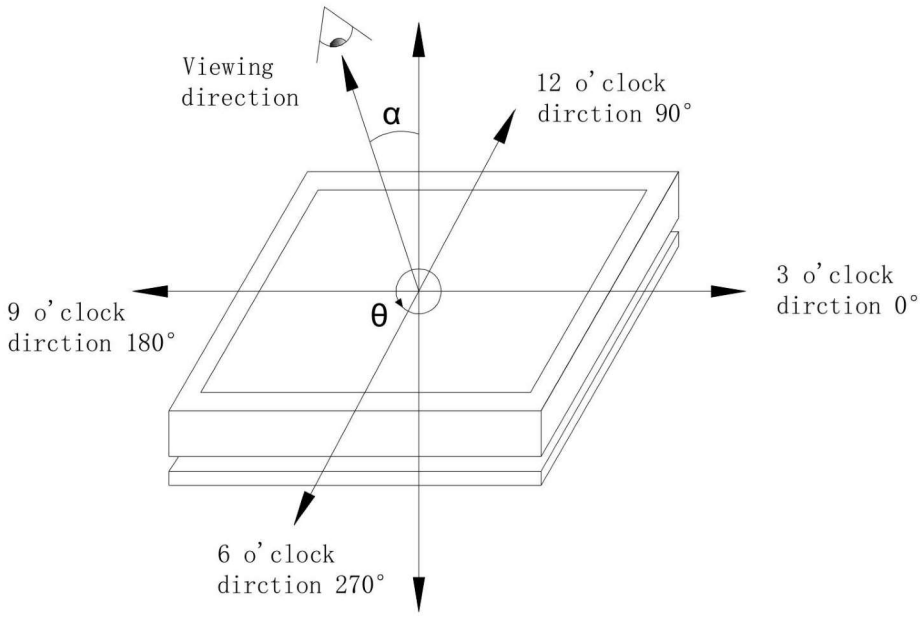


9-3) Reflection Ratio

The reflection ratio is expressed as:

$R = \text{Reflectance Factor}_{\text{white board}} \times (L_{\text{center}} / L_{\text{white board}})$

L_{center} is the luminance measured at center in a white area (R=G =B=1). $L_{\text{white board}}$ is the luminance of a standard white board. Both are measured with equivalent illumination source. The viewing angle shall be no more than 2 degrees.



9-4) Bi-stability

The Bi-stability standard as follows:

Bi-stability	Result		
		AVG	MAX
24 hours Luminance drift	White state △L*	-	3
	Black state △L*	-	3

10. Handling, Safety And Environmental Requirements

WARNING
The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

CAUTION
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
Disassembling the display module can cause permanent damage and invalidate the warranty agreements.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

Data sheet status	
Product specification	The data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and dose not form part of the specification.	

Product Environmental certification
RoHS

11. Reliability test

	TEST	CONDITION	METHOD	REMARK
1	High-Temperature Operation	T = 50℃, RH=35% for 240 hrs	When the experimental cycle finished, the EPD samples will be taken out from the high temperature environmental chamber and set aside for a few minutes. As EPDs return to room temperature, testers will observe the appearance, and test electrical and optical performance based on standard # IEC 60 068-2-2Bp.	When experiment finished, the EPD must meet electrical and optical performance standards.
2	Low-Temperature Operation	T = 0℃ for 240 hrs	When the experimental cycle finished, the EPD samples will be taken out from the low temperature environmental chamber and set aside for a few minutes. As EPDs return room temperature, testers will observe the appearance, and test electrical and optical performance based on standard # IEC 60 068-2-2Ab.	When experiment finished, the EPD must meet electrical and optical performance standards.
3	High-Temperature Storage	T = +70℃, RH=35% for 240 hrs Test in white pattern	When the experimental cycle finished, the EPD samples will be taken out from the high temperature environmental chamber and set aside for a few minutes. As EPDs return to room temperature, testers will observe the appearance, and test electrical and optical performance based on standard # IEC 60 068-2-2Bp.	When experiment finished, the EPD must meet electrical and optical performance standards.
4	Low-Temperature Storage	T = -25℃ for 240 hrs Test in white pattern	When the experimental cycle finished, the EPD samples will be taken out from the low temperature environmental chamber and set aside for a few minutes. As EPDs return to room temperature, testers will observe the appearance, and test electrical and optical performance based on standard # IEC 60 068-2-2Ab	When experiment finished, the EPD must meet electrical and optical performance standards.
5	High Temperature, High-Humidity Operation	T=+40℃, RH=80% for240hrs	When the experimental cycle finished, the EPD samples will be taken out from the environmental chamber and set aside for a few minutes. As EPDs return to room temperature, testers will observe the appearance, and test electrical and optical performance based on standard # IEC 60 068-2-3CA.	When experiment finished, the EPD must meet electrical and optical performance standards.
6	High Temperature, High-Humidity Storage	T=+60℃, RH=80% for240hrs Test in white pattern	When the experimental cycle finished, the EPD samples will be taken out from the environmental chamber and set aside for a few minutes. As EPDs return to room temperature, testers will observe the appearance, and test electrical and optical performance based on standard # IEC 60 068-2-3CA.	When experiment finished, the EPD must meet electrical performance standards.
7	Temperature Cycle	[-25℃ 30mins]→ [+70℃, RH=35% 30mins], 70cycles,	1. Samples are put in the Temp & Humid. Environmental Chamber. Temperature cycle starts with -25℃, storage period 30 minutes. After 30 minutes, it needs 30min to let temperature rise to 70℃. After 30min, temperature	When experiment finished, the EPD must meet electrical and optical

		Test in white pattern	will be adjusted to 70℃, RH=35% and storage period is 30 minutes. After 30 minutes, it needs 30min to let temperature rise to -25℃. One temperature cycle (2hrs) is complete. 2. Temperature cycle repeats 70 times. 3. When 70 cycles finished, the samples will be taken out from experiment chamber and set aside a few minutes. As EPDs return to room temperature, tests will observe the appearance, and test electrical and optical performance based on standard # IEC 60 068-2-14NB.	performance standards.
8	UV exposure Resistance	765 W/m^2 for 168 hrs,40℃	Standard # IEC 60 068-2-5 Sa	
9	Electrostatic discharge	Machine model: +/-250V, 0Ω,200pF	Standard # IEC61000-4-2	
10	Package Vibration	1.04G,Frequency : 10~500Hz Direction : X,Y,Z Duration:1hours in each direction	Full packed for shipment	
11	Package Drop Impact	Drop from height of 122 cm on Concrete surface Drop sequence:1 corner, 3edges, 6face One drop for each.	Full packed for shipment	

Actual EMC level to be measured on customer application.

Note: (1) The protective film must be removed before temperature test.

(2) In order to make sure the display module can provide the best display quality, the update should be made after putting the display module in stable temperature environment for 4 hours at 25℃.

12. Point and line standard

Shipment Inseption Standard

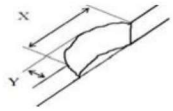
Part-A： Active area　　Part-B： Border area

Equipment： Electrical test fixture, Point gauge

Outline dimension：

92.99(H)×53(V) ×1.18(D)　　Unit： mm

Environment	Temperature	Humidity	Illuminance	Distance	Time	Angle
	23±2℃	55± 5%RH	1200～ 1500Lux	300 mm	35 Sec	

Name	Causes	Spot size			Part-A	Part-B
Spot	B/W spot in glass or protection sheet, foreign mat. Pin hole	D ≤ 0.25mm			Ignore	Ignore
		0.25mm < D ≤ 0.4mm			4	
		0.4mm < D			0	
Scratch or line defect	Scratch on glass or Scratch on FPL or Particle is Protection sheet.	Length		Width	Part-A	Ignore
		L ≤2.0mm		W≤0.2 mm	Ignore	
		2.0 mm < L≤ 5.0mm		0.2 mm<W≤ 0.3mm	2	
		5.0 mm < L		0.3mm < W	0	
Air bubble	Air bubble	D1, D2 ≤ 0.2 mm			Ignore	Ignore
		0.2 mm < D1,D2 ≤ 0.35mm			4	
		0.35mm < D1, D2			0	
Side Fragment						
	X≤5mm， Y≤1mm & display is ok, Ignore					

Remarks: Spot define: That only can be seen under WS or DS defects.

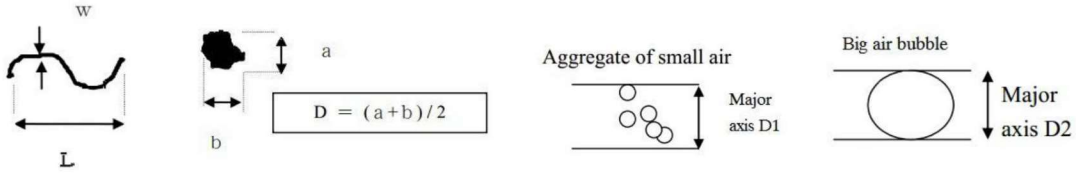
Any defect which is visible under gray pattern or transition process but invisible under black and white is disregarded.

Here is definition of the “Spot” and “Scratch or line defect”.

Spot: W > 1/4L　　Scratch or line defect: W ≤1/4L

Definition for L/W and D (major axis)

FPC bonding area pad doesn’t allowed visual inspection.



Note: AQL = 0.4

13. Packing