2.7 inch
E-paper Display Series

BLGDEW027C44

1. General Description

1.1 Over View

The display is a TFT active matrix electrophoretic display, with interface and a reference system design. The 2.7" active area contains 264×176 pixels, and has 1-bit white/black and 1-bit red full display capabilities. An integrated circuit contains gate buffer, source buffer, interface, timing control logic, oscillator, DC-DC, SRAM, LUT, VCOM and border are supplied with each panel.

1.2 Features

- High contrast
- High reflectance
- Ultra wide viewing angle
- Ultra low power consumption
- Pure reflective mode
- Bi-stable
- Commercial temperature range
- Landscape, portrait mode
- Antiglare hard-coated front-surface
- Low current sleep mode
- On chip display RAM
- Waveform stored in On-chip OTP
- Serial peripheral interface available
- On-chip oscillator
- On-chip booster and regulator control for generating VCOM, Gate and source driving voltage
- I^2C Signal Master Interface to read external temperature sensor
- Available in COG package IC thickness 280um

1.3 Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	2.7	Inch	
Display Resolution	264(H) × 176(V)	Pixel	Dpi: 117
Active Area	57.288(H) × 38.192(V)	mm	
Pixel Pitch	0.217 × 0.217	mm	
Pixel Configuration	Rectangle		
Outline Dimension	70.42(H) × 45.8(V) × 0.98(D)	mm	
Weight	6.08±0.5	g	

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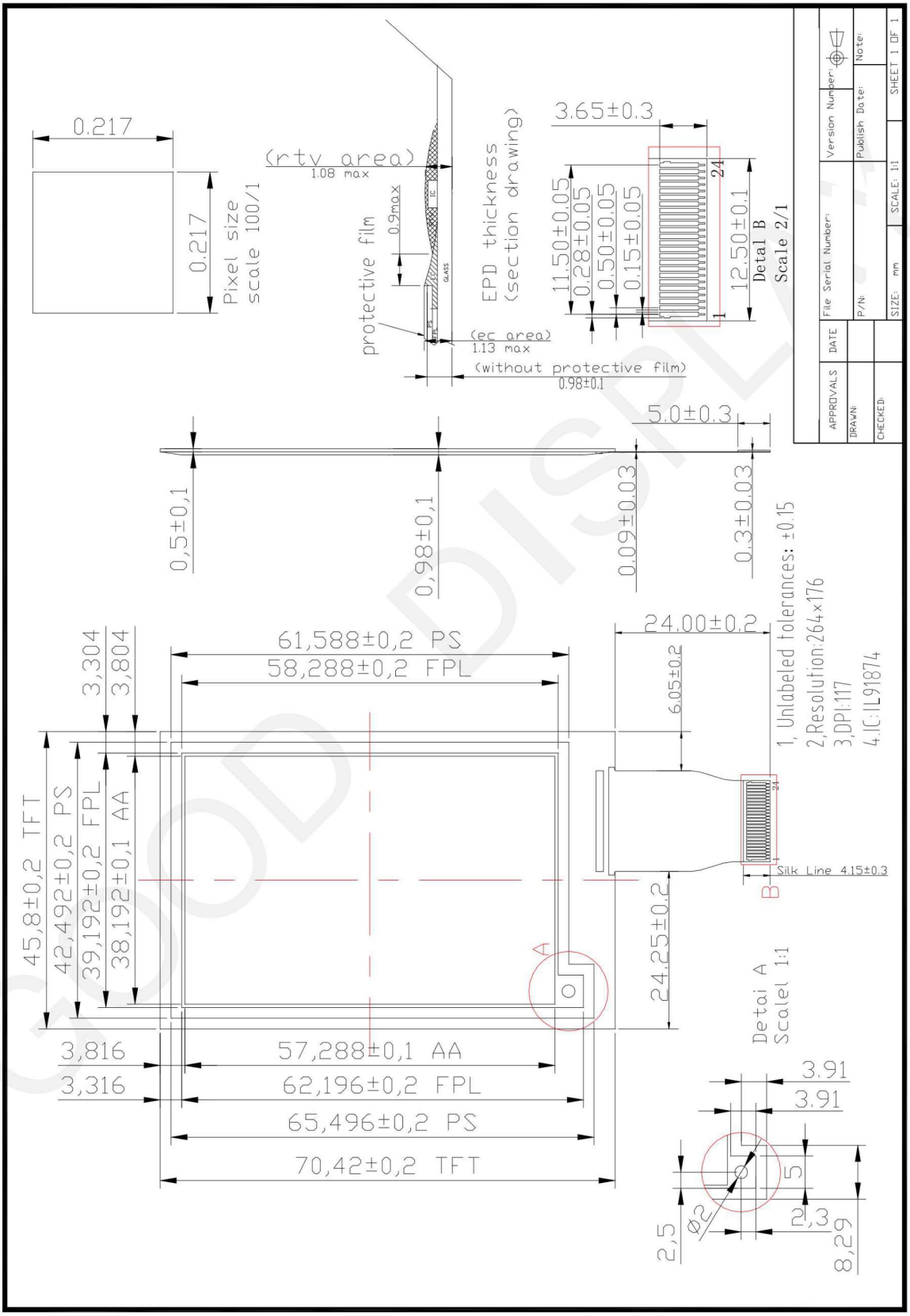
1.4 Mechanical Drawing of EPD module



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1.5 Input/Output Terminals

1.5-1) Pin out List

Pin #	Type	Single	Description	Remark
1		NC	No connection and do not connect with other NC pins	Keep Open
2	O	GDR	N-Channel MOSFET Gate Drive Control	
3	O	RESE	Current Sense Input for the Control Loop	
4	C	VGL	Negative Gate driving voltage	
5	C	VGH	Positive Gate driving voltage	
6	O	TSCL	I^2C Interface to digital temperature sensor Clock pin	
7	I/O	TSDA	I^2C Interface to digital temperature sensor Date pin	
8	I	BS1	Bus selection pin	Note 1.5-5
9	O	BUSY	Busy state output pin	Note 1.5-4
10	I	RES #	Reset	Note 1.5-3
11	I	D/C #	Data /Command control pin	Note 1.5-2
12	I	CS #	Chip Select input pin	Note 1.5-1
13	I/O	D0	serial clock pin (SPI)	
14	I/O	D1	serial data pin (SPI)	
15	I	VDDIO	Power for interface logic pins	
16	I	VCI	Power Supply pin for the chip	
17		VSS	Ground	
18	C	VDD	Core logic power pin	
19	C	VPP	Power Supply for OTP Programming	
20	C	VSH	Positive Source driving voltage	
21	C	PREVGH	Power Supply pin for VGH and VSH	
22	C	VSL	Negative Source driving voltage	
23	C	PREVGL	Power Supply pin for VCOM, VGL and VSL	
24	C	VCOM	VCOM driving voltage	

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Note 1.5-1: This pin (CSB) is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CSB is pulled Low.

Note 1.5-2: This pin (DC) is Data/Command control pin connecting to the MCU. When the pin is pulled High, the data will be interpreted as data. When the pin is pulled Low, the data will be interpreted as command.

Note 1.5-3: This pin (RST_N) is reset signal input. The Reset is active Low.

Note 1.5-4: This pin (BUSY_N) is BUSY_N state output pin. When BUSY_N is Low the operation of chip should not be interrupted and any commands should not be issued to the module. The driver IC will put BUSY_N pin Low when the driver IC is working such as:

- Outputting display waveform; or
- Programming with OTP
- Communicating with digital temperature sensor

Note 1.5-5: This pin (BS) is for 3-line SPI or 4-line SPI selection. When it is "Low", 4-line SPI is selected. When it is "High", 3-line SPI (9 bits SPI) is selected. Please refer to below Table.

Table: Bus interface selection

BS	MPU Interface
L	4-lines serial peripheral interface (SPI)
H	3-lines serial peripheral interface (SPI) – 9 bits SPI

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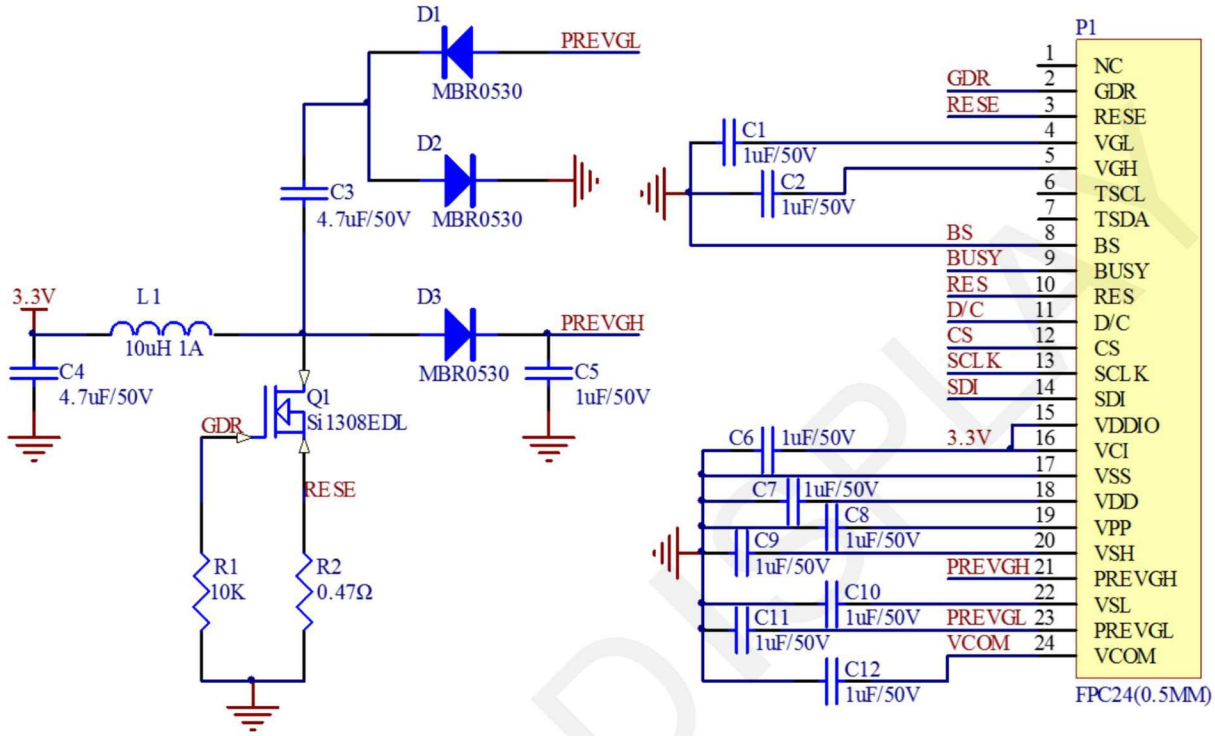
1.6 Reference Circuit



Note :

1. Inductor L1 is wire-wound inductor. There are no special requirements for other parameters.

2. Suggests using Si1304BDL or Si1308EDL TUBE MOS (Q1) , otherwise it may affect the normal boost of the circuit.

3. The default circuit is 4-wire SPI. If the user wants to use 3-wire SPI, the resistor R4 can be removed when users design.

4. Default voltage value of all capacitors is 50V.

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2. Environmental

2.1 Handling, Safety and Environmental Requirements

WARNING
The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

CAUTION
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
Disassembling the display module can cause permanent damage and invalidate the warranty agreements.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

Data sheet status	
Product specification	The data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and dose not form part of the specification.	

Product Environmental certification
RoHS

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2.2 Reliability test

	TEST	CONDITION	METHOD	REMARK
1	High-Temperature Operation	T =40℃, RH=35% for 240 hrs	When the experimental cycle finished, the EPD samples will be taken out from the high temperature environmental chamber and set aside for a few minutes. As EPDs return to room temperature, testers will observe the appearance, and test electrical and optical performance based on standard # IEC 60068-2-2Bp.	When experiment finished, the EPD must meet electrical and optical performance standards.
2	Low-Temperature Operation	T = 0℃for 240 hrs	When the experimental cycle finished, the EPD samples will be taken out from the low temperature environmental chamber and set aside for a few minutes. As EPDs return room temperature, testers will observe the appearance, and test electrical and optical performance based on standard # IEC 60068-2-2Ab.	When experiment finished, the EPD must meet electrical and optical performance standards.
3	High-Temperature Storage	T = +60℃, RH=35% for 240 hrs Test in white pattern	When the experimental cycle finished, the EPD samples will be taken out from the high temperature environmental chamber and set aside for a few minutes. As EPDs return to room temperature, testers will observe the appearance, and test electrical and optical performance based on standard # IEC 60068-2-2Bp.	When experiment finished, the EPD must meet electrical and optical performance standards.
4	Low-Temperature Storage	T = -25℃ for 240 hrs Test in white pattern	When the experimental cycle finished, the EPD samples will be taken out from the low temperature environmental chamber and set aside for a few minutes. As EPDs return to room temperature, testers will observe the appearance, and test electrical and optical performance based on standard # IEC 60068-2-2Ab.	When experiment finished, the EPD must meet electrical and optical performance standards.
5	High Temperatur e, High-Humidity Operation	T=+40℃, RH=80% for 240 hrs	When the experimental cycle finished, the EPD samples will be taken out from the environmental chamber and set aside for a few minutes. As EPDs return to room temperature, testers will observe the appearance, and test electrical and optical performance based on standard # IEC 60068-2-3CA.	When experiment finished, the EPD must meet electrical and optical performance standards.
6	High Temperatur e, High-Humidity Storage	T=+50℃, RH=80% for 240 hrs Test in white pattern	When the experimental cycle finished, the EPD samples will be taken out from the environmental chamber and set aside for a few minutes. As EPDs return to room temperature, testers will observe the appearance, and test electrical and optical performance based on standard # IEC 60068-2-3CA.	When experiment finished, the EPD must meet electrical performance standards.

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7	Temperature Cycle	[-25℃ 30mins]→ [+60℃,RH=35% 30mins], 50cycles Test in white pattern	1. Samples are put in the Temp & Humid. Environmental Chamber. Temperature cycle starts with -25℃, storage period 30 minutes. After 30 minutes, it needs 30min to let temperature rise to 60℃. After 30min, temperature will be adjusted to 60℃, RH=35% and storage period is 30 minutes. After 30 minutes, it needs 30min to let temperature rise to -25℃. One temperature cycle (2hrs) is complete. 2. Temperature cycle repeats 50 times. 3. When 50 cycles finished, the samples will be taken out from experiment chamber and set aside a few minutes. As EPDs return to room temperature, tests will observe the appearance, and test electrical and optical performance based on standard # IEC 60068-2-14NB.	When experiment finished, the EPD must meet electrical and optical performance standards.
8	UV exposure Resistance	765 W/m^2 for 168 hrs,40℃	Standard # IEC 60068-2-5 Sa	
9	Electrostatic discharge	Machine model:+/- 250V, 0Ω, 200pF	Standard # IEC61000-4-2	
10	Package Vibration	1.04G,Frequency : 10~500Hz Direction : X,Y,Z Duration:1hours in each direction	Full packed for shipment	
11	Package Drop Impact	Drop from height of 122 cm on Concrete surface Drop sequence:1 corner, 3edges, 6face One drop for each.	Full packed for shipment	

Actual EMC level to be measured on customer application.

Note: (1) The protective film must be removed before temperature test.

(2) In order to make sure the display module can provide the best display quality, the update should be made after putting the display module in stable temperature environment for 4 hours at 25℃.

(3) There's temperature vs display quality limitation in our display module, we guarantee 1pixel display quality from 0℃~40℃.

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3. Electrical Characteristics

3.1 Absolute maximum rating

Parameter	Symbol	Rating	Unit
Logic Supply Voltage	V_{CI}	-0.3 to +6.0	V
Logic Input Voltage	V_{IN}	-0.3 to VCI +2.4	V
Operating Temp. range	T_{OPR}	0 to + 40	℃
Storage Temp. range	T_{STG}	-25 to + 60	℃
Humidity range	-	40~70	%RH

***Note: Avoid direct sunlight.**

3.2 Panel DC Characteristics

The following specifications apply for: VSS = 0V, VCI = 3.3V, TA = 25℃

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Single ground	V_{SS}	-	-	0	-	V
Logic Supply Voltage	VCI	-	2.3	3.3	3.6	V
High level input voltage	VIH	Digital input pins	0.7VCI	-	VCI	V
Low level input voltage	VIL	Digital input pins	0	-	0.3VCI	V
High level output voltage	VOH	Digital input pins , IOH= 400uA	VCI-0.4	-	-	V
Low level output voltage	VOL	Digital input pins , IOL= -400uA	GND	-	GND+0.4	V
Image update current	I_{UPDATE}	-	-	8	10	mA
Operating temperature	-	-	0	-	40	℃
Storage temperature	-	-	-25	-	60	℃
Image update Time at 25℃	-	-	-	16	43	Sec
Deep sleep mode current	I_{VCI}	DC/DC off No clock No input load Ram data not retain	-	2	5	uA

The Typical power consumption is measured with following pattern transition: from horizontal 2 gray scale pattern to vertical 2 gray scale pattern. (Note 3-1)

The standby power is the consumed power when the panel controller is in standby mode.

The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by Good Display.

Vcom is recommended to be set in the range of assigned value ± 0.1V.

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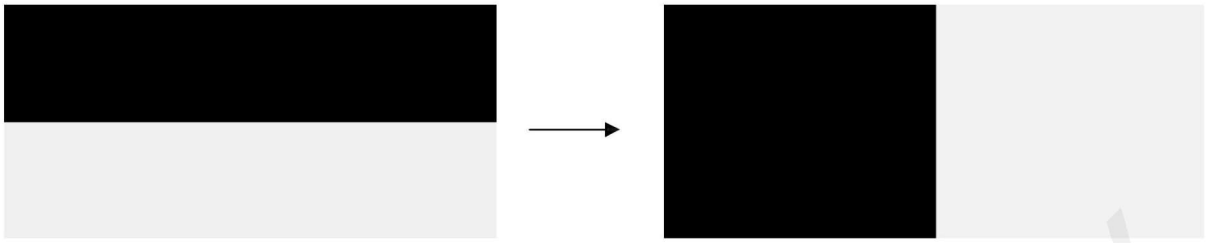
Note 3-1: The Typical power consumption



3.3 Panel AC Characteristics

3.3-1) Oscillator frequency

The following specifications apply for: VSS = 0V, VCI = 3.3V, T_A = 25℃

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Internal Oscillator frequency	Fosc	VCI=2.3 to 3.6V	-	1.625	-	MHz

3.3-2) MCU Interface

3.3-2-1) MCU Interface Selection

In this module, there are 4-wire SPI and 3-wire SPI that can communicate with MCU. The MCU interface mode can be set by hardware selection on BS pins. When it is "Low", 4-wire SPI is selected. When it is "High", 3-wire SPI (9 bits SPI) is selected.

Pin Name	Data/Command Interface		Control Signal		
Bus interface	D1	D0	CSB	DC	RST_N
SPI4	SDA	SCL	CSB	DC	RST_N
SPI3	SDA	SCL	CSB	L	RST_N

Table 3-1: MCU interface assignment under different bus interface mode

Note 3-2: L is connected to VSS

Note 3-3: H is connected to VCI

3.3-2-2) MCU Serial Interface (4-wire SPI)

The 4-wire SPI consists of serial clock SCL, serial data SDA, DC, CSB. In SPI mode, D0 acts as SCL, D1 acts as SDA.

Function	CSB	DC	SCL
Write Command	L	L	↑
Write data	L	H	↑

Table 3-2: Control pins of 4-wire Serial Peripheral interface

Note 3-4: ↑stands for rising edge of signal

SDA is shifted into an 8-bit shift register in the order of D7, D6, ... D0. The data byte in the shift register is written to the Graphic Display Data RAM (RAM) or command register in the same clock. Under serial mode, only write operations are allowed.

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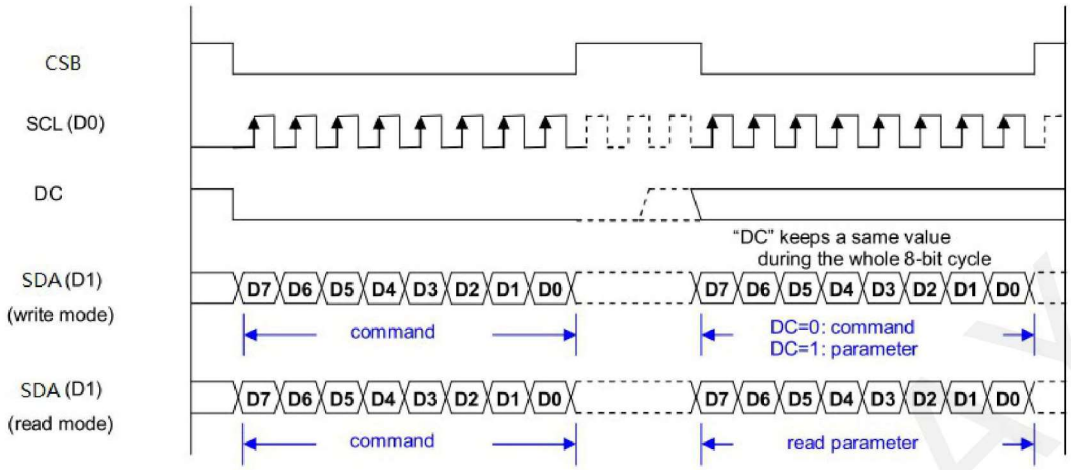

Figure 3-1: Write procedure in 4-wire Serial Peripheral Interface mode

3-3-2-3) MCU Serial Interface (3-wire SPI)

The 3-wire serial interface consists of serial clock SCL, serial data SDA and CSB.

In 3-wire SPI mode, D0 acts as SCL, D1 acts as SDA, The pin DC can be connected to an external ground.

The operation is similar to 4-wire serial interface while DC pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: DC bit, D7 to D0 bit. The DC bit (first bit of the sequential data) will determine the following data byte in shift register is written to the Display Data RAM (DC bit = 1) or the command register (DC bit = 0).Under serial mode, only write operations are allowed.

Function	CSB	DC	SCL
Write Command	L	Tie LOW	↑
Write data	L	Tie LOW	↑

Table 3-3: Control pins of 3-wire Serial Peripheral Interface

Note 3-5: ↑stands for rising edge of signal

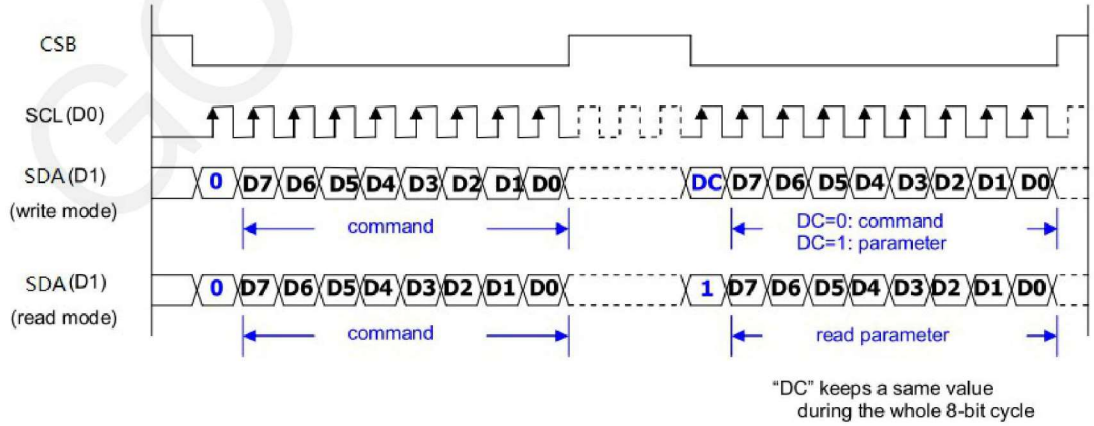

Figure 3-2: Write procedure in 3-wire Serial Peripheral Interface mode

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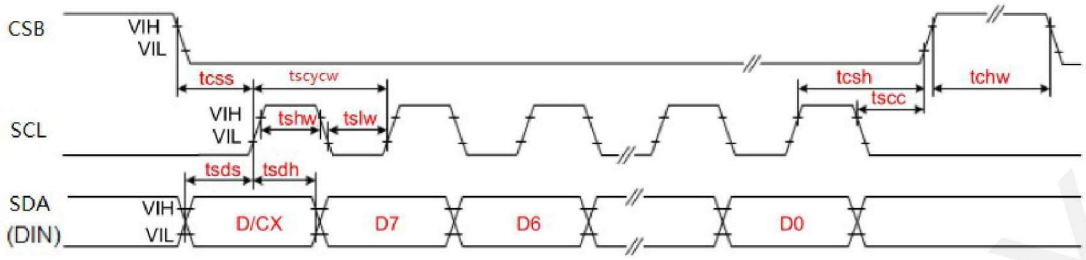
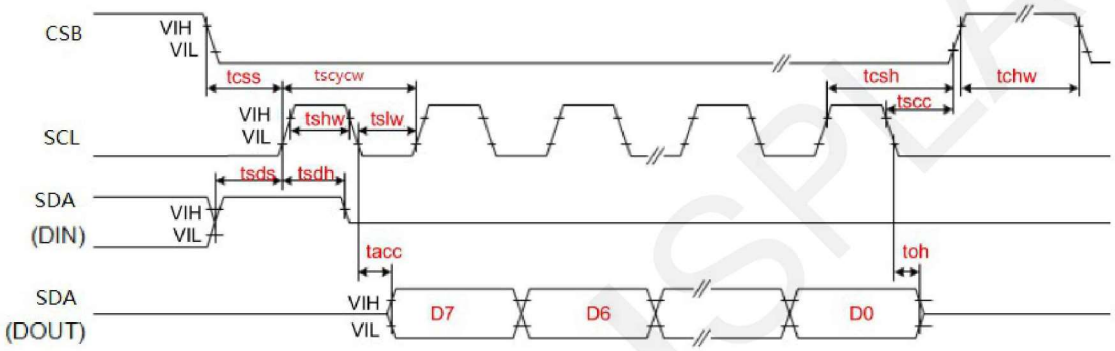
3.3-3) Timing Characteristics of Series Interface



3-wire Serial Interface – Write



3-wire Serial Interface – Read

Symbol	Signal	Parameter	Min	Typ	Max	Unit
tcss	CSB	Chip Select Setup Time	60	-	-	ns
tcsh		Chip Select Hold Time	65	-	-	ns
tscc		Chip Select Setup Time	20	-	-	ns
tchw		Chip Select Setup Time	150	-	-	ns
tscycw	SCL	Serial clock cycle (write)	100	-	-	ns
tshw		SCL "H" pulse width (write)	35	-	-	ns
tslw		SCL"L" pulse width (write)	35	-	-	ns
tscycr		Serial clock cycle (Read)	150	-	-	ns
tshr		SCL "H" pulse width (Read)	60	-	-	ns
tslr		SCL "L" pulse width (Read)	60	-	-	ns
tsds	SDA (DIN) (DOUT)	Data setup time	30	-	-	ns
tsdh		Data hold time	30	-	-	ns
tacc		Access time	10	-	-	ns
toh		Output disable time	15	-	-	ns

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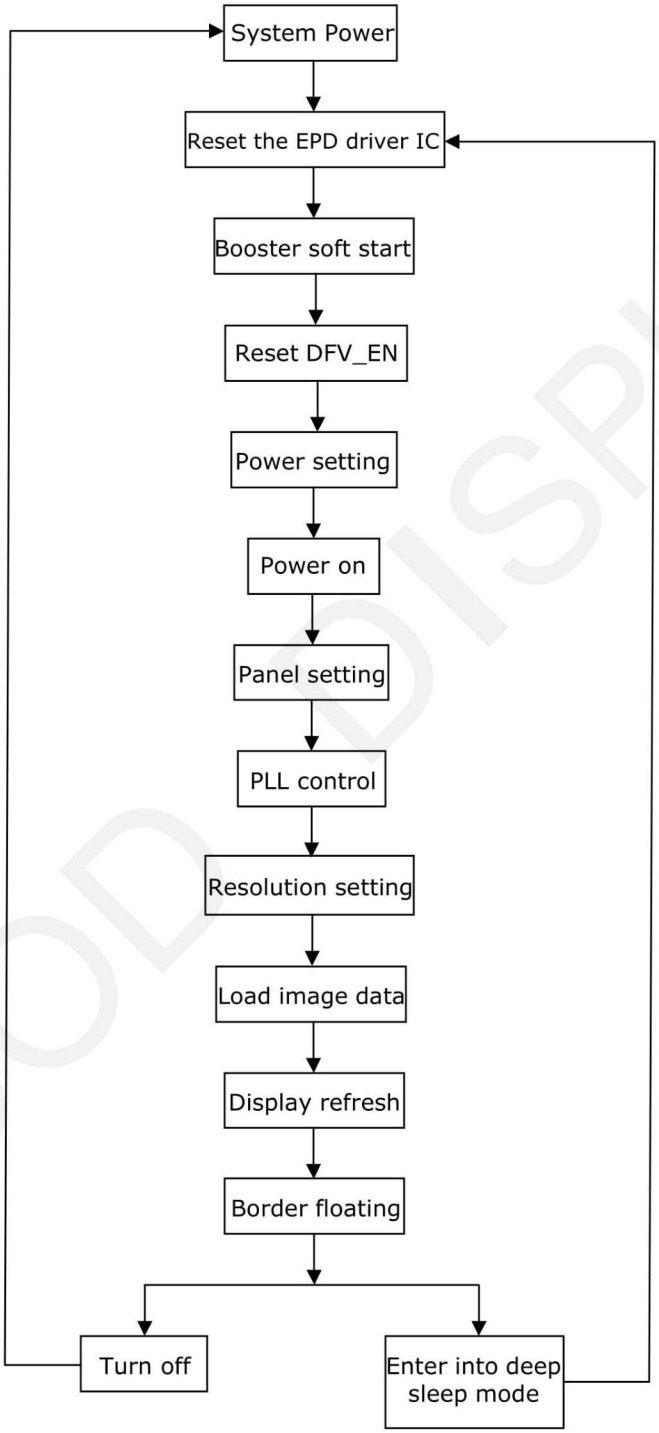
4. Typical Operating Sequence

4.1 Normal Operation Flow

4.1-1) BWR mode & LUT from Register



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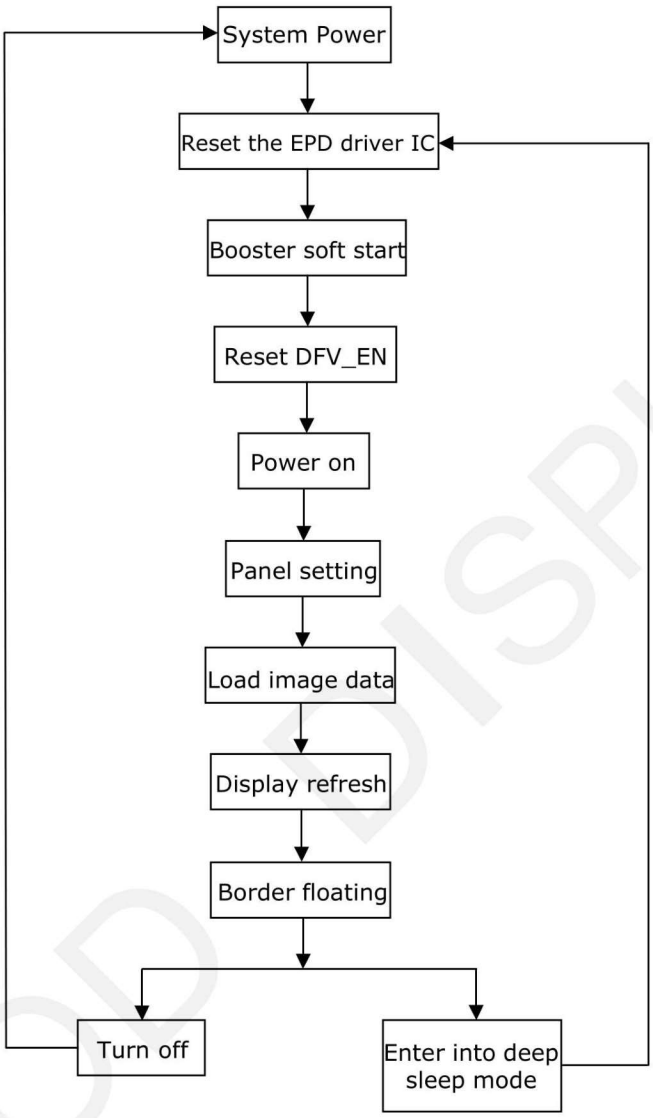
4.1-2) BWR mode & LUT from OTP



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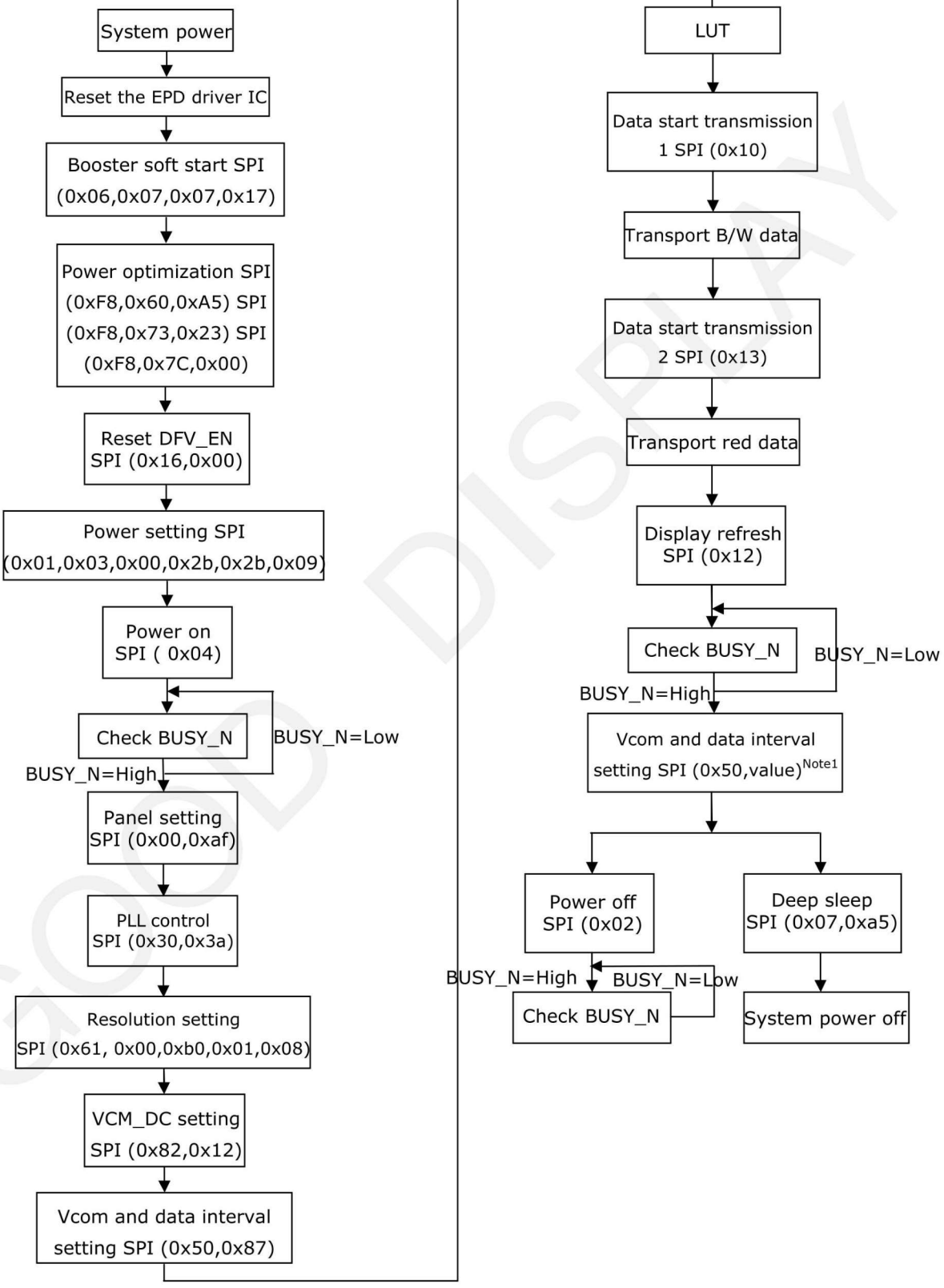
4.2 Reference Program Code

4.2-1) BWR mode & LUT from register



Note1: Set border to floating.

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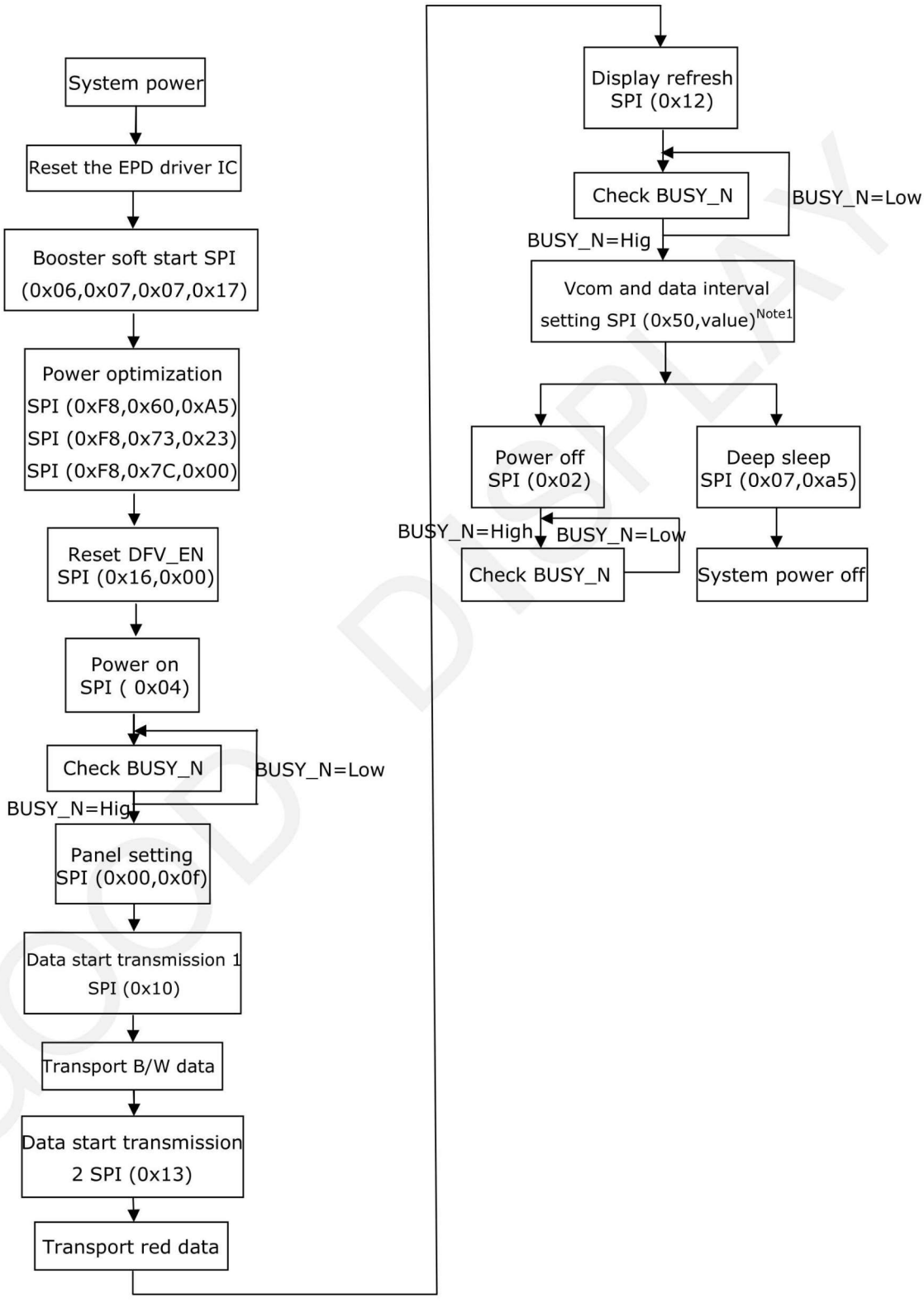
4.2-2) BWR mode & LUT from OTP



Note1: Set border to floating.

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5. Command Table

W/R: 0: Write cycle 1: Read cycle C/D: 0: Command 1: Data

D7~D0: -: Don't care #: Valid Data

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
1	Panel Setting(PSR)	0	0	0	0	0	0	0	0	0	0		00h
		0	1	#	#	#	#	#	#	#	#	ES[1],RES[0],LUT_EN,BWR, UD,SHL, SHD_N,RST_N	07h
2	Power setting (PWR)	0	0	0	0	0	0	0	0	0	1		01h
		0	1	-	-	-	-	-	-	#	#	VDS_EN, VDG_EN	03h
		0	1	-	-	-	-	-	#	#	#	VCOM_HV,VGHL_LV[1],VGHL_LV[0]	20h
		0	1	-	-	#	#	#	#	#	#	VDH[5:0]	26h
		0	1	-	-	#	#	#	#	#	#	VDL[5:0]	26h
		0	1	-	-	#	#	#	#	#	#	VDHR[5:0]	03h
3	Power OFF(POF)	0	0	0	0	0	0	0	0	1	0		02h
4	Power OFF Sequence Setting (PFS)	0	0	0	0	0	0	0	0	1	1		03h
		0	1	-	-	#	#	-	-	-	-	T_VDS_OFF[1:0]	00h
5	Power ON(PON)	0	0	0	0	0	0	0	1	0	0		04h
6	Power ON Measure (PMES)	0	0	0	0	0	0	0	1	0	1		05h
7	Booster Soft Start (BTST)	0	0	0	0	0	0	0	1	1	0		06h
		0	1	#	#	#	#	#	#	#	#	BT_PHA[7:0]	03h
		0	1	#	#	#	#	#	#	#	#	BT_PHB[7:0]	00h
		0	1	-	-	#	#	#	#	#	#	BT_PHC[5:0]	26h
8	Deep Sleep	0	0	0	0	0	0	0	1	1	1		07h
		0	1	1	0	1	0	0	1	0	1		A5h
9	Data Start Transmission 1 (DTM1)	0	0	0	0	0	1	0	0	0	0		10h
		0	1	#	#	#	#	#	#	#	#		00h
10	Data Stop(DSP)	0	0	0	0	0	1	0	0	0	1		11h
		1	1	#	-	-	-	-	-	-	-	Data_flag	00h
11	Display Refresh (DRF)	0	0	0	0	0	1	0	0	1	0		12h
12	Data start transmission 2(DTM2)	0	0	0	0	0	1	0	0	1	1		13h
		0	1	#	#	#	#	#	#	#	#		00h
13	Partial Data Start transmission 1(PDTM1)	0	0	0	0	0	1	0	1	0	0		14h
		0	1	#	#	#	#	#	#	#	#		00h

GOOD DISPLAY

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
14	Partial Data Start transmission2(PDTM2)	0	0	0	0	0	1	0	1	0	1		15h
		0	1	#	#	#	#	#	#	#	#		00h
15	Partial Display Refresh (PDRF)	0	0	0	0	0	1	0	1	1	0		16h
		0	1	#	#	#	#	#	#	#	#		00h
16	LUT for VCOM(LUT1)	0	0	0	0	1	0	0	0	0	0		20h
17	White to white LUT (LUTWW)	0	0	0	0	1	0	0	0	0	1		21h
18	Black to white LUT (LUTBW/LUTR)	0	0	0	0	1	0	0	0	1	0		22h
19	White to Black LUT(LUTWB/LUTW)	0	0	0	0	1	0	0	0	1	1		23h
20	Black to Black LUT (LUTBB/LUTB)	0	0	0	0	1	0	0	1	0	0		24h
21	PLL control(PLL)	0	0	0	0	1	1	0	0	0	0		30h
		0	1	#	#	#	#	#	#	#	#	SEL_DIV[1:0], SEL_F[5:0]	3Ch
22	Temperature Sensor Command (TSC)	0	0	0	1	0	0	0	0	0	0		40h
		1	1	#	#	#	#	#	#	#	#	D[10:3]/TS[7:0]	00h
		1	1	#	#	#	-	-	-	-	-	D[2:0]/-	00h
23	Temperature Sensor Calibration (TSE)	0	0	0	1	0	0	0	0	0	1		41h
		0	1	#	-	-	-	#	#	#	#	TSE,TO[3:0]	00h
24	Temperature Sensor Write (TSW)	0	0	0	1	0	0	0	0	1	0		42h
		0	1	#	#	#	#	#	#	#	#	WATTR[7:0]	00h
		0	1	#	#	#	#	#	#	#	#	WMSB[7:0]	00h
		0	1	#	#	#	#	#	#	#	#	WLSB[7:0]	00h
25	Temperature Sensor Read (TSR)	0	0	0	1	0	0	0	0	1	1		43h
		1	1	#	#	#	#	#	#	#	#	RMSB[7:0]	00h
		1	1	#	#	#	#	#	#	#	#	RLSB[7:0]	00h
26	Vcom and Data interval setting (CDI)	0	0	0	1	0	1	0	0	0	0		50h
		0	1	#	#	#	#	#	#	#	#	VBD[1:0],DDX[1:0],CDI[3:0]	D7h
27	Low power Detection (LPD)	0	0	0	1	0	1	0	0	0	1		51h
		1	1	-	-	-	-	-	-	-	LPD		-
28	TCON Setting (TCON)	0	0	0	1	1	0	0	0	0	0		60h
		0	1	#	#	#	#	#	#	#	#	S2G[3:0],G2S[3:0]	22h
29	TCON resolution (TRES)	0	0	0	1	1	0	0	0	0	1		61h
		0	1	-	-	-	-	-	-	-	#	HRES[8]	00h
		0	1	#	#	#	#	#	#	#	-	HRES[7:1]	00h
		0	1	-	-	-	-	-	-	-	#	VRES[8]	00h
		0	1	#	#	#	#	#	#	#	#	VRES[7:0]	00h

GOOD DISPLAY

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
30	Source & gate start setting	0	0	0	1	1	0	0	0	1	0		62h
		0	1	-	-	-	-	-	-	-	#	S_start[8]	00h
		0	1	#	#	#	#	#	#	#	#	S_start[7:0]	00h
		0	1	-	-	-	#	-	-	-	#	gscan, G_start[8]	00h
		0	1	#	#	#	#	#	#	#	#	G_start[7:0]	00h
31	Get Status (FLG)	0	0	0	1	1	1	0	0	0	1		71h
		1	1	-	-	#	#	#	#	#	#	I²C_ERR,I²C_BUSY_N, Data_flag, PON, POF, BUSY_N	02h
32	Auto Measure Vcom (AMV)	0	0	1	0	0	0	0	0	0	0		80h
		1	1	-	-	#	#	#	#	#	#	AMV[1:0],XON,AMVS,AMV, AMVE	10h
33	Vcom Value (VV)	0	0	1	0	0	0	0	0	0	1		81h
		0	1	-	#	#	#	#	#	#	#	VV[6:0]	00h
34	VCM_DC Setting register (VDCS)	0	0	1	0	0	0	0	0	1	0		82h
		0	1	-	#	#	#	#	#	#	#	VDCS[6:0]	00h
35	Program Mode(PGM)	0	0	1	0	1	0	0	0	0	0		A0h
		0	1	1	0	1	0	0	1	0	1		A5h
36	Active Program(APG)	0	0	1	0	1	0	0	0	0	1		A1h
37	Read OTP Data(ROTP)	0	0	1	0	1	0	0	0	1	0		A2h
		1	1	#	#	#	#	#	#	#	#		-

GOOD DISPLAY

(1) Panel Setting (PSR) (Register: R00H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Setting the panel	0	0	0	0	0	0	0	0	0	0
	0	1	RES1	RES0	LUT_EN	BWR	UD	SHL	SHD_N	RST_N

RES[1:0]: Display resolution setting (source×gate)

00b: 320×300 (default)

01b: 300×200

10b: 296×160

11b: 296×128

LUT_EN: LUT selection setting.

0: Using LUT from OTP. (default)

1: Using LUT from register.

BWR: Color selecting setting.

0: Pixel with B/W/Red. Run both LU1 and LU2. (default)

1: Pixel with B/W. Run LU1 only.

UD: Gate Scan Direction

0: Scan down First line to last: Gn→...→ G1 (default)

1: Scan up. (default) First line to last: G1→...→ Gn

SHL: Source shift direction

0: shift left. First data to last data: Sn→...→ S1

1: shift right First data to last data: S1→... →Sn (default)

SHD_N: Booster switch

0: Booster OFF, register data are kept, and SEG/BG/VCOM are kept floating.

1: Booster ON (default)

When SHD_N become low, DC-DC will turn OFF. Register and SRAM data will keep until VDD OFF. SD output and VCOM will base on previous condition and keep floating.

RST_N: Soft Reset

0: No effect.

1: Booster OFF, Register data are set to their default values, and SEG/BG/VCOM: 0V. (default)

When RST_N become low, driver will reset. All register will reset to default value. Driver all function will disable. SD output and VCOM will base on previous condition and keep floating.

GOOD DISPLAY

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(2) Power Setting Register (R01H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Selecting Internal/External Power	0	0	0	0	0	0	0	0	0	1
	0	1	-	-	-	-	-	-	VDS_EN	VDG_EN
	0	1	-	-	-	-	-	VCOM_HV	VGHL_LV[1:0]	
	0	1	-	-	VDH[5:0]					
	0	1	-	-	VDL[5:0]					
	0	1	-	-	VDHR[5:0]					

VDS_EN: Source power selection

0: External source power from VDH/VDL pins

1: Internal DC/DC function for generate VDH/VDL

VDG_EN: Gate power selection

0: External VDNS power from VGH/VGL pins. (VDNG_EN open)

1: Internal DC/DC function for generate VGH/VGL.

VCOM_HV: VCOM Voltage Level

0: VCOMH=VDH+VCOMDC, VCOML=VHL+VCOMDC

1: VCOML=VGH, VCOML=VGL

VGHL_LV[1:0]: VGH / VGL Voltage Level selection.

VGHL_LV	VGHL voltage level
00(Default)	VGH=16V,VGL= -16V
01	VGH=15V,VGL= -15V
10	VGH=14V,VGL= -14V
11	VGH=13V,VGL= -13V

VDH[5:0]: Internal VDH power selection for B/W pixel.(Default value: 100110b)

VDH	VDH_V	VDH	VDH_V
000000	2.4V	…	…
000001	2.6V	100110	10.0V
000010	2.8V	100111	10.2V
000011	3.0V	101000	10.4V
000100	3.2V	101001	10.6V
000101	3.4V	101010	10.8V
000110	3.6V	101011	11.0V
000111	3.8V	(others)	11.0V

VDL[5:0]: Internal VDL power selection for B/W pixel. (Default value: 100110b)

VDL	VDL_V	VDL	VDL_V
000000	-2.4V	…	…
000001	-2.6V	100110	-10.0V
000010	-2.8V	100111	-10.2V
000011	-3.0V	101000	-10.4V
000100	-3.2V	101001	-10.6V
000101	-3.4V	101010	-10.8V
000110	-3.6V	101011	-11.0V
000111	-3.8V	(others)	-11.0V

GOOD DISPLAY

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VDHR[5:0]: Internal VDHR power selection for Red pixel. (Default value: 000011b)

VDHR	VDHR _V	VDHR	VDHR _V
000000	2.4V	…	…
000001	2.6V	100110	10.0V
000010	2.8V	100111	10.2V
000011	3.0V	101000	10.4V
000100	3.2V	101001	10.6V
000101	3.4V	101010	10.8V
000110	3.6V	101011	11.0V
000111	3.8V	(others)	11.0V

(3) Power OFF (PWR) (R02H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Turning OFF the power	0	0	0	0	0	0	0	0	1	0

After the Power Off command, the driver will power off following the Power Off Sequence.

After the Power Off command, BUSY_N signal will drop from high to low. When finish the power off sequence, BUSY_N signal will rise from low to high.

This command will turn off charge pump, T-con, source driver, gate driver, VCOM, and temperature sensor, but register data and SRAM data will kept until VDD OFF.

Source Driver output and Vcom will base on previous condition, which may have 2 condition: 0V or floating.

(4) Power OFF Sequence Setting (R03H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Setting Power OFF Sequence	0	0	0	0	0	0	0	0	1	1
	0	1	-	-	Vsh_off[1:0]		Vsl_off[1:0]		Vshr_off[1:0]	

Vshr_off[1:0]: 00: 5 ms (Default) 01: 10 ms 10: 20 ms 11: 40 ms

Vsl_off[1:0]: 00: 5 ms (Default) 01: 10 ms 10: 20 ms 11: 40 ms

Vsh_off[1:0]: 00: 5 ms (Default) 01: 10 ms 10: 20 ms 11: 40 ms

(5) Power ON (R04H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Turnning ON the Power	0	0	0	0	0	0	0	1	0	0

After the Power ON command, driver will power on based on the Power ON Sequence.

After Power On command, BUSY_N signal will drop from high to low. When finishing the power off sequence, BUSY_N signal will rise from low to high.

GOOD DISPLAY

(6) Power ON Measure (PMES) (R05H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
	0	0	0	0	0	0	0	1	0	1

If user want to read temperature sensor or detect low power in power off mode, user has to send this command. After power on measure command, driver will switch on relevant commend with Low Power detection (R51H) and temperature measurement. (R40H).

(7) Booster Soft Start (BTST) (R06H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Starting data transmission	0	0	0	0	0	0	0	1	1	0
	0	1	BT_PHA7	BT_PHA6	BT_PHA5	BT_PHA4	BT_PHA3	BT_PHA2	BT_PHA1	BT_PHA0
	0	1	BT_PHB7	BT_PHB6	BT_PHB5	BT_PHB4	BT_PHB3	BT_PHB2	BT_PHB1	BT_PHB0
	0	1	-	-	BT_PHC5	BT_PHC4	BT_PHC3	BT_PHC2	BT_PHC1	BT_PHC0

BTPHA[7:6]: Soft start period of phase A.
00b: 10mS 01b: 20mS 10b: 30mS 11b: 100mS

BTPHA[5:3]: Driving strength of phase A
000b:strength1 001b:strength2 **010b:strength3** 011b:strength4
100b:strength5 101b:strength6 110b:strength7 111b:strength8 (strongest)

BTPHA[2:0]: Minimum OFF time setting of GDR in phase B
000b: 0.27uS 001b: 0.34uS 010b: 0.40uS 011b: 0.54uS
100b: 0.80uS 101b: 1.54uS 110b: 3.34uS **111b: 6.58uS**

BTPHB[7:6]: Soft start period of phase B.
00b: 10mS 01b: 20mS 10b: 30mS 11b: 100mS

BTPHB[5:3]: Driving strength of phase B
000b:strength1 001b:strength2 **010b:strength3** 011b:strength4
100b:strength5 101b:strength6 110b:strength7 111b:strength8 (strongest)

BTPHB[2:0]: Minimum OFF time setting of GDR in phase B
000b: 0.27uS 001b: 0.34uS 010b: 0.40uS 011b: 0.54uS
100b: 0.80uS 101b: 1.54uS 110b: 3.34uS **111b: 6.58uS**

BTPHC[5:3]: Driving strength of phase C
000b:strength1 001b:strength2 **010b:strength3** 011b:strength4
100b:strength5 101b:strength6 110b:strength7 111b:strength8 (strongest)

BTPHC[2:0]: Minimum OFF time setting of GDR in phase C
000b: 0.27uS 001b: 0.34uS 010b: 0.40uS 010b: 0.40uS
100b: 0.80uS 101b: 1.54uS 110b: 3.34uS **111b: 6.58uS**

(8) Deep Sleep (DSLP) (R07H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Deep Sleep	0	0	0	0	0	0	0	1	1	1
	0	1	1	0	1	0	0	1	0	1

GOOD DISPLAY

After this command is transmitted, the chip would enter the deep-sleep mode to save power.

The deep sleep mode would return to standby by hardware reset.

The only one parameter is a check code, the command would be executed if check code = 0xA5.

(9) Data Start Transmission 1 (R10H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Starting data transmission	0	0	0	0	0	1	0	0	0	0
	0	1	Pixel1	Pixel2	Pixel3	Pixel4	Pixel5	Pixel6	Pixel7	Pixel8
	0	1	..	..	..	..	..	..	..	..
	0	1	Pixel(n-7)	Pixel(n-6)	Pixel(n-5)	Pixel(n-4)	Pixel(n-3)	Pixel(n-2)	Pixel(n-1)	Pixel(n)

The register is indicates that user start to transmit data, then write to SRAM. While data transmission complete, user must send command 11H. Then chip will start to send data/VCOM for panel.

In B/W mode, this command writes "OLD" data to SRAM.

In B/W/Red mode, this command writes "B/W" data to SRAM.

(10) Data stop (R11H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Stopping data transmission	0	0	0	0	0	1	0	0	0	1
	1	1	data_flag	-	-	-	-	-	-	-

While finished the data transmitting, user must send this command to driver and read Data_flag information.

Data_flag: Data flag of receiving user data.

0: Driver didn't receive all the data.

1: Driver has already received all the one-frame data (DTM1 and DTM2).

After "Data Start" (10h) or "Data Stop" (11h) commands and when data_flag=1, BUSY_N signal will become "0" and the refreshing of panel starts. This command only actives when BUSY_N = "1".

(11) Display Refresh Command (R12H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Refreshing the display	0	0	0	0	0	1	0	0	1	0

After this command is issued, driver will refresh display (data/VCOM) according to SRAM data and LUT. After Display Refresh command, BUSY_N signal will become "0".

This command only active when BUSY_N = "1".

GOOD DISPLAY

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(12) Data start transmission 2 register (R13H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Data start transmission 2 (DTM2)	0	0	0	0	0	1	0	0	1	0
	0	1	Kpixel1	Kpixel2	Kpixel3	Kpixel4	Kpixel5	Kpixel6	Kpixel7	Kpixel8
	0	1	..	..	..	..	..	..	..	..
	0	1	Kpixel(n-7)	Kpixel(n-6)	Kpixel(n-5)	Kpixel(n-4)	Kpixel(n-3)	Kpixel(n-2)	Kpixel(n-1)	Kpixel(n)

The register is indicates that user start to transmit data, then write to SRAM. While data transmission complete, user must send command 11H.

Then chip will start to send data/VCOM for panel.

In B/W mode, this command writes “NEW” data to SRAM.

In B/W/Red mode, this command writes “RED” data to SRAM.

(13) Partial Data Start transmission 1 register (R14h)

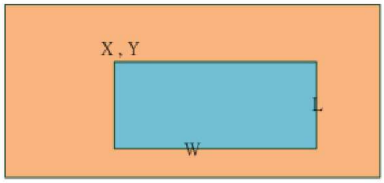
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Partial Data Start transmission 1	0	0	0	0	0	1	0	1	0	0
	0	1	-	-	-	-	-	-	-	X[8]
	0	1	X[7]	X[6]	X[5]	X[4]	X[3]	0	0	0
			-	-	-	-	-	-	-	Y[8]
	0	1	Y[7]	Y[6]	Y[5]	Y[4]	Y[3]	Y[2]	Y[1]	Y[0]
	0	1	-	-	-	-	-	-	-	W[8]
	0	1	W[7]	W[6]	W[5]	W[4]	W[3]	0	0	0
			-	-	-	-	-	-	-	L[8]
	0	1	L[7]	L[6]	L[5]	L[4]	L[3]	L[2]	L[1]	L[0]
	0	1	Kpixel1	Kpixel2	Kpixel3	Kpixel4	Kpixel5	Kpixel6	Kpixel7	Kpixel8
	0	1	..	..	..	..	..	..	..	..
	0	1	Kpixel(n-7)	Kpixel(n-6)	Kpixel(n-5)	Kpixel(n-4)	Kpixel(n-3)	Kpixel(n-2)	Kpixel(n-1)	Kpixel(n)

The command define as follows: The register is indicates that user start to transmit data, then write to SRAM. While data transmission complete, user must send command 11H. Then chip will start to send data/VCOM for panel.

In B/W mode, this command writes “OLD” data to SRAM.

In B/W/Red mode, this command writes “B/W” data to SRAM.

Partial update location and area



Note: X and W should be the multiple of 8.

GOOD DISPLAY

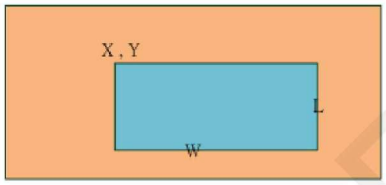
(14) Partial Data Start transmission 2 register (R15h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Partial Data Start transmission 2	0	0	0	0	0	1	0	1	0	1
	0	1	-	-	-	-	-	-	-	X[8]
	0	1	X[7]	X[6]	X[5]	X[4]	X[3]	0	0	0
			-	-	-	-	-	-	-	Y[8]
	0	1	Y[7]	Y[6]	Y[5]	Y[4]	Y[3]	Y[2]	Y[1]	Y[0]
	0	1	-	-	-	-	-	-	-	W[8]
	0	1	W[7]	W[6]	W[5]	W[4]	W[3]	0	0	0
			-	-	-	-	-	-	-	L[8]
	0	1	L[7]	L[6]	L[5]	L[4]	L[3]	L[2]	L[1]	L[0]
	0	1	Kpixel1	Kpixel2	Kpixel3	Kpixel4	Kpixel5	Kpixel6	Kpixel7	Kpixel8
	0	1	..	..	..	..	..	..	..	..
	0	1	Kpixel(n-7)	Kpixel(n-6)	Kpixel(n-5)	Kpixel(n-4)	Kpixel(n-3)	Kpixel(n-2)	Kpixel(n-1)	Kpixel(n)

The command define as follows: The register is indicates that user start to transmit data, then write to SRAM. While data transmission complete, user must send command 11H. Then chip will start to send data/VCOM for panel.

In B/W mode, this command writes “NEW” data to SRAM.

In B/W/Red mode, this command writes “RED” data to SRAM. Partial update location and area



Note: X and W should be the multiple of 8.

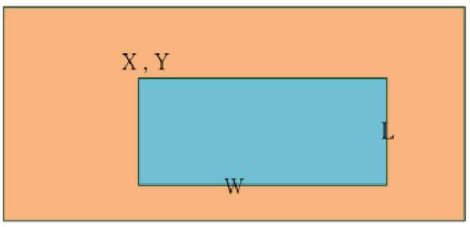
(15) Partial Display Refresh Command (R16h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Partial Display Refresh	0	0	0	0	0	1	0	1	1	0
	0	1	DFV_EN							X[8]
	0	1	X[7]	X[6]	X[5]	X[4]	X[3]	0	0	0
										Y[8]
	0	1	Y[7]	Y[6]	Y[5]	Y[4]	Y[3]	Y[2]	Y[1]	Y[0]
	0	1								W[8]
	0	1	W[7]	W[6]	W[5]	W[4]	W[3]	W[2]	W[1]	W[0]
										L[8]
	0	1	L[7]	L[6]	L[5]	L[4]	L[3]	L[2]	L[1]	L[0]

GOOD DISPLAY

While user sent this command, driver will refresh display (data/VCOM) base on SRAM data and LUT.

Only the area (X,Y, W, L) would update, the others pixel output would follow VCOM LUT After display refresh command, BUSY_N signal will become “0”.



Note: X and W should be the multiple of 8.

DFV_EN: data follow VCOM function on display area.

DFV_EN=1: Only effective in B/W mode, if pixel from “New data” SRAM equal to “Old data” SRAM on display area, this pixel output would follow VCOM LUT.

DFV_EN=0: Data doesn’t follow VCOM LUT.

This command only active when BUSY_N = “1”.

(16) VCOM LUT (LUTC) (R20H)

This command builds Look-up Table for VCOM

(17) W2W LUT (LUTWW) (R21H)

This command builds Look-up Table for White-to-White.

(18) B2W LUT (LUTBW/LUTR) (R22H)

This command builds Look-up Table for Black-to-White.

(19) W2B LUT (LUTWB/LUTW) (R23H)

This command builds Look-up Table for White - to- Black.

(20) B2B LUT (LUTBB / LUTB) (R24H)

This command builds Look-up Table for Black - to- Black.

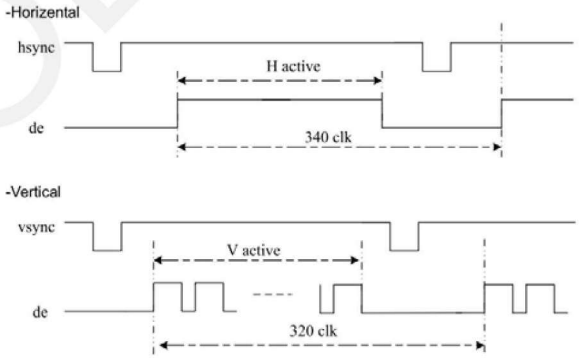
(21) PLL Control (R30H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Controlling PLL	0	0	0	0	1	1	0	0	0	0
	0	1	-SEL_DIV[1:0]		SEL_F[5:0]					

The command controls the PLL clock frequency. The PLL structure must support the following frame rates:

GOOD DISPLAY

SEL_F[5:0]	SEL_DIV[1:0]				SEL_F[5:0]	SEL_DIV[1:0]			
	00	01	10	11		00	01	10	11
000000	156.25	78.13	39.06	-	100000	153.49	76.75	38.37	-
000001	159.01	79.5	39.75	-	100001	150.74	75.37	37.68	-
000010	161.76	80.88	40.44	20.22	100010	147.98	73.99	36.99	-
000011	164.52	82.26	41.13	20.57	100011	145.22	72.61	36.31	-
000100	167.28	83.64	41.82	20.91	100100	142.46	71.23	35.62	-
000101	170.04	85.02	42.51	21.25	100101	139.71	69.85	34.93	-
000110	172.79	86.4	43.2	21.6	100110	136.95	68.47	34.24	-
000111	175.55	87.78	43.89	21.94	100111	134.19	67.1	33.55	-
001000	178.31	89.15	44.58	22.29	101000	131.43	65.72	32.86	-
001001	181.07	90.53	45.27	22.63	101001	128.68	64.34	32.17	-
001010	183.82	91.91	45.96	22.98	101010	125.92	62.96	31.48	-
001011	186.58	93.29	46.65	23.32	101011	123.16	61.58	30.79	-
001100	189.34	94.67	47.33	23.67	101100	120.4	60.2	30.1	-
001101	192.1	96.05	48.02	24.01	101101	117.65	58.82	29.41	-
001110	194.85	97.43	48.71	24.36	101110	114.89	57.44	28.72	-
001111	197.61	98.81	49.4	24.7	101111	112.13	56.07	28.03	-
010000	-	100.18	50.09	25.05	110000	109.38	54.69	27.34	-
010001	-	101.56	50.78	25.39	110001	106.62	53.31	26.65	-
010010	-	102.94	51.47	25.74	110010	103.86	51.93	25.97	-
010011	-	104.32	52.16	26.08	110011	101.1	50.55	25.28	-
010100	-	105.7	52.85	26.42	110100	98.35	49.17	24.59	-
010101	-	107.08	53.54	26.77	110101	95.59	47.79	23.9	-
010110	-	108.46	54.23	27.11	110110	92.83	46.42	23.21	-
010111	-	109.83	54.92	27.46	110111	90.07	45.04	22.52	-
011000	-	111.21	55.61	27.8	111000	87.32	43.66	21.83	-
011001	-	112.59	56.3	28.15	111001	84.56	42.28	21.14	-
011010	-	113.97	56.99	28.49	111010	81.8	40.9	20.45	-
011011	-	115.35	57.67	28.84	111011	79.04	39.52	-	-
011100	-	116.73	58.36	29.18	111100	76.29	38.14	-	-
011101	-	118.11	59.05	29.53	111101	73.53	36.76	-	-
011110	-	119.49	59.74	29.87	111110	70.77	35.39	-	-
011111	-	120.86	60.43	30.22	111111	68.01	34.01	-	-



GOOD DISPLAY

(22) Temperature Sensor Calibration (R40H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Sensing Temperature	0	0	0	1	0	0	0	0	0	0
	1	1	D10	D9/TS6	D8/TS5	D7/TS4	D6/TS3	D5/TS2	D4/TS1	D3/TS0
	1	1	D2	D1	D0	-	-	-	-	-

This command reads the temperature sensed by the temperature sensor.

TS[7:0]: When TSE (R41h) is set to 0, this command reads internal temperature sensor value.

D[10:0]: When TSE (R41h) is set to 1, this command reads external LM75 temperature sensor value.

(23) Temperature Sensor Calibration (R41H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Calibrate Temperature Sensor	0	0	0	1	0	0	0	0	0	1
	0	1	TSE	-	-		TO[3:0]			

This command selects Internal or External temperature sensor.

TSE: Internal temperature sensor switch

0: Enable (default) 1: Disable; using external sensor.

TO[3:0]: Temperature offset.

TO[3]: sign bit 0b: + 1b: -

TO[2:0]: offset value

TO[3:0]	Calculation	TO[3:0]	Calculation
0000 b	0	1000	-8
0001	1	1001	-7
0010	2	1010	-6
…	…	…	…
0110	6	1110	-2
0111	7	1111	-1

(24) Temperature Sensor Write (TSW) (R42H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Write External Temperature Sensor	0	0	0	1	0	0	0	0	1	0
	0	1	WATTR[7:0]							
	0	1	WMSB[7:0]							
	0	0	WLSB[7:0]							

This command reads the temperature sensed by the temperature sensor.

WATTR: D[7:6]: I2C Write Byte Number

00b : 1 byte (head byte only)

01b : 2 bytes (head byte + pointer)

10b : 3 bytes (head byte + pointer + 1st parameter)

11b : 4 bytes (head byte + pointer + 1st parameter + 2nd parameter)

D[5:3]: User-defined address bits (A2, A1, A0)

D[2:0]: Pointer setting

COG DISPLAY

WMSB[7:0]: MSByte of write-data to external temperature sensor.
WLSB[7:0]: LSByte of write-data to external temperature sensor.
This command only actives after R04H(PON) or R05H(PMES).

(25) Temperature Sensor Read (TSR) (R43H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Read External Temperature Sensor	0	0	0	1	0	0	0	0	1	1
	1	1	RMSB[7:0]							
	1	1	RLSB[7:0]							

This command reads the temperature sensed by the temperature sensor.
RMSB[7:0]: MSByte read data from external temperature sensor.
RLSB[7:0]: LSByte read data from external temperature sensor.
This command only actives after R04H(PON) or R05H(PMES).

(26) VCOM and Data Interval Setting (R50H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set Interval between Vcom and Data	0	0	0	1	0	1	0	0	0	0
	0	1	VBD[1:0]		DDX[1:0]		CDI[3:0]			

This command indicates the interval of Vcom and data output. When setting the vertical back porch, the total blanking will be kept (20 Hsync).
VBD[1:0]: Border data selection
B/W/Red mode (BWR=0)

DDX[0]	VBD[1:0]	LUT	DDX[0]	VBD[1:0]	LUT
0	00	Floating	1(Default)	00	LUTB
	01	LUTR		01	LUTW
	10	LUTW		10	LUTR
	11	LUTB		11(default)	Floating

B/W mode (BWR=1)

DDX[0]	VBD[1:0]	LUT	DDX[0]	VBD[1:0]	LUT
0	00	Floating	1(Default)	00	Floating
	01	LUTBW (1→0)		01	LUTWB (1→0)
	10	LUTWB (0→1)		10	LUTBW (0→1)
	11	Floating		11	Floating

DDX[1:0]: Data polality
DDX[1] for RED data, DDX[0] for BW data in the B/W/Red mode.
DDX[0] for B/W mode.

B/W/Red mode (BWR=0)

GOOD DISPLAY

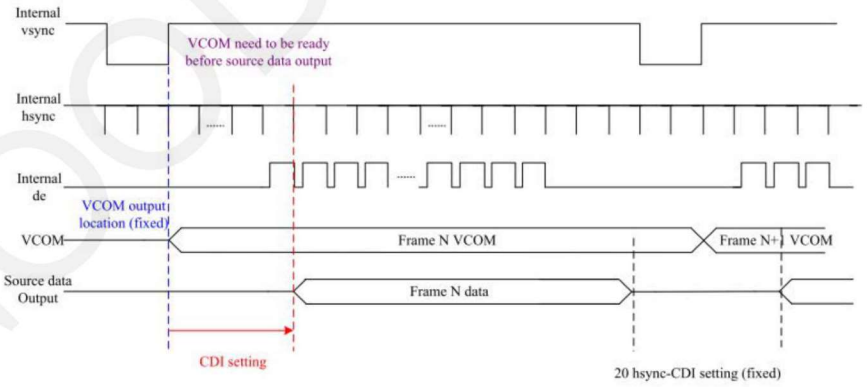
DDX[1:0]	Data{Red, B/W}	LUT	DDX[1:0]	Data{Red, B/W}	LUT
00	00	LUTW	10	00	LUTR
	01	LUTB		01	LUTR
	10	LUTR		10	LUTW
	11	LUTR		11	LUTB
01(Default)	00	LUTB	11	00	LUTR
	01	LUTW		01	LUTR
	10	LUTR		10	LUTB
	11	LUTR		11	LUTW

B/W mode (BWR=1)

DDX[0]	Data{New, Old}	LUT	DDX[0]	Data{New, Old}	LUT
0	00	LUTWW (0→0)	1(Default)	00	LUTBB (0→0)
	01	LUTBW (1→0)		01	LUTWB (1→0)
	10	LUTWB (0→1)		10	LUTBW (0→1)
	11	LUTBB (1→1)		11	LUTWW (1→1)

CDI[3:0]: Vcom and data interval

CDI[3:0]	Vcom and Data Interval	CDI[3:0]	Vcom and Data Interval
0000 b	17 hsync	0110	11
0001	16	0111	10 (Default)
0010	15	…	…
0011	14	1101	4
0100	13	1110	3
0101	12	1111	2



(27) Low Power Detection (LPD) (R51H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Detect Low Power	0	0	0	1	0	1	0	0	0	1
	1	1	-	-	-	-	-	-	-	LPD

This command indicates the input power condition. Host can read this flag to learn the battery condition.

GOOD DISPLAY

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LPD: Interval Low Power Detection Flag

0: Low power input (VDD < 2.5V) 1: Normal status (default)

(28) TCON Setting (TCON) (R60H)

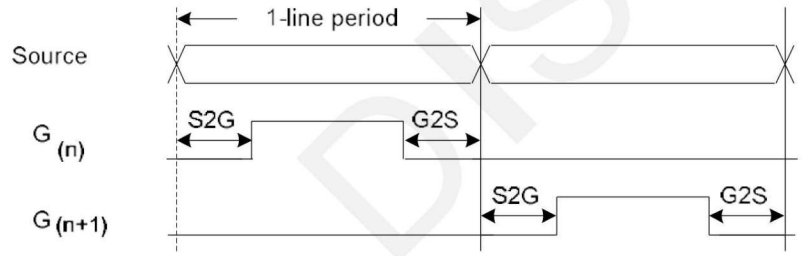
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set Gate/Source Non-overlap Period	0	0	0	1	0	1	0	0	0	0
	0	1	S2G[3:0]				G2S[3:0]			

This command defines non-overlap period of Gate and Source.

S2G[3:0] or G2S[3:0]: Source to Gate / Gate to Source Non-overlap period

S2G[3:0] or G2S[3:0]	Period		S2G[3:0] or G2S[3:0]	Period
0000b	4		...	...
0001	8		1011	48
0010	12(Default)		1100	52
0011	16		1101	56
0100	20		1110	60
0101	24		1111	64

Period = 660 nS.



(29) Resolution Setting (R61H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set Display Resolution Action	0	0	0	1	1	0	0	0	0	1
	0	1	-	-	-	-	-	-	-	HRES[8]
	0	1	HRES[7:1]							-
	0	1	-	-	-	-	-	-	-	VRES[8]
	0	1	VRES[7:0]							

This command defines alternative resolution and this setting is of higher priority than the RES[1:0] in R00H (PSR).

HRES[8:1]: Horizontal Display Resolution

VRES[8:0]: Vertical Display Resolution

Channel disable calculation:

GD: First G active = G0; LAST active GD= first active +VRES [7:0] -1

SD: First active channel =S0; LAST active SD= first active +HRES [8:1]*2-1

GOOD DISPLAY

(30) Source & gate start setting(R62H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Source & gate start setting	0	0	0	1	1	0	0	0	0	1
	0	1	-	-	-	-	-	-	-	S_start[8]
	0	1	S_start[7]	S_start[6]	S_start[5]	S_start[4]	S_star[3]	S_start[2]	S_start[1]	S_start[0]
	0	1	-	-	-	gscan	-	-	-	G_start[8]
	0	1	G_start[7]	G_start[6]	G_start[5]	G_start[4]	G_start[3]	G_start[2]	G_start[1]	G_start[0]

1. S_Start [8:0]: which source output line is the first date line
2. G_Start[8:0]: which gate line is the first scan line
3. gscan: Gate scan select
   0: Normal scan
   1: Cascade type 2 scan

(31) Get status (R71H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Read Flags	0	0	0	1	1	1	0	0	0	1
	1	1	-	-	I²C_ERR	I²C_BUSY_N	Data_flag	PON	POF	BUSY_N

This command reads the IC status.
I²C_ERR: I²C master error status.
I²C_BUSY_N: I²C master BUSY_N status (low active)
Data_flag: Driver has already received all the one frame data.
PON: 0: Not in PON mode. 1: In PON mode.
POF: 0: Not in POF mode. 1: In POF mode.
BUSY_N: Driver BUSY_N status (low active)

(32) Auto Measure Vcom (AMV) (R80H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Automatically measure Vcom	0	0	1	0	0	0	0	0	0	0
	0	1	-	-	AMVT[1:0]		XON	AMVS	AMV	AMVE

This command reads the IC status.
AMVT[1:0]: Auto Measure Vcom Time
00b: 3s 01b: 5s (Default)
10b: 8s 11b: 10s
XON: All Gate ON of AMV
0: Gate normally scan during Auto Measure VCOM period. (default)
1: All Gate ON during Auto Measure VCOM period.
AMVS: Source output of AMV
0: Source output 0V during Auto Measure VCOM period. (default)
1: Source output VDHR during Auto Measure VCOM period.

GOOD DISPLAY

AMV: Analog signal

0: Get Vcom value with the VV command (R81h) (default)

1: Get Vcom value in analog signal. (External analog to digital converter)

AMVE: Auto Measure Vcom Enable (Disable)

0: Auto measure VCOM disable (default)

1: Auto measure VCOM enable

(33) Vcom Value (VV) (R81H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Automatically measure Vcom	0	0	1	0	0	0	0	0	0	1
	1	1	-	VV[6:0]						

This command gets the Vcom value.

VV[5:0]: Vcom Value Output

VV[5:0]	Vcom value
000 0000b	-0.10 V
000 0001b	-0.15 V
000 0010b	-0.20 V
:	:
100 1110b	-4.00 V

(34) VCOM-DC Setting (R82H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set VCM_DC	0	0	1	0	0	0	0	0	1	0
	0	1	-	VDCS[6:0]						

This command sets VCOM_DC value.

VDCS[5:0]: VCOM_DC Setting

VDCS[6:0]	VCOM_DC Value
000 0000b	-0.1V(default)
000 0001b	-0.15V
000 0010b	-0.2v
..	..
100 1110b	-4.0v

(35) Program Mode (PGM) (RA0H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Enter Program Mode	0	0	1	0	1	0	0	0	0	0
	0	1	1	0	1	0	0	1	0	1

After this command is issued, the chip would enter the program mode.

The mode would return to standby by hardware reset.

The only one parameter is a check code, the command would be excuted if check code = 0xA5.

GOOD DISPLAY

(36) Active Program (APG) (RA1H)

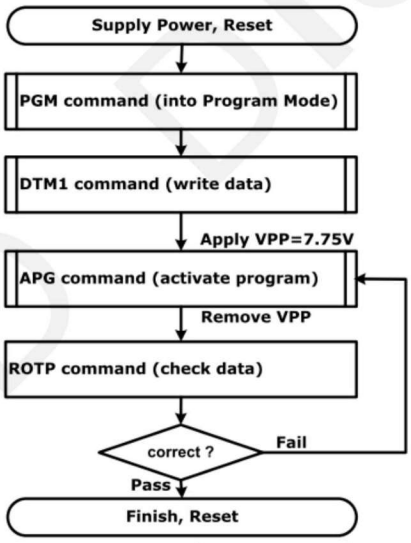
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Active Program OTP	0	0	1	0	1	0	0	0	0	1

After this command is issued, the chip would enter the program mode.

(37) Read OTP Data (ROTP) (RA2H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Read OTP data for check	0	0	1	0	1	0	0	0	1	0
	1	1	Dummy							
	1	1	The data of address 0x000 in the OTP							
	1	1	The data of address 0x001 in the OTP							
	1	1	..							
	1	1	The data of address (n-1) in the OTP							
	1	1	The data of address (n) in the OTP							

The command is used for reading the content of OTP for checking the data of programming. The value of (n) is depending on the amount of programmed data, the max address = 0xFFF.



The sequence of programming OTP

GOOD DISPLAY

6. Optical characteristics

6.1 Specifications

Measurements are made with that the illumination is under an angle of 45 degrees, the detection is perpendicular unless otherwise specified.

T=25℃

SYMBOL	PARAMETER	CONDITIONS	MIN	TYPE	MAX	UNIT	Note
R	Reflectance	White	30	35	-	%	Note 6-1
Gn	2Grey Level	-	-	DS+(WS-DS)xn(m-1)	-	L*	-
CR	Contrast Ratio	indoor	8		-	-	-
Panel's life		0℃~40℃		1000000 times			Note 6-2
Panel	Image Update	Storage and transportation		Update the white screen			
	Update Time	Operation		Suggest update once every 24 hours or at least 10 days to update again.			

WS: White state, DS: Dark state

Gray state from Dark to White：DS、WS

m: 2

Note 6-1: Luminance meter: Eye – One Pro Spectrophotometer

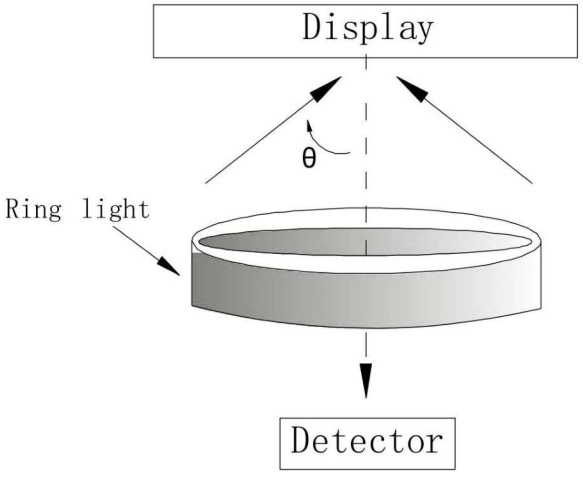
Note 6-2: Panel life will not guaranteed when work in temperature below 0 degree or above 40 degree. Each update interval time should be minimum at 180 seconds.

6.2 Definition of contrast ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (R1) and the reflectance in a dark area (Rd)() :

R1: white reflectance Rd: dark reflectance

CR = R1/Rd



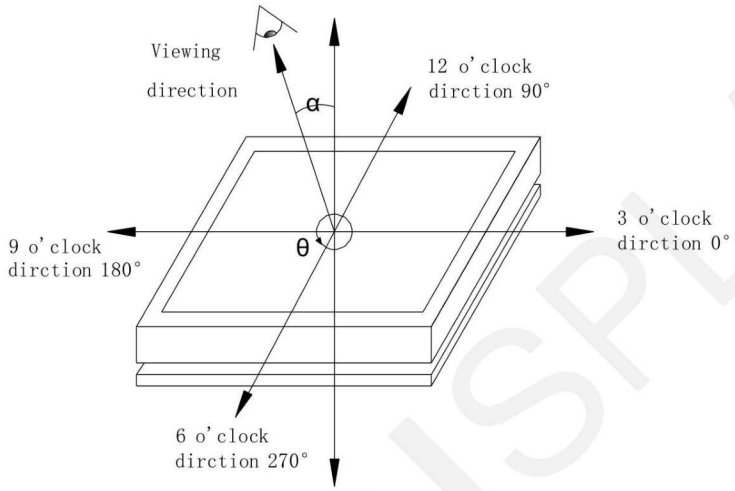
GOOD DISPLAY

6.3 Reflection Ratio

The reflection ratio is expressed as:

R = Reflectance Factor $_{\text{white board}}$ × (L_{center} / $L_{\text{white board}}$)

L_{center} is the luminance measured at center in a white area (R=G =B=1). $L_{\text{white board}}$ is the luminance of a standard white board. Both are measured with equivalent illumination source. The viewing angle shall be no more than 2 degrees.



6.4 Bi-stability

The Bi-stability standard as follows:

Bi-stability	Result		
		AVG	MAX
24 hours Luminance drift	White state △L*	-	3
	Black state △L*	-	3

GOOD DISPLAY

7. Point and line standard

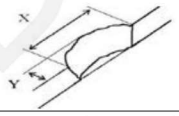
Shipment Inseption Standard

Part-A：Active area　　Part-B：Border area

Equipment：Electrical test fixture, Point gauge

Outline dimension：

70.42(H)×45.8(V) ×0.98 (D)　　Unit：mm

<table>
<tr><td rowspan="2">Environment</td><td>Temperature</td><td>Humidity</td><td>Illuminance</td><td>Distance</td><td>Time</td><td>Angle</td></tr>
<tr><td>23±2℃</td><td>55± 5%RH</td><td>1200～1500Lux</td><td>300 mm</td><td>35 Sec</td><td></td></tr>
<tr><td>Name</td><td>Causes</td><td colspan="3">Spot size</td><td>Part-A</td><td>Part-B</td></tr>
<tr><td rowspan="3">Spot</td><td rowspan="3">B/W spot in glass or protection sheet, foreign mat. Pin hole</td><td colspan="3">D ≤ 0.25mm</td><td>Ignore</td><td rowspan="3">Ignore</td></tr>
<tr><td colspan="3">0.25mm ＜ D ≤ 0.4mm</td><td>4</td></tr>
<tr><td colspan="3">0.4mm ＜ D</td><td>0</td></tr>
<tr><td rowspan="4">Scratch or line defect</td><td rowspan="4">Scratch on glass or Scratch on FPL or Particle is Protection sheet.</td><td>Length</td><td colspan="2">Width</td><td>Part-A</td><td rowspan="4">Ignore</td></tr>
<tr><td>L ≤2.0mm</td><td colspan="2">W≤0.2 mm</td><td>Ignore</td></tr>
<tr><td>2.0 mm＜L≤ 5.0mm</td><td colspan="2">0.2 mm＜W≤ 0.3mm</td><td>2</td></tr>
<tr><td>5.0 mm＜L</td><td colspan="2">0.3mm＜W</td><td>0</td></tr>
<tr><td rowspan="3">Air bubble</td><td rowspan="3">Air bubble</td><td colspan="3">D1, D2 ≤ 0.2 mm</td><td>Ignore</td><td rowspan="3">Ignore</td></tr>
<tr><td colspan="3">0.2 mm＜D1,D2 ≤ 0.35mm</td><td>4</td></tr>
<tr><td colspan="3">0.35mm＜D1, D2</td><td>0</td></tr>
<tr><td rowspan="2">Side Fragment</td><td colspan="6">  </td></tr>
<tr><td colspan="6">X≤5mm，Y≤1mm & display is ok, Ignore</td></tr>
</table>

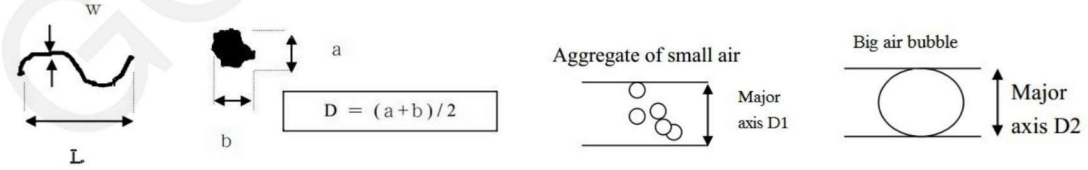
Remarks: Spot define: That only can be seen under WS or DS defects.

Any defect which is visible under gray pattern or transition process but invisible under black and white is disregarded. Here is definition of the “Spot” and “Scratch or line defect”.

Spot: W > 1/4L　　Scratch or line defect: W ≤1/4L

Definition for L/W and D (major axis)

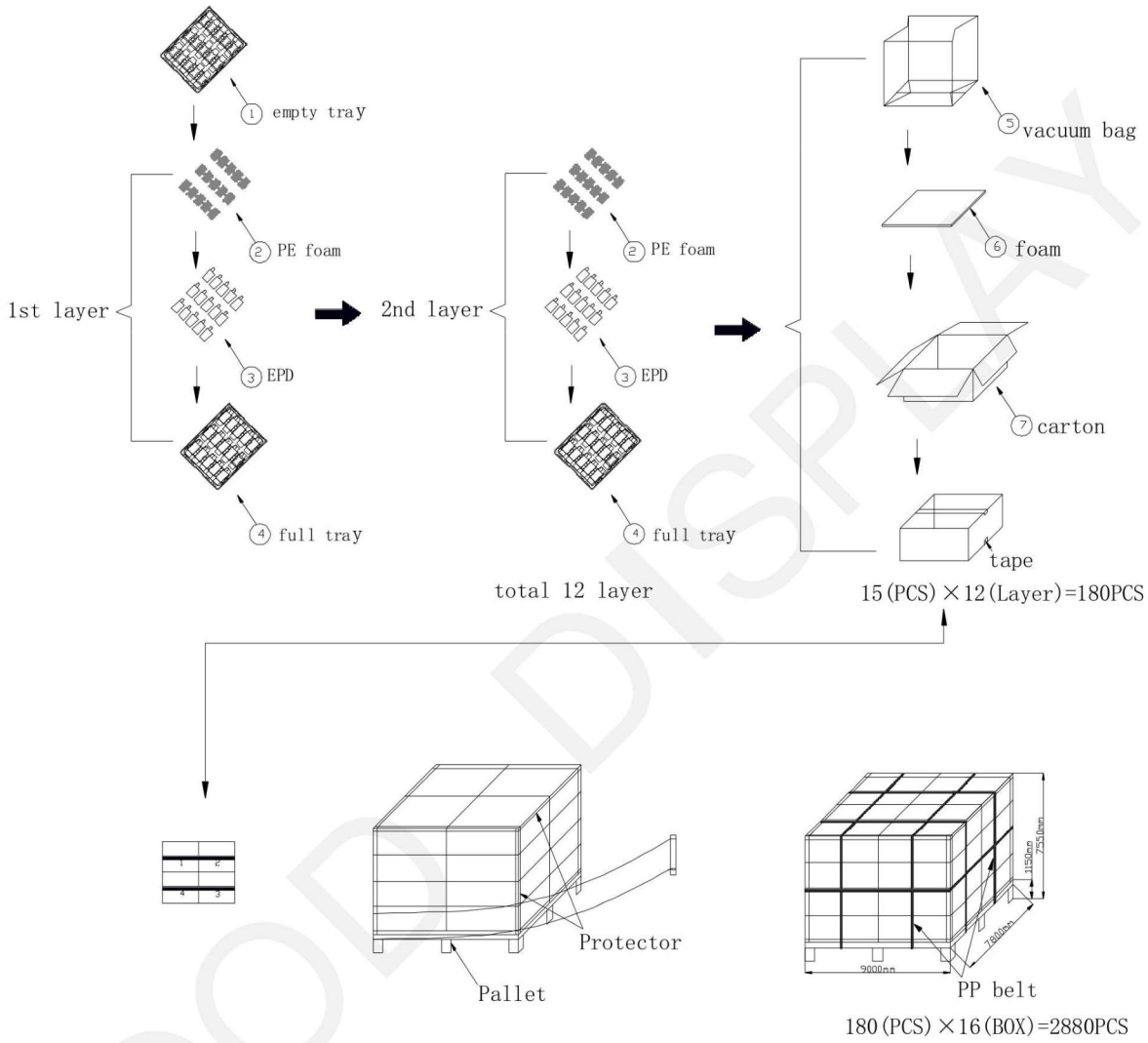
FPC bonding area pad doesn’t allowed visual inspection.



Note: AQL = 0.

GOOD DISPLAY

8. Packing



GOOD DISPLAY

9. Precautions

(1) Do not apply pressure to the EPD panel in order to prevent damaging it.

(2) Do not connect or disconnect the interface connector while the EPD panel is in operation.

(3) Do not touch IC bonding area. It may scratch TFT lead or damage IC function.

(4) Please be mindful of moisture to avoid its penetration into the EPD panel, which may cause damage during operation.

(5) If the EPD Panel / Module is not refreshed every 24 hours, a phenomena known as "Ghosting" or "Image Sticking" may occur. It is recommended to refreshed the ESL / EPD Tag every 24 hours in use case. It is recommended that customer ships or stores the ESL / EPD Tag with a completely white image to avoid this issue

(6) High temperature, high humidity, sunlight or fluorescent light may degrade the EPD panel's performance. Please do not expose the unprotected EPD panel to high temperature, high humidity, sunlight, or fluorescent for long periods of time.

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