1.54 inch
With Touch Screen
E-paper Display Series

BLGDEH0154D27-T

1. General Description

1.1 Over View

Active Matrix Electrophoretic Display(AMEPD) with capacitive touch screen , with interface and a reference system design. The 1.54'' active area contains 200×200pixels, and has 1-bit B/W full display capabilities. An integrated circuit contains gate buffer, source buffer, interface, timing control logic, oscillator, DC-DC. SRAM. LUT ,VCOM,and border are supplied with each panel.

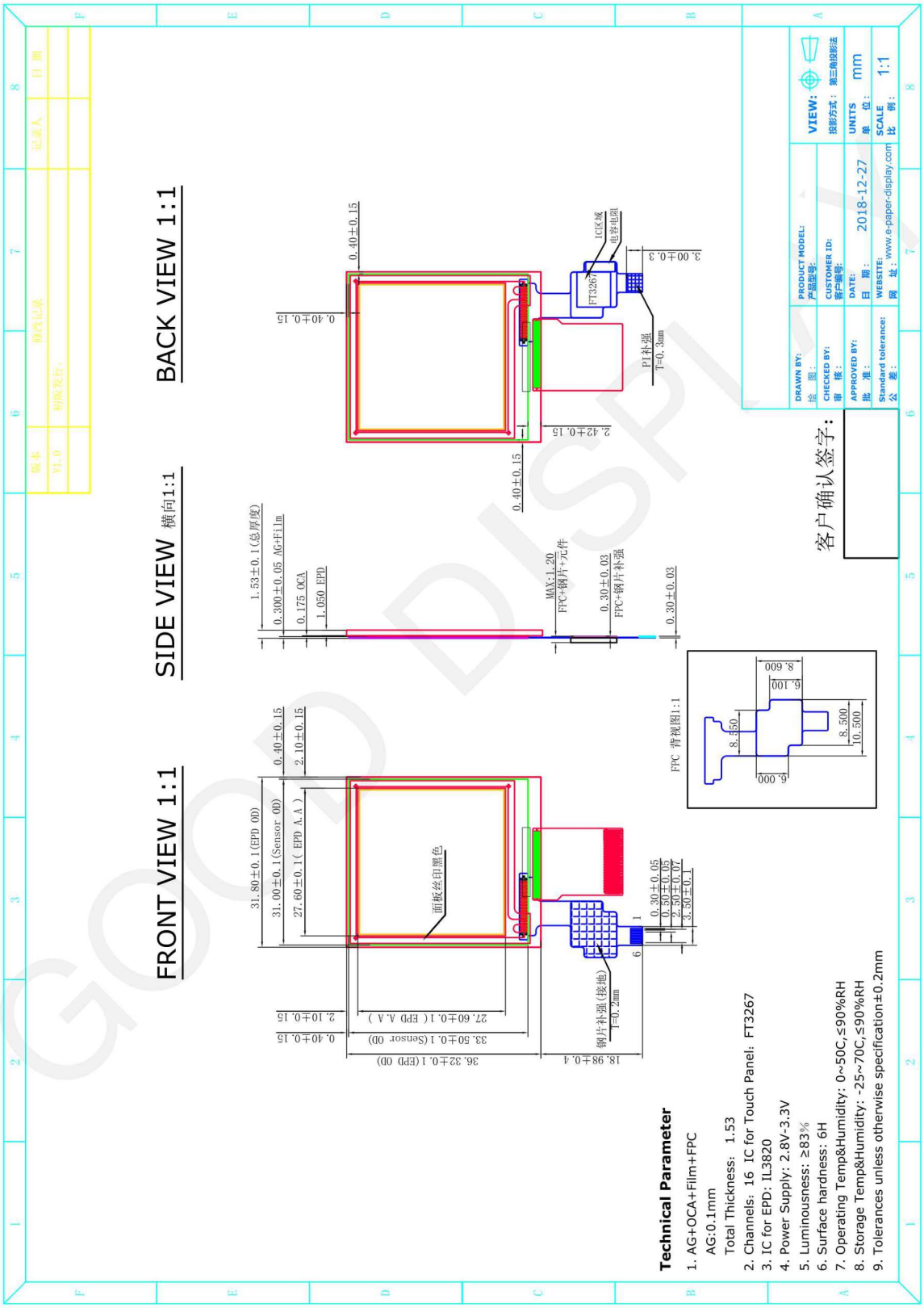
1.2 Features

- Support partial refresh
- With Capacitive Touch Screen
- 200×200 pixels display
- White reflectance above 35%
- Contrast ratio 10:1
- Ultra wide viewing angle
- Ultra low power consumption
- Pure reflective mode
- Bi-stable display Commercial temperature range
- Landscape, portrait modes
- Hard-coat antiglare display surface
- Ultra Low current deep sleep mode
- On chip display RAM
- Low voltage detect for supply voltage
- High voltage ready detect for driving voltage
- Internal temperature sensor
- 10-byte OTP space for module identification
- Waveform stored in On-chip OTP
- Serial peripheral interface available
- On-chip oscillator
- On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- I2C signal master interface to read external temperature sensor

1.3 Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	1.54	Inch	
Display Resolution	200(H)×200(V)	Pixel	dpi:183
Active Area	27.6×27.6	mm	
Pixel Pitch	0.138×0.138	mm	
Pixel Configuration	Square		
Outline Dimension	31.8(H)×36.32 (V)x1.53(D)	mm	
Weight	3±0.5	g	

1.4 Mechanical Drawing of EPD module



1.5 Input/Output Terminals

1.5-1) Pin out List

Pin #	Single	Description	Remark
1	NC	No connection and do not connect with other NC pins	Keep Open
2	GDR	N-Channel MOSFET Gate Drive Control	
3	RESE	Current Sense Input for the Control Loop	
4	VGL	Negative Gate driving voltage	
5	VGH	Positive Gate driving voltage	
6	TSCL	I2C Interface to digital temperature sensor Clock pin	
7	TSDA	I2C Interface to digital temperature sensor Date pin	
8	BS1	Bus selection pin	Note 1.5-5
9	BUSY	Busy state output pin	Note 1.5-4
10	RES #	Reset	Note 1.5-3
11	D/C #	Data /Command control pin	Note 1.5-2
12	CS #	Chip Select input pin	Note 1.5-1
13	D0	serial clock pin (SPI)	
14	D1	serial data pin (SPI)	
15	VDDIO	Power for interface logic pins	
16	VCI	Power Supply pin for the chip	
17	VSS	Ground	
18	VDD	Core logic power pin	
19	VPP	Power Supply for OTP Programming	
20	VSH	Positive Source driving voltage	
21	PREVGH	Power Supply pin for VGH and VSH	
22	VSL	Negative Source driving voltage	
23	PREVGL	Power Supply pin for VCOM, VGL and VSL	
24	VCOM	VCOM driving voltage	

Note 1.5-1: This pin (CS#) is the chip select input connecting to the MCU. The chip is enabled for MCU communication:only when CS# is pulled LOW.

Note 1.5-2: This pin (D/C#) is Data/Command control pin connecting to the MCU. When the pin is pulled HIGH,the data will be interpreted as data. When the pin is pulled LOW, the data will be interpreted as command.

Note 1.5-3: This pin (RES#) is reset signal input. The Reset is active low.

Note 1.5-4: This pin (BUSY) is Busy state output pin. When Busy is high the operation of chip should not be interrupted and any commands should not be issued to the module. The driver IC will put Busy pin high when the driver IC is working such as:

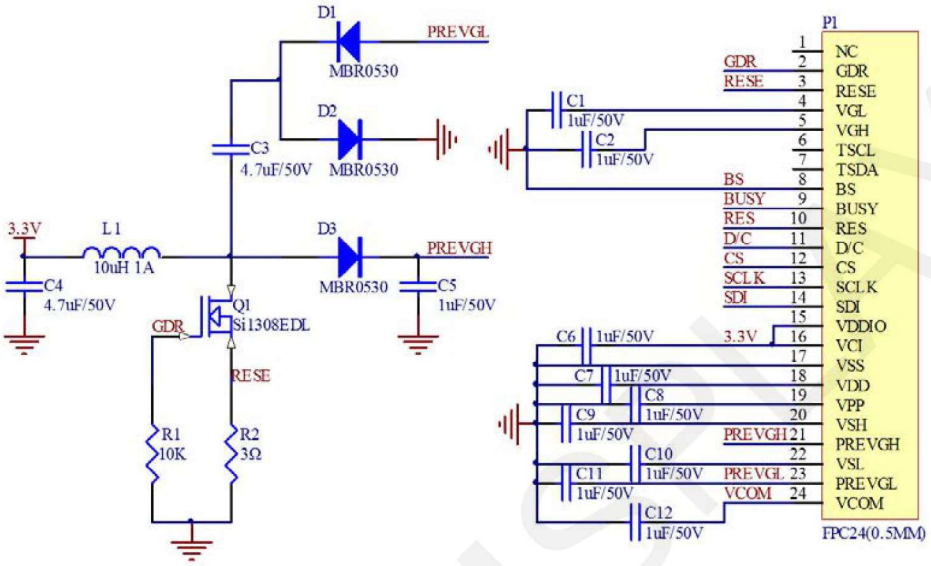
- Outputting display waveform; or
- Communicating with digital temperature sensor

Note 1.5-5: This pin (BS1) is for 3-line SPI or 4-line SPI selection. When it is "Low", 4-line SPI is selected. When it is "High", 3-line SPI (9 bits SPI) is selected. Please refer to below Table.

Table: Bus interface selection

BS1	MPU Interface
L	4-lines serial peripheral interface (SPI)
H	3-lines serial peripheral interface (SPI) - 9 bits SPI

1.6 Reference Circuit



Note :

1. Inductor L1 is wire-wound inductor. There are no special requirements for other parameters.

2. Suggests using Si1304BDL or Si1308EDL TUBE MOS (Q1) , otherwise it may affect the normal boost of the circuit.

3. The default circuit is 4-wire SPI. If the user wants to use 3-wire SPI, the resistor R4 can be removed when users design.

4. Default voltage value of all capacitors is 50V.

1.7 Touch screen technical parameters

1.7.1 Product Features

Item	Spec.
Cover lens material	FILM
Touch Panel Size	1.54inch
Sensing Area(Active area)	27.6*27.6mm(±0.10mm)
Total Thickness（T/P+EPD)	1.53±0.1mm
TP Outline Dimension	36.32*31.8mm(±0.05mm)
O.D. Fillet	/
Coverlens Thickness	/
TP sensor Area(View area)	31.0*33.5mm
ITO FILM Thickness	0.3mm

1.7.2 Electrical structure

Item	Spec.
Sensing IC	FT3267
Number of Channels	S16
Support Contact	1
Number of Touch Keys	0
Interface form	I2C
Work voltage	3.3V

1.7.3 Optical and mechanical properties

Item	Spec.
Transparency	≥83%
Haze	/
Surface hardness	2H(Apply 750G force)

1.7.4 PIN Definition

PIN No.	**Symbol**
1	SDA
2	SCL
3	VCC
4	RST
5	INT
6	GDN

2. Environmental

2.1 HANDLING, SAFETY AND ENVIROMENTAL REQUIREMENTS

WARNING
The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

CAUTION
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic
Disassembling the display module can cause permanent damage and invalidate the warranty
IPA solvent can only be applied on active area and the back of a glass. For the rest part, it is not allowed.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

Mounting Precautions	
(1) It`s recommended that you consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module.	
(2) It`s recommended that you attach a transparent protective plate to the surface in order to protect the EPD. Transparent protective plate should have sufficient strength in order to resist external force.	
(3) You should adopt radiation structure to satisfy the temperature specification.	
(4) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the PS at high temperature and the latter causes circuit break by electro-chemical reaction.	
(5) Do not touch, push or rub the exposed PS with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of PS for bare hand or greasy cloth. (Some cosmetics deteriorate the PS)	
(6) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach the PS. Do not use acetone, toluene and alcohol because they cause chemical damage to the PS.	
(7) Wipe off saliva or water drops as soon as possible. Their long time contact with PS causes deformations and color fading.	
Product specification	The data sheet contains final product specifications.

Limiting values
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.
Application information
Where application information is given, it is advisory and dose not form part of the specification.

Product Environmental certification
ROHS

REMARK
All The specifications listed in this document are guaranteed for module only. Post-assembled operation or component(s) may impact module performance or cause unexpected effect or damage and therefore listed specifications is not warranted after any Post-assembled operation.

2.2 Reliability test

	TEST	CONDITION	METHOD	REMARK
1	High-Temperature Operation	：，RH=30%RH，For 240Hr	IEC 60 068-2-2Bb	
2	Low-Temperature Operation	T = 0℃ for 240 hrs	IEC 60 068-2-2Ab	
3	High-Temperature Storage	T=70℃RH=40%RH For 240Hr Test in white pattern	IEC 60 068-2-2Bb	
4	Low-Temperature Storage	T = -25℃ for 240 hrs Test in white pattern	IEC 60 068-2-2Ab	
5	High Temperature, High-Humidity Operation	T = 40℃, RH=90%RH，For 168Hr	IEC 60 068-2-3CA	
6	High Temperature, High-Humidity Storage	T=60℃，RH=80%RH，For 480Hr Test in white pattern	IEC 60 068-2-3CA	
7	Temperature Cycle	-25℃(30min)~70℃ (30min), 50 Cycle Test in white pattern	IEC 60 068-2-14NB	
8	Package Vibration	1.04G,Frequency : 10~500Hz Direction : X,Y,Z Duration: 1hours in each direction	Full packed for shipment	
9	Package Drop Impact	Drop from height of 122 cm on Concrete surface Drop sequence: 1 corner, 3edges, 6face One drop for each.	Full packed for shipment	
10	UV exposure Resistance	765 W/㎡ for 168hrs,40℃	IEC 60068-2-5 Sa	
11	Electrostatic discharge	Machine model: +/-250V,0Ω,200pF	IEC61000-4-2	

Actual EMC level to be measured on customer application.

Note1: The protective film must be removed before temperature test.

Note2：Stay white pattern for storage and non-operation test.

3. Electrical Characteristics

3.1 Maximum Ratings

Table 3.1-1: Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{CI}	Logic supply voltage	-0.5 to +4.0	V
T_{OPR}	Operation temperature range	0~50	°C
T_{STG}	Storage temperature range	-25~60	°C
-	Humidity range	40~70	%RH

*** Note: Avoid direct sunlight.**

3.2 DC Characteristics

The following specifications apply for: VSS=0V, VCI=3.3V, TOPR=25℃.

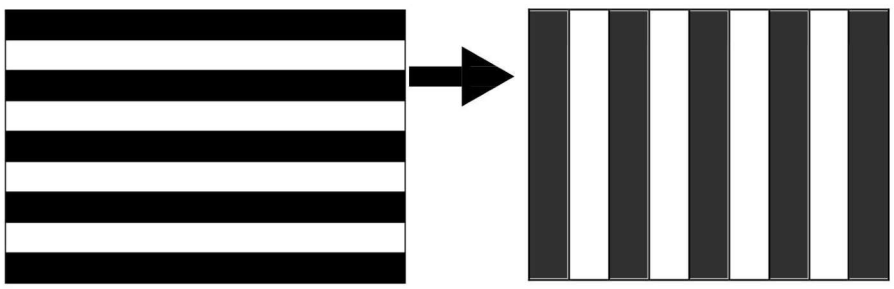
Table 3.2-1: DC Characteristics

Symbol	Parameter	Test Condition	Applicable pin	Min.	Typ.	Max.	Unit
VCI	VCI operation voltage	-	VCI	2.4	3.3	3.7	V
VIH	High level input voltage	-	D1 (SDIN), D0 (SCLK), CS#, D/C#, RES#, BS1,	0.8VDDIO	-	-	V
VIL	Low level input voltage	-		-	-	0.2VDDIO	V
VOH	High level output voltage	IOH = -100uA	BUSY, TSDA, TSCL	0.9VDDIO	-	-	V
VOL	Low level output voltage	IOL = 100uA		-	-	0.1VDDIO	V
Iupdate	Module operating current	-	-	-	4	-	mA
Isleep	Deep sleep mode	VCI=3.3V	-	-	0.6	1	uA

- The Typical power consumption is measured using associated 25℃ waveform with following pattern transition: from horizontal scan pattern to vertical scan pattern. (Note 3.2-1)
- The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by Good Display.
- Vcom value will be provided by Good Display.

Note 3.2-1

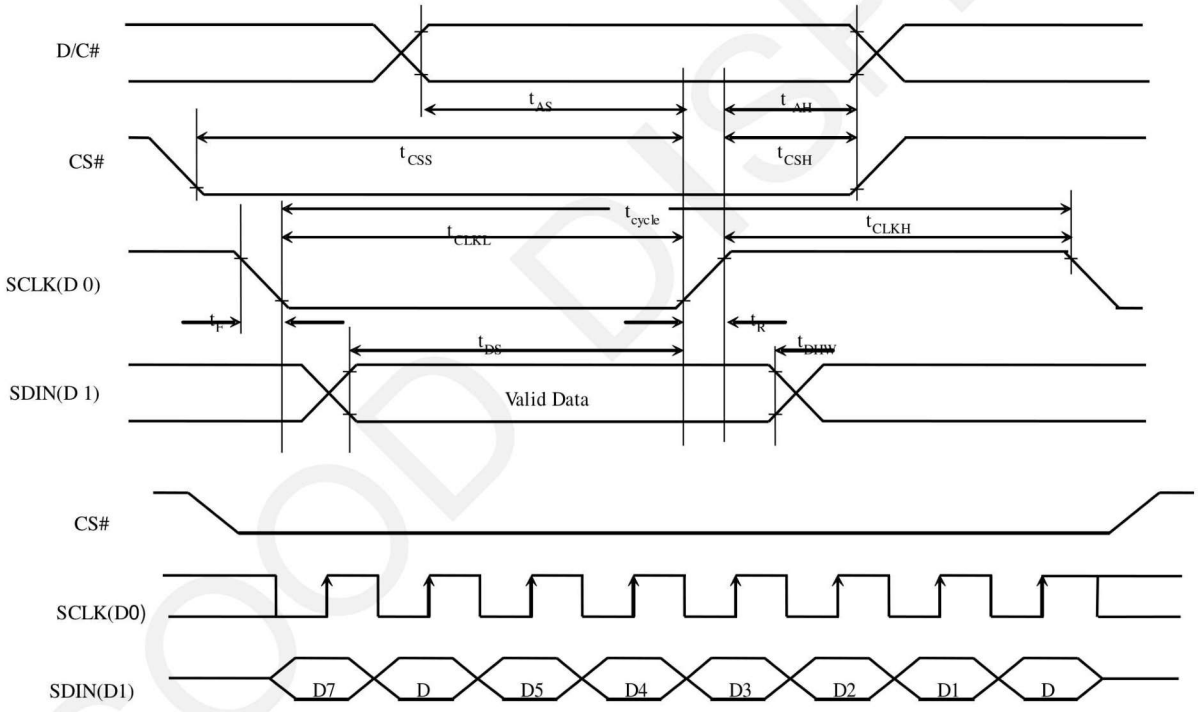
The Typical power consumption



3.3 Serial Peripheral Interface Timing

The following specifications apply for: VSS=0V, VCI=2.4V to 3.7V, TOPR=25℃

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	250	-	-	ns
t_{AS}	Address Setup Time	150	-	-	ns
t_{AH}	Address Hold Time	150	-	-	ns
t_{CSS}	Chip Select Setup Time	120	-	-	ns
t_{CSH}	Chip Select Hold Time	60	-	-	ns
t_{DSW}	Write Data Setup Time	50	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	100	-	-	ns
t_{CLKH}	Clock High Time	100	-	-	ns
t_R	Rise Time [20% ~ 80%]	-	-	15	ns
t_F	Fall Time [20% ~ 80%]	-	-	15	ns



3.4 Power Consumption

Parameter	Symbol	Condition	TYP	Max	Unit	Remark
Panel power consumption during update	-	25℃	23	-	mAs	-
Deep sleep mode	-	25℃	0.6	-	uA	-

3.5 MCU Interface

3.5-1) MCU Serial Peripheral Interface (4-wire SPI)

The 4-wire SPI consists of SCLK (serial clock), SDIN (serial data), D/C# and CS#. D0 acts as SCLK and D1 acts as SDIN.

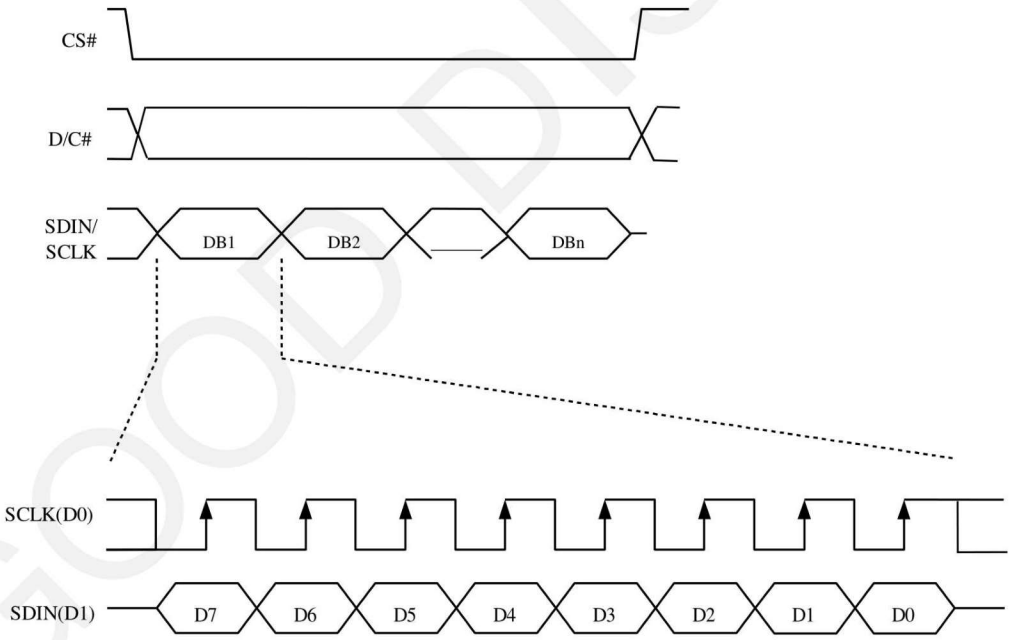
Table 3.5-1 : Control pins of 4-wire Serial Peripheral interface

Function	CS# pin	D/C# pin	SCLK pin
Write command	L	L	↑
Write data	L	H	↑

Note: ↑ stands for rising edge of signal

SDIN is shifted into an 8-bit shift register in the order of D7, D6, ... D0. The data byte in the shift register is written to the Graphic Display Data RAM (RAM) or command register in the same clock. Under serial mode, only write operations are allowed.

Figure 3.5-1 : Write procedure in 4-wire Serial Peripheral Interface mode



3.5-2) MCU Serial Peripheral Interface (3-wire SPI)

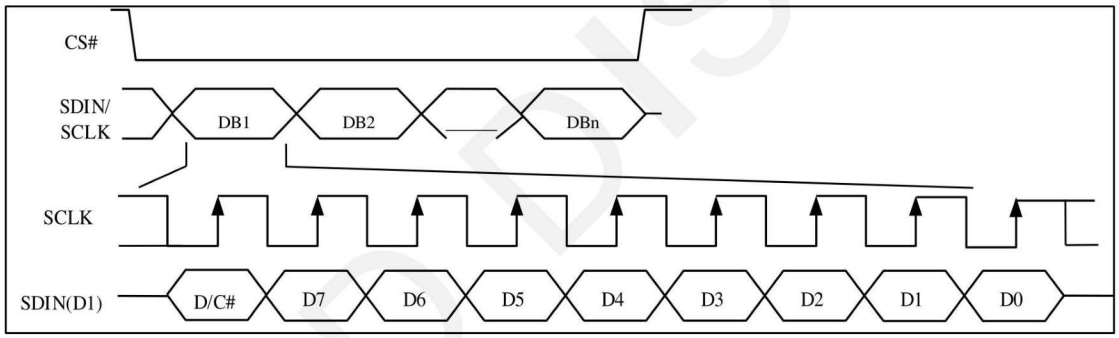
The 3-wire serial interface consists of SCLK (serial clock), SDIN (serial data) and CS#. In SPI mode, D0 acts as SCLK and D1 acts as SDIN. The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits will be shifted into the shift register in sequence: D/C# bit, D7 to D0 bit. The D/C# bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (D/C# bit = 1) or the command register (D/C# bit = 0). Under serial mode, only write operations are allowed.

Table 3.5-2 : Control pins of 3-wire Serial Peripheral interface

Function	CS# pin	D/C# pin	SCLK pin
Write command	L	Tie LOW	↑
Write data	L	Tie LOW	↑

Note: ↑ stands for rising edge of signal

Figure 3.5-1 : Write procedure in 3-wire Serial Peripheral Interface mode



3.6 External Temperature Sensor operation

There are two ways to let the module get the ambient temperature,

1) use the external temperature sensor interface, The module provides two I/O lines [TSDA and TSCL] for connecting digital temperature sensor for temperature reading sensing. TSDA will be treated as SDA line and TSCL will be treated as SCL line. They are required connecting with the external pull-up resistors when they are used to connect to the temperature sensor, then the module will check the temperature automatically.

2) use any kinds of external temperature sensor to get the temperature value then converted to hex format, then use the spi interface send command 0x1A and the temperature value into the module. The temperature value how to converted to hex as the follow:

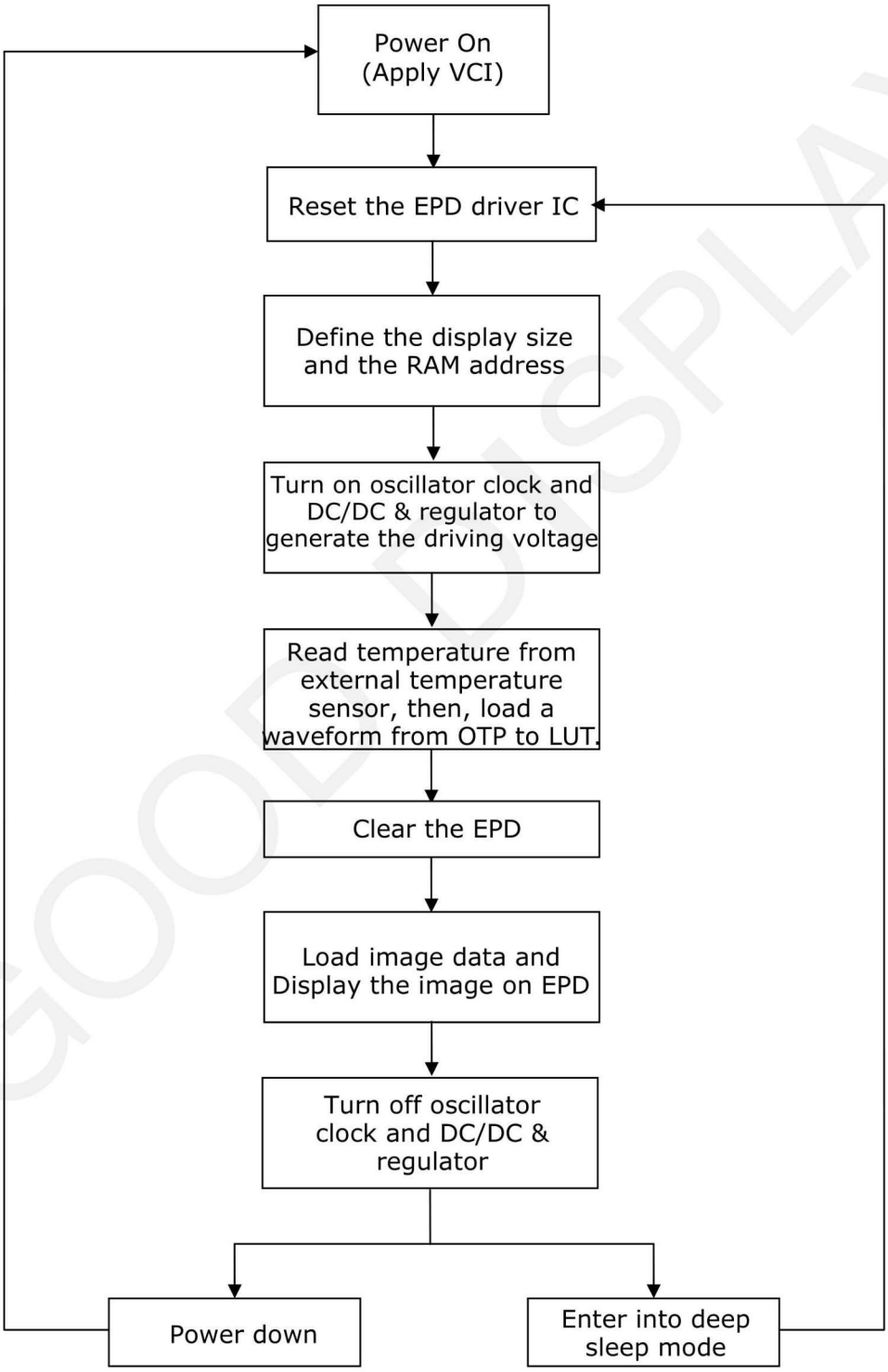
   1. When the Temperature value MSByte bit D11 = 0, the temperature is positive and value (DegC) = + (Temperature value)/16

   2. When the Temperature value MSByte bit D11 = 1, the temperature is negative and value (DegC) = ~ (2's complement of Temperature value)/16

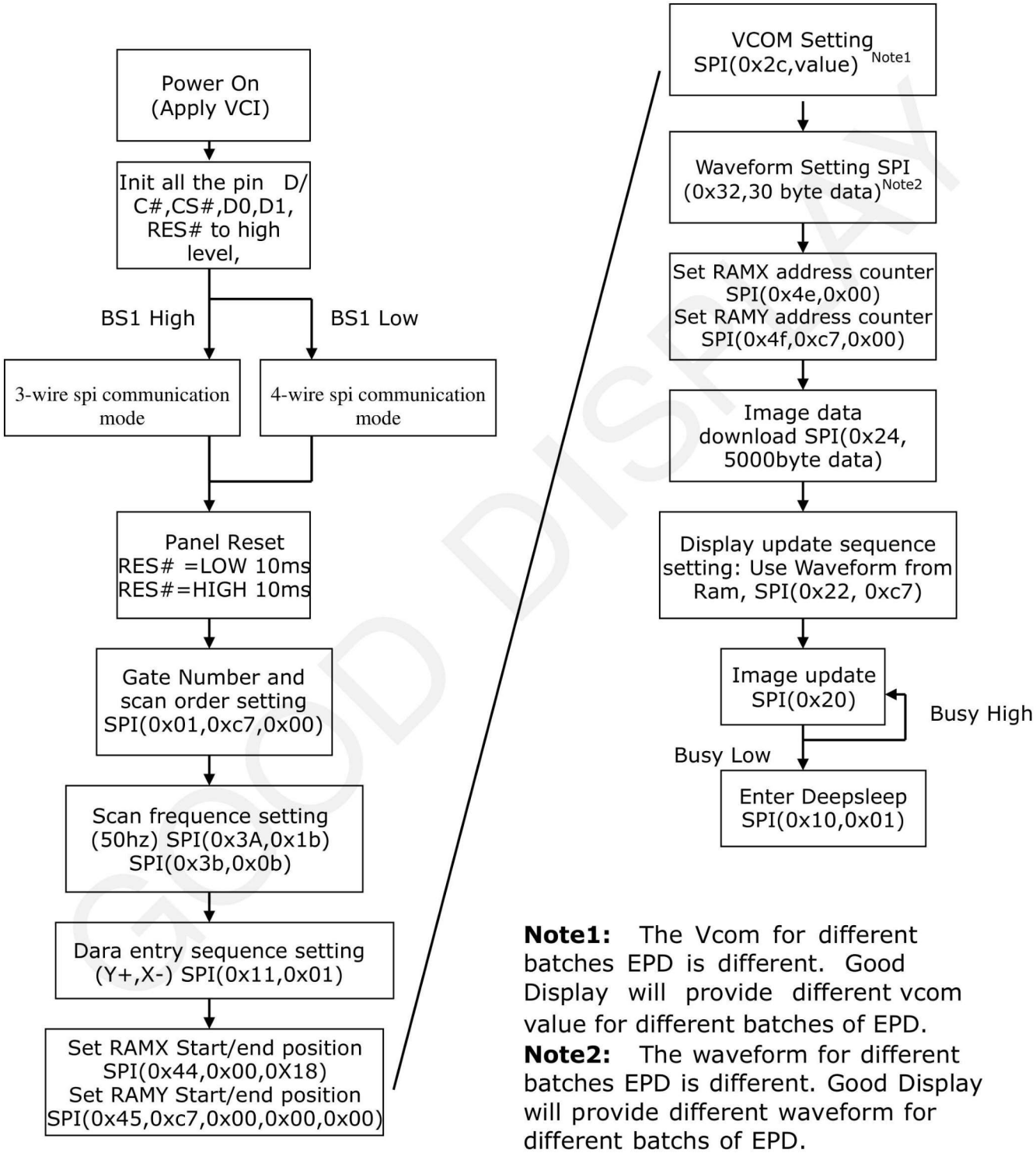
12-bit binary (2's complement)	Hexadecimal Value	Decimal Value	Value [DegC]
0111 1111 0000	7F0	2032	127
0111 1110 1110	7EE	2030	126.875
0111 1110 0010	7E2	2018	126.125
0111 1101 0000	7D0	2000	125
0001 1001 0000	190	400	25
0000 0000 0010	002	2	0.125
0000 0000 0000	000	0	0
1111 1111 1110	FFE	-2	-0.125
1110 0111 0000	E70	-400	-25
1100 1001 0010	C92	-878	-54.875
1100 1001 0000	C90	-880	-55

4. Typical Operating Sequence

4.1 Normal Operation Flow



4.2 Reference Program Code



Note1: The Vcom for different batches EPD is different. Good Display will provide different vcom value for different batches of EPD.

Note2: The waveform for different batches EPD is different. Good Display will provide different waveform for different batchs of EPD.

5. Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	01	0	0	0	0	0	0	0	1	Driver Output control	Set the number of gate. Setting for 152 gates is: Set A[8:0] = 0C7h Set B[2:0] = 00h
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	1		0	0	0	0	0	0	0	A8		
0	1		0	0	0	0	0	B2	B1	B0		
0	0	0C	0	0	0	0	1	1	0	0	Booster Soft start Control	Set A[7:0]=CFh[POR] Set B[7:0]=CEh[POR] Set C[7:0]= 8Dh[POR]
0	1		1	A6	A5	A4	A3	A2	A1	A0		
0	1		1	B6	B5	B4	B3	B2	B1	B0		
0	1		1	C6	C5	C4	C3	C2	C1	C0		
0	0	10	0	0	0	1	0	0	0	0	Deep Sleep mode	Deep Sleep mode Control
0	1		0	0	0	0	0	0	0	A0		A[0] : Description 0 Normal Mode [POR] 1 Enter Deep Sleep Mode
0	0	11	0	0	0	1	0	0	0	1	Data Entry mode setting	Define data entry sequence A [1:0]=ID[1:0] Address automatic increment / decrement setting The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address. 00 –Y decrement, X decrement, 01 –Y decrement, X increment, 10 –Y increment, X decrement, 11 –Y increment, X increment [POR] A[2] = AM Set the direction in which the address counter is updated automatically after data are written to the RAM. AM= 0, the address counter is updated in the X direction. [POR] AM = 1, the address counter is updated in the Y direction.
0	1		0	0	0	0	0	A2	A1	A0		
0	0	12	0	0	0	1	0	0	1	0	SWRESET	It resets the commands and parameters to their S/W Reset default values except R10h-Deep Sleep Mode Note: RAM are unaffected by this command.

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	1A	0	0	0	1	1	0	1	0	Temperature Sensor Control (Write to temperature register)	Write to temperature register. A[7:0] – MSByte 01111111[POR] B[7:0] – LSByte 11110000[POR]
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	1		B7	B6	B5	B4	0	0	0	0		
0	0	20	0	0	1	0	0	0	0	0	Master Activation	Activate Display Update Sequence The Display Update Sequence Option is located at R22h User should not interrupt this operation to avoid corruption of panel images.
0	0	21	0	0	1	0	0	0	0	1	Display Update Control 1	Option for Display Update Bypass Option used for Pattern Display, which is used for display the RAM content into the Display OLD RAM Bypass option A [7] A[7] = 1: Enable bypass A[7] = 0: Disable bypass [POR] A[4] value will be used as for bypass. A[4] = 0 [POR] A[1:0] Initial Update Option – Source Control
0	1		A7	0	0	A4	A3	A2	A1	A0		

A[1:0]	GSC	GSD
01 [POR]	GS0	GS1

<table>
<tr><th>R/W#</th><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>22</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td rowspan="2">Display Update Control 2</td><td colspan="2">Display Update Sequence Option:
Enable the stage for Master Activation</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_5</td><td>A_4</td><td>A_3</td><td>A_2</td><td>A_1</td><td>A_0</td><td colspan="2"><table>
<tr><td></td><td>Paramete (in Hex)</td></tr>
<tr><td>Enable Clock Signal, Then Enable CP
Then Load Temperature value
Then Load LUT
Then INIITIAL DISPLAY
Then PATTERN DISPLAY
Then Disable CP Then Disable OSC</td><td>FF [POR]</td></tr>
<tr><td>To Enable Clock Signal (CLKEN=1)</td><td>80</td></tr>
<tr><td>To Enable Clock Signal, then Enable CP (CLKEN=1, CPEN=1)</td><td>C0</td></tr>
<tr><td>To INITIAL DISPLAY + PATTEN DISPLAY</td><td>0C</td></tr>
<tr><td>To INITIAL DISPLAY</td><td>08</td></tr>
<tr><td>To DISPLAY PATTEN</td><td>04</td></tr>
<tr><td>To Disable CP,
then Disable Clock Signal (CLKEN=1, CPEN=1)</td><td>03</td></tr>
<tr><td>To Disable Clock Signal (CLKEN=1)</td><td>01</td></tr>
<tr><td colspan="2">Remark:
CLKEN=1:
If CLS=VDDIO then Enable OSC If CLS=VSS then Enable External Clock
CLKEN=0:
If CLS=VDDIO then Disable OSC
AND
INTERNAL CLOCK Signal = VSS,</td></tr>
</table></td></tr>
<tr><td>0</td><td>0</td><td>24</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>Write RAM</td><td colspan="2">After this command, data entries will be written into the RAM until another command is written. Address pointers will advance accordingly.</td></tr>
<tr><td>0</td><td>0</td><td>2C</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td rowspan="2">Write VCOM register</td><td colspan="2" rowspan="2">Write VCOM register from MCU interface</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
</table>

<table>
<tr><th>R/W#</th><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>32</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td rowspan="2">Write LUT register</td><td rowspan="2">Write LUT register from MCU [240 bits],
(excluding the VSH/VSL and Dummy bit)</td></tr>
<tr><td>0
0
0
...
0
0</td><td>1
1
1
...
1
1</td><td></td><td colspan="8">LUT
[30 bytes]</td></tr>
<tr><td>0</td><td>0</td><td>3A</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td rowspan="2">Set dummy line period</td><td rowspan="2">Set A[7:0] = 1Bh</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
<tr><td>0</td><td>0</td><td>3B</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td rowspan="2">Set Gate line width</td><td>Set B[3:0] = Bh</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td><td></td></tr>
<tr><td>0</td><td>0</td><td>3C</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td rowspan="2">Border Waveform Control</td><td rowspan="2">Select border waveform for VBD
A [7] Follow Source at Initial Update Display
A [7]=0: [POR]
A [7]=1: Follow Source at Initial Update Display for VBD, A [6:0] setting are being overridden at Initial Display STAGE.

A [6] Select GS Transition/ Fix Level for VBD
A [6]=0: Select GS Transition A[3:0] for VBD
A [6]=1: Select FIX level Setting A[5:4] for VBD [POR]
A [5:4] Fix Level Setting for VBD

<table><tr><td>A[5:4]</td><td>VBD level</td></tr><tr><td>00</td><td>VSS</td></tr><tr><td>01</td><td>VSH</td></tr><tr><td>10</td><td>VSL</td></tr><tr><td>11[POR]</td><td>HiZ</td></tr></table>A [1:0] GS transition setting for VBD (Select waveform like data A[3:2] to data A[1:0])

<table><tr><td>A[1:0]</td><td>GSA</td><td>GSB</td></tr><tr><td>01 [POR]</td><td>GS0</td><td>GS1</td></tr></table></td></tr>
<tr><td>0</td><td>1</td><td></td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>0</td><td>0</td><td>A1</td><td>A0</td></tr>
</table>

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	44	0	1	0	0	0	1	0	0	Set RAM X - address Start / End position	Specify the start/end positions of the window address in the X direction by an address unit A[4:0] = 00h B[4:0] = 18h
0	1		0	0	0	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	0	B_4	B_3	B_2	B_1	B_0		
0	0	45	0	1	0	0	0	1	0	1	Set Ram Y- address Start / End position	Specify the start/end positions of the window address in the Y direction by an address unit A[8:0] = 0C7h B[8:0] = 0000h
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	0	0	0	0	0	A_8		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		0	0	0	0	0	0	0	B_8		
0	0	4E	0	1	0	0	1	1	1	0	Set RAM X address counter	Make initial settings for the RAM X address in the address counter (AC) A[4:0] = 00h
0	1		0	0	0	A_4	A_3	A_2	A_1	A_0		
0	0	4F	0	1	0	0	1	1	1	1	Set RAM Y address counter	Make initial settings for the RAM Y address in the address counter (AC) A[8:0] = 0C7h
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	0	0	0	0	0	A_8		
0	1	FF	1	1	1	1	1	1	1	1	NOP	This command is an empty command; it does not have any effect on the display module. However it can be used to terminate Frame Memory Write or Read Commands.

6. Optical characteristics

6.1 Specifications

Measurements are made with that the illumination is under an angle of 45 degrees, the detection is perpendicular unless otherwise specified.

T=25℃

SYMBOL	PARAMETER	CONDITIONS	MIN	TYPE	MAX	UNIT	Note
R	Reflectance	White	30	35	-	%	Note 6-1
Gn	2Grey Level	-	-	DS+(WS-DS)×n(m-1)	-	L*	-
CR	Contrast Ratio	indoor	-	10	-	-	-
Panel's life	-	0℃～50℃		5years or 1000000 times	-	-	Note 6-2

WS: White state, DS：Dark state

m: 2

Note 6-1: Luminance meter：Eye - One Pro Spectrophotometer

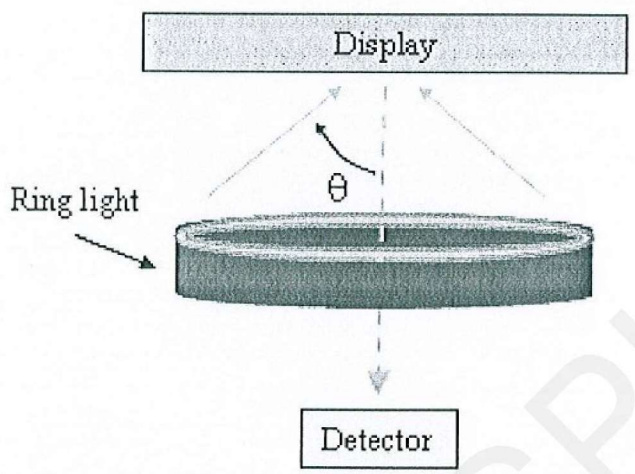
Note 6-2: We guarantee display quality from 10℃～30℃generally, If operation ambient temperature from 0℃～50℃，will add external temperature sensor.

6.2 Definition of contrast ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (R1) and the reflectance in a dark area (Rd)() :

R1: white reflectance Rd: dark reflectance

CR = R1/Rd

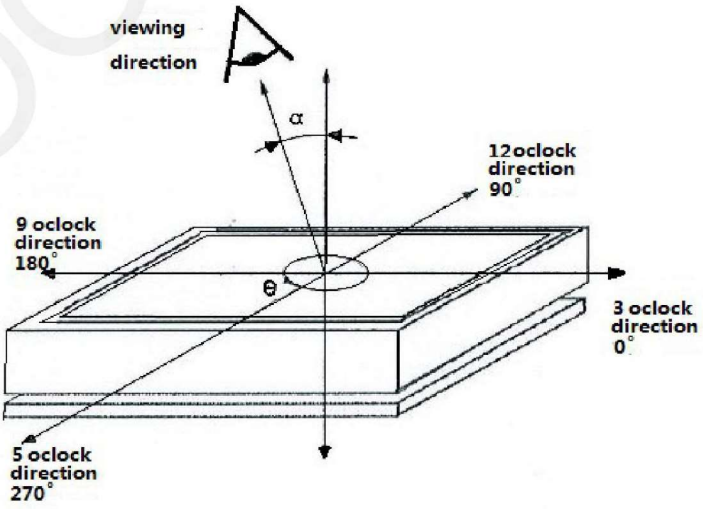


6.3 Reflection Ratio

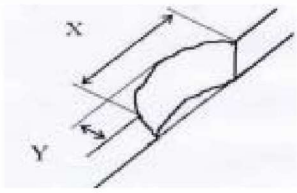
The reflection ratio is expressed as :

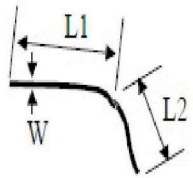
R = Reflectance Factor white board x (L center / L white board)

L center is the luminance measured at center in a white area (R=G =B=1) . L white board is the luminance of a standard white board . Both are measured with equivalent illumination source . The viewing angle shall be no more than 2 degrees.



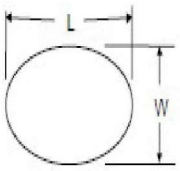
7. Point and line standard

<table>
<tr><th colspan="7">Shipment Inspection Standard</th></tr>
<tr><td colspan="7">Equipment：Electrical test fixture, Point gauge</td></tr>
<tr><td>Outline dimension</td><td>36.32(H)×31.8(V)×1.05(D)</td><td>Unit：㎜</td><td>Part-A</td><td>Active area</td><td>Part-B</td><td>Border area</td></tr>
<tr><td rowspan="2">Environment</td><td>Temperature</td><td>Humidity</td><td>Illuminance</td><td>Distance</td><td>Time</td><td>Angle</td></tr>
<tr><td>19℃～25℃</td><td>55%±5%RH</td><td>800～1300Lux</td><td>300 ㎜</td><td>35Sec</td><td></td></tr>
<tr><td>Defet type</td><td>Inspection method</td><td colspan="2">Standard</td><td colspan="2">Part-A</td><td>Part-B</td></tr>
<tr><td rowspan="3">Spot</td><td rowspan="3">Electric Display</td><td colspan="2">D≤0.25 ㎜</td><td colspan="2">Ignore</td><td>Ignore</td></tr>
<tr><td colspan="2">0.25 ㎜＜D≤0.4 ㎜</td><td colspan="2">N≤4</td><td>Ignore</td></tr>
<tr><td colspan="2">D＞0.4 ㎜</td><td colspan="2">Not Allow</td><td>Ignore</td></tr>
<tr><td>Display unwork</td><td>Electric Display</td><td colspan="2">Not Allow</td><td colspan="2">Not Allow</td><td>Ignore</td></tr>
<tr><td>Display error</td><td>Electric Display</td><td colspan="2">Not Allow</td><td colspan="2">Not Allow</td><td>Ignore</td></tr>
<tr><td rowspan="3">Scratch or line defect(include dirt)</td><td rowspan="3">Visual/Film card</td><td colspan="2">L≤2 ㎜，W≤0.2 ㎜</td><td colspan="2">Ignore</td><td>Ignore</td></tr>
<tr><td colspan="2">2.0mm＜L≤5.0mm，0.2＜W≤0.3mm,</td><td colspan="2">N≤2</td><td>Ignore</td></tr>
<tr><td colspan="2">L＞5 ㎜，W＞0.3 ㎜</td><td colspan="2">Not Allow</td><td>Ignore</td></tr>
<tr><td rowspan="3">PS Bubble</td><td rowspan="3">Visual/Film card</td><td colspan="2">D≤0.2mm</td><td colspan="2">Ignore</td><td>Ignore</td></tr>
<tr><td colspan="2">0.2mm≤D≤0.35mm & N≤4</td><td colspan="2">N≤4</td><td>Ignore</td></tr>
<tr><td colspan="2">D＞0.35 mm</td><td colspan="2">Not Allow</td><td>Ignore</td></tr>
<tr><td rowspan="2">Side Fragment</td><td rowspan="2">Visual/Film card</td><td colspan="5">X≤5mm，Y≤0.5mm, Do not affect the electrode circuit, Ignore</td></tr>
<tr><td colspan="5"> 
</td></tr>
<tr><td rowspan="3">Remark</td><td colspan="6">1.Cannot be defect & failure cause by appearance defect;</td></tr>
<tr><td colspan="6">2.Cannot be larger size cause by appearance defect;</td></tr>
<tr><td colspan="6">L=long W=wide D=point size N=Defects NO</td></tr>
</table>



L = L1 + L2

Line Defect

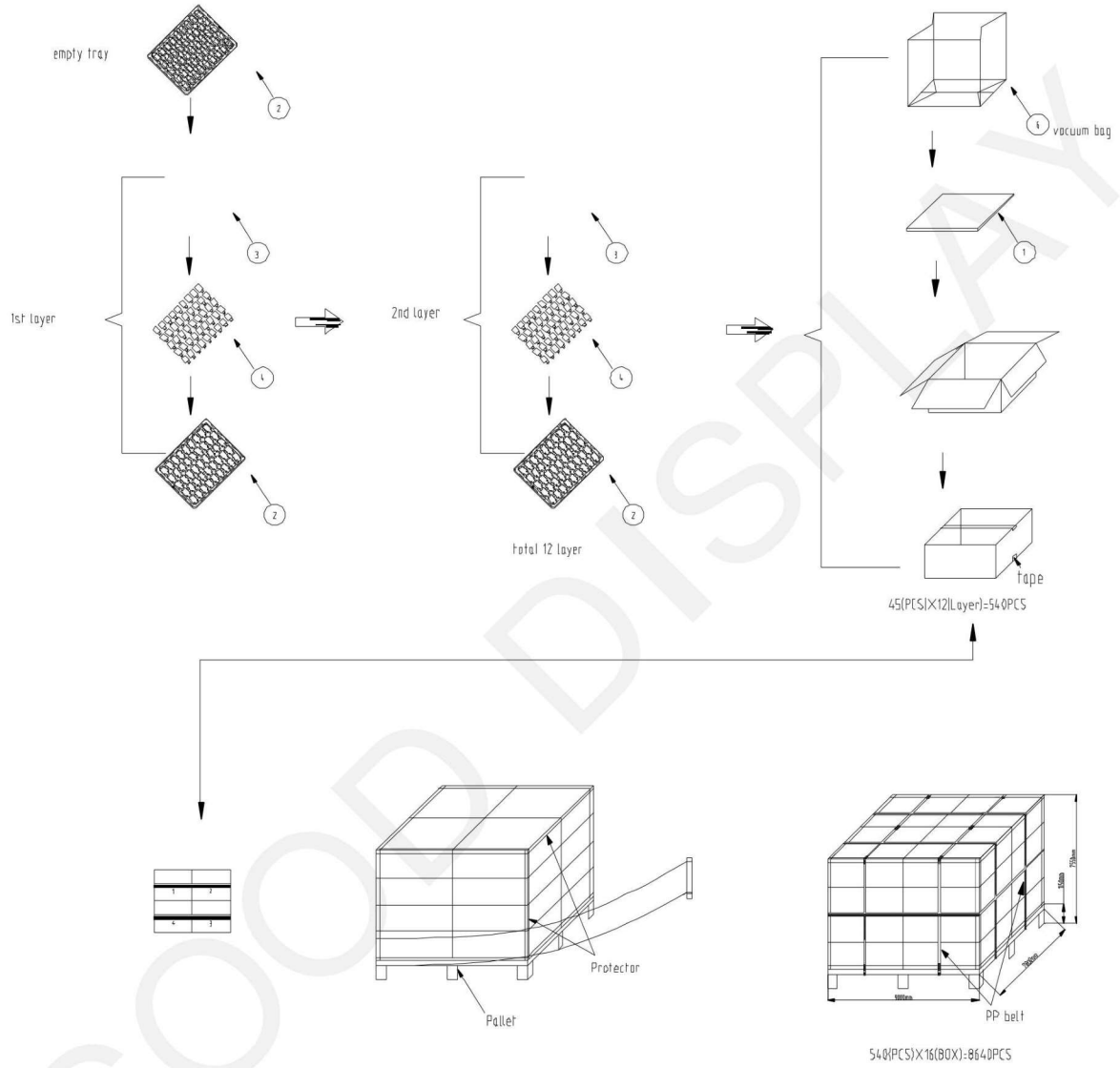


D = (L + W) / 2

Spot Defect

L=long W=wide D=point size

8. Packing



9. Precautions

(1) Do not apply pressure to the EPD panel in order to prevent damaging it.

(2) Do not connect or disconnect the interface connector while the EPD panel is in operation.

(3) Do not touch IC bonding area. It may scratch TFT lead or damage IC function.

(4) Please be mindful of moisture to avoid its penetration into the EPD panel, which may cause damage during operation.

(5) If the EPD Panel / Module is not refreshed every 24 hours, a phenomena known as "Ghosting" or "Image Sticking" may occur. It is recommended to refreshed the ESL / EPD Tag every 24 hours in use case. It is recommended that customer ships or stores the ESL / EPD Tag with a completely white image to avoid this issue

(6) High temperature, high humidity, sunlight or fluorescent light may degrade the EPD panel's performance. Please do not expose the unprotected EPD panel to high temperature, high humidity, sunlight, or fluorescent for long periods of time.