2.13 inch
E-paper Display Series

BLGDTH0213ZHFT34

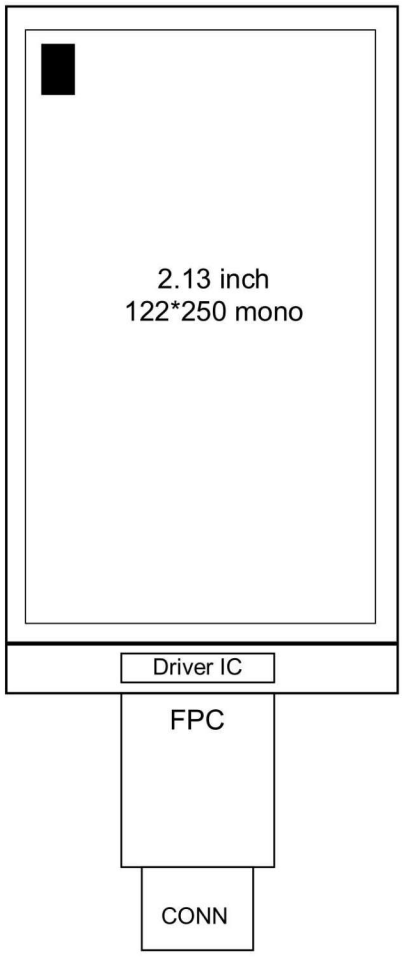
1. General Specifications

Feature		Spec
Display Spec.	Size	2.13inch
	Resolution	250G*122G
	Interface	4-wire SPI
	Color Depth	2 Black and White
	Technology Type	ECB
	Pixel Pitch (mm)	195um*194um
	Pixel Configuration	Mono
	Display Mode	Reflective, Normally black
	Surface Treatment(Up Polarizer)	
Mechanical Characteristics	LCM (W x H x D) (mm)	26.71*55.75*0.55
	Active Area(mm)	23.79*48.50
	With/Without TSP	NA
	Weight (g)	2±0.5
	LED Numbers	None
Electronic	Driver IC	ST7302

Note 1: Requirements on Environmental Protection: Q/S0002

Note 2: LCM weight tolerance : +/- 5%

2. BLOCK DIAGRAM



3. INPUT/OUTPUT TERMINALS PIN ASSIGNMENT

3.1 CN1 of FPC

No	Symbol	I/O	Description	Comment
1	VSS	P	ground power	
2	VDDI	P	Power Supply (Digital)	
3	CSB	I	Chip select input pin.	
4	A0	I	It determines whether the access is related to data or command	
5	RSTB	I	Reset input pin.	
6	SCL	I	serial input clock	
7	SDA	I/O	serial input/output data	
8	TE	O	Tearing effect signal	
9	VDDA	P	Power Supply (Analog)	
10	VCOM	O	COM outputs	
11	VCCIO	O	the power source of digital circuits.	
12	VMREF	O	Monitor pin for internal regulator.	
13	VCOMH	O	Positive voltage output of VCOM	
14	VSL	O	Power output pin for source driver.	
15	VSH	O	Power output pin for source driver.	
16	VSS	P	ground power	
17	VGL	O	Power output (Negative) pin for gate driver.	
18	CD2P	O	Capacitor connecting pins for step-up circuit. (for VGL)	
19	CD2N	O	Capacitor connecting pins for step-up circuit. (for VGL)	
20	CD1N	O	Capacitor connecting pins for step-up circuit. (for VGL)	
21	CD1P	O	Capacitor connecting pins for step-up circuit. (for VGL)	
22	VGH	O	Power output (Positive) pin for gate driver.	
23	CC2N	O	Capacitor connecting pins for step-up circuit. (for VGH)	
24	CC2P	O	Capacitor connecting pins for step-up circuit. (for VGH)	
25	CC1P	O	Capacitor connecting pins for step-up circuit. (for VGH)	
26	CC1N	O	Capacitor connecting pins for step-up circuit. (for VGH)	
27	CB2N	O	Capacitor connecting pins for step-up circuit. (for AVDD)	
28	CB2P	O	Capacitor connecting pins for step-up circuit. (for AVDD)	
29	AVDD	O	Power output pin for analog circuit.	
30	VSS	P	ground power	

Table 3.1 input terminal pin assignments

4. DC ELECTRICAL CHARACTERISTICS

4.1 Absolute maximum ratings

Item	Symbol	MIN	MAX	Unit	Remark
Logic Supply Voltage	VDDI	-0.3	4.0	V	Pin VDD supply both voltage
Analog Supply Voltage	VDDA	-0.3	4.0	V	
Operating Temperature	T_{OPR}	-20	70	℃	
Storage Temperature	T_{STG}	-30	80	℃	

Table 4.1 absolute maximum rating

4.2 Recommended Operating Condition

Item		Symbol	MIN	TYP	MAX	Unit	Remark
Logic Supply Voltage		VDDI	2.55	3.3	3.6	V	
Analog Supply Voltage		VDDA	2.55	3.3	3.6	V	
Input Signal Voltage	Low Level	V_{IL}	0	-	0.3* VDDI	V	
	High Level	V_{IH}	0.7* VDDI	-	VDDI	V	
Output Signal Voltage	Low Level	V_{OL}	0	-	0.2* VDDI	V	
	High Level	V_{OH}	0.8* VDDI	-	VDDI	V	
(Panel+LSI) Power Consumption Logic Supply Voltage		Normal Mode(1HZ)	-	TBD	66	uW	

Table 4.2 LCD module electrical characteristics

5. AC ELECTRICAL CHARACTERISTICS

5.1 SPI Interface Characteristics

System Bus Timing for 4 wire SPI MCU Interface

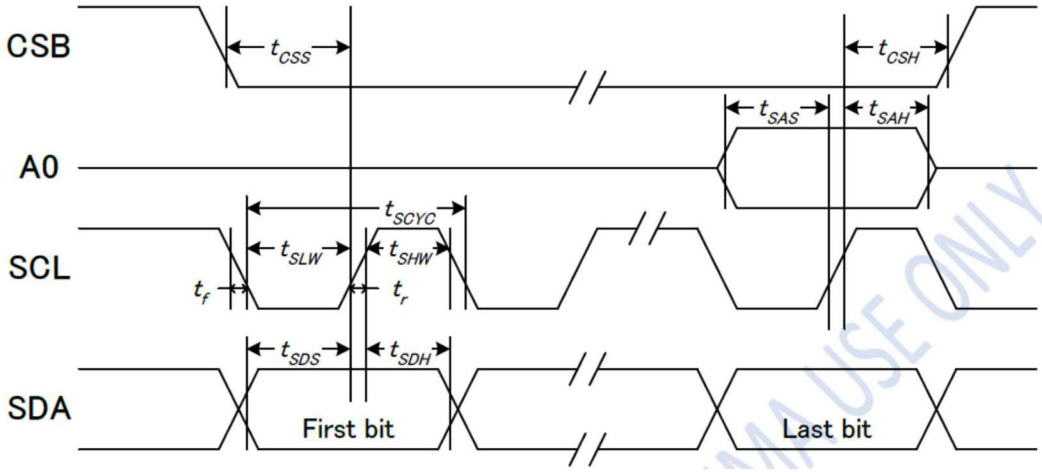


Figure5.1 System Bus Timing for 4 wire SPI MCU Interface

VDDI = 1.8~3.3V, Ta = 25˚C

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period	SCL	tSCYC		30	—	ns
SCLK "H" pulse width		tSHW		15	—	
SCLK "L" pulse width		tSLW		15	—	
Address setup time	A0	tSAS		10	—	
Address hold time		tSAH		10	—	
Data setup time	SDA	tSDS		10	—	
Data hold time		tSDH		10	—	
CSB-SCLK time	CSB	tCSS		10	—	
CSB-SCLK time		tCSH		10	—	

Note:

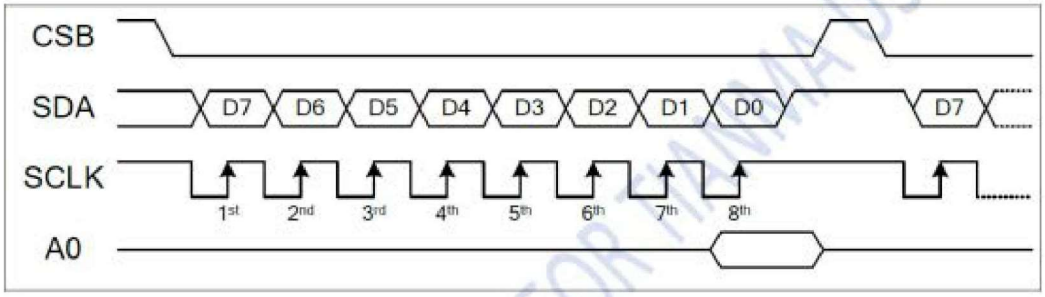
1. The input signal rise and fall time (tr, tf) are specified at 15 ns or less.
2. All timing is specified using 20% and 80% of VDDI as the standard.

Table 5.1 3SPI Interface characteristics

4-Line Serial Interface

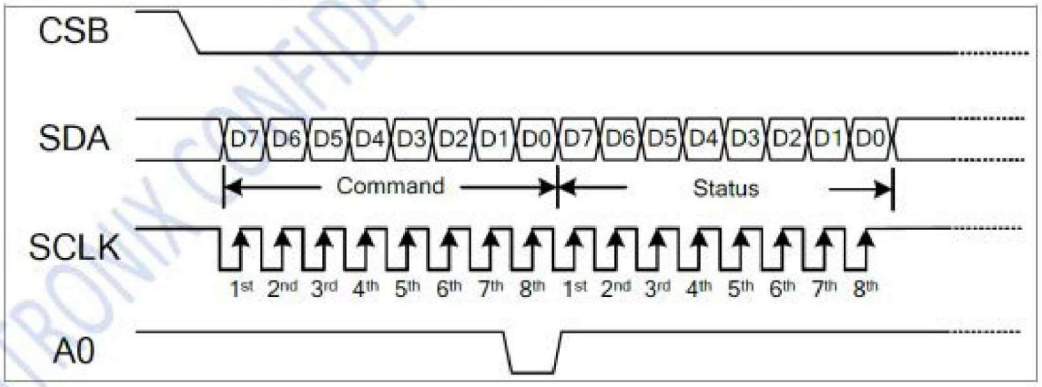
ST7302 is active when CSB is "L", serial data (SDA) and serial clock (SCLK) inputs are enabled. When CSB is "H", ST7302 is not active, the internal 8-bit shift register and 3-bit counter are reset. The DDRAM column address pointer will be increased by one automatically after writing each byte of DDRAM.

The display data/command indication is controlled by the register selection pin (A0). The signals transferred on data bus will be display data when A0 is high and will be instruction when A0 is low. Serial data (SDA) is latched at the rising edge of serial clock (SCLK). After the 8th serial clock, the serial data will be processed as 8-bit parallel data. The DDRAM column address pointer will be increased by one automatically after each byte of DDRAM access.



Write Operation of Single 4-Line SPI

After entering the "Read Status" instruction to read IC status, the information is shifted out as shown below. CSB signal must be kept at "L" during this period. All read out data will be 8 bits.



Read Status Operation of Single 4-Line SPI

5.2 Data Input Mode

TYPE1: There are 4 write operations for 24-bit data. (Set by "BPS=0" of command 0x3Ah)

Command	A0	D7	D6	D5	D4	D3	D2	D1	D0
DDRAM write	0	0	0	1	0	1	1	0	0
1st write	1	P1	P2	P3	P4	P5	P6	-	-
2nd write	1	P7	P8	P9	P10	P11	P12	-	-
3rd write	1	P13	P14	P15	P16	P17	P18	-	-
4th write	1	P19	P20	P21	P22	P23	P24	-	-

Note: - don't care

TYPE2: There are 3 write operations for 24-bit data. (Set by "BPS=1" of command 0x3Ah)

Command	A0	D7	D6	D5	D4	D3	D2	D1	D0
DDRAM write	0	0	0	1	0	1	1	0	0
1st write	1	P1	P2	P3	P4	P5	P6	P7	P8
2nd write	1	P9	P10	P11	P12	P13	P14	P15	P16
3rd write	1	P17	P18	P19	P20	P21	P22	P23	P24

The data mapping of Mono display is as below.

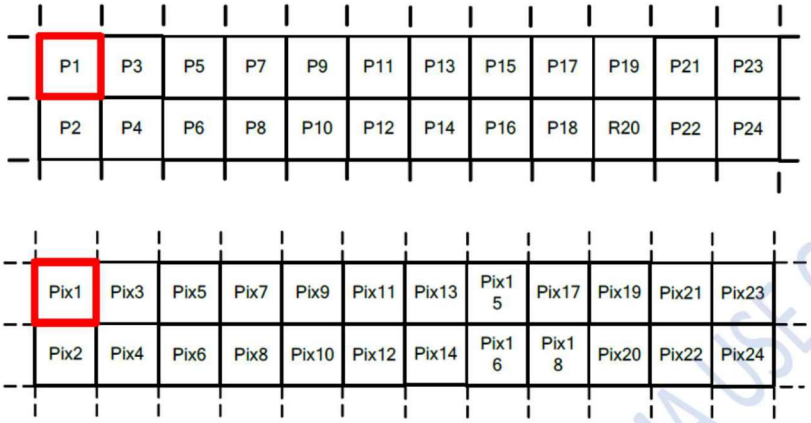
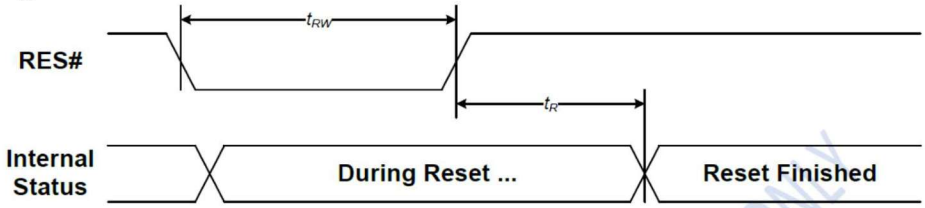


Figure5.2 Data to Display Mapping

5.3 Reset timing



VDDI = 1.8~3.3V, Ta = 25°C

Item	Symbol	Condition	Min.	Max.	Unit
Reset time	tR		—	1	ms
Reset "L" pulse width	tRW		1	—	ms

6. POWER ON/OFF SEQUENCE

VDDI and VDDA can be applied in any order.

VDDA and VDDI can be power down in any order.

During power off, if LCD is in the Sleep Out mode, VDDA and VDDI must be powered down minimum 500msec after RSTB has been released.

During power off, if LCD is in the Sleep In mode, VDDI or VDDA can be powered down minimum 0msec after RSTB has been released.

CSB can be applied at any timing or can be permanently grounded. RSTB has priority over CSB.

Note 1: There will be no damage to the display module if the power sequences are not met.
Note 2: There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.
Note 3: There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.
Note 4: If RSTB line is not held stable by host during Power On Sequence as defined in the sequence below, then it will be necessary to apply a Hardware Reset (RSTB) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

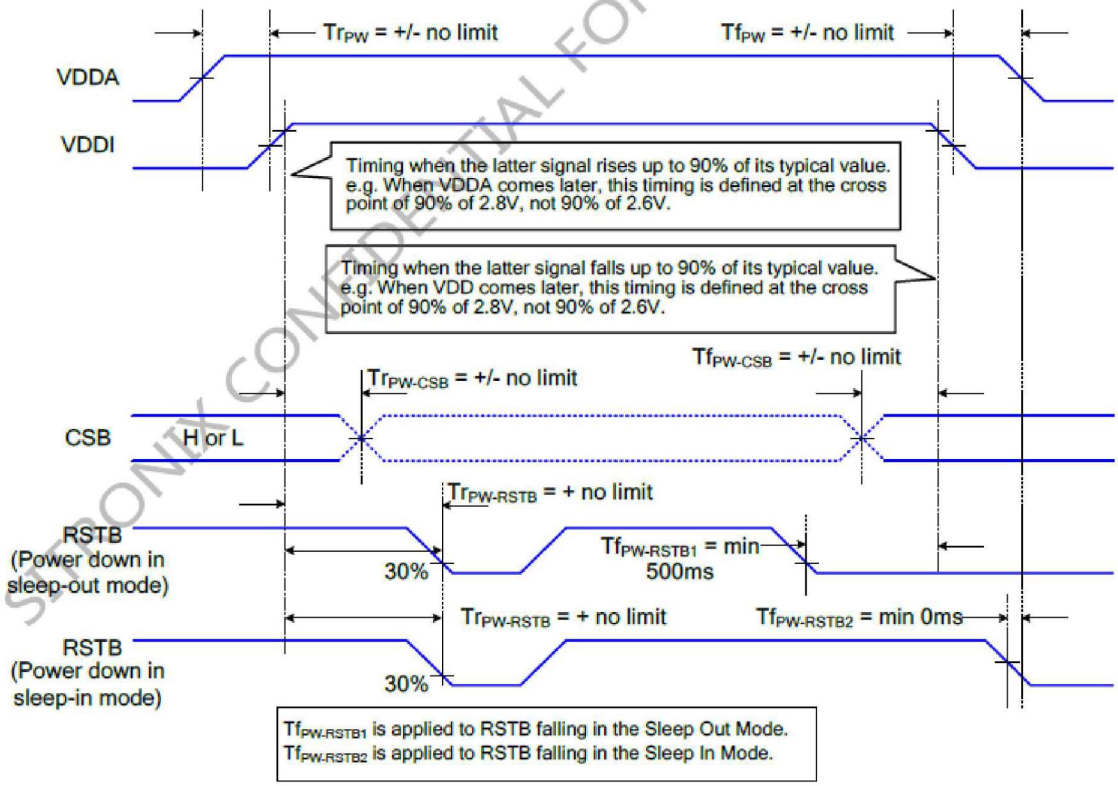


Figure 6.1 power on/off sequence

7. Optical Characteristics

7.1 Optical Specification

Ta=25℃

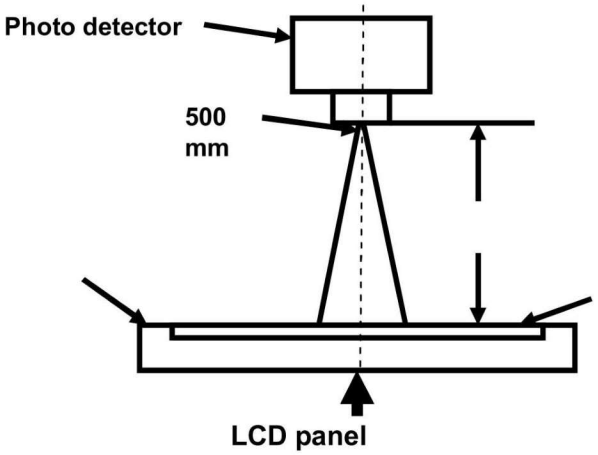
Item		Symbol	Condition	Min	Typ	Max	Unit	Remark
View Angles		θT	CR≧2	40	55	-	Degree	Note 2
		θB		40	55	-		
		θL		40	55	-		
		θR		40	55	-		
Contrast Ratio		CR	θ=0°	6	9	-	-	Note3
Reflectivity				-	13%	16%	-	Note1
Response Time		T_{ON}	25℃	-	20	30	ms	Note4
		T_{OFF}						
Chromaticity	White	x	Backlight is off		0.33			Note5
		y			0.36			

Test Conditions:

1. the ambient temperature is 25℃.
2. The test systems refer to Note 1 and Note 2.

Note 1: Definition of optical measurement system.

The optical characteristics should be measured in dark room. After 5 minutes operation, the optical properties are measured at the center point of the LCD screen. All input terminals LCD panel must be ground when measuring the center area of the panel.



Item	Photo detector	Field
Contrast Ratio	CM-3600A	10°
luminance		
Chromaticity		
Lum Uniformity		
Response Time	DMS-803	

Note 2: Definition of viewing angle range and measurement system.

viewing angle is measured at the center point of the LCD by DMS-803。

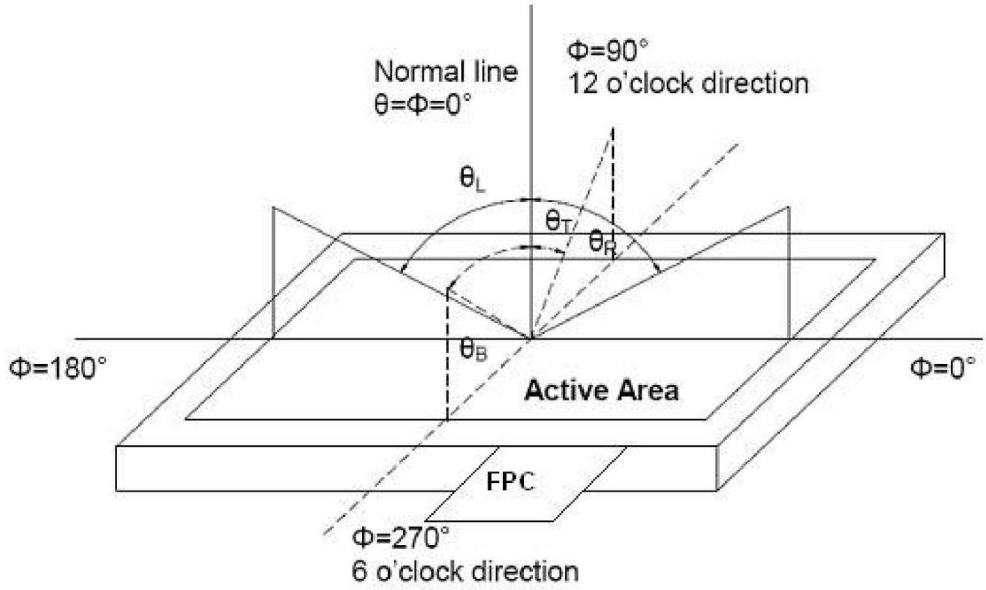


Fig. 7.1 Definition of viewing angle

Note 3: Definition of contrast ratio

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD is on the "White" state}}{\text{Luminance measured when LCD is on the "Black" state}}$$

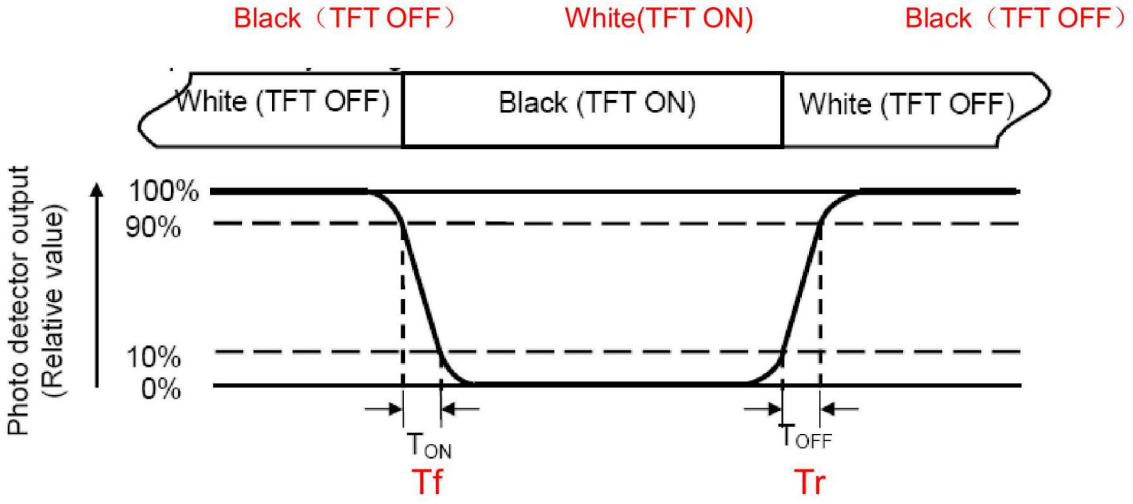
“White state “:The state is that the LCD should be driven by Vwhite.

“Black state”: The state is that the LCD should be driven by Vblack.

Vwhite: To be determined Vblack: To be determined.

Note 4: Definition of Response time

The response time is defined as the LCD optical switching time interval between “White” state and “Black” state. Rise time (T_r) is the time between photo detector output intensity changed from 10% to 90%. And fall time (T_f) is the time between photo detector output intensity changed from 90% to 10%.



Note 5: Definition of color chromaticity (CIE1931)

Color coordinates measured at center point of LCD.

8 . Environmental / Reliability Tests

No	Test Item	Condition	Remarks
1	High Temperature Operation	Ta=50℃, 30%RH, 240Hr	IEC60 068-2-2Bb
2	Low Temperature Operation	Ta=-0℃, 240 hours	IEC60068-2-2Ab
3	High Temperature Storage	Ta=70℃, 40%RH, 240 hours (test in white pattern)	IEC60068-2-2Bb
4	Low Temperature Storage	Ta = -25℃, 240hours (test in white pattern)	IEC60068-2-2Ab
5	High Temperature and Humidity Storage	Ta=40℃，90%RH，168H hours	IEC60068-2-3CA
6	High Temperature, High-Humidity Storage	T=60℃，80%RH，480Hr Test in white pattern	IEC60068-2-3CA
7	Temperature Cycle	-25℃(30min)~70℃(30min) ，50 Cycle (Test in white pattern)	IEC 60 068-2-14NB
8	Vibration Test	振动方式：随机振动（模拟路跑） 10-500HZ 额定功率，振动加速度 1.04G， X，Y，Z 三轴各 60 分钟，振幅 1.5mm	Full packed for shipment
9	Package Drop Test	Height:122cm, 1corner,3edges,6surfaces	Full packed for shipment
10	Electronstatic discharge	Machine model: +/- 250V，0Ω，200pF	IEC61000-4-2

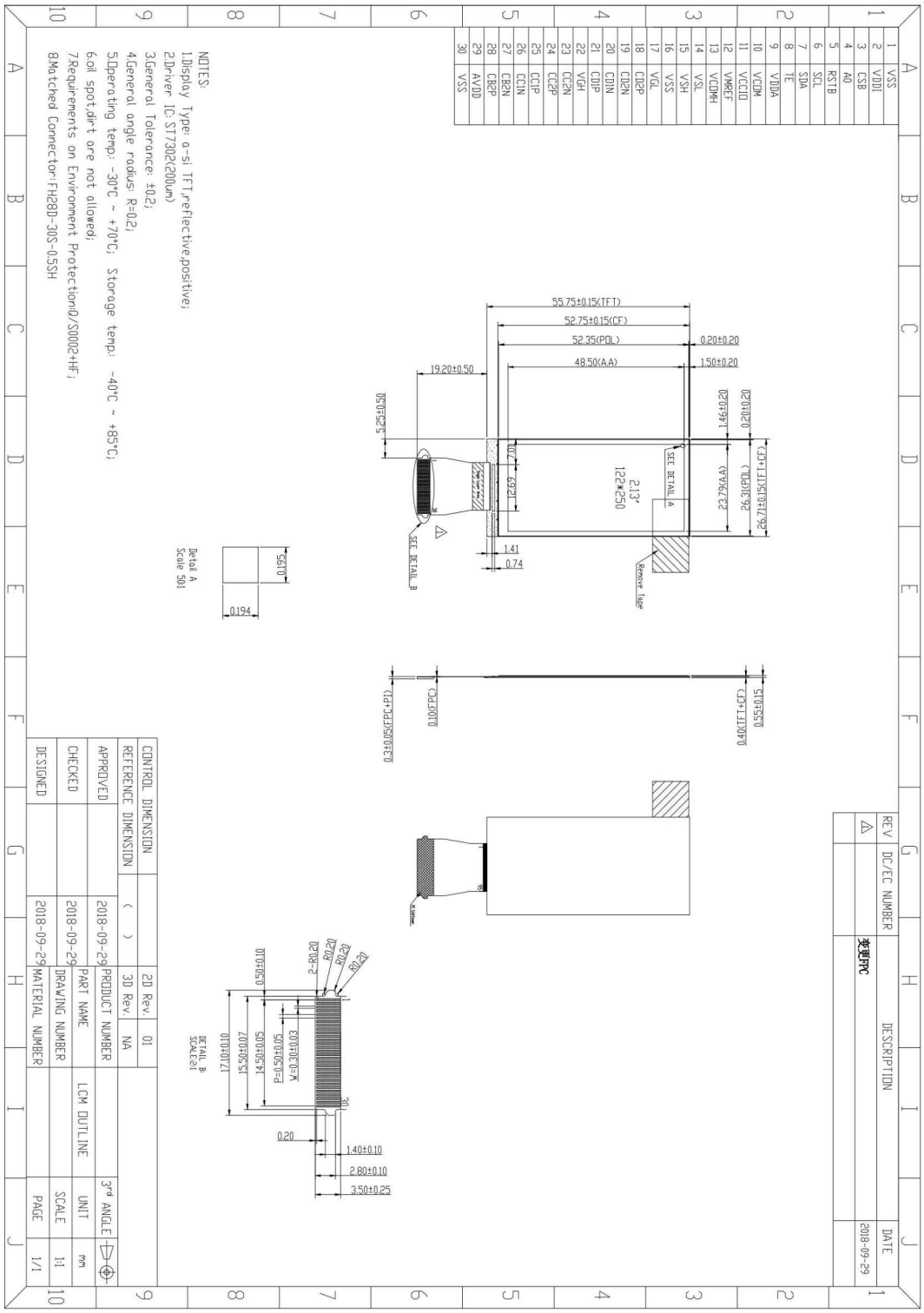
Note1: Ts is the temperature of panel's surface.

Note2: Ta is the ambient temperature of sample.

Note3: Before cosmetic and function test, the product must have enough recovery time, at least 2 hours at room temperature.

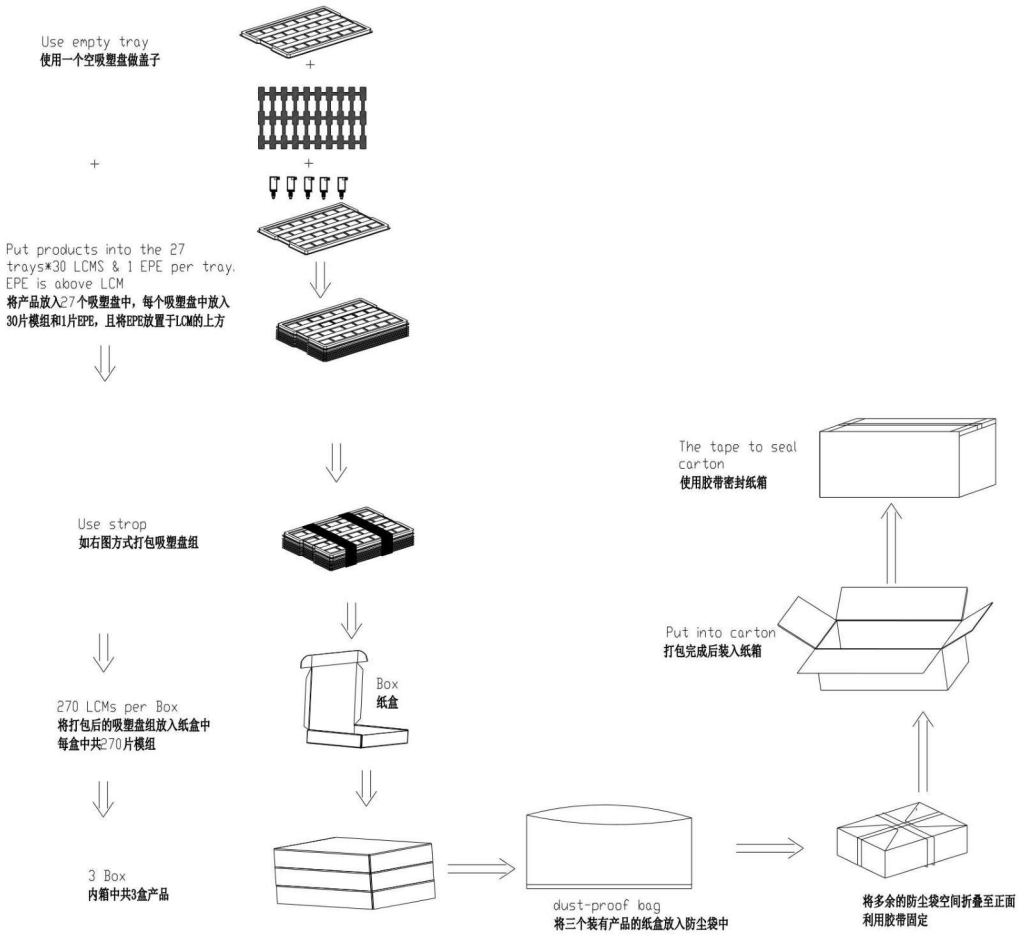
Note 4: In the standard condition, there shall be no practical problem that may affect the display function. After the reliability test, the product only guarantees operation, but don't guarantee all of the cosmetic specification.

9.Mechanical Drawing



10 . Packing Drawing

No	Item	Model (Material)	Dimensions(mm)	Unit Weight(Kg)	Quantity	Material Number
1	LCM module	GDTH0213ZHFT34	26.71×55.75×0.55	TBD	810	GDTH0213ZHFT34
2	Tray	PET	485×330×13.8	0.22	30	1150342430
3	EPE	EPE	420.10×242.25×1.00	TBD	27	1680350950
4	Dust-proof Bag	PE	700×545×0.05	0.021	1	1680009800
5	Carton	Corrugated Paper	544×365×250	1.01	1	1680007612
6	BOX	Corrugated Paper	520×345×74	0.227	3	1680000540
7	Label		100×52	TBD	1	1690000280
8	Total weight	TBD Kg				



Precautions for Use of LCD Modules

11.1 Handling Precautions

11.1.1 The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

11.1.2 If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

11.1.3 Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

11.1.4 The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

11.1.5 If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

- Isopropyl alcohol
- Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

- Water
- Ketone
- Aromatic solvents

11.1.6 Do not attempt to disassemble the LCD Module.

11.1.7 If the logic circuit power is off, do not apply the input signals.

11.1.8 To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

11.1.8.1 Be sure to ground the body when handling the LCD Modules.

11.1.8.2 Tools required for assembly, such as soldering irons, must be properly ground.

11.1.8.3 To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

11.1.8.4 The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

11.2 Storage precautions

11.2.1 When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.

11.2.2 The LCD modules should be stored under the storage temperature range. If the LCD modules will be stored for a long time, the recommend condition is:

Temperature : 0℃ ～ 40℃ Relatively humidity: ≤80%

11.2.3 The LCD modules should be stored in the room without acid, alkali and harmful gas.

11.3 Transportation Precautions:

The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.