SPECIFICATION
FOR
OLED Module
BLKD032BE001

MODULE:	
CUSTOMER:	

REV	DESCRIPTION	DATE
1.0	FIRST ISSUE	2018.03.06

	INITIAL	DATE
PREPARED BY		
CHECKED BY		
APPROVED BY		

CUSTOMER	INITIAL	DATE
APPROVED BY		

Revision History

Date	Rev. No.	Page	Summary
2018.03.06	V1.0	ALL	FIRST ISSUE

Contents

1. Basic Specifications

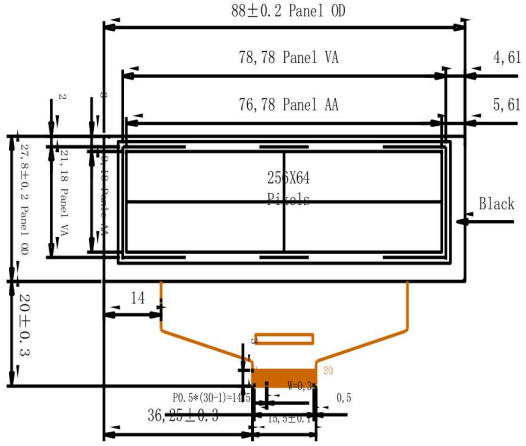
General Information Items	Specification	Unit	Note
	Main Panel		
OLED Display area(AA)	76.78(H)*19.18(V) (3.2inch)	mm	-
Display color	Monochrome (Yellow)	colors	-
Drive Duty	1/64 Duty	-	-
Number of pixels	256(H)*64(V)	dots	-
Pixel pitch	0.2999(H)*0.2999(V)	mm	-
OLED Controller IC	SSD1322U	-	-
Display mode	Passive Matrix	-	-
Operating temperature	-20°C ~ +70°C	℃	-
Storage temperature	-30°C ~ +80°C	℃	-

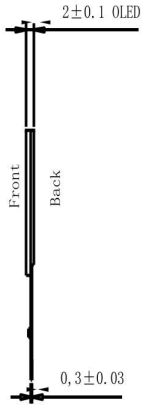
*** Mechanical Information**

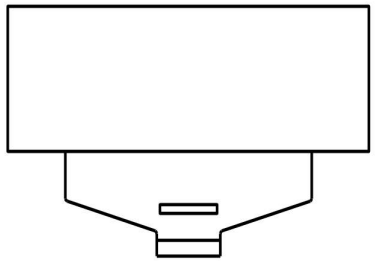
Item		Min.	Typ.	Max.	Unit	Note
Module size	Horizontal(H)		88.00		mm	-
	Vertical(V)		27.80		mm	-
	Depth(D)		2.0		mm	-
Weight			TBD		g	-

2. Outline dimension

ReV	Revision content description	Date
A	FIRST	2018.05.07







NO.	Pin Name
1	GND
2	VSS
3	VCC
4	VCOMH
5	VLSS
6	D7
7	D6
8	D5
9	D4
10	D3
11	D2
12	D1
13	D0
14	E/RD
15	R/W
16	BS0
17	BS1
18	D/C#
19	CS#
20	RES#
21	FR
22	IREF
23	NC
24	VDDIO
25	VDD
26	VCI
27	VSL
28	VLSS
29	VCC
30	GND

NOTE:

1. Coating protective tape on the module two sides.
2. Must follow the RoHS international standard Cosmetic Work Instruction for all cosmetic criteria.
3. OLED DRIVER IC: SSD1322U
4. Dimensions are in millimeters, the tolerances haven't been listed will be ±0.2 .
5. OLED Interface: 8BIT 68XX/80XX Paraller,3/4-Wire SPI

TOLERANCE(公差)	DRAWING NAME		
	PARTS NO.		
TOLERANCE UNLESS X.X±0.3	Drawn		Unit
OTHERWISE SPECIFIED X.XX±0.2	Checked		mm
Scale 1:1	Approve		Page 1/1

3. Input terminal Pin Assignment

3.1 OLED

NO.	SYMBOL	DISCRIPTION	I/O
1	GND	Ground	P
2	VSS	Ground of Logic Circuit This is a ground pin. It also acts as a reference for the logic pins. It must be connected to external ground	P
3	VCC	Power Supply for OEL Panel This is the most positive supply pin of the chip. They must be connected to external source.	P
4	VCOMH	Voltage Output High Level for COM Signal This pin is the input pin for the voltage output high level for COM signals. A tantalum capacitor should be connected between this pin and VSS.	P
5	VLSS	Ground of Analog Circuit This is analog ground pin. IT should be connected to VSS externally	P
6-13	D7-D0	Host Data Input/Output Bus These pins are 8-bit bi-directional data bus to be connected to the microprocessors data bus. When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK. Unused pins must be connected to VSS except for D2 in serial mode.	I/O
14	E/RD	Read/Write Enable or Read This pin is MCU interface input. When interfacing to a 68XXsseries microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the CS# is pulled low. When connecting to an 80XX-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is low and CS# is pulled low. When serial mode is selected, this pin must be connected to VSS	I

<table>
<tr><td>15</td><td>R/W</td><td>Read/Write Select or Write
This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Pull this pin to “High” for read mode and pull it “Low” for write mode.
When 80XX interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the CS# is pulled low.
When serial mode is selected, this pin must be connected to VSS</td><td>I</td></tr>
<tr><td>16</td><td>BS0</td><td rowspan="2">Communicating Protocol Select
These pins are MCU interface selection input. See the following table:<table><tr><td></td><td>BS0</td><td>BS1</td></tr><tr><td>3-wire SPI</td><td>1</td><td>0</td></tr><tr><td>4wire SPI</td><td>0</td><td>0</td></tr><tr><td>8-bit 68XX Parallel</td><td>1</td><td>1</td></tr><tr><td>8-bit 80XX Parallel</td><td>0</td><td>1</td></tr></table></td><td rowspan="2">I</td></tr>
<tr><td>17</td><td>BS1</td></tr>
<tr><td>18</td><td>DC#</td><td>Data/Command Control
This pin is Data/Command control pin. When the pin is pulled high, the input at D7~D0 is treated as display data. When the pin is pulled low, the input at D7~D0 will be transferred to the command register. For detailed relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams</td><td>I</td></tr>
<tr><td>19</td><td>CS#</td><td>Chip Select
This pin is the chip select input. When the pin is enabled for MCU communication only when CS# is pulled low..</td><td>I</td></tr>
<tr><td>20</td><td>RES#</td><td>Power Reset for Controller and Driver
This pin is reset signal input. When the pin is low, initialization of the chip is executed.</td><td>I</td></tr>
<tr><td>21</td><td>FR</td><td>Cascade Application Connection Pin
This pin is No Connection pins. Nothing should be connected to this pin. It should be left open individually.</td><td>O</td></tr>
<tr><td>22</td><td>IREF</td><td>Current Reference for Brightness Adjustment
This pin is segment current reference pin. A resistor should be connected between this pin and VSS. Set the current lower than</td><td>I</td></tr>
</table>

		10µA	
23	NC	Reserved Pin The N.C. pin between function pins are reserved for compatible and flexible design.	-
24	VDDIO	Power Supply for I/O Pin This pin is a power supply pin of I/O buffer. It should be connected to VDD or external source. All I/O signals should have VIH reference to VDDIO. When I/O signal pins (BS0~BS1, D0~D7, control signals…) pull high, they should be connected to VDDIO.	P
25	VDD	Power Supply for Core Logic Circuit This is a voltage supply pin. It can be supplied externally (within the range of 2.4~2.6V) or regulated internally from VCI. A capacitor should be connected between this pin & VSS under all circumstances	P
26	VCI	Power Supply for Operation This is a voltage supply pin. It must be connected to external source &always be equal or higher than VDD & VDDIO.	P
27	VSL	Voltage Output Low Level for SEG Signal This is segment voltage reference pin. When external VSL is not used, this pin should be left open. When external VSL is used, this pin should connect with resistor and diode to ground.	P
28	VLSS	Ground of Analog Circuit This is the analog ground pin. It should be connected to VSS externally	P
29	VCC	Power Supply for OEL Panel This is the most positive supply pin of the chip. They should be connected to external source.	P
30	GND	Ground	P

4. LECTRICAL SPECIFICATION OLED

4.1 Absolute Maximum Ratings

Item	Symbol	Min	Max	Unit	Note
Supply Voltage for Operation	V_{CI}	-0.3	4	V	1, 2
Supply Voltage for Logic	V_{DD}	-0.5	2.75	V	1, 2
Supply Voltage for I/O pins	V_{DDIO}	-0.5	V_{CI}	V	1, 2
Supply Voltage for Display	V_{CC}	-0.5	16	V	1, 2
Operating Current for V_{CC}	I_{CC}	-	55	mA	1,2
Operating Temperature	Top	-30	+85	°C	
Storage Temperature	Tst	-40	+90	°C	
Static Electricity	Be sure that you are grounded when handling displays.				

Note 1: All the above voltages are on the basis of “VSS = 0V”.

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the c onditions cording to Section 3.2 “Electrical Characteristics”. If this module is used beyond these condit ions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

4.2 ELECTRICAL CHARACTERISTICS OLED

Item	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage for Operation	V_{CI}		2.4	2.8	3.5	V
Supply Voltage for Logic	V_{DD}		2.4	2.5	2.6	V
Supply Voltage for I/O Pins	V_{DDIO}		1.65	1.8	V_{CI}	V
Supply Voltage for Display	V_{CC}		11.5	12	12.5	V
High Level Input	V_{IH}		0.8xV_{DDIO}	--	V_{DDIO}	V
Low Level Input	V_{IL}		0	--	0.2xV_{DDIO}	V
High Level Output	V_{OH}	I_{OUT}=100µA, 3.3MHz	0.9xV_{DDIO}	--	V_{DDIO}	V
Low Level Output	V_{OL}	I_{OUT}=100µA, 3.3MHz	0	--	0.1xV_{DDIO}	V
Operating Current for V_{CI}	I_{CI}	Note 4	-	1.8	2.25	mA
		Note 5	-	1.8	2.25	mA
Operating Current for V_{CC}	I_{CC}	Note 4	-	26.3	32.9	mA
		Note 5	-	41.1	51.4	mA
Sleep Mode Current for V_{CI}	$I_{CI,SLEEP}$		-	1	5	µA
Sleep Mode Current for V_{CC}	$I_{CC,SLEEP}$		-	1	5	µA

Note 3: Brightness (Lbr) and Supply Voltage for Display (VCC) are subject to the change of panel characteristics and the customers request.
Note 4: VCI = 2.8V, VCC = 12V, 50% Display Area Turn on.
Note 5: VCI = 2.8V, VCC = 12V, 100% Display Area Turn on.

5. Optics Characteristics

5.1 Optics Characteristics OLED

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Brightness	L_{br}	With Polarizer (Note 3)	60	80	-	cd/m^2
C.I.E. (Yellow)	(x) (y)	See section 5.4				
Dark Room Contrast	CR		-	>2000:1	-	
View Angle			>160	-	-	degree

Note 3: Optical measurement taken at $V_{CI} = 2.8V$, $V_{CC} = 12V$

5.2 C.I.E colour

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
DD-PO-25664YW-4A & DD-PT-25664YW-4A						
C.I.E. (Yellow)	(x) (y)	Without Polarizer	0.44 0.46	0.48 0.50	0.52 0.54	
DD-PO-25664WE-1A & DD-PT-25664WE-1A						
C.I.E. (White)	(x) (y)	Without Polarizer	0.28 0.29	0.32 0.33	0.36 0.37	
DD-PO-25664BE-3A & DD-PT-25664BE-3A						
C.I.E. (Blue)	(x) (y)	Without Polarizer	0.12 0.22	0.16 0.26	0.20 0.30	
DD-PO-25664GE-4A & DD-PT-25664GE-4A						
C.I.E. (Green)	(x) (y)	Without Polarizer	0.27 0.58	0.31 0.62	0.35 0.66	

6. UNCTIONAL SPECIFICATION OLED

6.1 COMMANDS

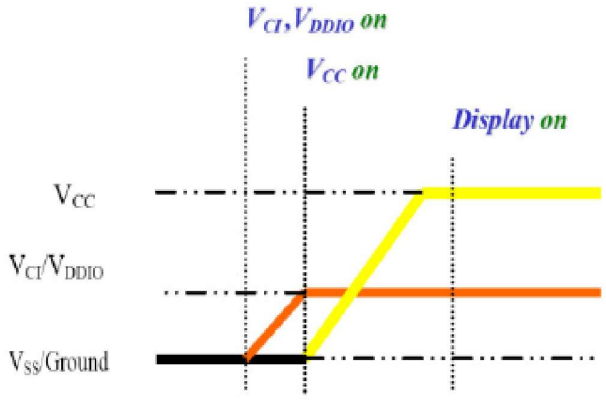
Refer to the Technical Manual for the SSD1322

6.2 POWER DOWN AND UP SEQUENCE

To protect the panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. Such that panel has enough time to charge and discharge before/after operation.

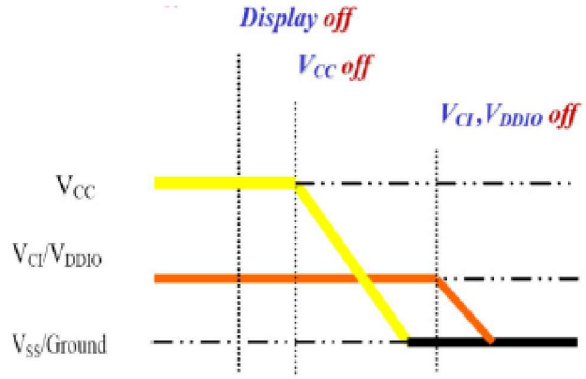
6.2.1 Power up Sequence:

1. Power up V_{CI} & V_{DDIO}
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up V_{CC}
6. Delay 100ms (when V_{CC} is stable)
7. Send Display on command



6.2.2 Power down Sequence:

1. Send Display off command
2. Power down V_{CC}
3. Delay 100ms (when V_{CC} is reach 0 and panel is completely discharges)
4. Power down V_{CI} & V_{DDIO}



6.3 ESET CIRCUIT

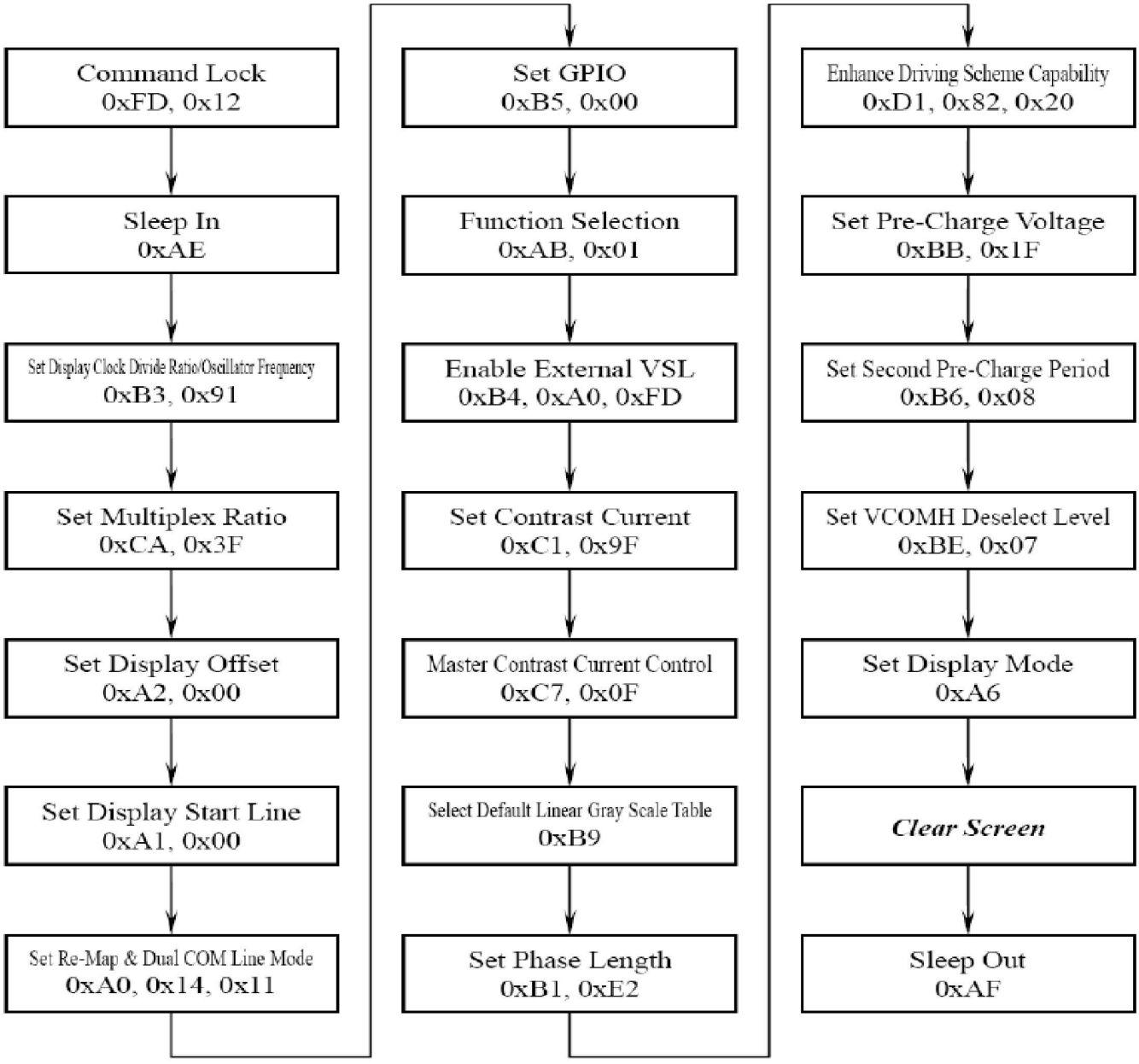
When RES# input is low, the chip initialized with the following status:

1. Display is OFF
2. 480x128 Display Mode
3. Normal segment and display data column and row address mapping (SEG0 mapped to column address 00h and COM0 mapped to row address 00h)
4. Display start line is set at display RAM address 0
5. Column address counter is set at 0
6. Normal scan direction of the COM outputs

7. Contrast control registers is set at 7Fh

6.4 ACTUAL APPLICATION EXAMPLE OLED

Command usage and explanation of an actual example
<Initialization>



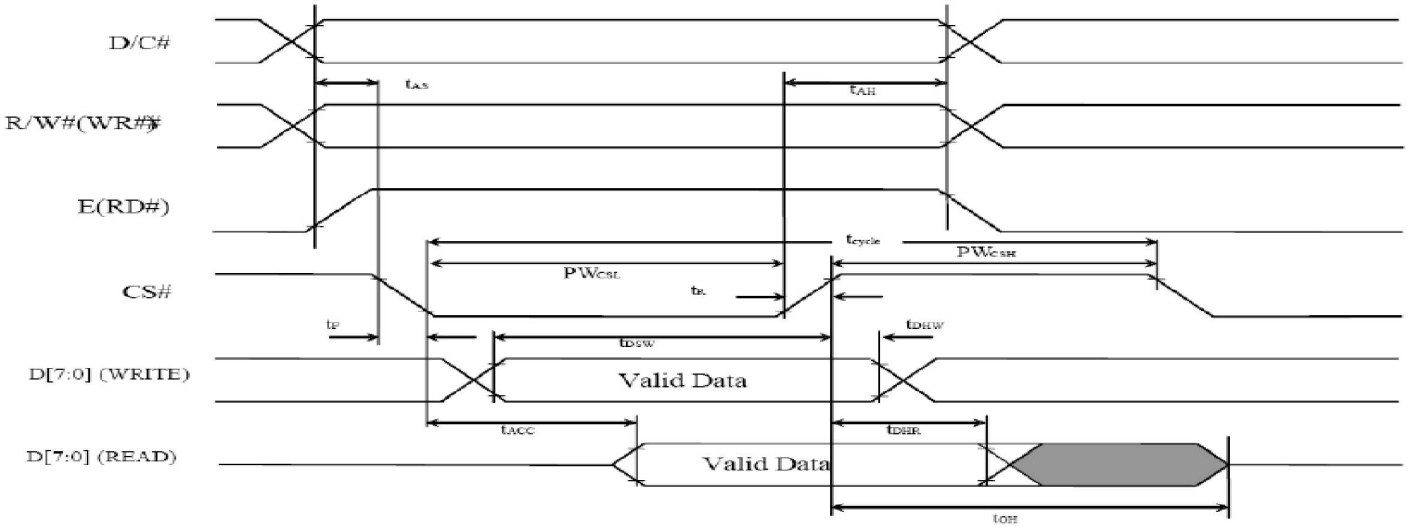
If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

7. TIMING CHARACTERISTICS

7.1 68XX-Series MPU Parallel Interface Timing Characteristics

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	10	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	7	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (Read) Chip Select Low Pulse Width (Write)	120 60	-	ns
PW_{CSH}	Chip Select High Pulse Width (Read) Chip Select High Pulse Width (Write)	60 60	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

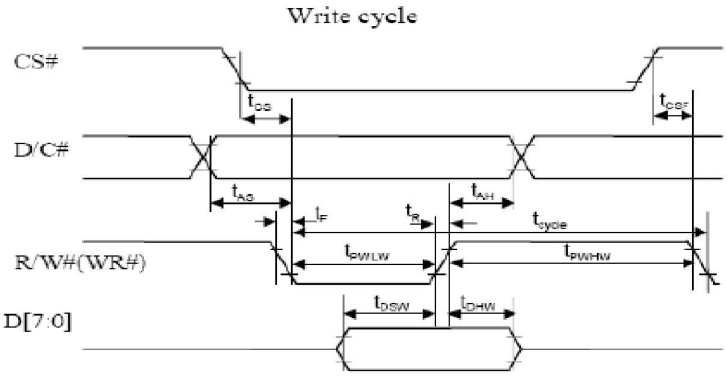
(V_{DD}-V_{SS} = 2.4V to 2.6V, V_{DDIO} = 1.6V, V_{CI} = 2.8V, T_a = 25°C)

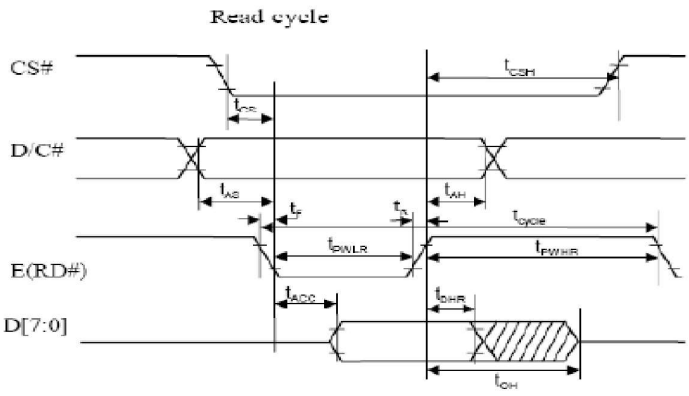


7.2 80XX-Series MPU Parallel Interface Timing Characteristics

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	10	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	7	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
t_{PWLR}	Read Low Time	150	-	ns
t_{PWLW}	Write Low Time	60	-	ns
t_{PWHR}	Read High Time	60	-	ns
t_{PWHW}	Write High Time	60	-	ns
t_{CS}	Chip Select Setup Time	0	-	ns
t_{CSH}	Chip Select Hold Time to Read Signal	0	-	ns
t_{CSF}	Chip Select Hold Time	20	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

(V_{DD}-V_{SS} = 2.4V to 2.6V, V_{DDIO} = 1.6V, V_{CI} = 2.8V, T_a = 25°C)

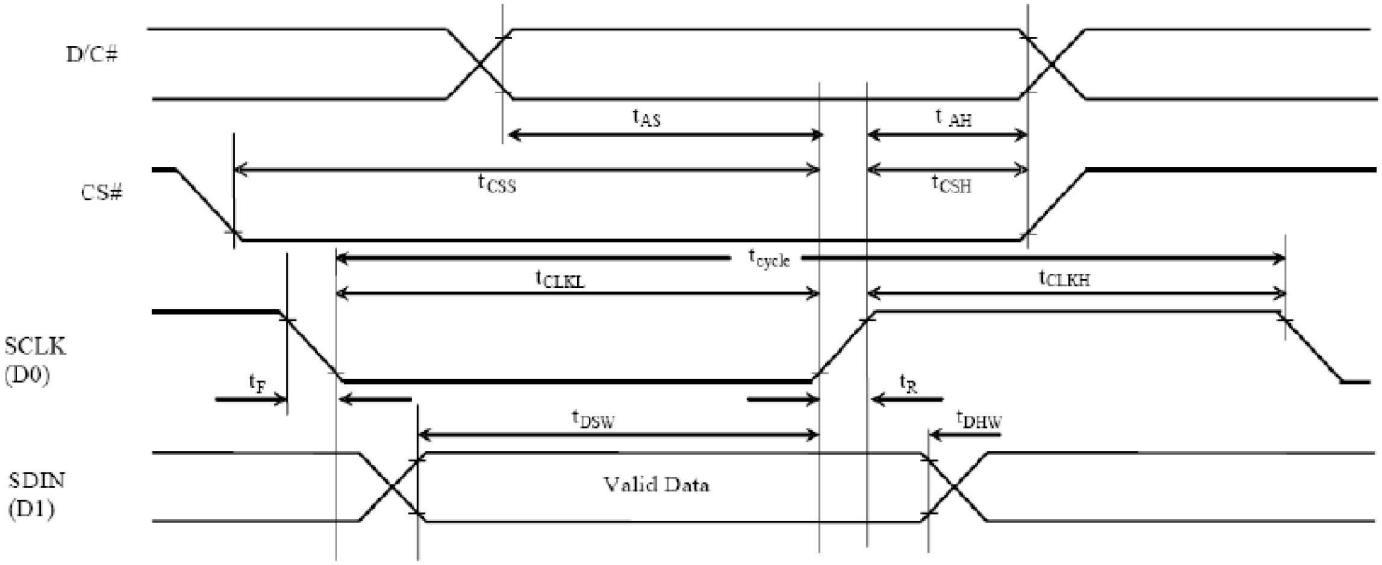




7.3 Serial Interface Timing Characteristics: (4-wire SPI)

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	ns
t_{AS}	Address Setup Time	15	-	ns
t_{AH}	Address Hold Time	15	-	ns
t_{CSS}	Chip Select Setup Time	20	-	ns
t_{CSH}	Chip Select Hold Time	10	-	ns
t_{DSW}	Write Data Setup Time	15	-	ns
t_{DHW}	Write Data Hold Time	15	-	ns
t_{CLKL}	Clock Low Time	20	-	ns
t_{CLKH}	Clock High Time	20	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

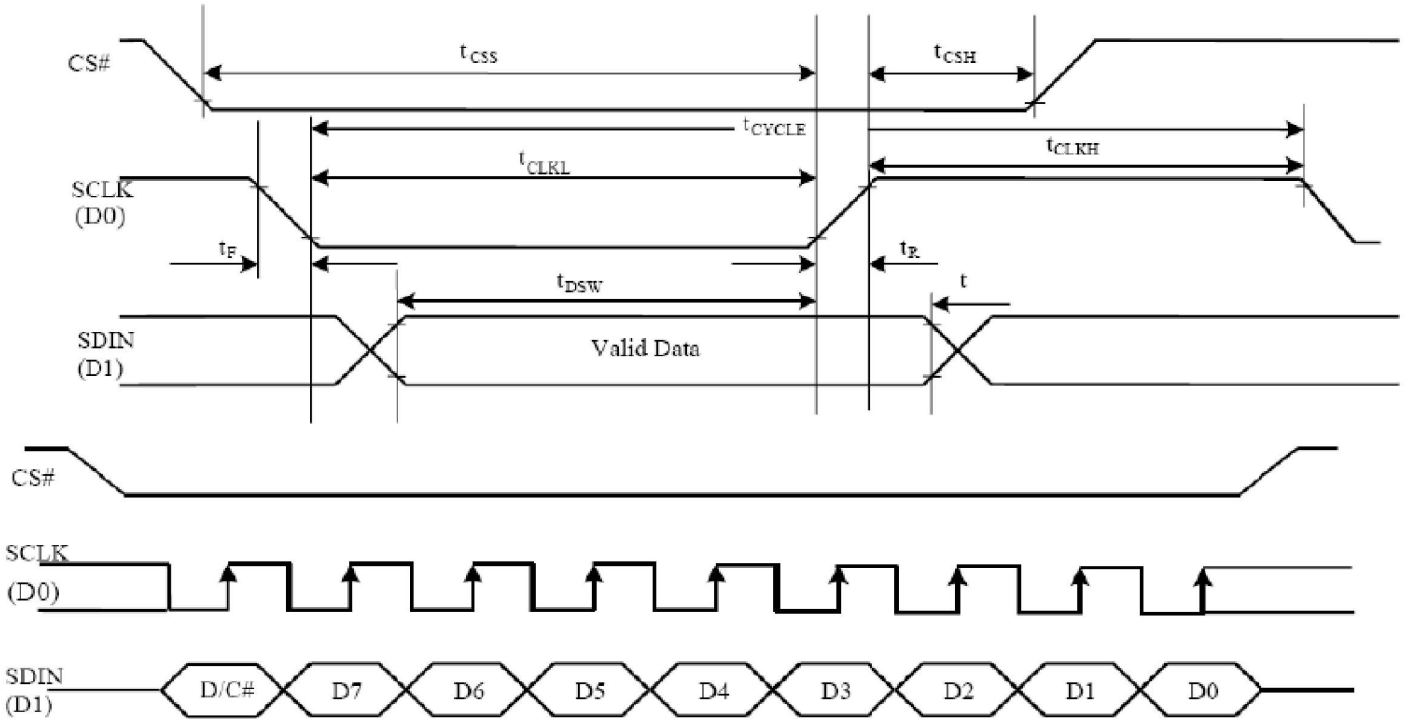
(V_{DD}-V_{SS} = 2.4V to 2.6V, V_{DDIO} = 1.6V, V_{CI} = 2.8V, T_a = 25°C)



7.4 Serial Interface Timing Characteristics: (3-wire SPI)

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	ns
t_{AS}	Address Setup Time	15	-	ns
t_{AH}	Address Hold Time	15	-	ns
t_{CSS}	Chip Select Setup Time	20	-	ns
t_{CSH}	Chip Select Hold Time	10	-	ns
t_{DSW}	Write Data Setup Time	15	-	ns
t_{DHW}	Write Data Hold Time	15	-	ns
t_{CLKL}	Clock Low Time	20	-	ns
t_{CLKH}	Clock High Time	20	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

(V_{DD}-V_{SS} = 2.4V to 2.6V, V_{DDIO} = 1.6V, V_{CI} = 2.8V, T_a = 25°C)



8. QUALITY ASSURANCE SPECIFICATION

8.1 CONFORMITY

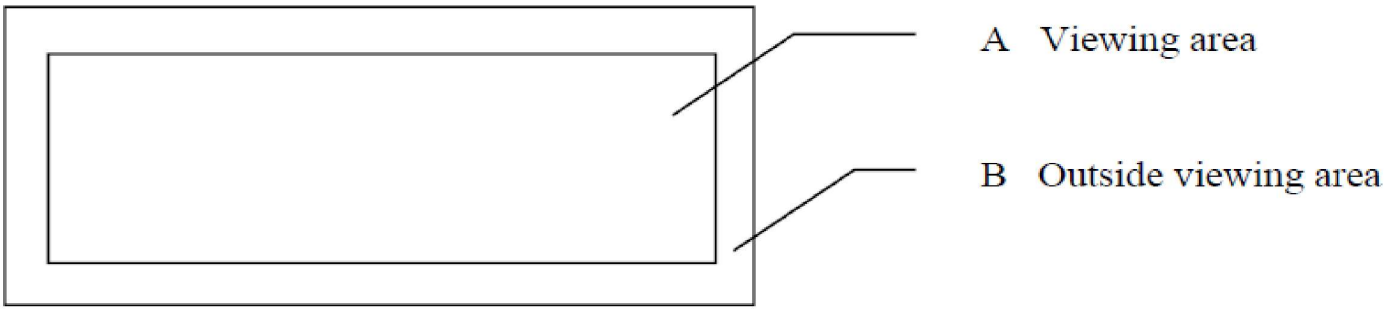
The performance, function and reliability of the shipped products conform to the Product Specification.

8.2 DELIVERY ASSURANCE

8.2.1 Delivery inspection standards

IPC-AA610 rev. C, class 2 electronic assemblies standard

8.2.2 Zone definition

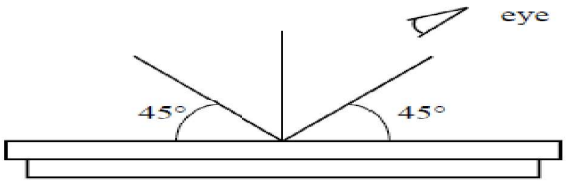


8.2.3 Visual inspection

Test and measurement to be conducted under following conditions :

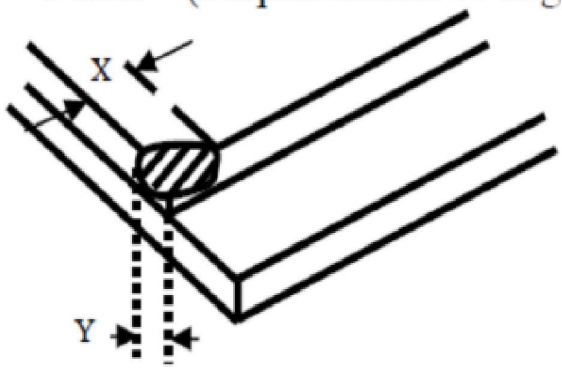
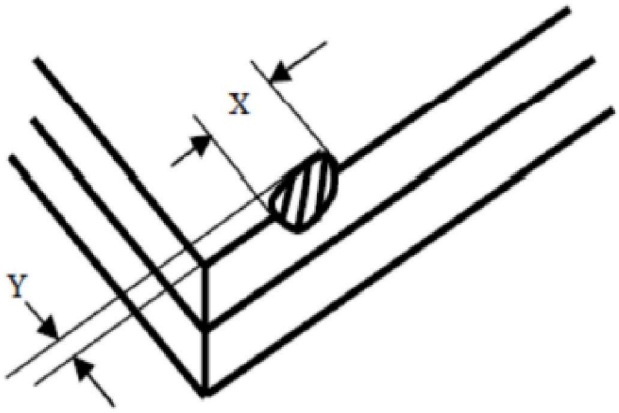
Temperature:	23±5℃
Humidity:	55±15%RH
Fluorescent lamp:	30 W
Distance between the Panel & Eyes of the Inspector:	≧30cm
Distance between the Panel & the lamp:	≧50cm

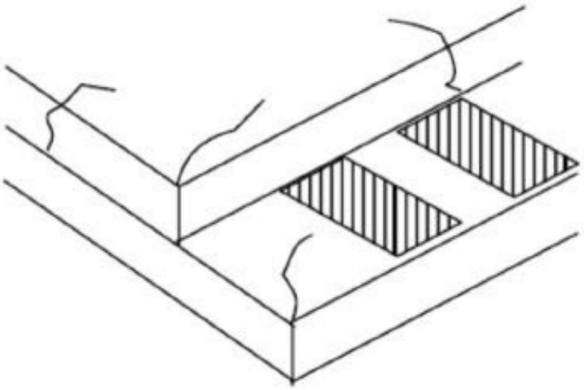
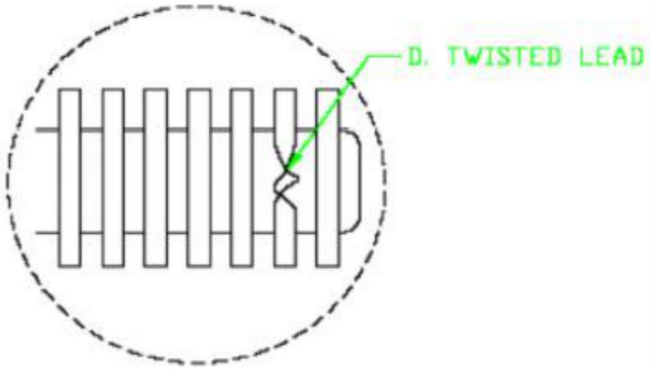
Finger glove (or finger cover) must be worn by the inspector.
Inspection table or jig must be anti-electrostatic

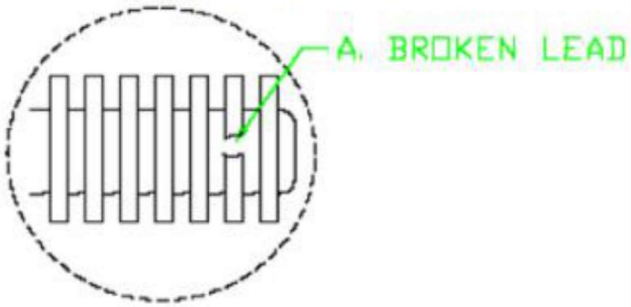
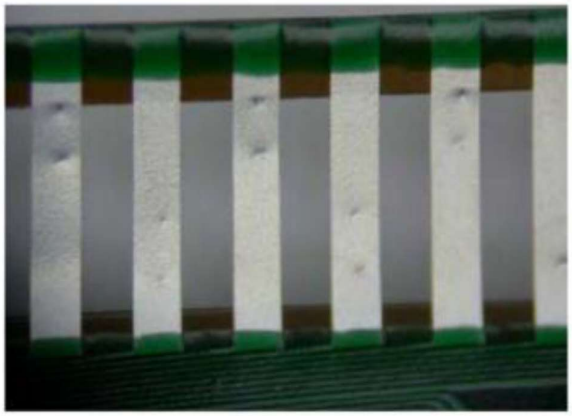


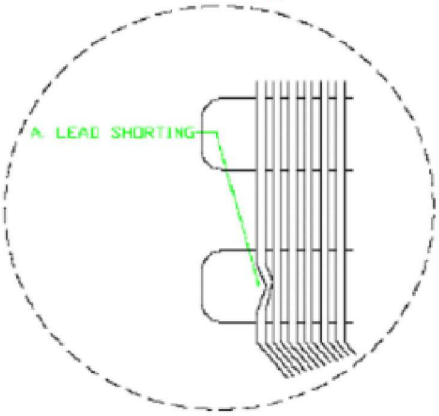
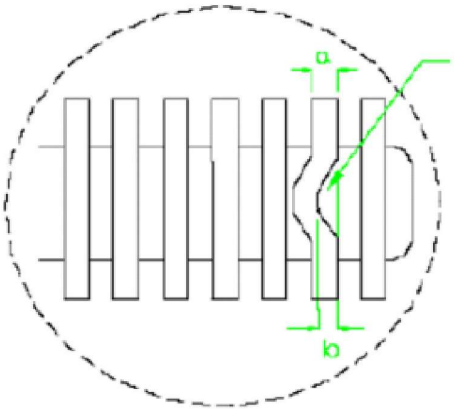
8.3 Standard of appearance inspection OLED

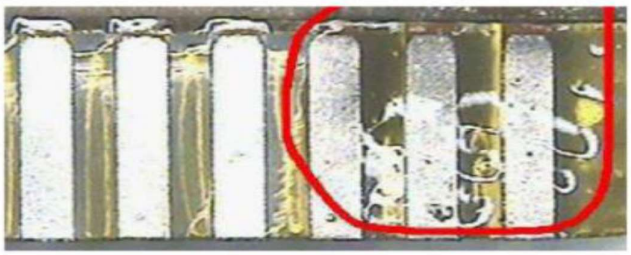
Partition	AQL	Definition
Major	0.65	Defects in Pattern Check (Display On)
Minor	1.0	Defects in Cosmetic Check (Display Off)

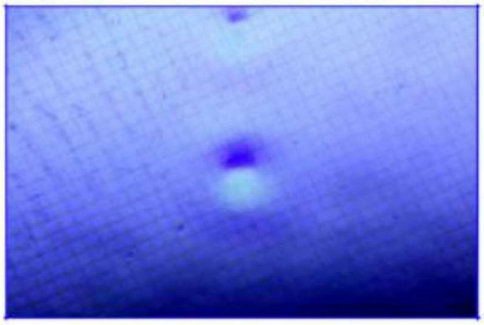
Check Item	Classification	Criteria
Panel General Chipping	Minor	X > 6 mm (Along with Edge) Y > 1 mm (Perpendicular to edge)  

Check Item	Classification	Criteria
Panel Crack	Minor	Any crack is not allowable. 
Cupper Exposed (Even Pin or Film)	Minor	Not Allowable by Naked Eye Inspection
Film or Trace Damage	Minor	
Terminal Lead Twist	Minor	Not Allowable 

Terminal Lead Broken	Minor	Not Allowable 
Terminal Lead Prober Mark	Acceptable	

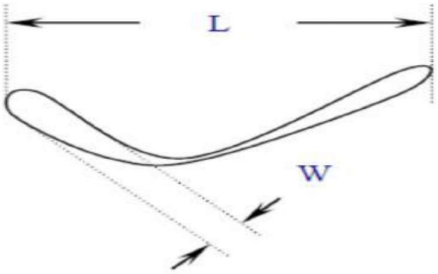
Check Item	Classification	Criteria
Terminal Lead Bent (Not Twist or Broken)	Minor	NG if any bent lead cause lead shorting. 
	Minor	NG for horizontally bent lead more than 50% of its width. 

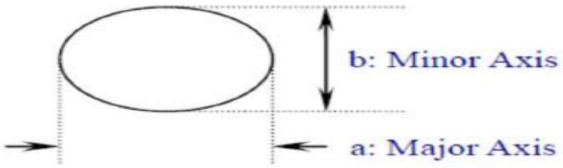
Glue or Contamination on Pin (Couldn't Be Removed by Alcohol)	Minor	
Ink Marking on Back Side of panel (Exclude on Film)	Acceptable	Ignore for Any

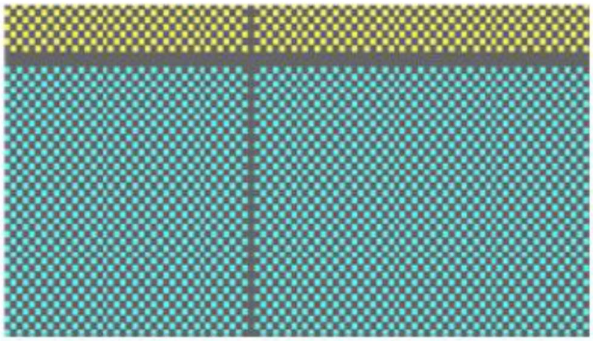
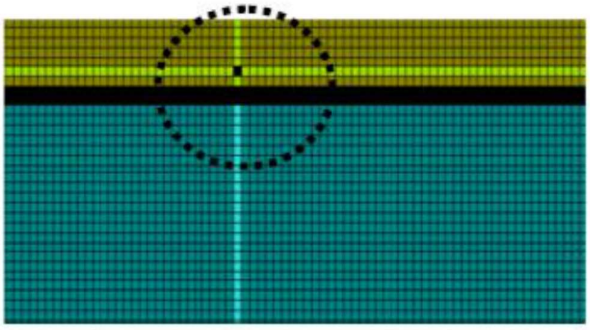
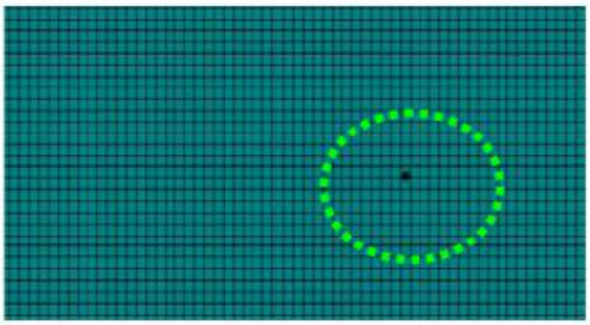
Check Item	Classification	Criteria
Any Dirt & Scratch on Polarizer's Protective Film	Acceptable	Ignore for not Affect the Polarizer
Scratches, Fiber, Line-Shape Defect (On Polarizer)	Minor	$W \le 0.1$ Ignore $W > 0.1, L \le 2$ $n \le 1$ $L > 2$ $n = 0$
Dirt, Black Spot, Foreign Material, (On Polarizer)	Minor	$\Phi \le 0.1$ Ignore $0.1 < \Phi \le 0.25$ $n \le 1$ $0.25 < \Phi$ $n = 0$
Dent, Bubbles, White spot (Any Transparent Spot on Polarizer)	Minor	$\Phi \le 0.5$ ➔ Ignore if no Influence on Display $0.5 < \Phi$ $n = 0$ 
Fingerprint, Flow Mark (On Polarizer)	Minor	Not Allowable

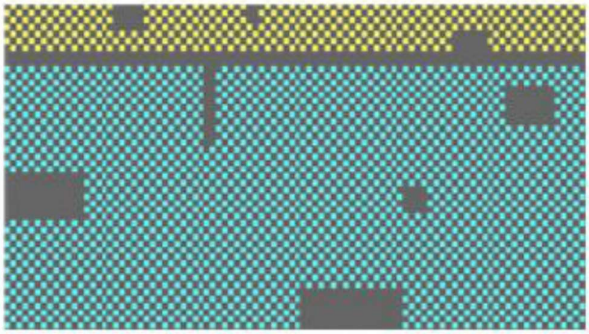
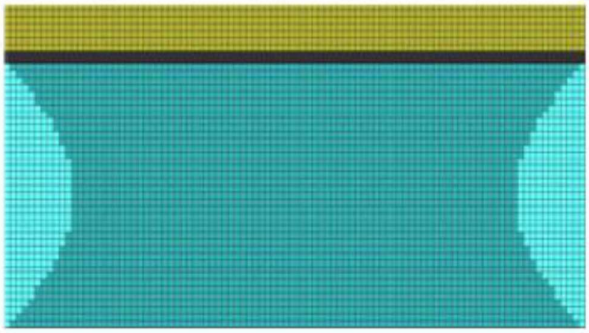
* Protective film should not be tear off when cosmetic check.

** Definition of W & L & Φ (Unit: mm): $\Phi = (a + b) / 2$





Check Item	Classification	Criteria
No Display	Major	
Flicker	Major	Not Allowable
Missing Line	Major	
Pixel Short	Major	
Darker Pixel	Major	

Wrong Display	Major	
Un-uniform	Major	

Item	Condition	Inspection after test
High Temperature Operating	70℃,96H	Inspection after 2~4hours storage at room temperature, the sample shall be free from defects: 1.Air bubble in the LCD; 2.Non-display; 3.Missing segments/line; 4.Glass crack; 5.Current IDD is twice higher than initial value.
Low Temperature Operating	-20℃, 96HR	
High Temperature Storage	80℃, 96HR	
Low Temperature Storage	-30℃, 96HR	
High Temperature & High Humidity Operating	+60℃, 90% RH ,96 hours.	
Thermal Shock (Non-operation)	-20℃,30 min ↔ 70℃,30 min, Change time:5min 20CYC.	
ESD test	C=150pF, R=330,5points/panel Air:±8KV, 5times; Contact:±6KV, 5 times; (Environment: 15℃~35℃, 30%~60%).	
Vibration (Non-operation)	Frequency range:10~55Hz, Stroke:1.5mm Sweep:10Hz~55Hz~10Hz 2 hours for each direction of X.Y.Z. (6 hours for total) (Package condition).	
Box Drop Test	1 Corner 3 Edges 6 faces,80㎝(MEDIUM BOX)	

9. Reliability Test Result

Remark:

1.The test samples should be applied to only one test item.

2.Sample size for each test item is 5~10pcs.

3.For Damp Proof Test, Pure water(Resistance > 10MΩ) should be used.

4.In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part.

5.Failure Judgment Criterion: Basic Specification, Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.

10. Cautions and Handling Precautions

10.1 Handling and Operating the Module.

(1) When the module is assembled, it should be attached to the system firmly.

Do not warp or twist the module during assembly work.

(2) Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.

(3) Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.

(4) Do not allow drops of water or chemicals to remain on the display surface.

If you have the droplets for a long time, staining and discoloration may occur.

(5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.

(6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane.

Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.

(8) Protect the module from static; it may cause damage to the CMOS ICs.

(9) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.

(10) Do not disassemble the module.

(11) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.

(12) Pins of I/F connector shall not be touched directly with bare hands.

(13) Do not connect, disconnect the module in the “Power ON” condition.

(14) Power supply should always be turned on/off by the item 6.1 Power On Sequence &6.2 Power Off Sequence

10.2 Storage and Transportation.

(1) Do not leave the panel in high temperature, and high humidity for a long time.

It is highly recommended to store the module with temperature from 0 to 35 ℃ and relative humidity of less than 70%

(2) Do not store the TFT-LCD module in direct sunlight.

(3) The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
(4) It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module.
In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.
(5) This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.

11. Packing

----TBD----------