SPECIFICATION
FOR
OLED Module
BLKD013LEDN001

MODULE:	
CUSTOMER:	

REV	DESCRIPTION	DATE
1.0	FIRST ISSUE	2018.03.07

	INITIAL	DATE
PREPARED BY		
CHECKED BY		
APPROVED BY		

CUSTOMER	INITIAL	DATE
APPROVED BY		

Revision History

Date	Rev. No.	Page	Summary
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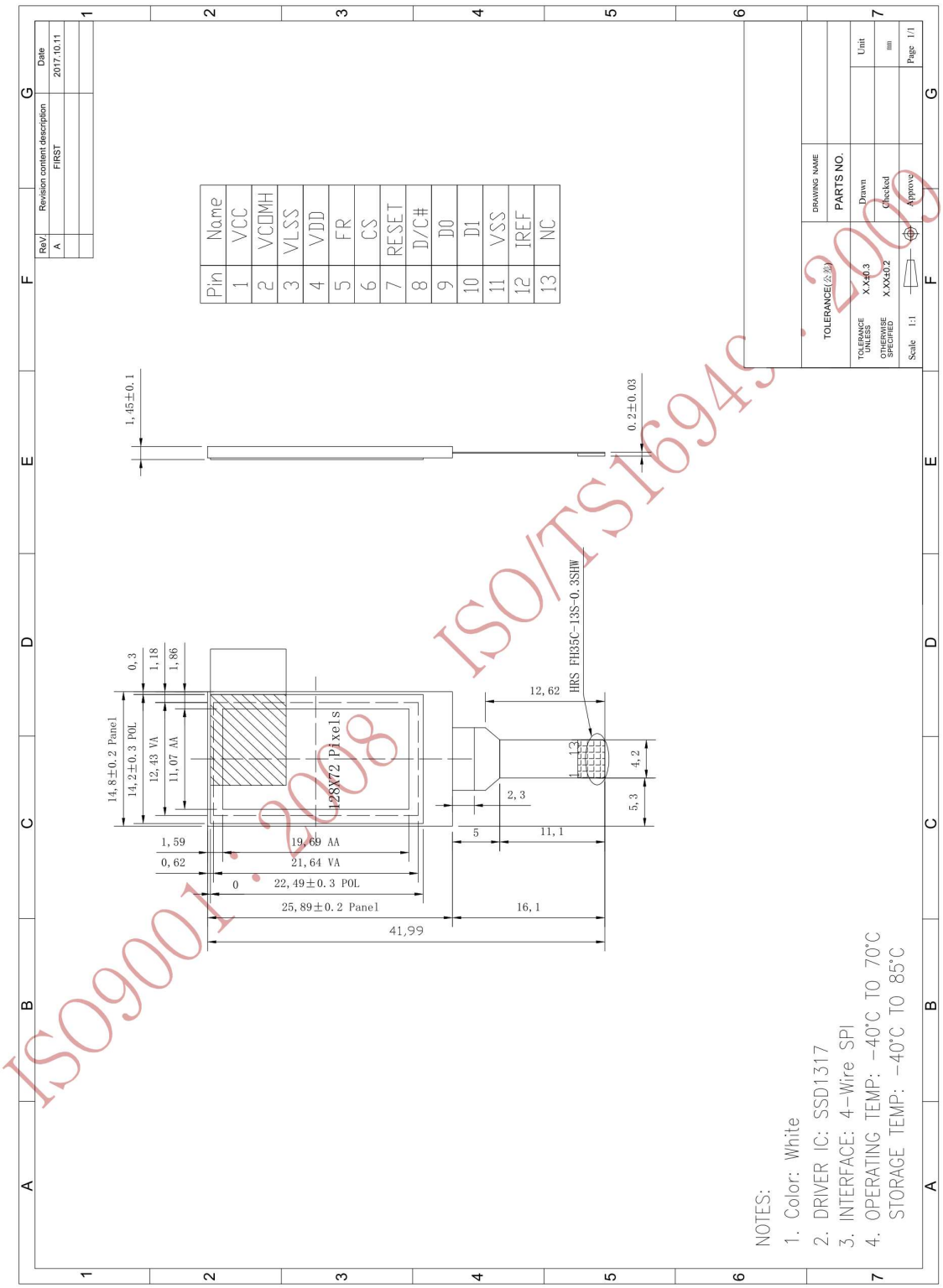
1. Basic Specifications

General Information Items	Specification	Unit	Note
	Main Panel		
OLED Display area(AA)	11.07(H) *19.69(V) (1.3 inch)	mm	-
Display color	Monochrome (White)	colors	-
Drive Duty	1/72 Duty	-	-
Number of pixels	72(H)*128(V)	dots	-
Pixel pitch	0.154 (H) x 0.154 (V)	mm	-
OLED Controller IC	SSD1317	-	-
Display mode	Passive Matrix	-	-
Operating temperature	-40～+70	℃	-
Storage temperature	-40～+85	℃	-

*** Mechanical Information**

Item		Min.	Typ.	Max.	Unit	Note
Module size	Horizontal(H)		14.8		mm	-
	Vertical(V)		25.89		mm	-
	Depth(D)		1.45		mm	-
Weight			TBD		g	-

2. Outline dimension



3. Input terminal Pin Assignment

3.1 OLED

NO.	SYMBOL	DISCRIPTION	I/O
1	VCC	Power Supply for OEL Panel This is the most positive voltage supply pin of the chip. It must be supplied externally.	P
2	VCOMH	Voltage Output High Level for COM Signal This pin is the input pin for the voltage output high level for COM signals. A capacitor should be connected between this pin and VSS.	P
3	VLSS	Ground of Analog Circuit These are the analog ground pins. They should be connected to VSS externally.	P
4	VDD	Power Supply for Logic This is a voltage supply pin. It must be connected to external source.	P
5	FR	Frame Frequency Triggering Signal This pin output RAM write synchronization signal. Proper timing between MCU data writing and frame display timing can be prevent tearing effect. It should be kept NC if it is not used.	P
6	CS#	Chip Select This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.	I/O
7	RESET	Power Reset for Controller and Driver This pin is reset signal input. When the pin is low, initialization of the chip is executed. Keep this pin pull high during normal operation.	I
8	D/C#	Data/Command Control This pin is Data/Command control pin. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams. When the pin is pulled high and serial interface mode is selected, the data at SDIN is treated as data. When it is pulled low, the data at SDIN will be transferred to the command register.	I
9	D0	Serial Clock Input Signal The transmission of information in the bus is following a clock signal. Each transmission of data bit is taken place during a single clock period of	I

		this pin.	
10	D1	Serial Data Input Signal This pin acts as a communication channel. The input data through SDIN are latched at the rising edge of SCLK in the sequence of MSB first and converted to 8-bit parallel data and handled at the rising edge of last serial clock.	
11	VSS	Ground of Logic Circuit This is a ground pin. It also acts as a reference for the logic pins. It must be connected to external ground.	I
12	IREF	Current Reference for Brightness Adjustment This pin is segment current reference pin. A resistor should be connected between this pin and VSS. Set the current at 18.75mA maximum. When internal IREF is used, this pin should be kept NC.	I
13	N.C.	Reserved Pin The N.C. pin between function pins is reserved for compatible and flexible design.	I

4. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage for Logic	V_{DD}	-0.3	4	V	1, 2
Supply Voltage for Display	V_{CC}	0	15	V	1, 2
Operating Temperature	T_{OP}	-40	70	°C	
Storage Temperature	T_{STG}	-40	85	°C	3
Life Time		5000	-	hour	4

Note 1: All the above voltages are on the basis of “VSS = 0V”.

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. “Optics & Electrical Characteristics”. If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

Note 3: The defined temperature ranges do not include the polarizer. The maximum withstood temperature of the polarizer should be 80°C.

Note 4: VCC = 12.0V, Ta = 25°C, 50% Checkerboard. Software configuration follows Section 4.5 Initialization. End of lifetime is specified as 50% of initial brightness reached. The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

5. Optics & Electrical Characteristics

5.1 Optics Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Brightness	L_{br}	Note 5	80	100	-	cd/m^2
C.I.E. (White)	(x) (y)	C.I.E. 1931	0.28 0.30	0.31 0.33	0.34 0.36	
Dark Room Contrast	CR		-	>10,000:1	-	
Viewing Angle			-	Free	-	degree

* Optical measurement taken at V_{DD} = 3.0V, V_{CC} = 12.0V.
Software configuration follows Section 4.5 Initialization.

5.2 DC Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage for Logic	VDD		1.65	2.8	3.3	V
Supply Voltage for Display	VCC	Note 5	11.5	12	12.5	V
High Level Input	VIH		0.8×VDD		VDD	V
Low Level Input	VIL		0		0.2×VDD	V
High Level Output	VOH	IOUT = 100μA, 3.3MHz	0.9×VDD		VDD	V
Low Level Output	VOL	IOUT = 100μA, 3.3MHz	0		0.1×VDD	V
Operating Current for VDD	IDD			180	300	uA
Operating Current for VCC	ICC	Note 6		12.3	15.4	mA
		Note 7		19.7	24.6	mA
		Note 8		38.3	47.9	mA
Sleep Mode Current for VDD	IDD, SLEEP				10	uA
Sleep Mode Current for VCC	IDD, SLEEP				10	uA

Note 5: Brightness (Lbr) and Supply Voltage for Display (VCC) are subject to the change of the panel characteristics and the customer's request.

Note 6: VDD = 3.0V, VCC = 12.0V, 30% Display Area Turn on.

Note 7: VDD = 3.0V, VCC = 12.0V, 50% Display Area Turn on.

Note 8: VDD = 3.0V, VCC = 12.0V, 100% Display Area Turn on.

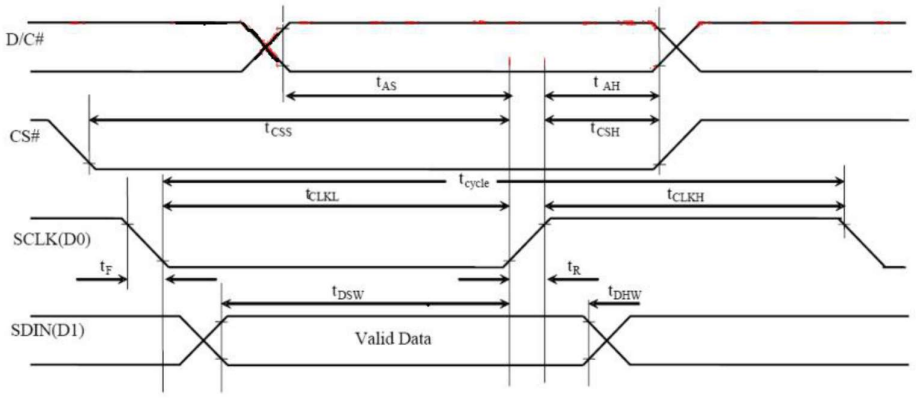
* Software configuration follows Section 4.5 Initialization.

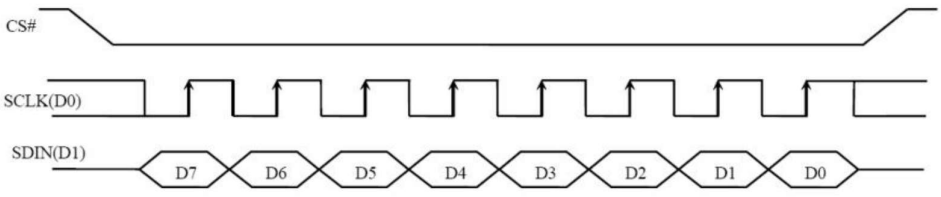
5.3 AC Characteristics

5.3.1 Serial Interface Timing Characteristics: (4-wire SPI)

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	ns
t_{AS}	Address Setup Time	15	-	ns
t_{AH}	Address Hold Time	15	-	ns
t_{CSS}	Chip Select Setup Time	20	-	ns
t_{CSH}	Chip Select Hold Time	50	-	ns
t_{DSW}	Write Data Setup Time	20	-	ns
t_{DHW}	Write Data Hold Time	20	-	ns
t_{CLKL}	Clock Low Time	50	-	ns
t_{CLKH}	Clock High Time	50	-	ns
t_R	Rise Time	-	40	ns
t_F	Fall Time	-	40	ns

* (V_{DD} - V_{SS} = 1.65V to 3.3V, T_a = 25°C)





6. Functional Specification

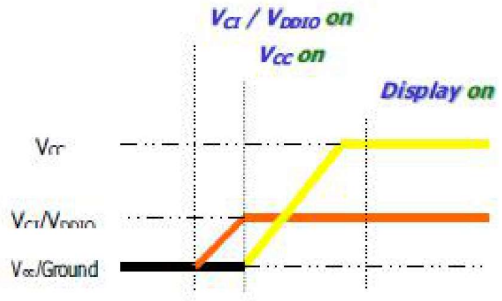
Refer to the Technical Manual for the SSD1317

6.1 Power down and Power up Sequence

To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.

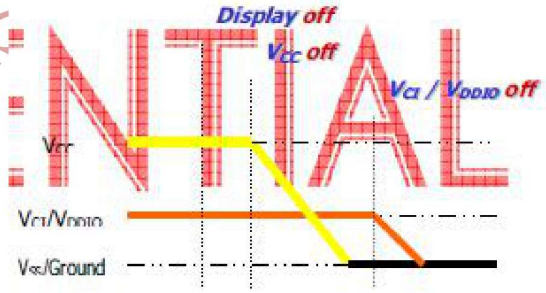
6.1.1 Power up Sequence:

1. Power up VDD
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up VCC
6. Delay 200ms
   (When VCC is stable)
7. Send Display on command



6.1.2 Power down Sequence:

1. Send Display off command
2. Power down VCC
3. Delay 100ms
   (When VCC is reach 0 and panel is completely discharges)
4. Power down VDD



Note 9:

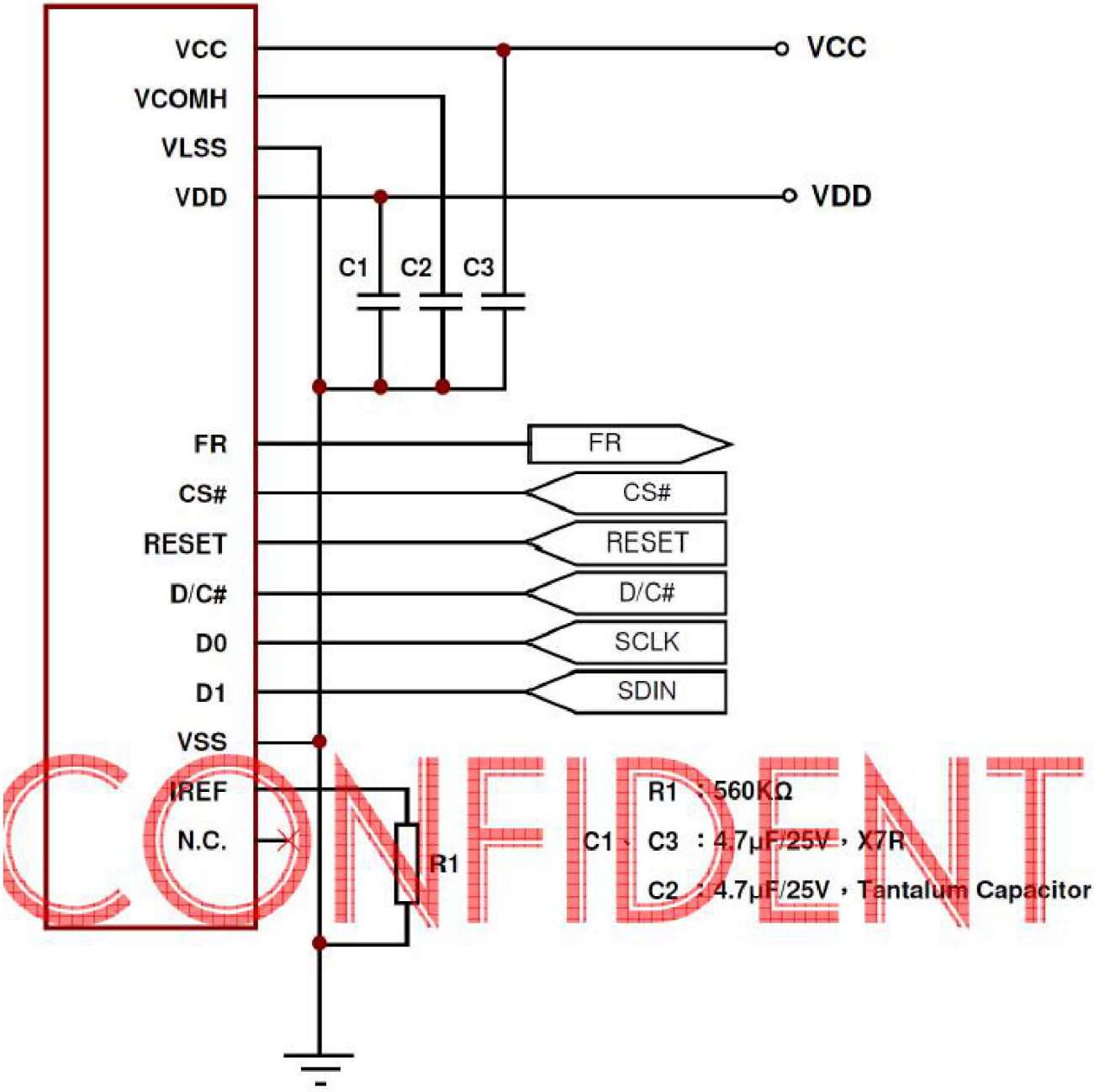
1) Since an ESD protection circuit is connected between VBDDB and VBCCB inside the driver IC, VBCCB becomes lower than VBDDB whenever VBDDB is ON and VBCCB is OFF.
2) VBCCB should be kept float (disable) when it is OFF.
3) Power Pins (VBDDB, VBCCB) can never be pulled to ground under any circumstance.
4) VBDDB should not be power down before VBCCB power down.

6.2 Reset Circuit

When RES# input is low, the chip is initialized with the following status:

1. Display is OFF
2. 128´96 Display Mode
3. Normal segment and display data column and row address mapping (SEG0 mapped to column address 00h and COM0 mapped to row address 00h)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Contrast control register is set at 7Fh
9. Normal display mode (Equivalent to A4h command)

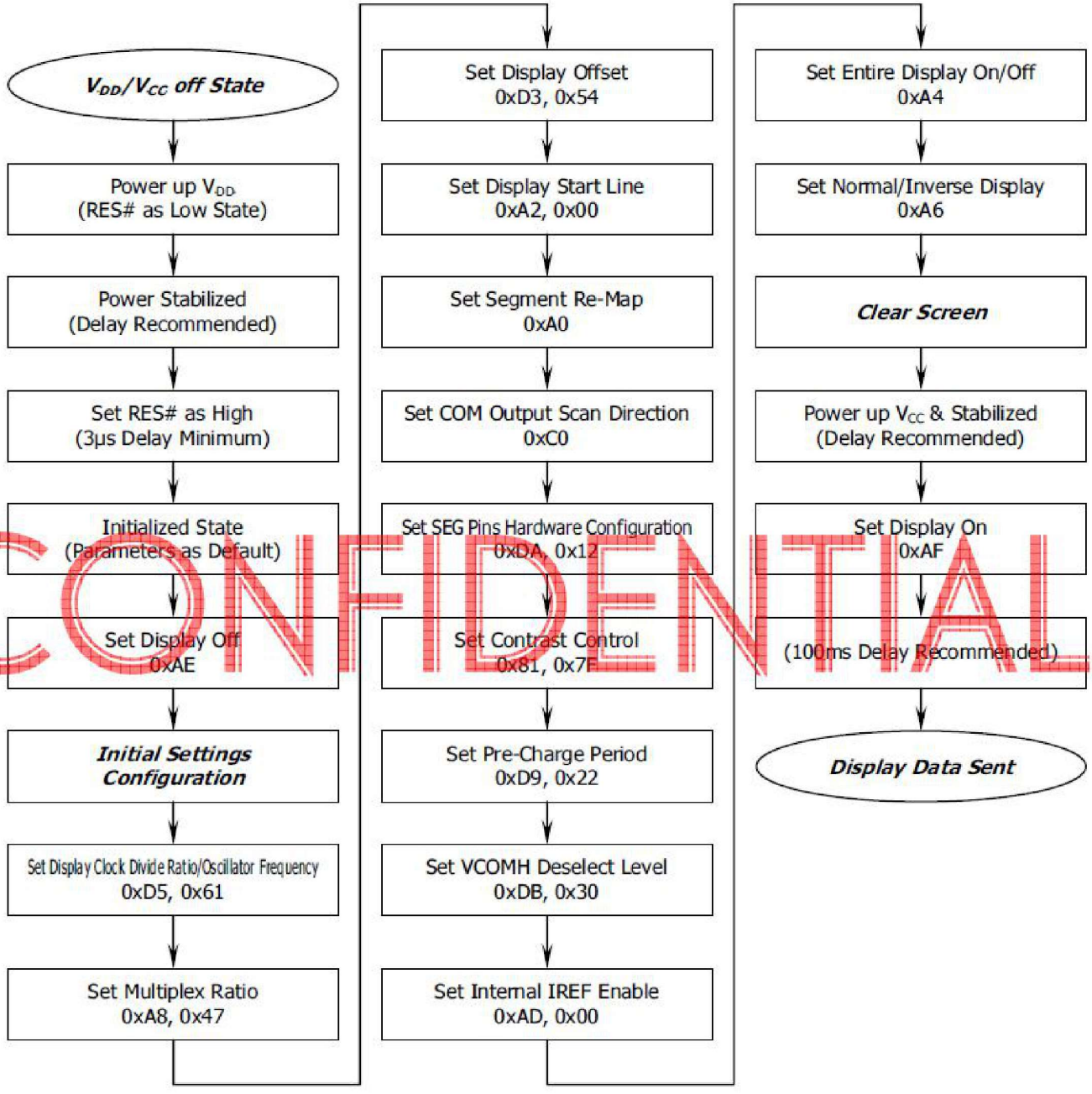
6.3 Application circuit



7. Actual Application Example

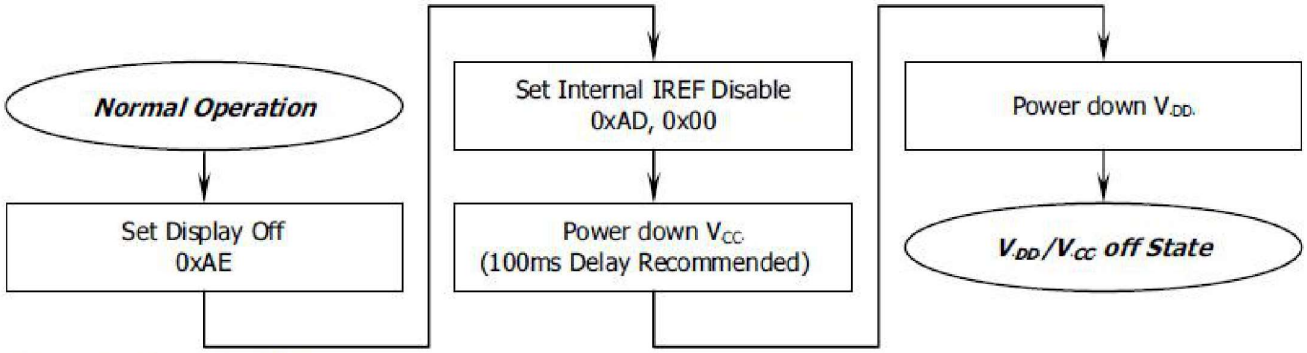
Command usage and explanation of an actual example

<Power up Sequence>

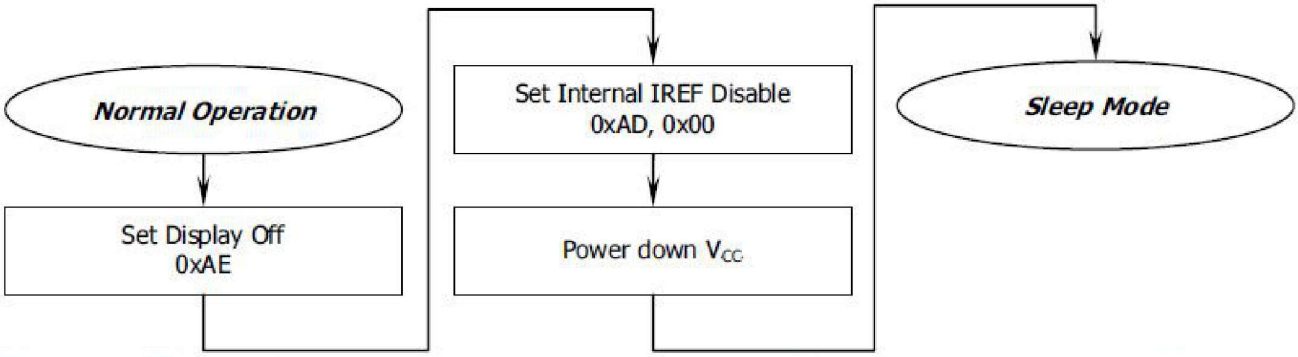


If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

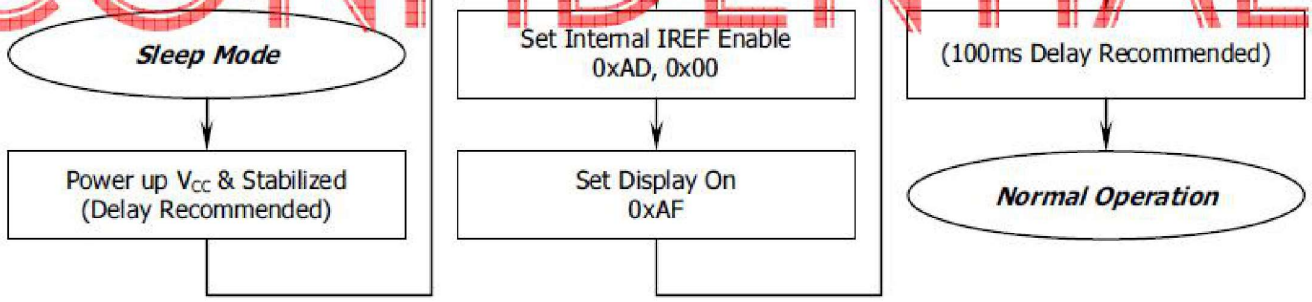
<Power down Sequence>



<Entering Sleep Mode>



<Exiting Sleep Mode>



8. Appearance Inspection

8.1 Appearance Condition

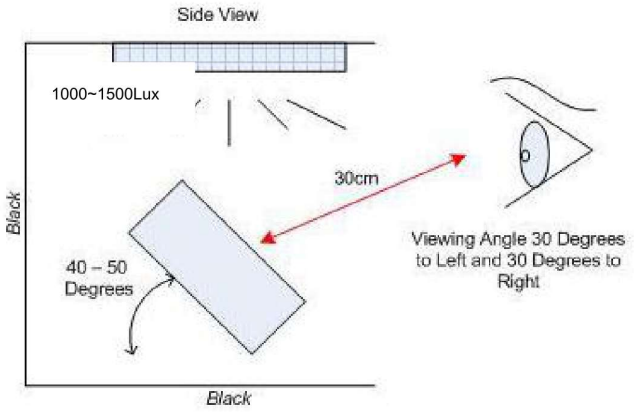
8.1.1 Environment: 22 ± 3ºC, Inspection distance：30 ± 5cm.

8.1.2 Rotation angle : ±45º

8.1.3 Lighting illumination：1000~1200Lux

8.1.4 Background：Black

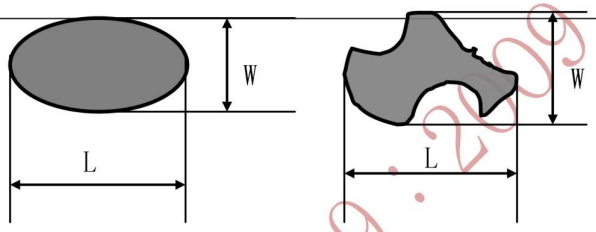
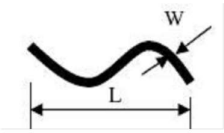
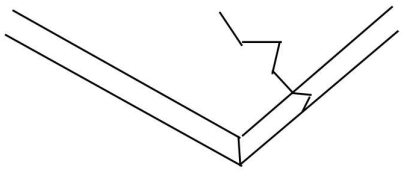
8.1.5 Inspection time：30s each piece



Remark:

Inspection criterions are valid for the complete Module (CTP + OLED) including reverse Printing and Logo printing

8.2 Appearance Criterion

No.	Item	Criteria for defects (Unit: mm)
1	**Dot Defects (Particle/Dirt/ Dent/Bubble)**	1、D≤0.2 mm; Ignore 2、0.2 mm＜D≤0.5 mm,N≤5，Distance ≥70mm D≥5mm is not allowed. D=(W + L)/2 
2	**Line type Defects (S cratch/Dirt/Particle)**	1、W≤0.063mm , Ignore 2、0.063mm＜W≤0.1mm,L≤8mm(length in total),N≤4; Distance ≥70mm Other is not allowed. 
3	**Edge Chipping**	Allow: Edge Chips/chamfered Edges: Corner: D≤ 0.3mm Polished edges: D≤ 0.25mm, Ignore; 0.25mm<D≤0.4 mm,N≤5 per edge allowed Heat marks on polished edged: Width max. 0.15mm, length max.4.0mm. Max.2 per 500mm,min. distance>40mm
4	**Glass Crack**	Crack is potential to enlarge, any type is not allowed. 
5	No visible color change when compared with the approved sample	

Remark	For No.1.2 and 2.2 8 defects in total are allowed A concentration of defects is not allowed, definition in accordance with DIN ISO 10110-7

9. Reliability Test Result

Item	Condition	Inspection after test
High Temperature Operating	70℃,96H	Inspection after 2~4hours storage at room temperature, the sample shall be free from defects: 1.Air bubble in the LCD; 2.Non-display; 3.Missing segments/line; 4.Glass crack; 5.Current IDD is twice higher than initial value.
Low Temperature Operating	-40℃, 96HR	
High Temperature Storage	85℃, 96HR	
Low Temperature Storage	-40℃, 96HR	
High Temperature & High Humidity Storage	+60℃, 90% RH ,96 hours.	
Thermal Shock (Non-operation)	-40℃,30 min ↔ 85℃,30 min, Change time:5min 20CYC.	
ESD test	C=150pF, R=330,5points/panel Air:±8KV, 5times; Contact:±6KV, 5 times; (Environment: 15℃~35℃, 30%~60%).	
Vibration (Non-operation)	Frequency range:10~55Hz, Stroke:1.5mm Sweep:10Hz~55Hz~10Hz 2 hours for each direction of X.Y.Z. (6 hours for total) (Package condition).	
Box Drop Test	1 Corner 3 Edges 6 faces,80㎝(MEDIUM BOX)	

Remark:

1.The test samples should be applied to only one test item.

2.Sample size for each test item is 5~10pcs.

3.For Damp Proof Test, Pure water(Resistance＞10MΩ) should be used.

4.In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part.

5.Failure Judgment Criterion: Basic Specification, Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.

10. Cautions and Handling Precautions

10.1 Handling and Operating the Module

(1) When the module is assembled, it should be attached to the system firmly.
Do not warp or twist the module during assembly work.
(2) Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
(3) Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
(4) Do not allow drops of water or chemicals to remain on the display surface.
If you have the droplets for a long time, staining and discoloration may occur.
(5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
(6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane.
Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
(8) Protect the module from static; it may cause damage to the CMOS ICs.
(9) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
(10) Do not disassemble the module.
(11) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
(12) Pins of I/F connector shall not be touched directly with bare hands.
(13) Do not connect, disconnect the module in the “Power ON” condition.
(14) Power supply should always be turned on/off by the item 6.1 Power On Sequence &6.2 Power Off Sequence

10.2 Storage and Transportation.

(1) Do not leave the panel in high temperature, and high humidity for a long time.
It is highly recommended to store the module with temperature from 0 to 35 ℃ and relative humidity of less than 70%
(2) Do not store the TFT-LCD module in direct sunlight.
(3) The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
(4) It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module.
In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.
(5) This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.

11. Packing

----TBD----------