SPECIFICATION

FOR

OLED Module

BLKD154OLEDN001

MODULE:	
CUSTOMER:	

REV	DESCRIPTION	DATE
1.0	FIRST ISSUE	2018.03.016

	INITIAL	DATE
PREPARED BY		
CHECKED BY		
APPROVED BY		

CUSTOMER	INITIAL	DATE
APPROVED BY		

Revision History

Date	Rev. No.	Page	Summary
2018.03.16	V1.0	ALL	FIRST ISSUE

Contents

1. Basic Specifications

General Information Items	Specification	Unit	Note
	Main Panel		
OLED Display area(AA)	35.05(H) *17.52(V) (1.54 inch)	mm	-
Display color	Monochrome (White)	colors	-
Drive Duty	1/64 Duty	-	-
Number of pixels	128(H)*64(V)	dots	-
Pixel pitch	0.274 (H) x 0.274 (V)	mm	-
OLED Controller IC	SSD1309	-	-
Display mode	Passive Matrix	-	-
Operating temperature	-40～+70	℃	-
Storage temperature	-40～+85	℃	-

* Mechanical Information

Item		Min.	Typ.	Max.	Unit	Note
Module size	Horizontal(H)		42.04		mm	-
	Vertical(V)		27.22		mm	-
	Depth(D)		1.45		mm	-
Weight			TBD		g	-

2. Outline dimension

FRONT   SIDE   BACK

Active Area 1.54"
128*64 Pixels

Pin	Symbol
1	N.C. (GND)
2	VLSS
3	VSS
4	N.C.
5	VDD
6	BS1
7	BS2
8	CS#
9	RES#
10	D/C#
11	R/W#
12	E/RD#
13	D0
14	D1
15	D2
16	D3
17	D4
18	D5
19	D6
20	D7
21	IREF
22	VCOMH
23	VCC
24	N.C.(GND)

42,04±0.2(Panel Size)
41,04±0.2(Polarizer)
37,05(V/A)
35,05(A/A)
15,00
8,00
0,50
2,49
3,49
3,00   17,52(A/A)
2,00   19,52(V/A)
0,50   21,80±0.3(Polarizer)
23,03±0.2(Cap Size)
27,22±0.2(Panel Size)
40,22±0.3

1,45±0.1
Protective Tape t=0.15mm Max
Polarizer t=0.2mm
Protective Tape(11,84*0.05mm)
Glue
Mated Height 1.5mm
Contact Side
0,30±0.03
1,61
4,50±0.3(Siffener)

2*⌀0,60
2-Copper pad(1.2*1.9)
5,00
10,00±0.2
9,60±0.2(Siffener)
11,20±0.2
13,60±0.2
0,15
4,40
16,02
0,68±0.2
2,28±0.3
3,88±0.2
3,96
10,72
6,50±0.2
13,00±0.3

Notes:
1. Color: White
2. Driver IC: SSD1309
3. FPC Number:TBD
4. Board to Board Connector:Panasonic AXK824145(Header),Mated Height 1.5mm
5. Interface:
   8-bit 68XX/80XX Parallel, 4-wire SPI, I2C
6. OPERATING TEMP: -20℃~+70℃, ≤90%RH
7. STORAGE TEMP: -30℃~+80℃, ≤90%RH
8. General Tolerance: ±0.30
9. The total thickness (1.55 Max) is without polarizer protective film & remove tape.
   The actual assembled total thickness with above materials should be 1.80 Max.

Rev	Revision content description	Date
A	FIRST	2017.10.18

DRAWING NAME
PARTS NO.
Drawn
Checked
Approve

TOLERANCE(±±) | X.X±0.3 | X.XX±0.2
TOLERANCE UNLESS OTHERWISE SPECIFIED
Scale 1:1
Unit mm
Page 1:1

3. Input terminal Pin Assignment

3.1 OLED

NO.	SYMBOL	DISCRIPTION	I/O
1	N.C.(GND)	Reserved Pin(supporting Pin) The supporting pins can reduce the influences from stresses on the function pins. These pins must be connected to external ground as the ESD protection circuit.	P
2	VLSS	Ground of Analog Circuit This is an analog ground pin. It should be connected to V SS externally.	P
3	VSS	Ground of Analog Circuit This is a ground pin. It also acts as a reference for the logic pins. It must be connected to external ground.	P
4	N.C.	Reserved Pin The N.C. pin between function pins are reserved for compatible and flexible design.	P
5	VDD	Power supply for logic Circuit This is a voltage supply pin. It must be connected to external source.	P
6	BS1	These pins are MCU interface selection input. See the following table: BS1 BS2 I 2 C 1 0	I
7	BS2	4-wire SPI 0 0 8-bit 68XX Parallel 0 1 8-bit 80XX Parallel 1 1	I
8	CS#	Chip select This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.	I
9	RES#	Power reset for controller and driver This pin is reset signal input. When the pin is low, initialization of the chip is executed. Keep this pin pull high during normal operation.	I
10	D/C#	Data/command control This pin is Data/Command control pin. When the pin is pulled high, the input at D7~D0 will be interpreted as display data. When the pin is pulled low, the input at D7~D0 will be transferred to the command register.	I

		When the pin is pulled high and serial interface mode is selected, the data at SDIN will be interpreted as data. When it is pulled low, the data at SDIN will be transferred to the command register. In I 2 C mode, this pin acts as SA0 for slave address selection. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.	
11	R/W#	Read/write select or write This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Pull this pin to "High" for read mode and pull it to "Low" for write mode. When 80XX interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the CS# is pulled low. When serial or I2C mode is selected, this pin must be connected to Vss .	I
12	E/RD#	Read/write Enable or Read This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the CS# is pulled low. When connecting to an 80XX-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and CS# is pulled low. When serial or I 2 C mode is selected, this pin must be connected to Vss.	I
13-20	D0-D7	Reserved Pin The N.C. pin between function pins is reserved for compatible and flexible design.	I/O
14	IREF	Current reference for brightness adjust This pin is segment current reference pin. A resistor should be connected between this pin and V SS . Set the current at 10 μ A maximum.	I

15	VCOMH	This pin is the input pin for the voltage output high level for COM signals. A capacitor should be connected between this pin and V S	O
16	VCC	This is the most positive voltage supply pin of the chip. It must be supplied externally.	P
17	N.C.(GND)	Reserved Pin(supporting Pin) The supporting pins can reduce the influences from stresses on the function pins. These pins must be connected to external ground as the ESD protection circuit.	

4. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage for Logic	V_{DD}	-0.3	4	V	1, 2
Supply Voltage for Display	V_{CC}	0	15	V	1, 2
Operating Temperature	T_{OP}	-40	70	°C	3
Storage Temperature	T_{STG}	-40	85	°C	3
Life Time (120 cd/m^2)		10,000	-	hour	4
Life Time (80 cd/m^2)		30,000	-	hour	4
Life Time (60 cd/m^2)		50,000	-	hour	4

Note 1: All the above voltages are on the basis of "V SS = 0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. "Optics & Electrical Characteristics". If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

Note 3: The defined temperature ranges do not include the polarizer. The maximum withstood temperature of the polarizer should be 80° C.

Note 4: V CC = 12.5V, T a = 25° C, 50% Checkerboard.
Software configuration follows Section 4.4 Initialization.
End of lifetime is specified as 50% of initial brightness reached. The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

5. Optics & Electrical Characteristics

5.1 Optics Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Brightness	L_{br}	Note 5	100	120	-	cd/m²
C.I.E. (White)	(x) (y)	C.I.E. 1931	0.25 0.27	0.29 0.31	0.33 0.35	
Dark Room Contrast	CR		-	>10,000:1	-	
Viewing Angle			-	Free	-	degree

* Optical measurement taken at V_{DD} = 2.8V, V_{CC} = 12.5V.
  Software configuration follows Section 4.4 Initialization.

5.2 DC Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage for Logic	V_{DD}		1.65	2.8	3.3	V
Supply Voltage for Display	V_{CC}	Note 5	12	12.5	13.0	V
High Level Input	V_{IH}	I_{OUT} = 100μA, 3.3MHz	0.8×V_{DD}		V_{DD}	V
Low Level Input	V_{IL}	I_{OUT} = 100μA, 3.3MHz	0		0.2×V_{DD}	V
High Level Output	V_{OH}	I_{OUT} = 100μA, 3.3MHz	0.9×V_{DD}		V_{DD}	V
Low Level Output	V_{OL}	I_{OUT} = 100μA, 3.3MHz	0		0.1×V_{DD}	V
Operating Current for VDD	I_{DD}			180	300	uA
Operating Current for VCC	I_{CC}	Note 6		12.7	15.9	mA
		Note 7		20.5	25.6	mA
		Note 8		35.8	44.8	mA
Sleep Mode Current for VDD	$I_{DD, SLEEP}$			1	5	uA
Sleep Mode Current for VCC	$I_{DD, SLEEP}$			2	10	uA

Note 5: Brightness (L br) and Supply Voltage for Display (V CC) are subject to the change of the panel characteristics and the customer's request.

Note 6: V DD = 2.8V, V CC = 12.5V, 30% Display Area Turn on.

Note 7: V DD = 2.8V, V CC = 12.5V, 50% Display Area Turn on.

Note 8: V DD = 2.8V, V CC = 12.5V, 100% Display Area Turn on.

* Software configuration follows Section 4.4 Initialization.

5.3 AC Characteristics

5.3.1 68XX-Series MPU Parallel Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	20	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DW}	Data Write Time	80	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	20	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (Read)	120	-	ns
	Chip Select Low Pulse width (Write)	60		
PW_{CSH}	Chip Select High Pulse Width (Read)	60	-	ns
	Chip Select High Pulse Width (Write)	60		
t_R	Rise Time	-	40	ns
t_F	Fall Time	-	40	ns

* ($V_{DD} - V_{SS}$ = 1.65V to 3.3V, T_a = 25°C)
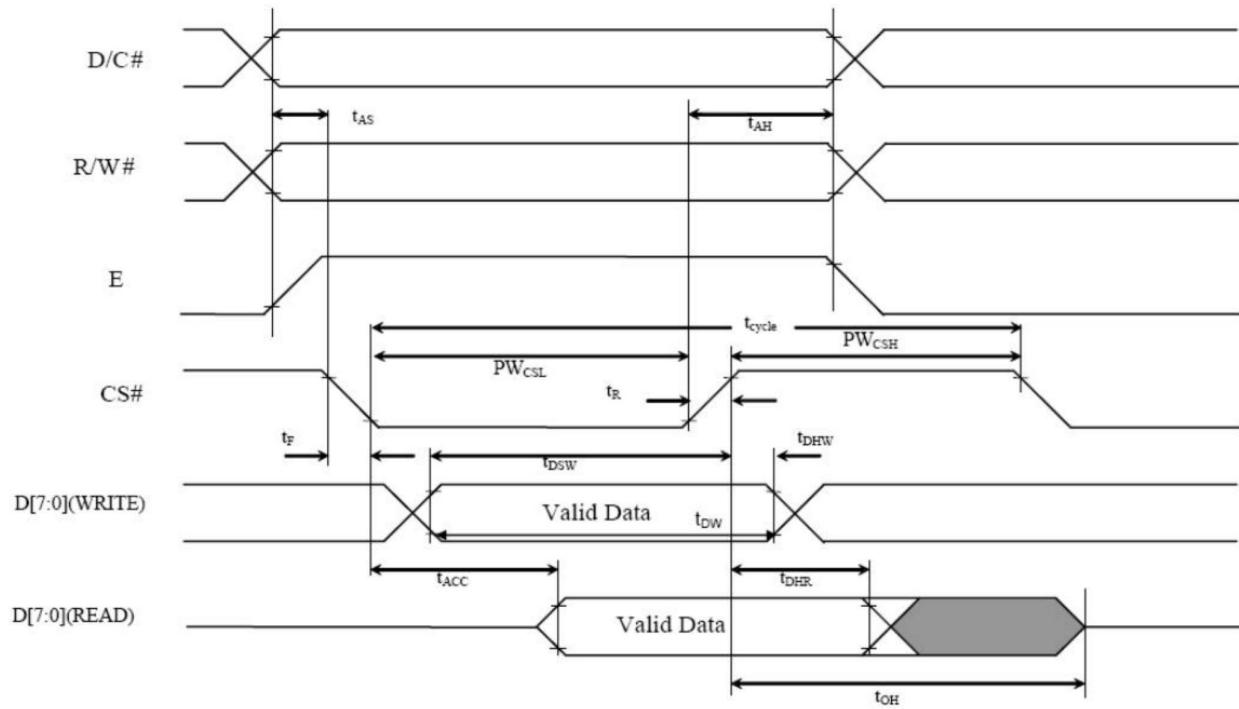
5.3.2 80XX-Series MPU Parallel Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	20	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DW}	Data Write Time	70	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	15	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
t_{PWLR}	Read Low Time	120	-	ns
t_{PWLW}	Write Low Time	60	-	ns
t_{PWHR}	Read High Time	60	-	ns
t_{PWHW}	Write High Time	60	-	ns
t_{CS}	Chip Select Setup Time	0	-	ns
t_{CSH}	Chip Select Hold Time to Read Signal	0	-	ns
t_{CSF}	Chip Select Hold Time	20	-	ns
t_R	Rise Time	-	40	ns
t_F	Fall Time	-	40	ns

* ($V_{DD} - V_{SS}$ = 1.65V to 3.5V, T_a = 25°C)

(*Read Timing*)
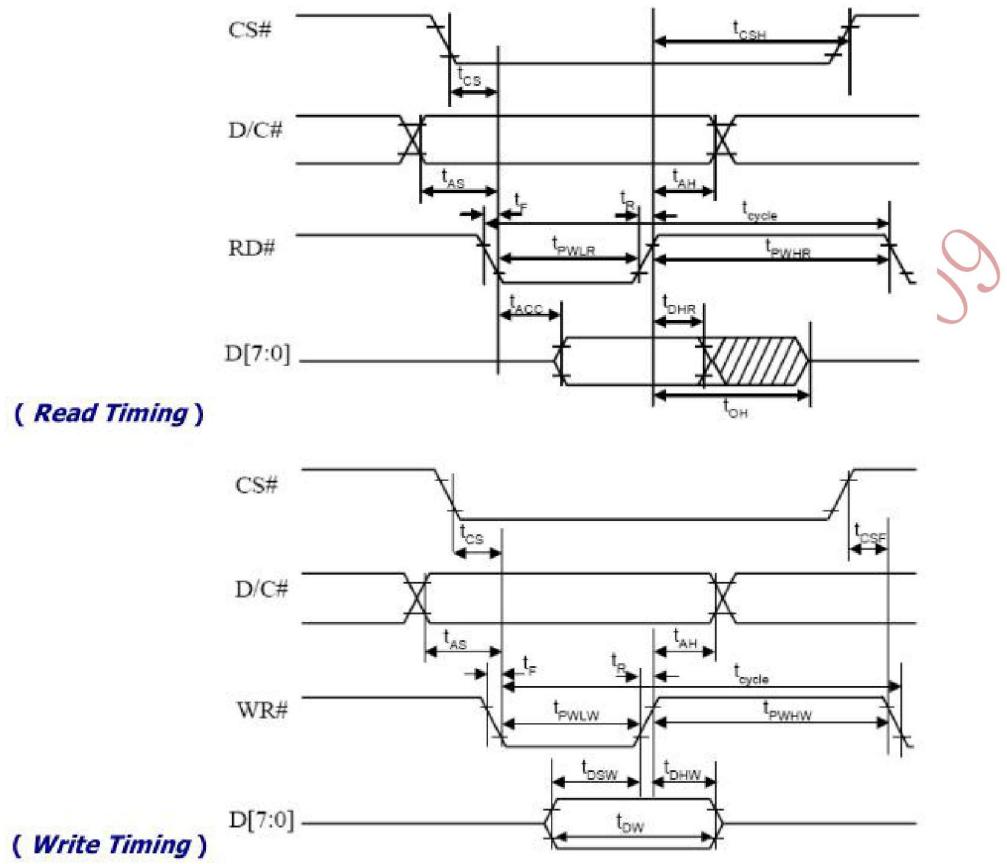
(*Write Timing*)

5.3.3 Serial Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	ns
t_{AS}	Address Setup Time	15	-	ns
t_{AH}	Address Hold Time	15	-	ns
t_{CSS}	Chip Select Setup Time	20	-	ns
t_{CSH}	Chip Select Hold Time	50	-	ns
t_{DW}	Data Write Time	55	-	ns
t_{DSW}	Write Data Setup Time	15	-	ns
t_{DHW}	Write Data Hold Time	15	-	ns
t_{CLKL}	Clock Low Time	50	-	ns
t_{CLKH}	Clock High Time	50	-	ns
t_R	Rise Time	-	40	ns
t_F	Fall Time	-	40	ns

* ($V_{DD} - V_{SS}$ = 1.65V to 3.5V, T_a = 25°C)
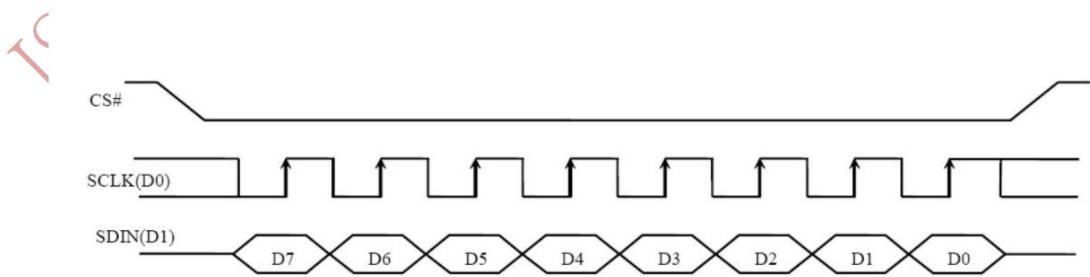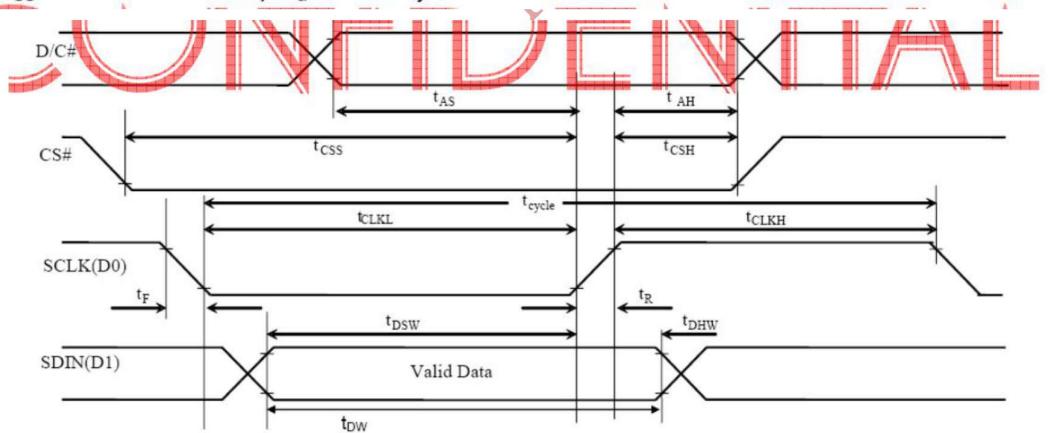
5.3.4 I 2 C Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	µs
t_{HSTART}	Start Condition Hold Time	0.6	-	µs
t_{HD}	Data Hold Time (for "SDA$_{OUT}$" Pin)	0	-	ns
	Data Hold Time (for "SDA$_{IN}$" Pin)	300		ns
t_{SD}	Data Setup Time	100	-	ns
t_{SSTART}	Start Condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	µs
t_{SSTOP}	Stop Condition Setup Time	0.6	-	µs
t_R	Rise Time for Data and Clock Pin		300	ns
t_F	Fall Time for Data and Clock Pin		300	ns
t_{IDLE}	Idle Time before a New Transmission can Start	1.3	-	µs

* (V_{DD} - V_{SS} = 1.65V to 3.5V, T_a = 25°C)
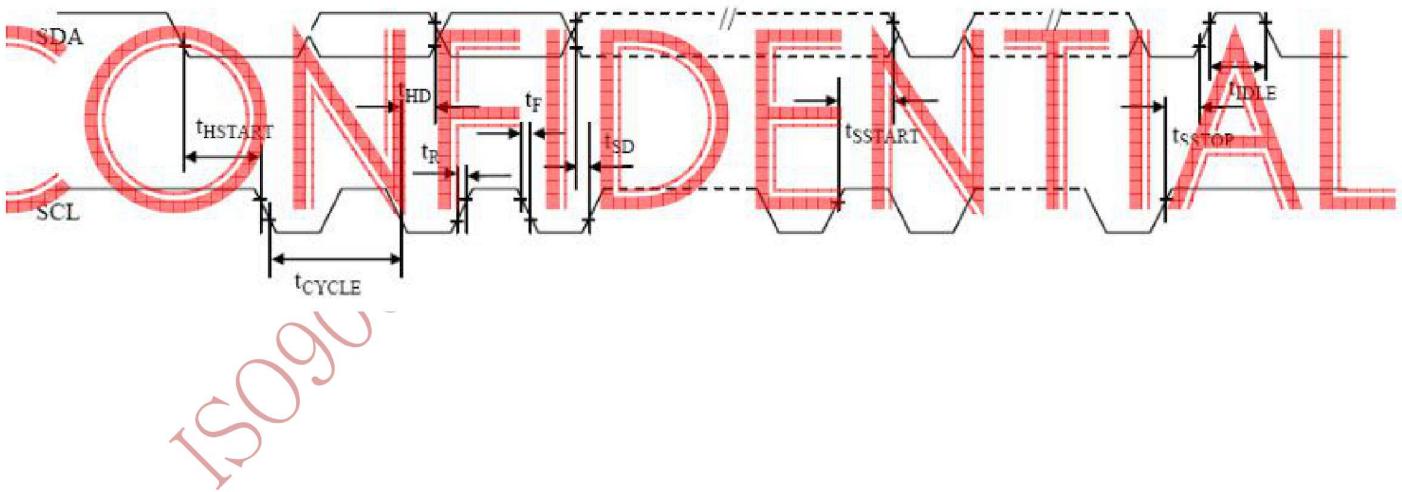
6. Functional Specification

Refer to the Technical Manual for the SSD1309

6.1 Power down and Power up Sequence

To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.

6.1.1 Power up Sequence:

1. Power up V_{DD}

2. Send Display off command

3. Initialization

4. Clear Screen

5. Power up V_{CC}

6. Delay 100ms

(When V_{CC} is stable)

7. Send Display on command
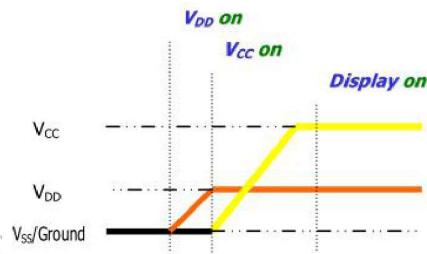
6.1.2 Power down Sequence:

1. Send Display off command

2. Power down V_{CC}

3. Delay 100ms

 (When V_{CC} is reach 0 and panel is completely discharges)

4. Power down V_{DD}
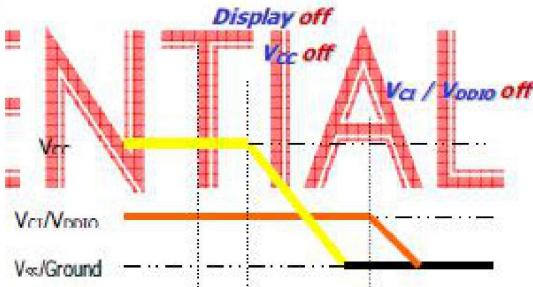
Note 9:

    1) Since an ESD protection circuit is connected between V_{DD} and V_{CC} inside the driver IC, V_{CC} becomes lower than V_{DD} whenever V_{DD} is ON and V_{CC} is OFF.

    2) V_{CC} should be kept float (disable) when it is OFF.

    3) Power Pins (V_{DD} , V_{CC}) can never be pulled to ground under any circumstance.

    4) V_{DD} should not be power down before V_{CC} power down.

6.2 Reset Circuit

When RES# input is low, the chip is initialized with the following status:

1. Display is OFF

2. 128×64 Display Mode

3. Normal segment and display data column and row address mapping (SEG0 mapped to column address 00h and COM0 mapped to row address 00h)

4. Shift register data clear in serial interface

5. Display start line is set at display RAM address 0

6. Column address counter is set at 0

7. Normal scan direction of the COM outputs

8. Contrast control register is set at 7Fh

9. Normal display mode (Equivalent to A4h command)

7. Actual Application Example

Command usage and explanation of an actual example

```
Vᴅᴅ/Vᴄᴄ off State
        ↓
Power up Vᴅᴅ
(RES# as Low State)
        ↓
Power Stabilized
(Delay Recommended)
        ↓
Set RES# as High
(3µs Delay Minimum)
        ↓
Initialized State
(Parameters as Default)
        ↓
Command Lock
0xFD, 0x12
        ↓
Set Display Off
0xAE
        ↓
Initial Settings
Configuration
        ↓
Set Display Clock Divide Ratio/Oscillator Frequency
0xD5, 0xA0
        ↓
```

```
Set Multiplex Ratio
0xA8, 0x3F
        ↓
Set Display Offset
0xD3, 0x00
        ↓
Set Display Start Line
0x40
        ↓
Set Segment Re-Map
0xA1
        ↓
Set COM Output Scan Direction
0xC8
        ↓
Set COM Pins Hardware Configuration
0xDA, 0x12
        ↓
Set Current Control
0x81, 0xCF
        ↓
Set Pre-Charge Period
0xD9, 0x22
        ↓
Set VCOMH Deselect Level
0xDB, 0x34
        ↓
```

```
Set Entire Display On/Off
0xA4
        ↓
Set Normal/Inverse Display
0xA6
        ↓
Clear Screen
        ↓
Power up Vᴄᴄ & Stabilized
(Delay Recommended)
        ↓
Set Display On
0xAF
        ↓
(100ms Delay Recommended)
        ↓
Display Data Sent
```

If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

<Power down Sequence>

```
┌─────────────────────┐      ┌──────────────────────────┐      ┌─────────────────────┐
│                     │      │   Power down V_CC        │      │                     │
│  Normal Operation   │      │ (100ms Delay Recommended)│      │  V_DD/V_CC off State│
│                     │      │                          │      │                     │
└──────────┬──────────┘      └────────────┬─────────────┘      └─────────────────────┘
           │                              │
           ▼                              ▼
┌─────────────────────┐      ┌──────────────────────────┐
│   Set Display Off   │      │    Power down V_DD       │
│       0xAE          │      │                          │
└─────────────────────┘      └──────────────────────────┘
```

<Entering Sleep Mode>

```
┌─────────────────────┐      ┌──────────────────────────┐
│                     │      │   Power down V_CC        │
│  Normal Operation   │      │                          │
└──────────┬──────────┘      └────────────┬─────────────┘
           │                              │
           ▼                              ▼
┌─────────────────────┐      ┌──────────────────────────┐
│   Set Display Off   │      │      Sleep Mode          │
│       0xAE          │      │                          │
└─────────────────────┘      └──────────────────────────┘
```

<Exiting Sleep Mode>

```
┌─────────────────────┐      ┌──────────────────────────┐      ┌─────────────────────┐
│                     │      │   Set Display On         │      │                     │
│    Sleep Mode       │      │       0xAF               │      │  Normal Operation   │
└──────────┬──────────┘      └────────────┬─────────────┘      └─────────────────────┘
           │                              │
           ▼                              ▼
┌─────────────────────┐      ┌──────────────────────────┐
│ Power up V_CC &     │      │                          │
│ Stabilized          │      │ (100ms Delay Recommended)│
│ (Delay Recommended) │      │                          │
└─────────────────────┘      └──────────────────────────┘
```
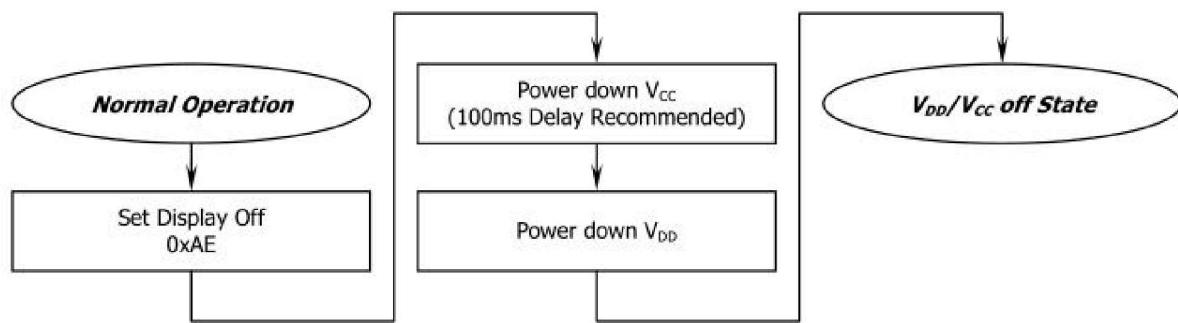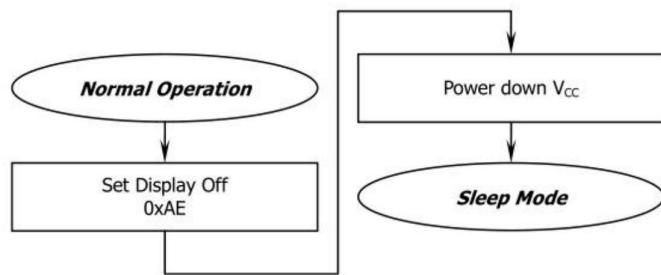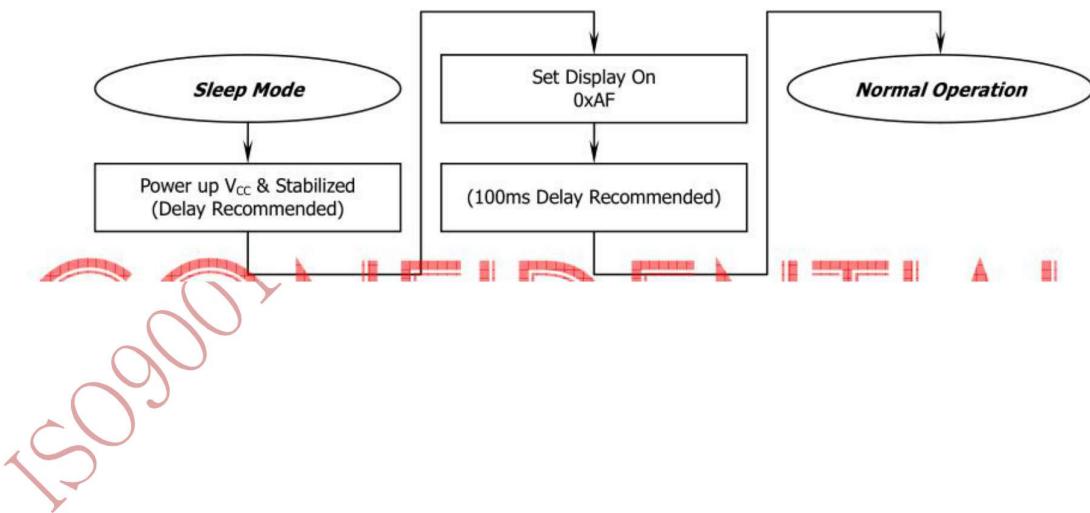
8. Appearance Inspection

8.1 Appearance Condition

8.1.1 Environment: 22 ± 3ºC, Inspection distance：30 ± 5cm.

8.1.2 Rotation angle : ±45º

8.1.3 Lighting illumination：1000~1200Lux

8.1.4 Background：Black

8.1.5 Inspection time：30s each piece
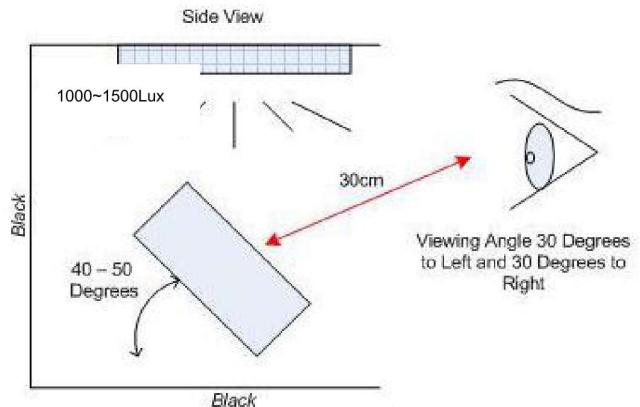
Remark:

Inspection criterions are valid for the complete Module (CTP + OLED) including reverse Printing and Logo printing

Side View

1000~1500Lux

Black

Black

40 – 50 Degrees

30cm

Viewing Angle 30 Degrees to Left and 30 Degrees to Right

8.2 Appearance Criterion

No.	Item	Criteria for defects (Unit: mm)
1	**Dot Defects (Particle/Dirt/ Dent/Bubble)**	1、D≤0.2 mm; Ignore 2、0.2 mm＜D≤0.5 mm,N≤5，Distance ≥70mm D≥5mm is not allowed. $D=(W+L)/2$ W L W L
2	**Line type Defects (S cratch/Dirt/Particle)**	1、W≤0.063mm , Ignore 2、0.063mm＜W≤0.1mm,L≤8mm(length in total),N≤4; Distance ≥70mm Other is not allowed. W L
3	**Edge Chipping**	Allow: Edge Chips/chamfered Edges: Corner: D≤ 0.3mm Polished edges: D≤ 0.25mm, Ignore; 0.25mm<D≤0.4 mm,N≤5 per edge allowed Heat marks on polished edged: Width max. 0.15mm, length max.4.0mm. Max.2 per 500mm,min. distance>40mm
4	**Glass Crack**	Crack is potential to enlarge, any type is not allowed.
5	No visible color change when compared with the approved sample	
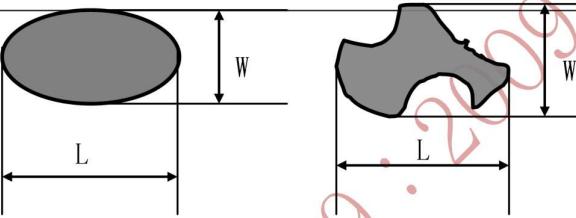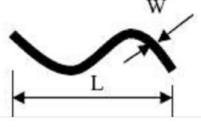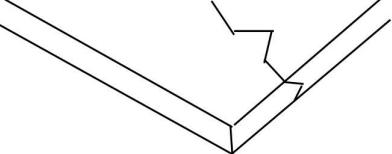
Remark	For No.1.2 and 2.2 8 defects in total are allowed A concentration of defects is not allowed, definition in accordance with DIN ISO 10110-7

9. Reliability Test Result

Item	Condition	Inspection after test
High Temperature Operating	70℃,96H	
Low Temperature Operating	-40℃, 96HR	
High Temperature Storage	85℃, 96HR	
Low Temperature Storage	-40℃, 96HR	Inspection after 2~4hours storage at room temperature, the sample shall be free from defects:
High Temperature & High Humidity Storage	+60℃, 90% RH ,96 hours.	1.Air bubble in the LCD;
Thermal Shock (Non-operation)	-40℃,30 min ↔ 85℃,30 min, Change time:5min 20CYC,	2.Non-display; 3.Missing segments/line;
ESD test	C=150pF, R=330,5points/panel Air:±8KV, 5times; Contact:±6KV, 5 times; (Environment: 15℃~35℃, 30%~60%).	4.Glass crack; 5.Current IDD is twice higher than initial value.
Vibration (Non-operation)	Frequency range:10~55Hz, Stroke:1.5mm Sweep:10Hz~55Hz~10Hz 2 hours for each direction of X.Y.Z. (6 hours for total) (Package condition).	
Box Drop Test	1 Corner 3 Edges 6 faces,80㎝(MEDIUM BOX)	

Remark:

1.The test samples should be applied to only one test item.

2.Sample size for each test item is 5~10pcs.

3.For Damp Proof Test, Pure water(Resistance＞10MΩ) should be used.

4.In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part.

5.Failure Judgment Criterion: Basic Specification, Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.

10. Cautions and Handling Precautions

10.1 Handling and Operating the Module

(1) When the module is assembled, it should be attached to the system firmly.

Do not warp or twist the module during assembly work.

(2) Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.

(3) Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.

(4) Do not allow drops of water or chemicals to remain on the display surface.

If you have the droplets for a long time, staining and discoloration may occur.

(5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.

(6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane.

Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.

(8) Protect the module from static; it may cause damage to the CMOS ICs.

(9) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.

(10) Do not disassemble the module.

(11) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.

(12) Pins of I/F connector shall not be touched directly with bare hands.

(13) Do not connect, disconnect the module in the "Power ON" condition.

(14) Power supply should always be turned on/off by the item 6.1 Power On Sequence &6.2 Power Off Sequence

10.2 Storage and Transportation.

(1) Do not leave the panel in high temperature, and high humidity for a long time.

It is highly recommended to store the module with temperature from 0 to 35 ℃ and relative humidity of less than 70%

(2) Do not store the TFT-LCD module in direct sunlight.

(3) The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.

(4) It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module.

In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.

(5) This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.

11. Packing

----TBD-------------