

**SPECIFICATION**  
**FOR**  
**LCM Module**  
**BLKD043WVFIA024-C016A**

MODULE:	
CUSTOMER:	

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ISO9001 : 2008      ISO/TS16949 : 2009



## \* Description

This is a color active matrix TFT (Thin Film Transistor) LCD (liquid crystal display) that uses amorphous silicon TFT as a switching device. This model is composed of a Transmissive type TFT-LCD Panel, driver circuit, back-light unit. The resolution of a 4.3'TFT-LCD contains 480x800 pixels, and can display up to 65K/262K/16.7M colors.

## \* Features

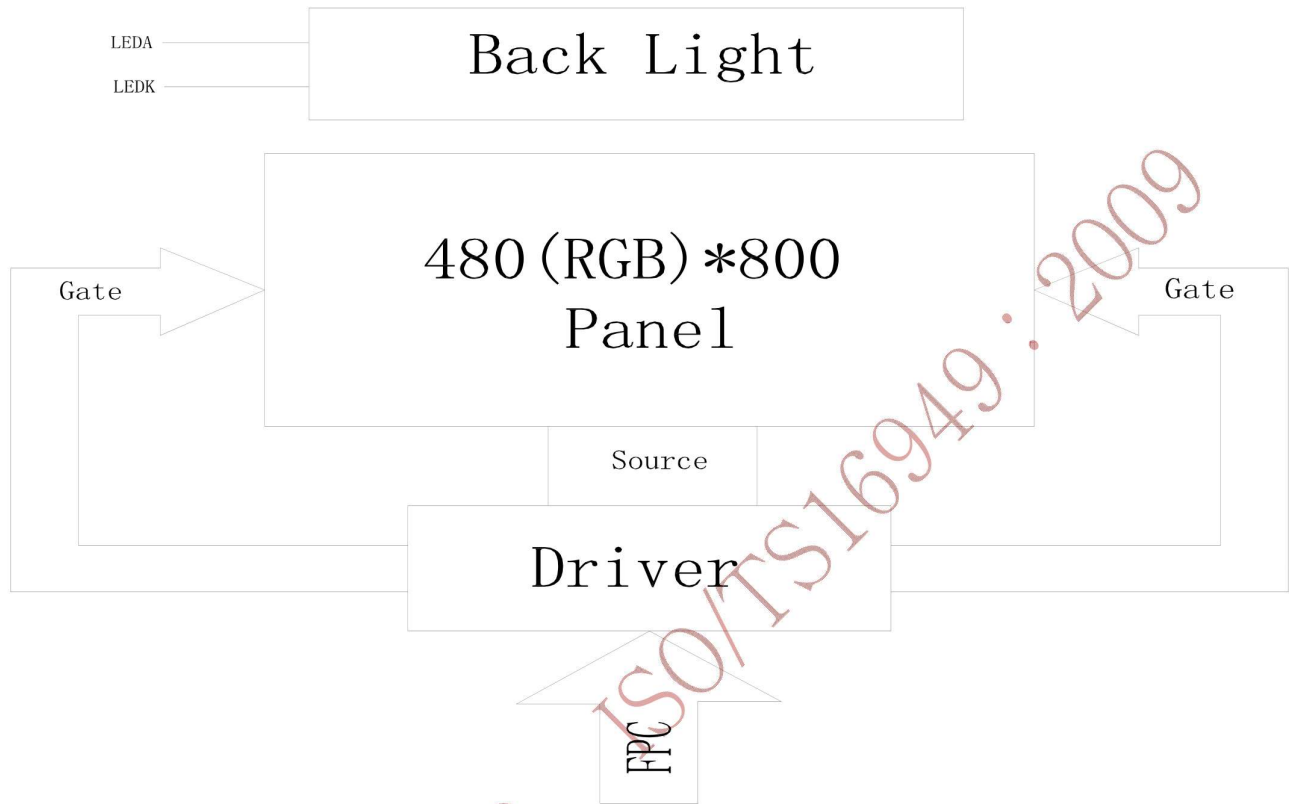
- Low Input Voltage: 3.3V(TYP)
- Display Colors of TFT LCD: 16.7M colors
- Interface: 2 Lane MIPI
- CTP Interface: I2C

General Information Items	Specification	Unit	Note
	Main Panel		
Display area(AA)	56.16(H)*93.60(V) (4.3inch)	mm	-
Driver element	TFT active matrix	-	-
Display colors	16.7M	colors	-
Number of pixels	480(RGB)*800	dots	-
TFT Pixel arrangement	RGB vertical stripe	-	-
Pixel pitch	0.117(H)*0.117(V)	mm	-
Viewing angle	ALL	o'clock	-
TFT Controller IC	ILI9806E	-	-
CTP Driver IC	GT911		
Display mode	Transmissive/Normally Black	-	-
Touch mode	5-point and Gestures		
Operating temperature	-20~+70	°C	-
Storage temperature	-30~+80	°C	-

## \* Mechanical Information

Item		Min.	Typ.	Max.	Unit	Note
Module size	Horizontal(H)		62.50		mm	-
	Vertical(V)		105.55		mm	-
	Depth(D)		3.93		mm	-
Weight			--		g	-

## 1. Block Diagram





### 3. Input terminal Pin Assignment

#### 3.1 TFT

NO.	SYMBOL	DISCRIPTION	I/O
1	NC		
2	LEDK	Cathode pin of backlight.	P
3	NC		
4	LEDA	Anode pin of backlight.	P
5	NC		
6	VCI	Supply Voltage (3.3V).	P
7	IOVCC	I/O power supply voltage.	P
8	TE	-Tearing effect output Leave the pin to open when not in use.	O
9	RESET	- The external reset input. Initializes the chip with a low input. Be sure to execute a power-on reset after supplying power.	I
10	GND	Ground.	P
11	MIPI_D1P	MIPI DSI differential data pair (DSI-Dn+/-).	I/O
12	MIPI_D1N	If MIPI are not used, they should be connected to DGND	I/O
13	GND	Ground.	P
14	MIPI_CLP	MIPI DSI differential clock pair (DSI-CLK+/-).	I
15	MIPI_CLN	If MIPI are not used, they should be connected to DGND.	I
16	GND	Ground.	P
17	MIPI_D0P	MIPI DSI differential data pair (DSI-Dn+/-).	I/O
18	MIPI_D0N	If MIPI are not used, they should be connected to DGND	I/O
19	GND	Ground.	P
20	GND	Ground.	P

### 3.2 CTP

NO.	SYMBOL	DISCRIPTION	I/O
1	GND	Ground.	P
2	NC		
3	VDD	Supply voltage.	P
4	SCL	I2C clock input.	I
5	SDA	I2C data input and output	I/O
6	INT	External interrupt to the host.	I
7	RST	External Reset, Low is active.	I
8	GND	Ground.	P

ISO9001 : 2008 ISO/TS16949 : 2009

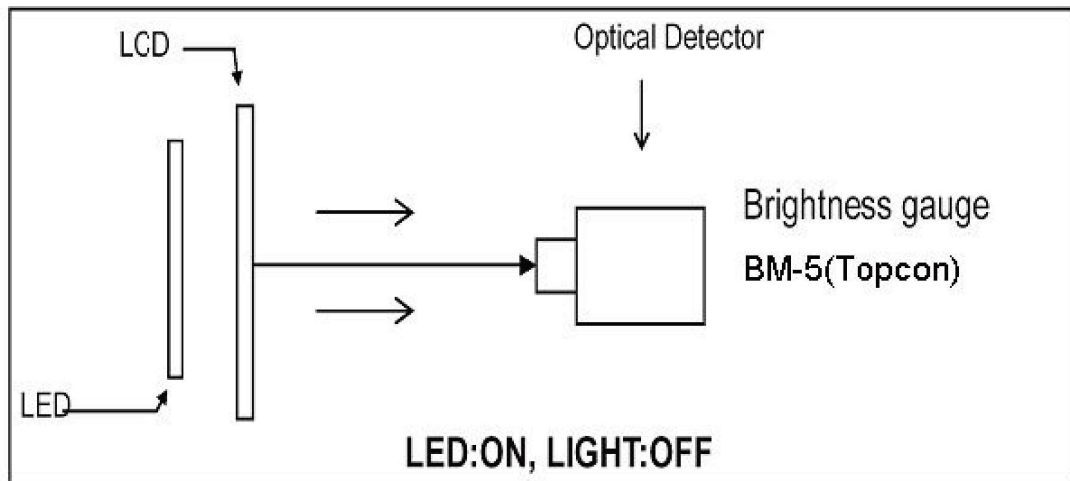
## 4. LCD Optical Characteristics

### 4.1 Optical specification

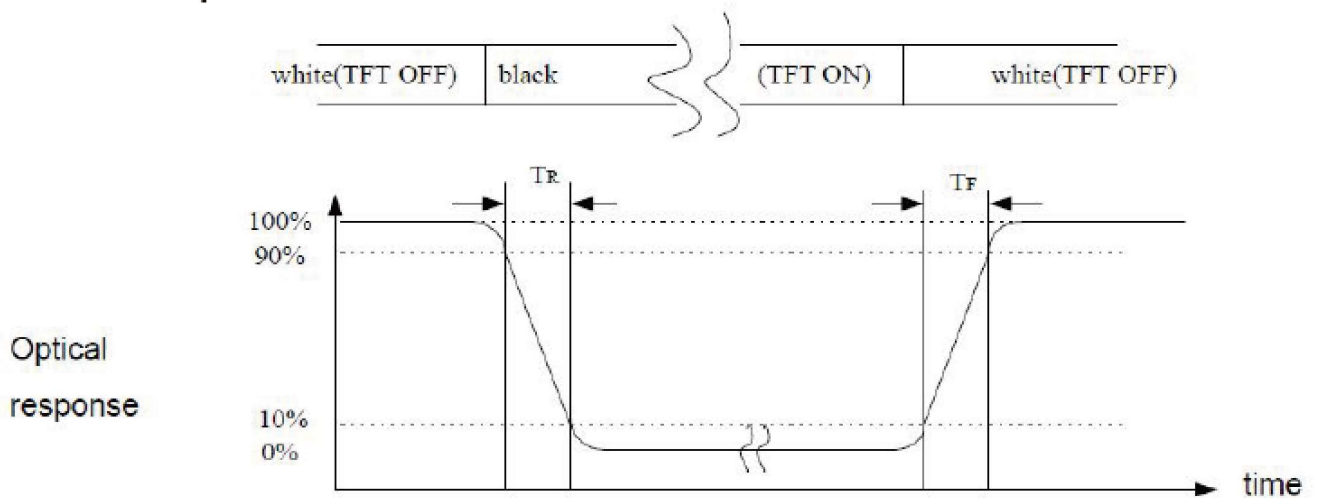
Item	Symbol	Condition	Min.	Typ.	Max.	Unit.	Note	
Contrast Ratio	CR	$\Theta=0$ Normal viewing angle	700	800	--		(3)	
Response time	Rising		$T_{R+T_F}$	--	30	45	msec	(2)
	Falling							
Color gamut	S(%)		--	70	--	%	C-light	
Color Filter Chromaticity	White		$W_X$	0.293	0.333	0.353	-	CF glass
			$W_Y$	0.353	0.393	0.413		
	Red		$R_X$	0.629	0.649	0.669		
			$R_Y$	0.319	0.339	0.359		
	Green		$G_X$	0.300	0.320	0.340		
			$G_Y$	0.605	0.625	0.645		
	Blue	$B_X$	0.130	0.150	0.170			
		$B_Y$	0.027	0.047	0.067			
Viewing angle	Hor.	$\Theta_L$	--	80	--	-	(1)(4) Measuring with Polarizer, Reference Only	
		$\Theta_R$	--	80	--			
	Ver.	$\Theta_U$	--	80	--			
		$\Theta_D$	--	80	--			
Option View Direction			Free			(5)		

**NOTE 1 :Test equipment setup**

After stabilizing and leaving the panel alone at a given temperature for 30 minutes, the measurement should be executed. Measurement should be executed in a stable, windless, and dark room. Optical specifications are measured by Topcon BM-5A with a viewing angle of 2° at a distance of 50cm and normal direction.



**NOTE 2: Response Time**

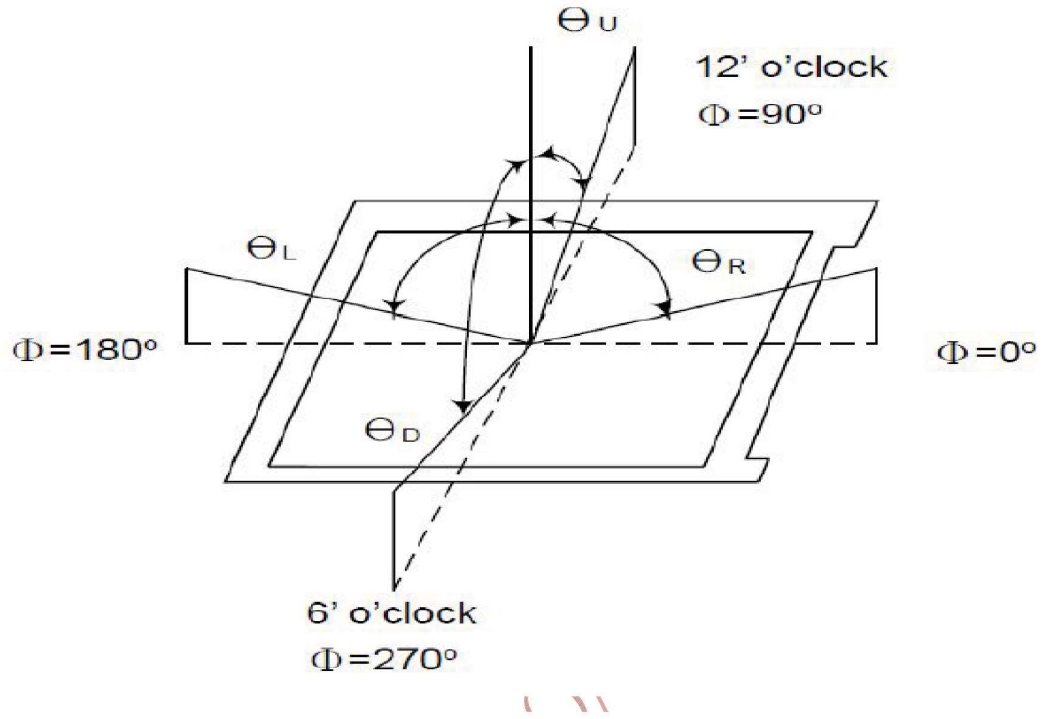


**NOTE 3: Definition of contrast ratio:**

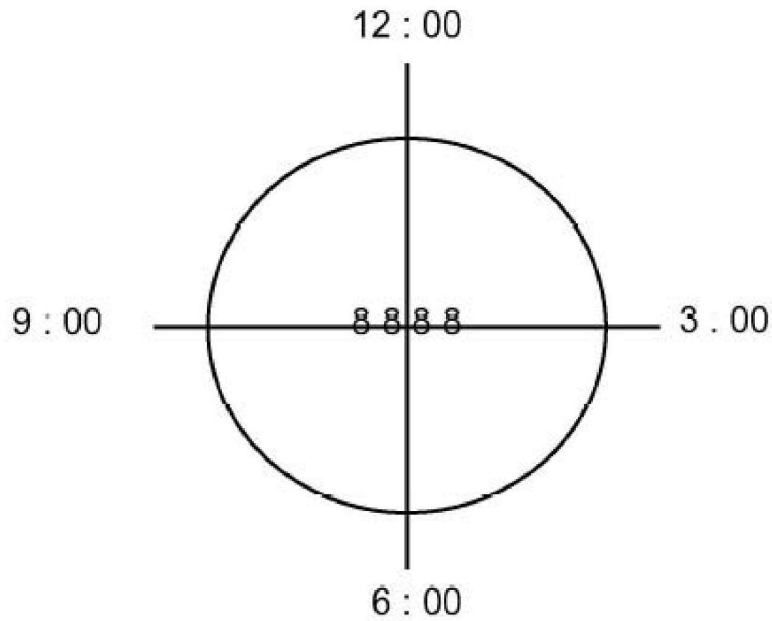
$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD is at "white state"}}{\text{Luminance measured when LCD is at "black state"}}$$



**NOTE 4 :  $\Phi$  、  $\theta$  Definition**



**NOTE 5: Visual angle direction priority**





## 5. TFT Electrical Characteristics

### 5.1 Absolute Maximum Rating (Ta=25 VSS=0V)

Characteristics	Symbol	Min.	Max.	Unit
Digital Supply Voltage	VCI	-0.3	4.6	V
Digital interface supply Voltage	IOVCC	-0.3	4.6	V
Operating temperature	T <sub>OP</sub>	-20	+70	°C
Storage temperature	T <sub>ST</sub>	-30	+80	°C

NOTE: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

### 5.2 DC Electrical Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Note
Digital Supply Voltage	VCI	2.5	2.8/3.3	3.6	V	--
Digital interface supply Voltage	IOVCC	1.65	1.8	3.6	V	--
Normal mode Current consumption	IDD	--	25	--	mA	--
Level input voltage	V <sub>IH</sub>	0.7 IOVCC	--	IOVCC	V	--
	V <sub>IL</sub>	-0.3	--	0.3 IOVCC	V	--
Level output voltage	V <sub>OH</sub>	0.8* IOVCC	--	IOVCC	V	--
	V <sub>OL</sub>	GND	--	0.2 IOVCC	V	--

### 5.3 LED Backlight Characteristics

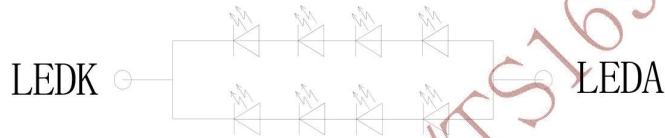
The back-light system is edge-lighting type with 8 chips White LED

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Forward Current	I <sub>F</sub>	30	40	--	mA	--
Forward Voltage	V <sub>F</sub>	--	12.8	--	V	--
LCM Luminance	L <sub>V</sub>	360	405	--	cd/m <sup>2</sup>	Note3
LED life time	Hr	50000			Hour	Note1,2

Uniformity	AVg	80	--	--	%	Note3
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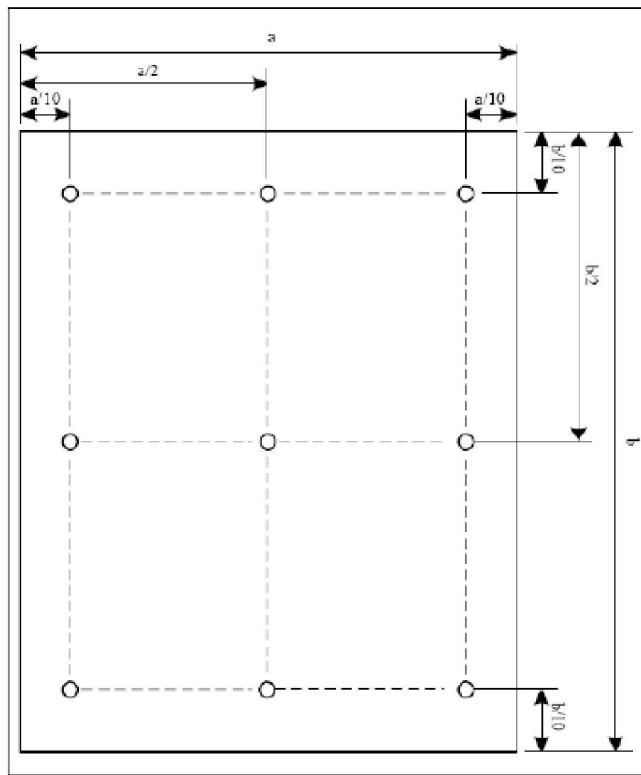
Note (1) LED life time (Hr) can be defined as the time in which it continues to operate under the condition:  $T_a=25\pm3\text{ }^\circ\text{C}$ , typical IL value indicated in the above table until the brightness becomes less than 50%.

Note (2) The "LED life time" is defined as the module brightness decrease to 50% original brightness at  $T_a=25^\circ\text{C}$  and  $I_L=40\text{mA}$ . The LED lifetime could be decreased if operating  $I_L$  is larger than 40mA. The constant current driving method is suggested.



LED(B/L) CIRCUIT

NOTE 3: Luminance Uniformity of these 9 points is defined as below:



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$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points (1-9)}}{\text{maximum luminance in 9 points (1-9)}}$$

$$\text{Luminance} = \frac{\text{Total Luminance of 9 points}}{9}$$

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## 6. MIPI Interface Characteristics

### 6.1 High Speed Mode – Clock Channel Timing

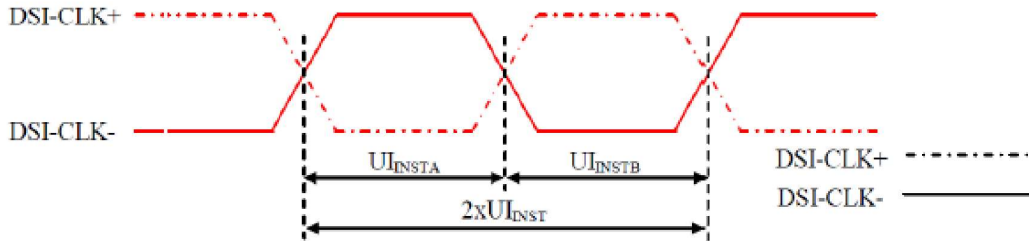


Figure 114 DSI Clock Channel Timing

Table 45 DSI Clock Channel Timing

Signal	Symbol	Parameter	Min	Max	Unit
DSI-CLK+/-	$2xUI_{INST}$	Double UI instantaneous	4	25	ns
DSI-CLK+/-	$UI_{INSTA}, UI_{INSTB}$	UI instantaneous Half	2	12.5	ns

Note:  $UI = UI_{INSTA} = UI_{INSTB}$

### 6.2 High Speed Mode – Data Clock Channel Timing

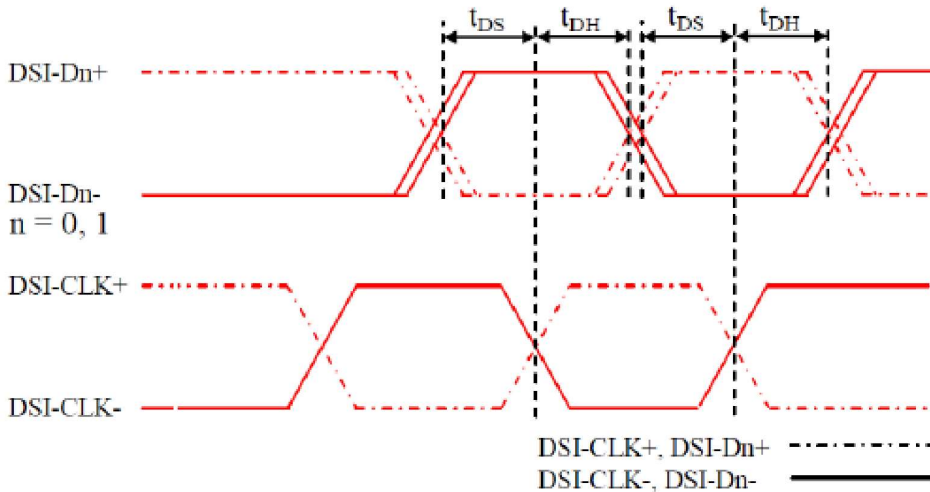


Figure 115 DSI Data to Clock Channel Timings

Table 46 DSI Data to Clock Channel Timings

Signal	Symbol	Parameter	Min	Max
DSI-Dn+/-, n=0 and 1	$t_{DS}$	Data to Clock Setup time	$0.15xUI$	-
	$t_{DH}$	Clock to Data Hold Time	$0.15xUI$	-

### 6.3 High Speed Mode – Rise and Fall Timings

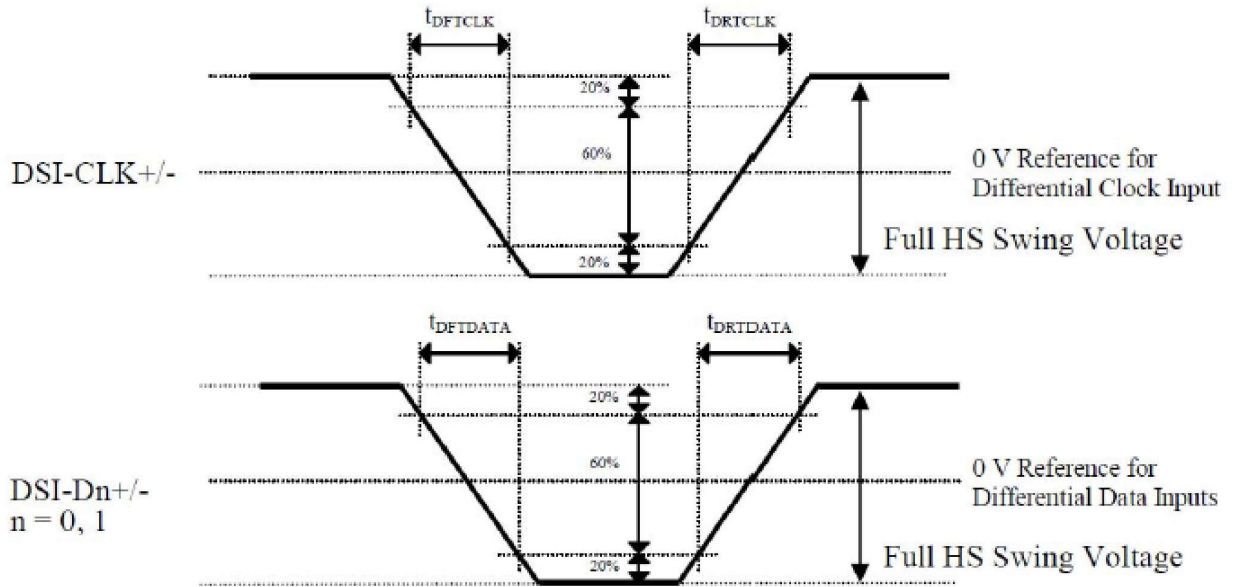


Figure 116 Rise and Fall Timings on Clock and Data Channels

Table 47 Rise and Fall Timings on Clock and Data Channels

Parameter	Symbol	Condition	Specification			Unit
			Min	Typ	Max	
Differential Rise Time for Clock	$t_{DRTCLK}$	DSI-CLK+/-	-	-	150 (Note )	ps
Differential Rise Time for Data	$t_{DRTDATA}$	DSI-Dn+/- n=0 and 1	-	-	150 (Note )	ps
Differential Fall Time for Clock	$t_{DFTCLK}$	DSI-CLK+/-	-	-	150 (Note )	ps
Differential Fall Time for Data	$t_{DFTDATA}$	DSI-Dn+/- n=0 and 1	-	-	150 (Note )	ps

Note: The display module has to meet timing requirements, what are defined for the transmitter (MPU) on MIPI D-Phy standard

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## 6.4 Low Speed Mode – Bus Turn Around

Lower Power Mode and its State Periods are illustrated for reference purposes on the Bus Turnaround (BTA) from the MPU to the Display Module (ILI9806E) sequence below.

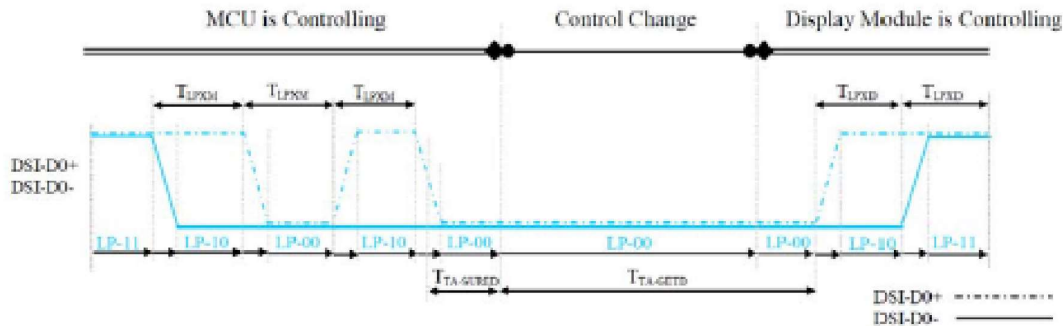


Figure 117 BTA from the MPU to the Display Module

Lower Power Mode and its State Periods are illustrated for reference purposes on the Bus Turnaround (BTA) from the Display Module (ILI9806E) to the MPU sequence below.

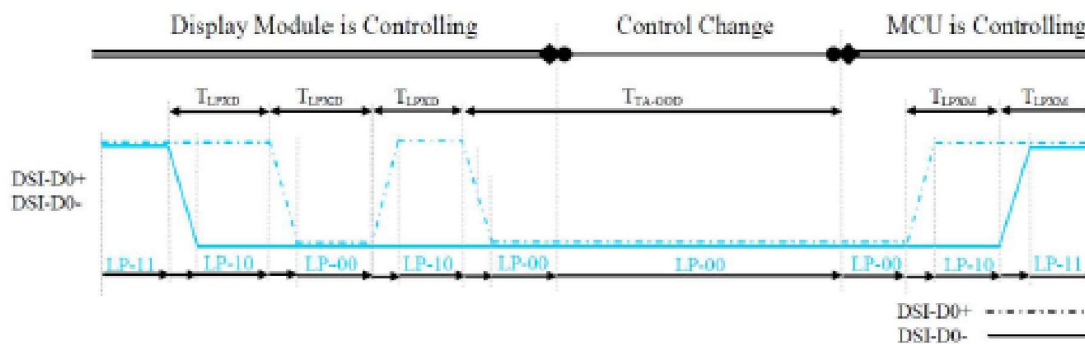


Figure 118 BTA from the Display Module to the MPU

Table 48 Low Power State Period Timings – A

Signal	Symbol	Description	Min	Max	Unit
DSI-D0+/-	$T_{LPXM}$	Length of LP-00, LP-01, LP-10 or LP-11 periods MPU → Display Module (ILI9806E)	50	75	ns
DSI-D0+/-	$T_{LPXD}$	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module (ILI9806E) → MPU	50	75	ns
DSI-D0+/-	$T_{TA-SURED}$	Time-out before the Display Module (ILI9806E) starts driving	$T_{LPXD}$	$2 \times T_{LPXD}$	ns

Table 49 Low Power State Period Timings – B

Signal	Symbol	Description	Time	Unit
DSI-D0+/-	$T_{TA-GETD}$	Time to drive LP-00 by Display Module (ILI9806E)	$5 \times T_{LPXD}$	ns
DSI-D0+/-	$T_{TA-00D}$	Time to drive LP-00 after turnaround request – MPU	$4 \times T_{LPXD}$	ns



## 6.5 Data Lanes from Low Power Mode to High Speed Mode

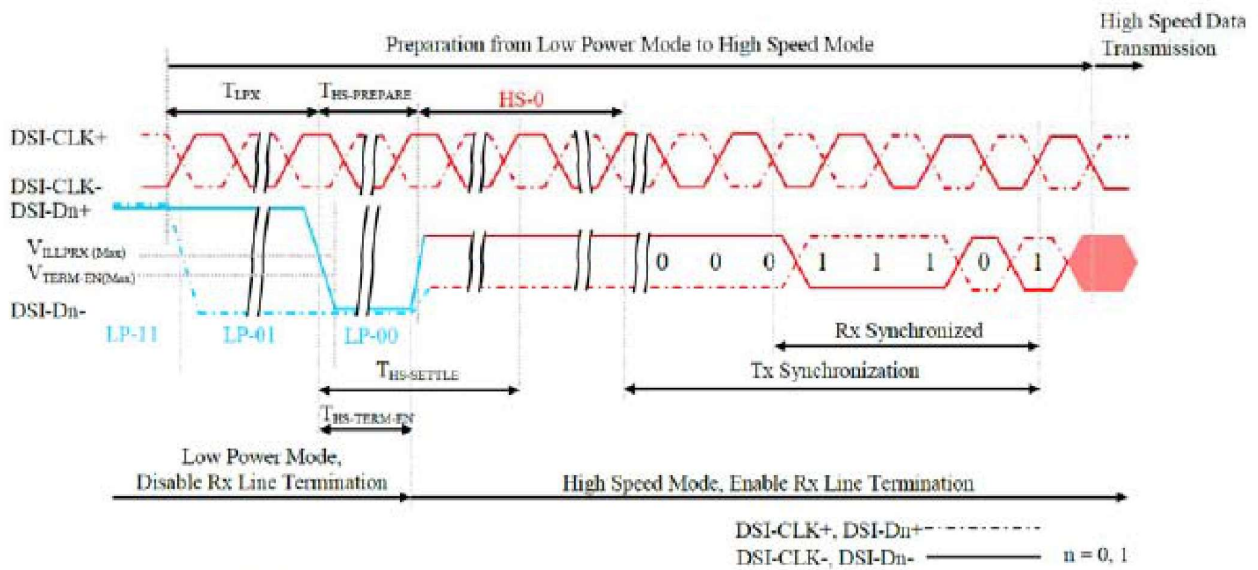


Figure 119 Data Lanes – Low Power Mode to High Speed Mode Timings

Table 50 Data Lanes – Low Power Mode to High Speed Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DSI-Dn+/-, n=0 and 1	$T_{LPX}$	Length of any Low Power State Period	50	-	ns
DSI-Dn+/-, n=0 and 1	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS Transmission	$40+4xUI$	$85+6xUI$	ns
DSI-Dn+/-, n=0 and 1	$T_{HS-TERM-EN}$	Time to enable Data Lane Receiver line termination measured from when Dn crosses $V_{ILMAX}$	-	$35+4xUI$	ns

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## 6.6 Data Lanes from Low Power Mode to High Speed Mode

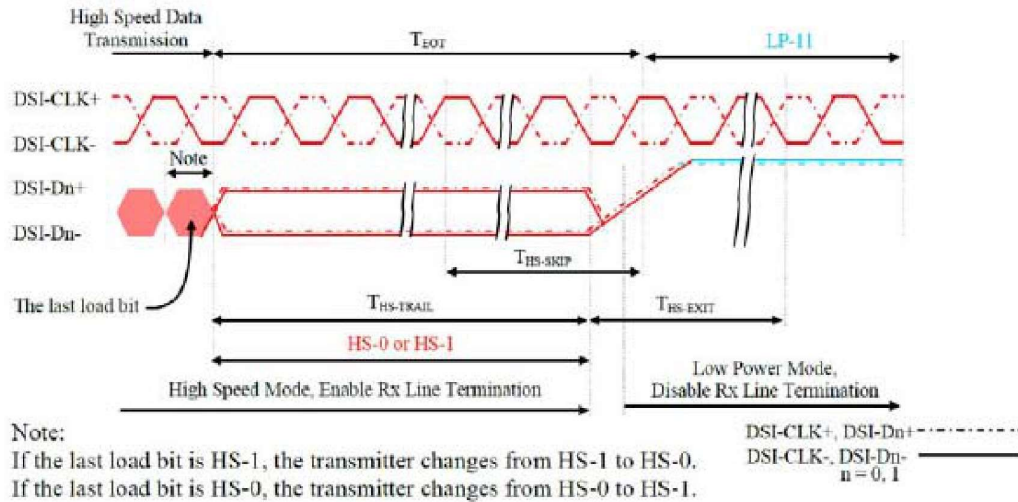


Figure 120 Data Lanes – High Speed Mode to Low Power Mode Timings

Table 51 Data Lanes – High Speed Mode to Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DSI-Dn+/-, n=0 and 1	$T_{HS-SKIP}$	Time-Out at Display Module (ILI9806E) to ignore transition period of EoT	40	$55+4xUI$	ns
DSI-Dn+/-, n=0 and 1	$T_{HS-EXIT}$	Time to driver LP-11 after HS burst	100	-	ns

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## 6.7 DSI Clock Burst – High Speed Mode to/from Low Power Mode

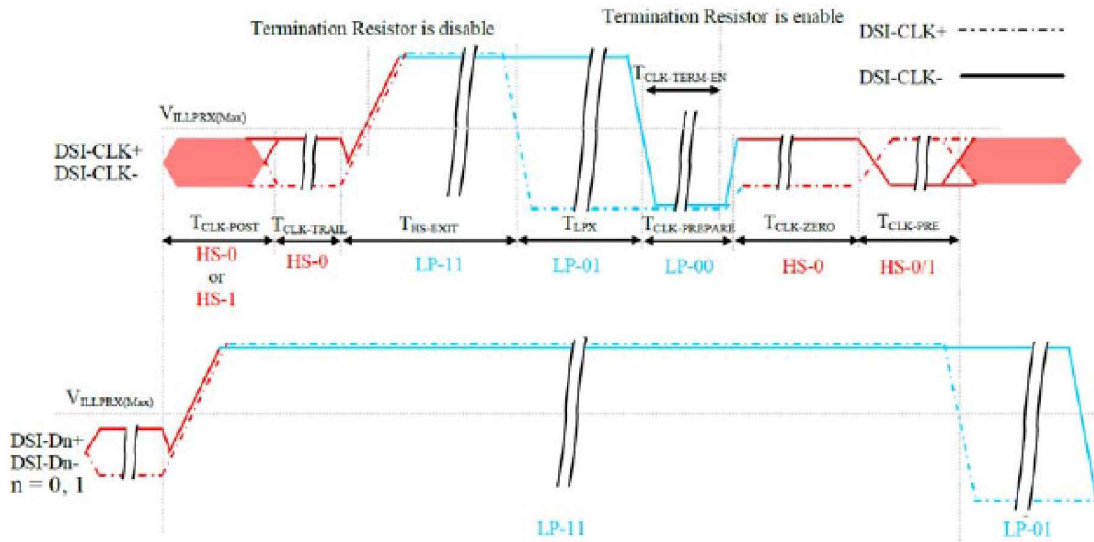


Figure 121 Clock Lanes – High Speed Mode to/from Low Power Mode Timings

Table 52 Clock Lanes – High Speed Mode to/from Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DSI-CLK+/-	$T_{CLK-POST}$	Time that the MPU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	$60+52xUI$	-	ns
DSI-CLK+/-	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns
DSI-CLK+/-	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	ns
DSI-CLK+/-	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38	95	ns
DSI-CLK+/-	$T_{CLK-TERM-EN}$	Time-out at Clock Lane to enable HS termination	-	38	ns
DSI-CLK+/-	$T_{CLK-PREPARE}$	Minimum lead HS-0 drive period before starting Clock	300	-	ns
DSI-CLK+/-	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	$8xUI$	-	ns

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## 6.8 Reset input timing

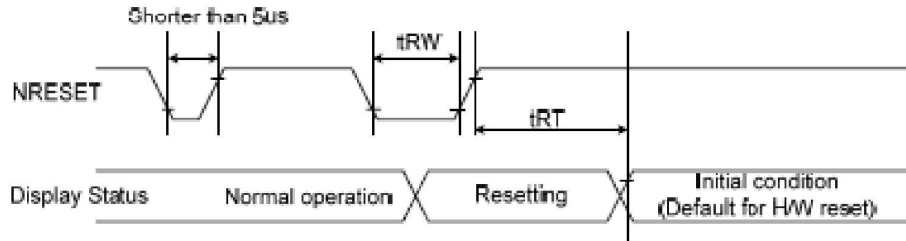


Figure 102 Reset Timing

Table 41 Reset Timing

Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		us
	tRT	Reset cancel		5 (note 1,5) 120 (note 1,6,7)	ms

Note:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from OTP to registers. This loading is done every time when there is H/W reset cancel time (tRT) within 5 ms after a rising edge of RESX.
2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the Table 43.

Table 42 Reset Descript

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out mode. The display remains the blank state in Sleep In mode.) and then return to Default condition for Hardware Reset.
4. Spike Rejection also applies during a valid reset pulse as shown below:

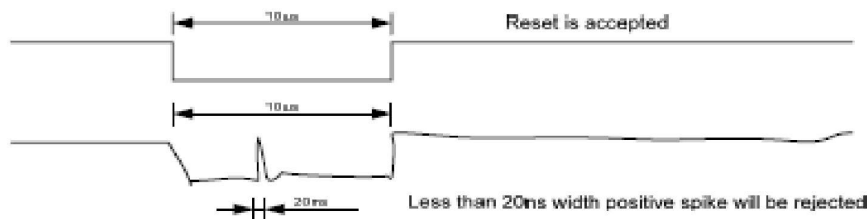


Figure 103 Positive Noise Pulse during Reset Low

5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

## 7. CTP Specification

### 7.1 Electrical Characteristics

#### 7.1.1 Absolute Maximum Rating

Item	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage	VDD	2.66	3.47	V	--
Operating temperature	T <sub>OP</sub>	-20	+70	°C	--
Storage temperature	T <sub>ST</sub>	-30	+80	°C	--

#### 7.1.2 DC Electrical Characteristics (Ta=25°C)

(Ambient temperature:25°C, AVDD=2.8V, VDDIO=1.8V or VDDIO=AVDD)

Item	Min.	Typ.	Max.	Unit	Note
Normal mode operating current	--	8	14.5	mA	
Green mode operating current	--	3.3	--	mA	
Sleep mode operating current	70	--	120	uA	
Doze mode operating current	--	0.78	--	mA	
Digital Input low voltage/VIL	-0.3	--	0.25*VDDIO	V	
Digital Input high voltage/VIH	0.75*VDDIO	--	VDDIO+0.3	V	
Digital Output low voltage/VOL	--		0.15*VDDIO	V	
Digital Output high voltage/VOH	0.85*VDDIO			V	

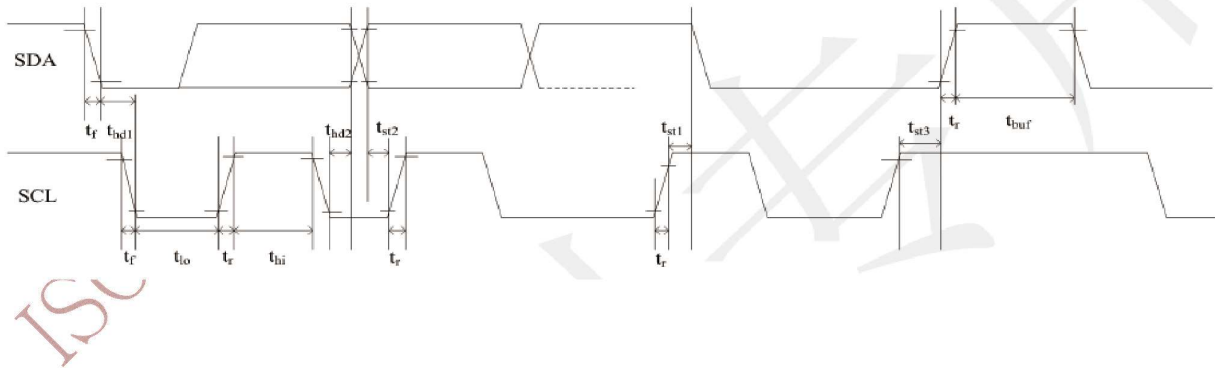
### 7.1.3 AC Characteristics

(Ambient temperature:25°C, AVDD=2.8V, VDDIO=1.8V)

Parameter	Min	Typ	Max	Unit
OSC oscillation frequency	59	60	61	MHZ
I/O output rise time,low to high	-	14	-	ns
I/O output rfall time,high to low	-	14	-	ns

### 7.2 I2C Timing

GT911 provides a standard I2C interface for SCL and SDA to communicate with the host. GT911 always serves as slave device in the system with all communication being initialized by the host. It is strongly recommended that transmission rate be kept at or below 400Kbps. The I2C timing is shown below:



**Test condition 1: 1.8V host interface voltage, 400Kbps transmission rate, 2K pull-up resistor**

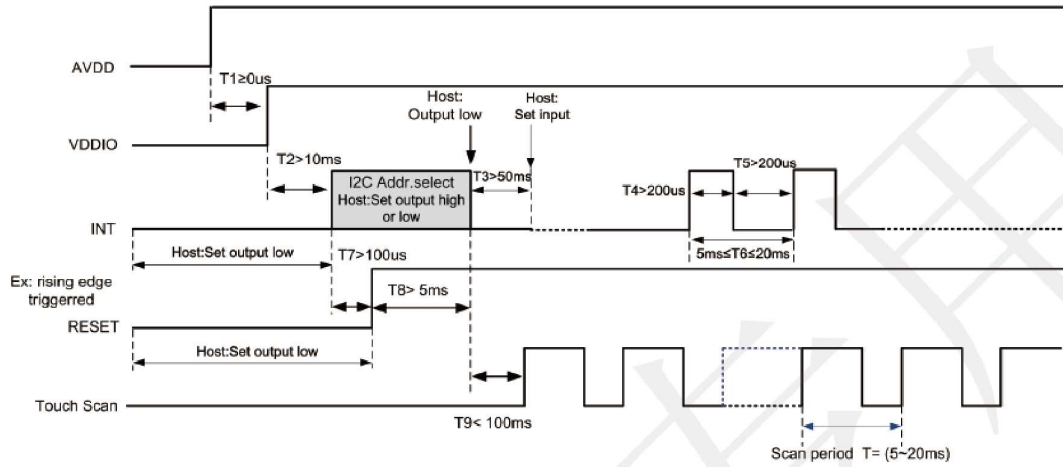
Parameter	Symbol	Min.	Max.	Unit
SCL low period	$t_{lo}$	1.3	-	us
SCL high period	$t_{hi}$	0.6	-	us
SCL setup time for Start condition	$t_{st1}$	0.6	-	us
SCL setup time for Stop condition	$t_{st3}$	0.6	-	us
SCL hold time for Start condition	$t_{hd1}$	0.6	-	us
SDA setup time	$t_{st2}$	0.1	-	us
SDA hold time	$t_{hd2}$	0	-	us

**Test condition 2: 3.3V host interface voltage, 400Kbps transmission rate, 2K pull-up resistor**

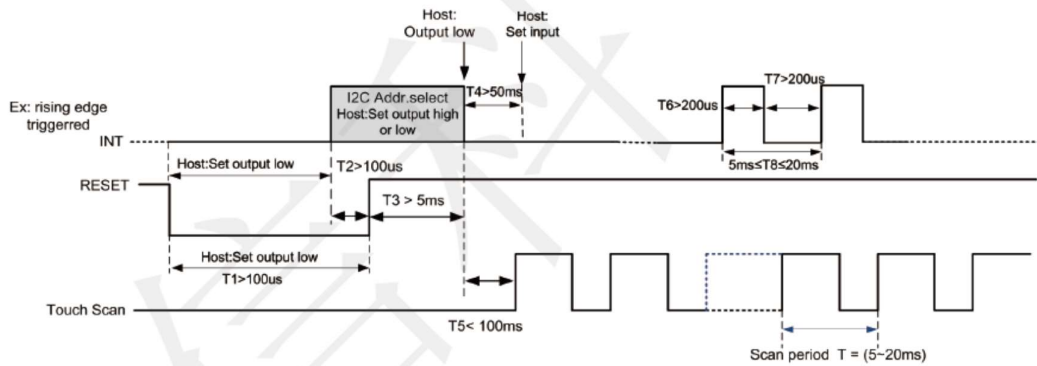
Parameter	Symbol	Min.	Max.	Unit
SCL low period	$t_{lo}$	1.3	-	us
SCL high period	$t_{hi}$	0.6	-	us
SCL setup time for Start condition	$t_{st1}$	0.6	-	us
SCL setup time for Stop condition	$t_{st3}$	0.6	-	us
SCL hold time for Start condition	$t_{hd1}$	0.6	-	us
SDA setup time	$t_{st2}$	0.1	-	us
SDA hold time	$t_{hd2}$	0	-	us

GT911 supports two I2C slave addresses: 0xBA/0xBB and 0x28/0x29. The host can select the address by changing the status of Reset and INT pins during the power-on initialization phase. See the diagram below for configuration methods and timings:

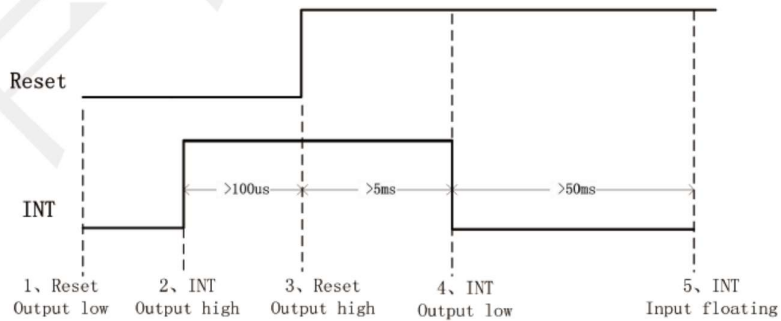
**Power-on Timing:**



**Timing for host resetting GT911:**

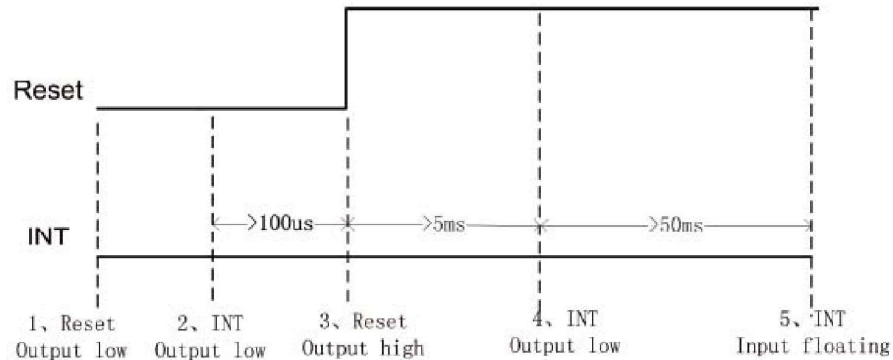


**Timing for setting slave address to 0x28/0x29:**





### Timing for setting slave address to 0xBA/0xBB:



#### a) Data Transmission

(For example: device address is 0xBA/0xBB)

Communication is always initiated by the host. Valid Start condition is signaled by pulling SDA line from “high” to “low” when SCL line is “high”. Data flow or address is transmitted after the Start condition.

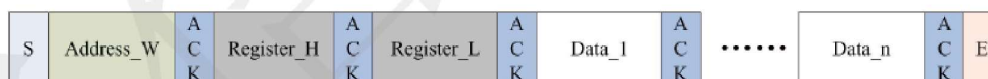
All slave devices connected to I<sup>2</sup>C bus should detect the 8-bit address issued after Start condition and send the correct ACK. After receiving matching address, GT911 acknowledges by configuring SDA line as output port and pulling SDA line low during the ninth SCL cycle. When receiving unmatched address, namely, not 0XBA or 0XBB, GT911 will stay in an idle state.

For data bytes on SDA, each of 9 serial bits will be sent on nine SCL cycles. Each data byte consists of 8 valid data bits and one ACK or NACK bit sent by the recipient. The data transmission is valid when SCL line is “high”.

When communication is completed, the host will issue the STOP condition. Stop condition implies the transition of SDA line from “low” to “high” when SCL line is “high”.

#### b) Writing Data to GT911

(For example: device address is 0xBA/0xBB)



Timing for Write Operation

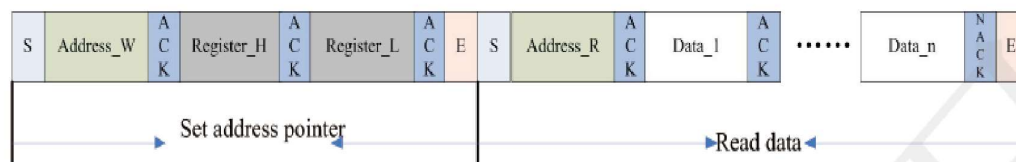
The diagram above displays the timing sequence of the host writing data onto GT911. First, the host issues a Start condition. Then, the host sends 0xBA (address bits and R/W bit; R/W bit as 0 indicates Write operation) to the slave device.

After receiving ACK, the host sends the 16-bit register address (where writing starts) and the 8-bit data bytes (to be written onto the register).

The location of the register address pointer will automatically add 1 after every Write Operation. Therefore, when the host needs to perform Write Operations on a group of registers of continuous addresses, it is able to write continuously. The Write Operation is terminated when the host issues the Stop condition.

### c) Reading Data from GT911

(For example: device address is 0xBA/0xBB)



#### Timing for Read Operation

The diagram above is the timing sequence of the host reading data from GT911. First, the host issues a Start condition and sends 0xBA (address bits and R/W bit; R/W bit as 0 indicates Write operation) to the slave device.

After receiving ACK, the host sends the 16-bit register address (where reading starts) to the slave device. Then the host sets register addresses which need to be read.

Also after receiving ACK, the host issues the Start condition once again and sends 0xBB (Read Operation). After receiving ACK, the host starts to read data.

GT911 also supports continuous Read Operation and, by default, reads data continuously. Whenever receiving a byte of data, the host sends an ACK signal indicating successful reception. After receiving the last byte of data, the host sends a NACK signal followed by a STOP condition which terminates communication.



## 8.LCD Module Out-Going Quality Level

### 8.1 VISUAL & FUNCTION INSPECTION STANDARD

#### 8.1.1 Inspection conditions

Inspection performed under the following conditions is recommended.

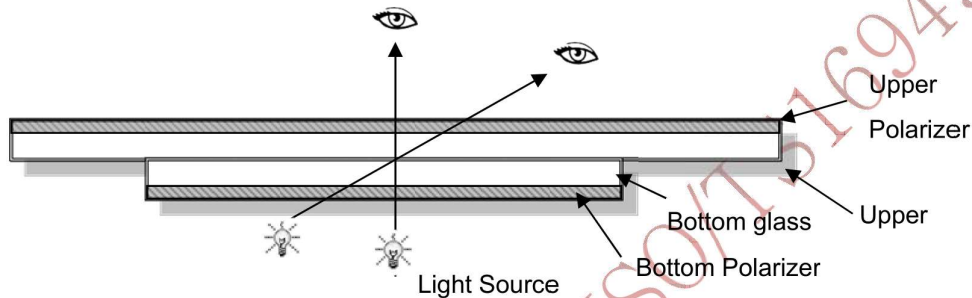
Temperature :  $25\pm 5^{\circ}\text{C}$

Humidity :  $65\%\pm 10\%\text{RH}$

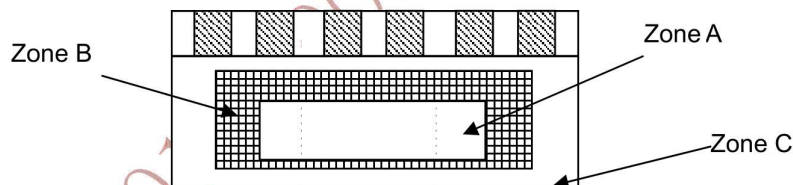
Viewing Angle : Normal viewing Angle.

Illumination: Single fluorescent lamp (300 to 700Lux)

Viewing distance:30-50cm



#### 8.1.2 Definition



Zone A : Effective Viewing Area(Character or Digit can be seen)

Zone B : Viewing Area except Zone A

Zone C : Outside (Zone A+Zone B) which can not be seen after assembly by customer .)

Note:

As a general rule ,visual defects in Zone C can be ignored when it doesn't effect product function or appearance after assembly by customer.

### 8.1.3 Sampling Plan

According to GB/T 2828-2003 ; , normal inspection, Class II

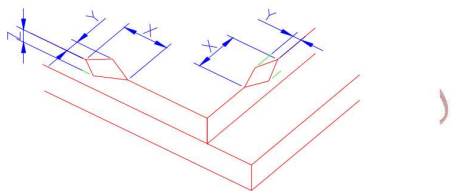
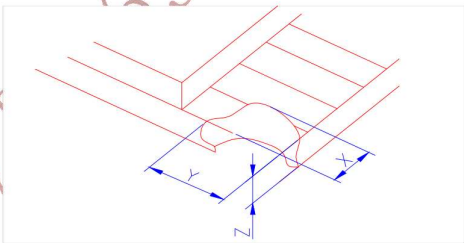
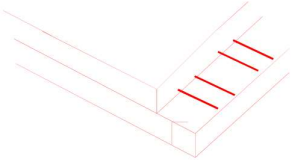
AQL:

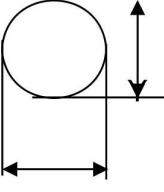
Major defect	Minor defect
0.65	1.5

LCD: Liquid Crystal Display , TP: Touch Panel , LCM: Liquid Crystal Module

No	Items to be inspected	Criteria	Classification of defects
1	Functional defects	1) No display, Open or miss line 2) Display abnormally, Short 3) Backlight no lighting, abnormal lighting. 4) TP no function	Major
2	Missing	Missing component	
3	Outline dimension	Overall outline dimension beyond the drawing is not allowed	
4	Color tone	Color unevenness, refer to limited sample	Minor
5	Soldering appearance	Good soldering , Peeling off is not allowed.	
6	LCD/Polarizer/TP	Black/White spot/line, scratch, crack, etc.	

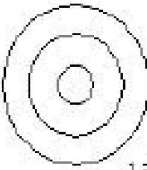


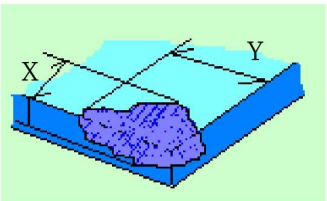
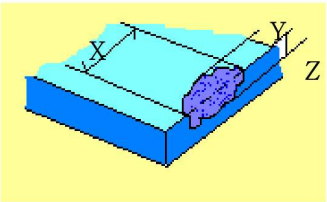
### 8.1.4 Criteria (Visual)

Number	Items	Criteria(mm)						
1.0 LCD Crack/Broken  NOTE: X: Length Y: Width Z: Height L: Length of ITO, T: Height of LCD	(1) The edge of LCD broken	 <table border="1" data-bbox="873 655 1409 800"> <thead> <tr> <th>X</th> <th>Y</th> <th>Z</th> </tr> </thead> <tbody> <tr> <td>≤3.0mm</td> <td>&lt;Inner border line of the seal</td> <td>≤T</td> </tr> </tbody> </table>	X	Y	Z	≤3.0mm	<Inner border line of the seal	≤T
	X	Y	Z					
	≤3.0mm	<Inner border line of the seal	≤T					
(2)LCD corner broken	 <table border="1" data-bbox="935 1115 1351 1207"> <thead> <tr> <th>X</th> <th>Y</th> <th>Z</th> </tr> </thead> <tbody> <tr> <td>≤3.0mm</td> <td>≤L</td> <td>≤T</td> </tr> </tbody> </table>	X	Y	Z	≤3.0mm	≤L	≤T	
X	Y	Z						
≤3.0mm	≤L	≤T						
(3) LCD crack	 <p data-bbox="1055 1512 1226 1585">Crack Not allowed</p>							

Number	Items	Criteria (mm)																									
2.0	Spot defect  $\Phi = (X+Y)/2$	① light dot (LCD/TP/Polarizer black/white spot , light dot, pinhole, dent, stain) <table border="1" data-bbox="487 367 1291 703"> <thead> <tr> <th rowspan="2">Zone Size (mm)</th> <th colspan="3">Acceptable Qty</th> </tr> <tr> <th>A</th> <th>B</th> <th>C</th> </tr> </thead> <tbody> <tr> <td><math>\Phi \leq 0.10</math></td> <td colspan="3">Ignore</td> </tr> <tr> <td><math>0.10 &lt; \Phi \leq 0.20</math></td> <td colspan="3">3( distance <math>\geq 10\text{mm}</math>)</td> </tr> <tr> <td><math>0.20 &lt; \Phi \leq 0.25</math></td> <td colspan="3">2</td> </tr> <tr> <td><math>\Phi &gt; 0.25</math></td> <td colspan="3">0</td> </tr> </tbody> </table>	Zone Size (mm)	Acceptable Qty			A	B	C	$\Phi \leq 0.10$	Ignore			$0.10 < \Phi \leq 0.20$	3( distance $\geq 10\text{mm}$ )			$0.20 < \Phi \leq 0.25$	2			$\Phi > 0.25$	0				
		Zone Size (mm)		Acceptable Qty																							
			A	B	C																						
		$\Phi \leq 0.10$	Ignore																								
		$0.10 < \Phi \leq 0.20$	3( distance $\geq 10\text{mm}$ )																								
		$0.20 < \Phi \leq 0.25$	2																								
		$\Phi > 0.25$	0																								
		② Dim spot (LCD/TP/Polarizer dim dot, light leakage, dark spot) <table border="1" data-bbox="487 745 1291 1092"> <thead> <tr> <th rowspan="2">Zone Size (mm)</th> <th colspan="3">Acceptable Qty</th> </tr> <tr> <th>A</th> <th>B</th> <th>C</th> </tr> </thead> <tbody> <tr> <td><math>\Phi \leq 0.1</math></td> <td colspan="3">Ignore</td> </tr> <tr> <td><math>0.10 &lt; \Phi \leq 0.20</math></td> <td colspan="3">3( distance <math>\geq 10\text{mm}</math>)</td> </tr> <tr> <td><math>0.20 &lt; \Phi \leq 0.30</math></td> <td colspan="3">2</td> </tr> <tr> <td><math>\Phi &gt; 0.30</math></td> <td colspan="3">0</td> </tr> </tbody> </table>	Zone Size (mm)	Acceptable Qty			A	B	C	$\Phi \leq 0.1$	Ignore			$0.10 < \Phi \leq 0.20$	3( distance $\geq 10\text{mm}$ )			$0.20 < \Phi \leq 0.30$	2			$\Phi > 0.30$	0				
		Zone Size (mm)		Acceptable Qty																							
			A	B	C																						
$\Phi \leq 0.1$	Ignore																										
$0.10 < \Phi \leq 0.20$	3( distance $\geq 10\text{mm}$ )																										
$0.20 < \Phi \leq 0.30$	2																										
$\Phi > 0.30$	0																										
③ Polarizer accidented spot <table border="1" data-bbox="487 1134 1291 1396"> <thead> <tr> <th rowspan="2">Zone Size (mm)</th> <th colspan="3">Acceptable Qty</th> </tr> <tr> <th>A</th> <th>B</th> <th>C</th> </tr> </thead> <tbody> <tr> <td><math>\Phi \leq 0.2</math></td> <td colspan="3">Ignore</td> </tr> <tr> <td><math>0.3 &lt; \Phi \leq 0.5</math></td> <td colspan="3">2( distance <math>\geq 10\text{mm}</math>)</td> </tr> <tr> <td><math>\Phi &gt; 0.5</math></td> <td colspan="3">0</td> </tr> </tbody> </table>	Zone Size (mm)	Acceptable Qty			A	B	C	$\Phi \leq 0.2$	Ignore			$0.3 < \Phi \leq 0.5$	2( distance $\geq 10\text{mm}$ )			$\Phi > 0.5$	0										
Zone Size (mm)		Acceptable Qty																									
	A	B	C																								
$\Phi \leq 0.2$	Ignore																										
$0.3 < \Phi \leq 0.5$	2( distance $\geq 10\text{mm}$ )																										
$\Phi > 0.5$	0																										
Line defect (LCD/TP/Polarizer black/white line, scratch, stain)	<table border="1" data-bbox="487 1459 1291 1795"> <thead> <tr> <th rowspan="2">Width(mm)</th> <th rowspan="2">Length(mm)</th> <th colspan="3">Acceptable Qty</th> </tr> <tr> <th>A</th> <th>B</th> <th>C</th> </tr> </thead> <tbody> <tr> <td><math>\Phi \leq 0.03</math></td> <td>Ignore</td> <td colspan="2">Ignore</td> <td rowspan="3">Ignore</td> </tr> <tr> <td><math>0.03 &lt; W \leq 0.05</math></td> <td><math>L \leq 3.0</math></td> <td colspan="2"><math>N \leq 2</math></td> </tr> <tr> <td><math>0.05 &lt; W \leq 0.08</math></td> <td><math>L \leq 2.0</math></td> <td colspan="2"><math>N \leq 2</math></td> </tr> <tr> <td><math>0.08 &lt; W</math></td> <td colspan="4">Define as spot defect</td> </tr> </tbody> </table>	Width(mm)	Length(mm)	Acceptable Qty			A	B	C	$\Phi \leq 0.03$	Ignore	Ignore		Ignore	$0.03 < W \leq 0.05$	$L \leq 3.0$	$N \leq 2$		$0.05 < W \leq 0.08$	$L \leq 2.0$	$N \leq 2$		$0.08 < W$	Define as spot defect			
Width(mm)	Length(mm)			Acceptable Qty																							
		A	B	C																							
$\Phi \leq 0.03$	Ignore	Ignore		Ignore																							
$0.03 < W \leq 0.05$	$L \leq 3.0$	$N \leq 2$																									
$0.05 < W \leq 0.08$	$L \leq 2.0$	$N \leq 2$																									
$0.08 < W$	Define as spot defect																										

3.0	Polarizer Bubble	Zone			Acceptable Qty		
		Size (mm)		A	B	C	
		$\Phi \leq 0.2$		Ignore			Ignore
		$0.2 < \Phi \leq 0.4$		3 (distance $\geq 10$ m)			
		$0.4 < \Phi \leq 0.6$		2			
$0.6 < \Phi$		0					
4.0	SMT	According to IPC-A-610C class II standard . Function defect and missing part are major defect ,the others are minor defect.					

		TP bubble/ accidented spot	Size $\Phi$ (mm)		Acceptable Qty			
					A	B	C	
			$\Phi \leq 0.1$		Ignore			Ignore
			$0.1 < \Phi \leq 0.25$		3 (distance $\geq$			
			$0.25 < \Phi \leq 0.3$		2			
$0.3 < \Phi$		0						
		Assembly deflection	beyond the edge of backlight $\leq 0.15$ mm					

5.0	TP Related	Newton Ring	Newton Ring area > 1/3 TP area NG			 1 规律性  2 非规律性  似牛顿环	Newton Ring area ≤ 1/3 TP area OK		
			TP corner broken X : length Y : width Z : height	X	Y		Z		
				X ≤ 3.0mm	Y ≤ 3.0mm		Z < LCD thickness		Circuitry broken is not allowed.
TP edge broken X : length Y : width Z : height	X	Y	Z						
	X ≤ 6.0mm	Y ≤ 2.0mm	Z < LCD thickness		* Circuitry broken is not allowed.				

Criteria ( functional items)

Number	Items	Criteria (mm)
1	No display	Not allowed
2	Missing segment	Not allowed
3	Short	Not allowed
4	Backlight no lighting	Not allowed
5	TP no function	Not allowed

## 9. Reliability Test Result

### 9.1 Condition

Item	Condition	Sample Size	Test Result	Note
Low Temperature Operating Life test	-20°C, 96HR	3ea	pass	-
Thermal Humidity Operating Life test	70°C90%RH, 96HR	3ea	pass	-
Temperature Cycle ON/OFF test	-20°C ↔ 70°C, ON/OFF, 20CYC	3ea	pass	(1)
High Temperature Storage test	80°C, 96HR	3ea	pass	-
Low Temperature Storage test	- 30°C, 96HR	3ea	pass	-
ESD test	150pF, 330Ω, ±6KV(Contact)/± 8KV(Air), 5 points/panel, 10 times/point	3ea	pass	
Thermal Shock Resistance	The sample should be allowed to stand the following 5 cycles of operation: TSTL for 30 minutes -> normal temperature for 5 minutes -> TSTH for 30 minutes -> normal temperature for 5 minutes, as one cycle, then taking it out and drying it at normal temperature, and allowing it stand for 24 hours	3ea	pass	
Box Drop Test	1 Corner 3 Edges 6 faces, 66cm(MEDIUM BOX)	1box	pass	-

Note (1) ON Time over 10 seconds, OFF Time under 10 seconds



## 10. Cautions and Handling Precautions

### 10.1 Handling and Operating the Module

(1) When the module is assembled, it should be attached to the system firmly.

Do not warp or twist the module during assembly work.

(2) Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.

(3) Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.

(4) Do not allow drops of water or chemicals to remain on the display surface.

If you have the droplets for a long time, staining and discoloration may occur.

(5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.

(6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane.

Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.

(8) Protect the module from static; it may cause damage to the CMOS ICs.

(9) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.

(10) Do not disassemble the module.

(11) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.

(12) Pins of I/F connector shall not be touched directly with bare hands.

(13) Do not connect, disconnect the module in the "Power ON" condition.

(14) Power supply should always be turned on/off by the item 6.1 Power On Sequence & 6.2 Power Off Sequence

### 10.2 Storage and Transportation.

(1) Do not leave the panel in high temperature, and high humidity for a long time.

It is highly recommended to store the module with temperature from 0 to 35 °C and relative humidity of less than 70%

(2) Do not store the TFT-LCD module in direct sunlight.

(3) The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.

(4) It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module.

In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.

(5) This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.



## 11. Packing

---TBD-----

ISO 9001 : 2008 ISO/TS 16949 : 2009