NCP1654

Product Preview

Power Factor Controller for Compact and Robust, Continuous Conduction Mode Pre-Converters

The NCP1654 is a controller for Continuous Conduction Mode (CCM) Power Factor Correction step−up pre−converters. It controls the power switch conduction time (PWM) in a fixed frequency mode and in dependence on the instantaneous coil current.

Housed in a DIP8 or SO8 package, the circuit minimizes the number of external components and drastically simplifies the PFC implementation. It also integrates high safety protection features that make the NCP1654 a driver for robust and compact PFC stages like an effective input power runaway clamping circuitry.

Features

- IEC1000−3−2 Compliant
- Average Current Continuous Conduction Mode
- Fast Transient Response
- Very Few External Components
- Very Low Startup Currents (<75 μA)
- Very Low Shutdown Currents (< 400 μA)
- Low Operating Consumption
- ±1.5 A Totem Pole Gate Drive
- Accurate Fully Integrated 65 kHz Oscillator
- Latching PWM for cycle−by−cycle Duty−Cycle Control
- Internally Trimmed Internal Reference
- 2 versions of Undervoltage Lockout with Hysteresis
- Soft−Start for Smoothly Startup Operation (B version only)
- Shutdown Function

Safety Features

- Inrush Currents Detection
- Overvoltage Protection
- Undervoltage Detection for Open Loop Detection (shutdown)
- Brown−Out Detection
- Soft−Start
- Accurate Overcurrent Limitation
- True Overpower Limitation

Typical Applications

- TV, Monitors, PC Desktop SMPS
- AC Adapters SMPS
- White Goods, other Off−line SMPS

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

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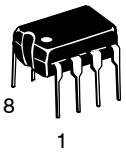
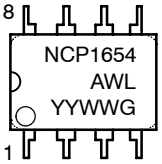
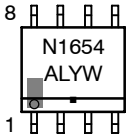
MARKING DIAGRAMS



PDIP−8
P SUFFIX
CASE 626

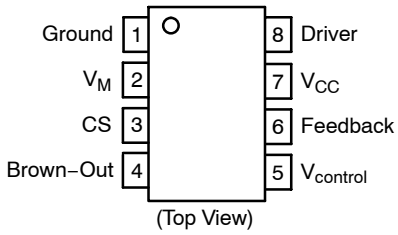


SO−8
D SUFFIX
CASE 751



NCP1654,
N1654 = Device Code
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
▪ or G = Pb−Free Package

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

Maximum Ratings Table

Symbol	Pin	Rating	Value	Unit
DRV	8	Output Drive Capability − Source Output Drive Capability − Sink	−1.5 +1.5	A
V_{CC}	7	Power Supply voltage, V_{CC} pin, continuous voltage	−0.3, +20	V
	7	Transient Power Supply voltage, duration < 10 ms, IV_{CC} < 10 mA	+25	V
Vin	2, 3, 4, 5, 6	Input Voltage	−0.3, +10	V
		Power Dissipation and Thermal Characteristics		
		P suffix, Plastic Package, Case 626		
P_D(DIP)		Maximum Power Dissipation @ T_A = 70°C	800	mW
$R_{\theta JA}$(DIP)		Thermal Resistance Junction−to−Air	100	°C/W
		D suffix, Plastic Package, Case 751		
P_D(SO)		Maximum Power Dissipation @ T_A−=−70°C	450	mW
$R_{\theta JA}$(SO)		Thermal Resistance Junction to Air	178	°C/W
T_J		Operating Junction Temperature Range	−40 to +125	°C
T_{Jmax}		Maximum Junction Temperature	150	°C
T_{Smax}		Storage Temperature Range	−65 to +150	°C
T_{Lmax}		Lead Temperature (Soldering, 10 s)	300	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. This device series contains ESD protection and exceeds the following tests:
   Pins 1 − 8: Human Body Model 2000 V per MIL−STD−883, Method 3015.
   Machine Model Method 200 V (except pin#7 which complies 150 V)
2. This device contains Latch−up Protection and exceeds ±100 mA per JEDEC Standard JESD78.

Typical Electrical Characteristics Table (V_{CC} = 15 V, T_J from −40°C to +125°C, unless otherwise specified) (Note 3)

Symbol	Rating	Min	Typ	Max	Unit
GATE DRIVE SECTION					
Rsource	Source Resistance @ Ipin8 = 100 mA	–	9	20	Ω
Rsink	Sink Resistance @ Ipin8 = −100 mA	–	6.6	18	Ω
T_{rise}	Gate Drive Voltage Rise Time from 1.5 V to 13.5 V (C_L = 2.2 nF)	–	60	–	ns
T_{fall}	Gate Drive Voltage Fall Time from 13.5 V to 1.5 V (C_L = 2.2 nF)	–	40	–	ns
REGULATION BLOCK					
Vref	Voltage Reference	2.425	2.5	2.575	V
I_{EA}	Error Amplifier Current Capability	–	±20	–	μA
G_{EA}	Error Amplifier Gain	100	200	300	μS
IBpin6	Pin 6 Bias Current @ V_{FB} = Vref	−500	–	500	nA
Vcontrol Vcontrol(max) Vcontrol(min) ΔVcontrol	Pin5 Voltage Maximum Control Voltage @ V_{FB} = 2 V Minimum Control Voltage @ V_{FB} = 3 V	– – 2.7	3.7 0.7 3	– – 3.3	V
VoutL / Vref	Ratio (Vout Low Detect Thresold / Vref)	94	95	96	%
HoutL / Vref	Ratio (Vout Low Detect Hysteresis / Vref)	–	0.5	–	%
I_{BOOST}	Pin 5 Source Current when (Vout Low Detect) is activated	180	220	250	μA
CURRENT SENSE BLOCK					
V_S	Current Sense Pin Offset Voltage, (I_{CS} = 100 μA)	–	10	–	mV
$I_{S(OCP)}$	Over−Current Protection Threshold	185	200	215	μA
POWER LIMITATION BLOCK					
I_{CS} x Iin	Over Power Limitation Threshold $\left(= I_{CS} \times \frac{V_{BO}}{2 \times R} \right)$	–	4	–	nA^2
$I_{CS(OPL1)}$ $I_{CS(OPL2)}$	Over−Power Current Threshold (V_{BO} = 0.9 V, V_M = 3 V) Over−Power Current Threshold (V_{BO} = 2.67 V, V_M = 3 V)	174 56	222 75	308 110	μA
PWM BLOCK					
Dcycle	Duty Cycle Range		0−97		%
OSCILLATOR / RAMP GENERATOR BLOCK					
Fsw	Switching Frequency	58	65	72	kHz
BROWN−OUT DETECTION BLOCK					
$V_{BO}H$	Brown−Out VoltageThreshold (rising)	TBD	1.3	TBD	V
$V_{BO}L$	Brown−Out Voltage Threshold (falling)	0.65	0.7	0.75	V
I_{IB}	Pin 4 Input Bias Current @ V_{BO} = 1 V	−500	–	500	nA
CURRENT MODULATION BLOCK					
I_{M1} I_{M2} I_{M3} I_{M4}	Multiplier Output Current ($V_{control}$ = $V_{control(max)}$, V_{BO} = 0.9 V, I_{CS} = 25 μA Multiplier Output Current ($V_{control}$ = $V_{control(max)}$, V_{BO} = 0.9 V, I_{CS} = 75 μA Multiplier Output Current ($V_{control}$ = $V_{control(min)}$ + 0.2 V, V_{BO} = 0.9 V, I_{CS} = 25 μA Multiplier Output Current ($V_{control}$ = $V_{control(min)}$ + 0.2 V, V_{BO} = 0.9 V, I_{CS} = 75 μA	0.7 2.1 8.3 24.2	1.9 5.6 28.1 84.4	3.8 10.3 46.4 146	μA
OVER−VOLTAGE PROTECTION					
V_{OVP} / Vref	Ratio (Over Voltage Threshold / Vref)	103	105	107	%
T_{OVP}	Propagation Delay (V_{FB} − 107% Vref) to Drive Low	–	500	–	ns

3. The above specification gives the targeted values of the parameters. The final specification will be available once the complete circuit characterization has been performed.

Typical Electrical Characteristics Table (V_{CC} = 15 V, T_J from −40°C to +125°C, unless otherwise specified) (Note 3)

Symbol	Rating	Min	Typ	Max	Unit
UNDER−VOLTAGE PROTECTION / SHUTDOWN					
$V_{UVP(on)}$/Vref	UVP Activate Threshold Ratio (T_J = 0°C to +105°C)	4	8	12	%
$V_{UVP(off)}$/Vref	UVP Deactivate Threshold Ratio (T_J = 0°C to +105°C)	6	12	18	%
$V_{UVP(H)}$	UVP Lockout Hysteresis	–	4	–	%
T_{UVP}	Propagation Delay (V_{FB} < 8% Vref) to Drive Low	–	500	–	ns
THERMAL SHUTDOWN					
T_{limit}	Thermal Shutdown Threshold	150	–	–	°C
H_{temp}	Thermal Shutdown Hysteresis	–	30	–	°C
V_{CC} UNDER−VOLTAGE LOCKOUT SECTION					
V_{stup}	Start−Up Threshold (Under−Voltage Lockout Threshold, V_{CC} rising) − Version A − Version B	12.5 9.6	13.75 10.5	15 11.4	V
$V_{disable}$	Disable Voltage after Turn−On (Under−Voltage Lockout Threshold, V_{CC} falling) Version A & B	8.25	9	9.75	V
H_{UVLO}	Under−Voltage Lockout Hysteresis − Version A − Version B	4 1	4.75 1.5	– –	V
DEVICE CONSUMPTION					
	Power Supply Current:				
I_{cc_stup}	Start−Up (@ V_{CC} = 12.4 V, version A and V_{CC} = 9.4 V, version B)	–	–	75	μA
I_{cc_op1}	Operating (@ V_{CC} = 15 V, no load, no switching)	–	3.7	5	mA
I_{cc_op2}	Operating (@ V_{CC} = 15 V, no load, switching)	–	4.7	6	mA
I_{cc_stdwn}	Shutdown Mode (@ V_{CC} = 15 V and V_{FB} = 0 V)	–	300	400	μA

3. The above specification gives the targeted values of the parameters. The final specification will be available once the complete circuit characterization has been performed.

NOTE: $I_M = \frac{I_{cs} \times I_{in}}{2 \times I_{control}}$, $I_{in} = \frac{V_{BO}}{2 \times R}$, $I_{control} = \frac{V_{control} - V_f}{R}$

Detailed Pin Description(s)

Pin Number	Name	Function
6	Feed−Back / Shutdown	This pin receives a feedback signal V_{FB} that is proportional to the PFC circuits output voltage. This information is used for both the output regulation, the over−voltage protection (OVP), and output undervoltage protection (UVP). When V_{FB} goes above 105% Vref, OVP is activated and the Drive Output is disabled. When V_{FB} goes below 8% Vref, the device enters a low−consumption shutdown mode.
5	Vcontrol / Soft−Start	The voltage of this pin Vcontrol directly controls the input impedance and hence the power factor of the circuit. This pin is connected to an external capacitor Ccontrol to limit the Vcontrol bandwidth typically below 20 Hz to achieve near unity power factor. The device provides no output when Vcontrol < 0.7 V. Vcontrol is grounded when the circuits is off. In B version, when it starts to operate, Vcontrol raises slowly by inside 20 μA current source after V_{FB} is higher than 95% of Vref, which obtains a linear control of the increasing duty cycle as a function of time. Hence reduce the voltage and current stress on the MOSFET. Soft Start function is achieved. In A version, when it starts to operate, Vcontrol raises rapidly by inside 200 μA current source. It is to boost the PFC output in a short time before the operation of the converter behind the PFC stage.
4	Brown−Out / In	Connect a resistor network among the rectified input voltage, pin4, and ground. And connect a capacitor between pin4 and ground. Pin4 detects a voltage signal proportional to the average input voltage. When V_{BO} goes below 0.7 V, the circuit that detects too low input voltage conditions (brown−out), turns off the output driver and keeps it in low state till V_{BO} exceeds 1.3 V (0.6 V hysteresis). This signal which is proportional to the RMS input voltage Vac is also for over−power limitation (OPL) and PFC duty cycle modulation. When the product $I_{CS} \times \frac{V_{BO}}{2 \times R} > 4nA^2$, OPL is activated and the Drive Output duty ratio is reduced by pulling down Vcontrol indirectly to reduce the input power.
3	Current Sense Input	This pin sources a current I_{CS} which is proportional to the inductor current I_L. The sense current I_{CS} is for over−current protection (OCP), over−power limitation (OPL) and PFC duty cycle modulation. When I_{CS} goes above 200 μA, OCP is activated and the Drive Output is disabled.
2	Multiplier Voltage	This pin provides a voltage V_M for the PFC duty cycle modulation. The input impedance of the PFC circuits is proportional to the resistor R_M externally connected to this pin. The device operates in average current mode if an external capacitor C_M is connected to the pin. Otherwise, it operates in peak current mode.
1	Ground	−
8	Drive	The high current capability of the totem pole gate drive (±1.5 A) makes it suitable to effectively drive high gate charge power MOSFET.
7	V_{CC}	This pin is the positive supply of the IC. The circuit typically starts to operate when V_{CC} exceeds 13.75 V (version A), 10.5 V (version B) and turns off when V_{CC} goes below 9 V. After start−up, the operating range is 9 V up to 20 V.

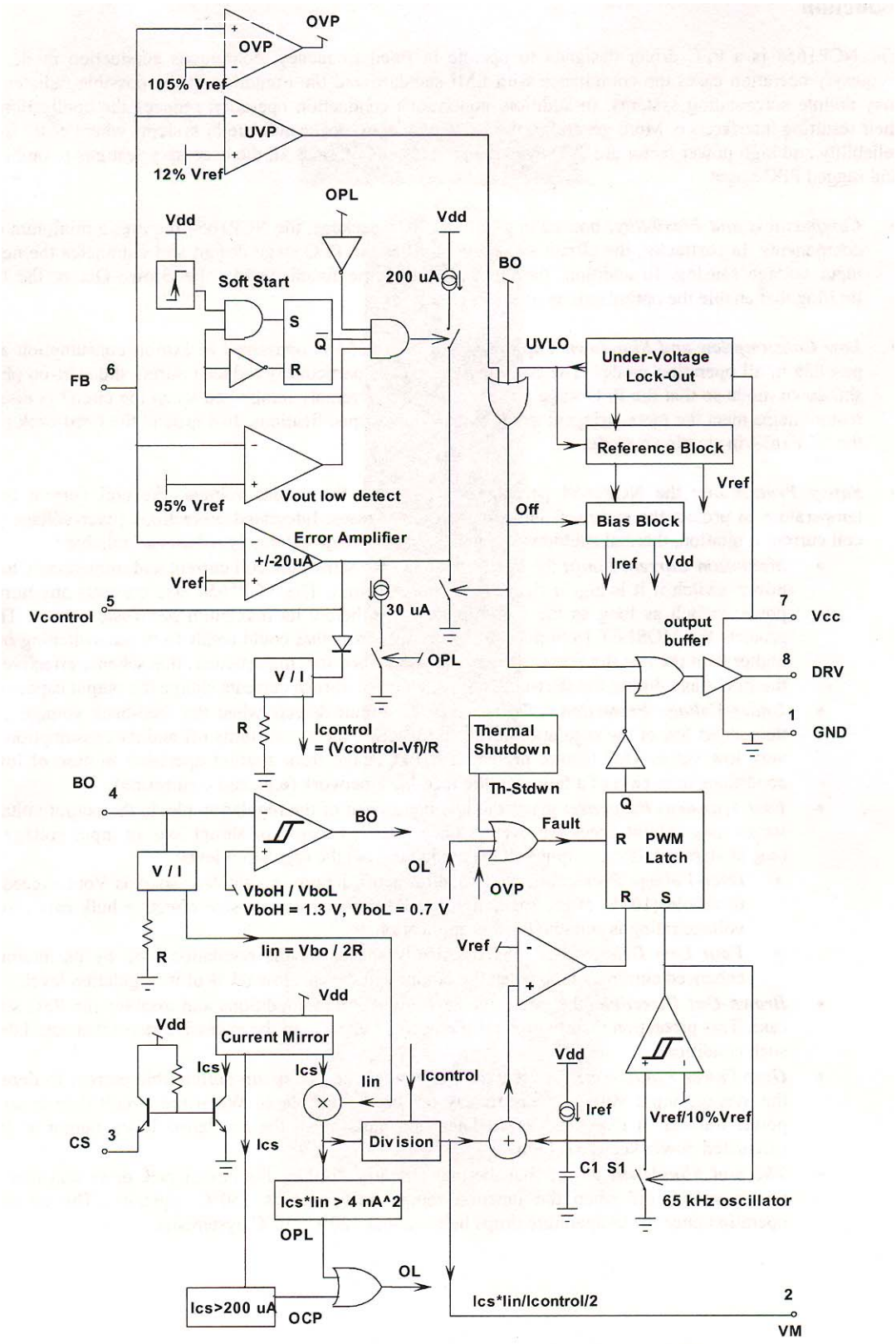


Figure 1. Block Diagram

DETAILED OPERATING DESCRIPTION

Introduction

The NCP1654 is a PFC driver designed to operate in fixed frequency, continuous conduction mode. The fixed frequency operation eases the compliance with EMI standard and the limitation of the possible radiated noise that may pollute surrounding systems. In addition, continuous conduction operation reduces the application dI/dt and their resulting interference. More generally, the NCP1654 is an ideal candidate in systems where cost−effectiveness, reliability and high power factor are the key parameters. It incorporates all the necessary features to build a compact and rugged PFC stage:

- **Compactness and Flexibility:** housed in a DIP8 or SO8 package, the NCP1654 requires a minimum of external components. In particular, the circuit scheme simplifies the PFC stage design and eliminates the need for any input voltage sensing. In addition, the circuit offers some functions like the Brown−Out or the true power limiting that enable the optimizations of the PFC design,
- **Low Consumption and Shutdown Capability:** the NCP1654 is optimized to exhibit consumption as small as possible in all operation modes. The consumed current is particularly reduced during the start−up phase and in shutdown mode so that the PFC stage power losses are extremely minimized when the circuit is disabled. This feature helps meet the more stringent stand−by low power specifications. Just ground the Feed−back pin to force the NCP1654 in shutdown mode,
- **Safety Protections:** the NCP1654 permanently monitors the output voltage, the coil current and the die temperature to protect the system from possible over−stresses. Integrated protections (over−voltage protection, coil current limitation, thermal shutdown…) make the PFC stage extremely robust and reliable:
  - **Maximum Current Limit:** the circuit permanently senses the coil current and immediately turns off the power switch if it is higher than the set current limit. The NCP1654 also prevents any turn on of the power switch as long as the coil current is not below its maximum permissible level. This feature protects the MOSFET from possible excessive stress that could result from the switching of a current higher than the one the power switch is dimensioned for. In particular, this scheme effectively protects the PFC stage during the start−up phase when large in−rush currents charge the output capacitor,
  - **Under−Voltage Protection / Shut−down:** the circuit detects when the feed−back voltage goes below than about 8% of the regulation level. In this case, the circuit turns off and its consumption drops to a very low value. This feature protects the PFC stage from starting operation in case of low AC line conditions or in case of a failure in the feed−back network (e.g., bad connection),
  - **Fast Transient Response:** given the low bandwidth of the regulation block, the output voltage of PFC stages may exhibit excessive over or under−shoots because of abrupt load or input voltage variations (e.g. at start up). If the output voltage is too far from the regulation level:
    - *Over−Voltage Protection:* NCP1654 turns off the power switch as soon as Vout exceeds the OVP threshold (105% of the regulation level). Hence a cost & size effective bulk capacitor of lower voltage rating is suitable for this application,
    - *Vout Low Detect:* NCP1654 drastically speeds up the regulation loop by its internal 200 μA enhanced current source when the output voltage is below 95% of its regulation level.
  - **Brown−Out Detection:** the circuit detects low AC line conditions and disables the PFC stage in this case. This protection mainly protects the power switch from the excessive stress that could damage it in such conditions,
  - **Over−Power Limitation:** the NCP1654 computes the maximum permissible current in dependence of the average input voltage measured by the brown−out block. When the circuit detects an excessive power transfer, it resets the PWM latch and pulls down the regulation block output as long as the calculated power keeps too high,
  - **Thermal Shutdown:** an internal thermal circuitry disables the circuit gate drive and then keeps the power switch off when the junction temperature exceeds 150°C typically. The circuit resumes operation once the temperature drops below about 120°C (30°C hysteresis),
  - **Soft Start:** Vcontrol is pulled low as the IC is off, which V_{CC} is lower than UVLO off, brown−out detection activates, or under−voltage protection activates, and no drive is provided.
    The soft−start function is done by disable the "200 μA enhanced current source" at start up. So there is only 20 μA to charge the Ccontrol, and makes Vcontrol increase slowly. This is to obtain a slow increasing duty cycle and hence reduce the voltage and current stress on the MOSFET.
    This soft−start function is designed in **B version only. A version** doesn't have this soft−start function, because V_{CC} of A version is supposed to start up by the resistors connected to input voltage and should be able to boost the PFC output as soon as possible before the 2nd stage converter operates. So at start up period, Ccontrol will be charged by 220 μA current source and the PFC output will rise rapidly.
- **Output Stage Totem Pole:** the NCP1654 incorporates a ±1.5A gate driver to efficiently drive TO220 or TO247 power MOSFETs.

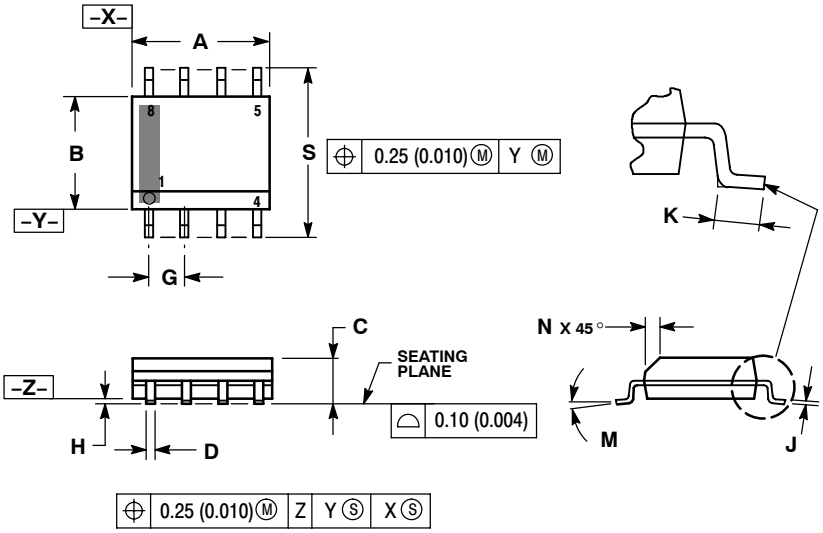
ORDERING INFORMATION

Device	Package	Shipping†
NCP1654P	PDIP−8	50 Units / Rail
NCP1654PG	PDIP−8 (Pb−Free)	50 Units / Rail
NCP1654DR2	SO−8	2500 Units / Tape & Reel
NCP1654DR2G	SO−8 (Pb−Free)	2500 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

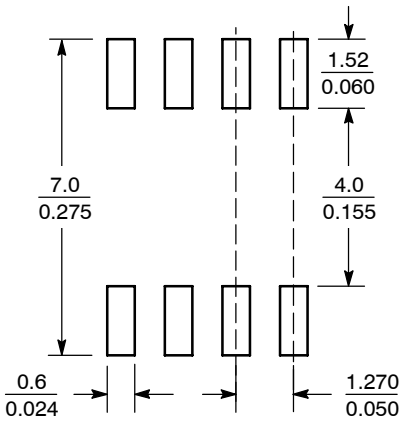
SO−8
D SUFFIX
CASE 751−07
ISSUE AG



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*

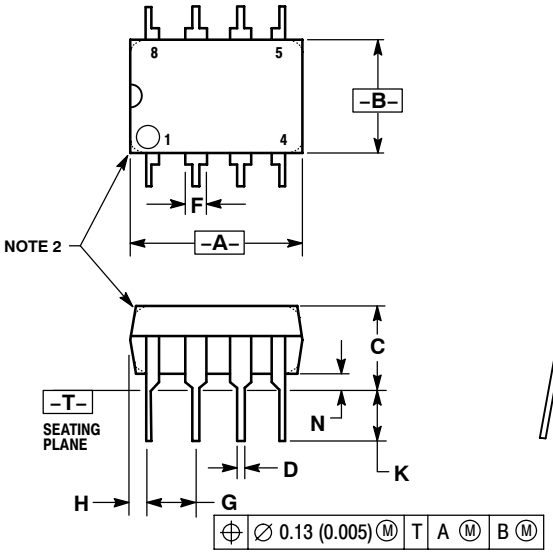


SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

PDIP−8
P SUFFIX
CASE 626−05
ISSUE L



NOTES:
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	---	10°	---	10°
N	0.76	1.01	0.030	0.040

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
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NCP1654/D