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CUSTOMER APPROVAL SHEET

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- fi **APPROVAL FOR SPECIFICATIONS ONLY (Spec. Ver. 1.0)**
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Product Specification

2.7" COLOR TFT-LCD MODULE

Model Name : A027DN04 V3

Planned Lifetime: From 2010/10/01 To 2011/12/31

Phase-out Control: From 2011/10/01 To 2011/12/31

EOL Schedule: 2011/12/31

< >Preliminary Specification

<◆>Final Specification

Note: The content of this specification is subject to change.

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Record of Revision

Version	Revise Date	Page	Content
0.0	2010/10/08		First draft
0.1	2010/10/22	51	P51 add silk line (module outline)
0.2	2010/11/02	7-8	Pin definition
		12	Add VL
		14-27	Timing table add minima and maximum setting
0.3	2010/11/10	30-32	Add R9, R10, R48-R79
		54	Application Circuit
0.4	2010/11/19	11	Update IVDD , VcomDC
		58-64	Update recommend power on/off command setting
0.5	2010/11/23	65	Update Gamma 2.2 Recommend Command Setting
1.0	2010/12/07	12	Update Backlight voltage 3.2 >6.4 V
		66-67	Add 5.1 S-Gamma setting (only reference)



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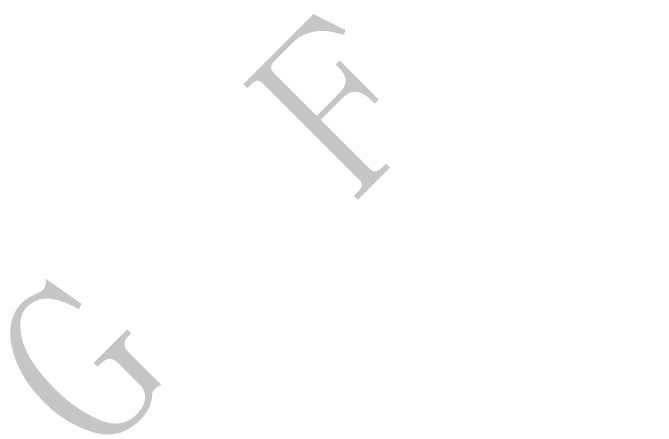
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A. Physical specifications

NO.	Item	Specification	Remark
1	Display resolution (dot)	960(W) x 240(H)	
2	Active area (mm)	54 x 40.5	
3	Screen size (inch)	2.658 (Diagonal)	
4	Dot pitch (um)	56.25 x 168.75	
5	Color configuration	R, G, B delta	
6	Overall dimension (mm)	63.5 x 46.6 x 2.2	Note 1
7	Weight (g)	18	
8	Panel surface treatment	HC	
9	IC		Raydium

Note 1: Refer to F. Outline Dimension



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B. Electrical specifications

1. Pin assignment

Pin no	Symbol	I/O	I/O Structure	Description	Remark
1	VCOM	I	-	Panel common voltage	
2	GRB	I	Type 4	Global reset bit	RST
3	CS	I	Type 4	Serial command enable	
4	SDA	I	Type 2	Serial command data input	
5	SCL	I	Type 3	Serial command clock input	
6	HSYNC	I	Type 1	Horizontal sync input	
7	VSYNC	I	Type 1	Vertical sync input	
8	DCLK	I	Type 1	Data clock input	DOTCLK
9	D7	I	Type 1	Data input; MSB	
10	D6	I	Type 1	Data input	
11	D5	I	Type 1	Data input	
12	D4	I	Type 1	Data input	
13	D3	I	Type 1	Data input	
14	D2	I	Type 1	Data input	
15	D1	I	Type 1	Data input	
16	D0	I	Type 1	Data input; LSB	
17	GND	P	-	Ground for digital circuit	GND
18	GND	P	-	Ground for digital circuit (LCD_ID)	GND
19	VDD	P	-	System power	3.0V~3.6V
20	VDDIO	P	-	System power	
21	DVDD	C	-	Power setting capacitor connect pin	
22	V1	C	-	Power setting capacitor connect pin	CP1P
23	V2	C	-	Power setting capacitor connect pin	CP1M
24	V3	C	-	Power setting capacitor connect pin	CP2P
25	V4	C	-	Power setting capacitor connect pin	CP2M
26	VDD2	C	-	Power setting capacitor connect pin	
27	V5	C	-	Power setting capacitor connect pin	CP3P
28	V6	C	-	Power setting capacitor connect pin	CP3M
29	VDD3	C	-	Power setting capacitor connect pin	
30	VDD5	C	-	Power setting capacitor connect pin	
31	V7	C	-	Power setting capacitor connect pin	CP4P
32	V8	C	-	Power setting capacitor connect pin	CP4M

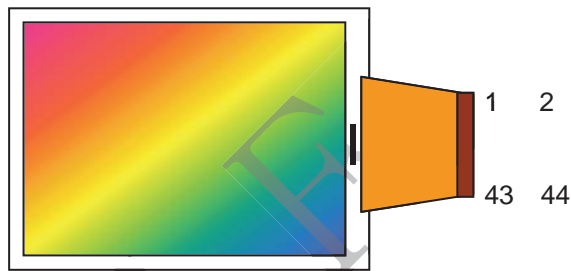


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33	GND	P	-	Ground for digital circuit	GND
34	VGL	C	-	Power setting capacitor connect pin	
35	FRP	O	Type 6	VCOM DC voltage output pin	
36	VGH	C	-	Power setting capacitor connect pin	
37	GND	P	-	Ground for digital circuit	GND
38	VDD	P	-	System power	3.0V~3.6V
39	VCOMDC	O	Type 5	VCOM DC voltage output pin	
40	LED+	P	-	LED power anode	
41	VCOMAC	O	Type 7	VLED boost transistor driving signal	
42	NC	D	-	No use	
43	VCOM	I	-	Panel common voltage	
44	LED-	P	Type 8	LED power cathode	

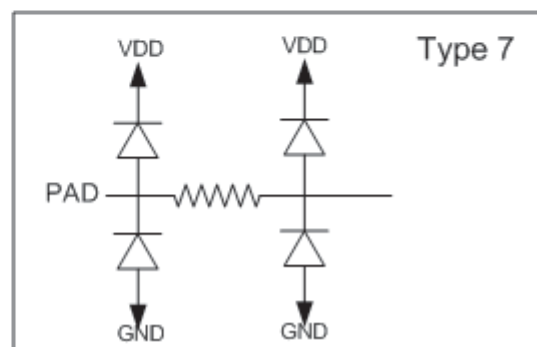
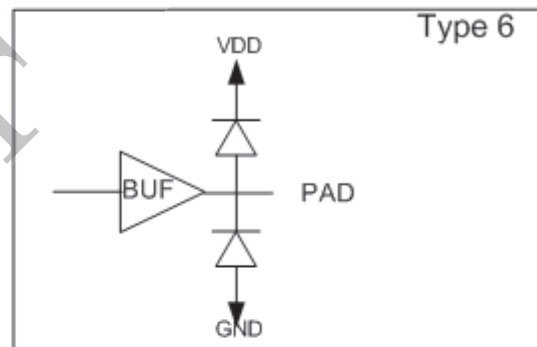
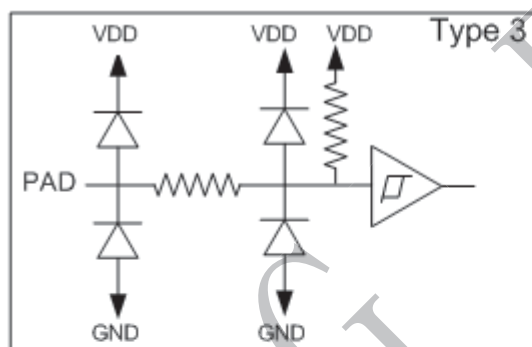
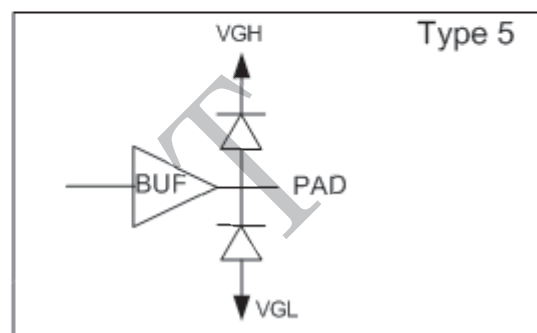
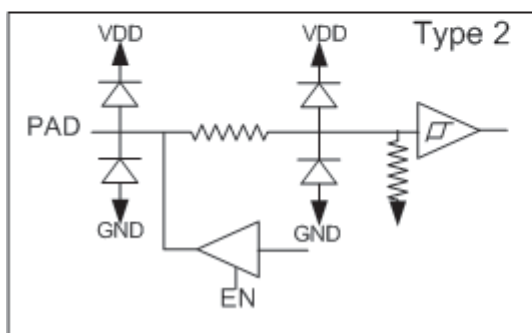
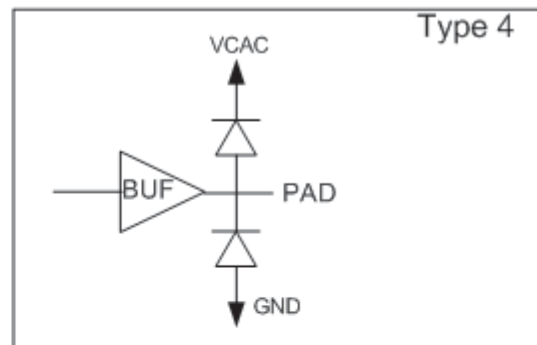
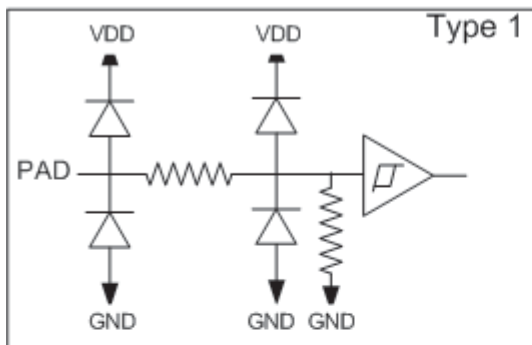
I : Input, O : Output, C : Capacitor, P : Power, D : Dummy

Note: Definition of scanning direction, Refer to figure as below :



I/O Pin Structure:

Pull high/low resistor is 700kΩ.





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2. Absolute maximum ratings

Item	Symbol	Condition	Min.	Max.	Unit	Remark
Supply Voltage	VDD	AGND=GND=0V	-0.3	4.5	V	
TFT-LCD Power Voltage	VGH	AGND=GND=0V	-0.3	16	V	
	VGL	AGND=GND=0V	-16	0.3	V	
Input Signal Voltage	CS,SDA,SCL,Vsync,Hsync,DCLK,D0~D7	AGND=GND=0V	-0.3	4.5	V	
VCOM AC Output Voltage	FRP	AGND=GND=0V	-0.3	8	V	
VCOM AC Power Voltage	VCAC	AGND=GND=0V	-0.3	8	V	
VCOM DC Output Voltage	COMDC	AGND=GND=0V	-0.3	8	V	
VCOM Input Voltage	VCOM	AGND=GND=0V	-0.3	8	V	
Charge Pump Voltage	VDD2	AGND=GND=0V	-0.3	8	V	
	VDD3	AGND=GND=0V	-0.3	16	V	
	VDD5	AGND=GND=0V	-0.3	20	V	
	V1	AGND=GND=0V	-0.3	8	V	
	V2	AGND=GND=0V	-0.3	8	V	
	V3	AGND=GND=0V	-0.3	8	V	
	V4	AGND=GND=0V	-0.3	8	V	
	V5	AGND=GND=0V	-0.3	16	V	
	V6	AGND=GND=0V	-0.3	16	V	
	V7	AGND=GND=0V	-0.3	16	V	
V8	AGND=GND=0V	-16	8	V		
Storage Temperature	Tstg	-	-25	80	°C	Ambient temperature
Operating Temperature	Topa	-	0	60	°C	Ambient temperature

3. Electrical characteristics

3.1 Recommended operating conditions (GND=AGND=0V)

Item	Symbol	Min.	Typ.	Max.	Unit	Remark	
Power supply	VDD	3.0	3.3	3.6	V	Note 1	
Input Signal	H Level	V_{IH}	$0.7 * VDD$	-	VDD	V	
	L Level	V_{IL}	GND	-	$0.3 * VDD$	V	

Note 1: A build-in power on reset circuit for VDD is provided within the integrated LCD driver IC. The LCD module is in power save mode in default, and a standby releasing is required after VDD power on through serial control. Please refer to the register STB setting for detail.

3.2 Electrical characteristics (GND=AGND=0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Input Current for VDD	I_{DD}	$V_{DD}=3.3V$	-	3.5	5.5	mA	Note 1
	$I_{DD(STANDBY)}$		-	0.005	-		Note 1
DC-DC voltage	V_{GH}	$V_{DD}=3.3V$	-	13	-	V	Note 2
	V_{GL}	$V_{DD}=3.3V$	-	-10	-	V	Note 2
VCOM voltage	V_{CAC}	-	3.6	4.2	4.8	Vp-p	AC component, Note 3
	V_{CDC}	-	-	0.34	-	V	DC component, Note 4

Note 1: Test Condition: 8colorbar+Grayscale pattern, UPS051 mode, DCLK=27MHz, Frame rate: 60Hz, other registers are default setting.

Note 2: V_{GH} and V_{GL} are output voltages of integrated LCD driver IC.

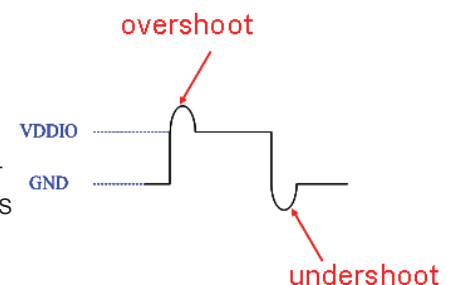
Note 3: The brightness of LCD panel could be adjusted by the adjustment of the AC component of VCOM.

Note 4: V_{CDC} could be adjusted, so as to minimize flicker and maximum contrast on each module.

3.3 Digital input signal overshoot and undershoot limitation

The digital input signal overshoot and undershoot voltage should keep under $VDDIO+0.5V$ and over $GND-0.5V$.

Symbol	Overshoot	Undershoot
D0-D7	$< VDDIO+0.5V$	$> GND-0.5V$
DCLK		
HSYNC		
VSYNC		
SCL		
SDA		
CS		



3.4 Recommended Capacitance Values of External Capacitor

The recommended capacitance values of the external capacitor are shown below. These values should be finally determined only after performing sufficient evaluation on the module.

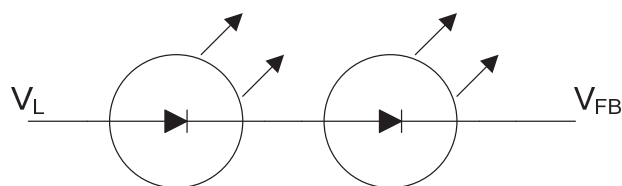
Pin name	Recommended value of capacitors (μF)	Withstanding voltage (V)
VGH	4.7 to 10	25
VGL	4.7 to 10	16
VDD5	4.7 to 10	25
VDD3	4.7 to 10	16
VDD2	4.7 to 10	10
DVDD	4.7 to 10	6.3
VCAC	4.7 to 10	10
V1, V2	2.2 to 10	10
V3, V4	2.2 to 10	10
V5, V6	2.2 to 10	16
V7, V8	2.2 to 10	16

3.5 Backlight driving conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Backlight current			25	27.5	mA	Note 1,2
Backlight voltage	V_L		6.4		V	2 LED
Feedback voltage	V_{FB}	-	0.75	-	V	

Note1: To consider LED driver and feedback resistor tolerance.

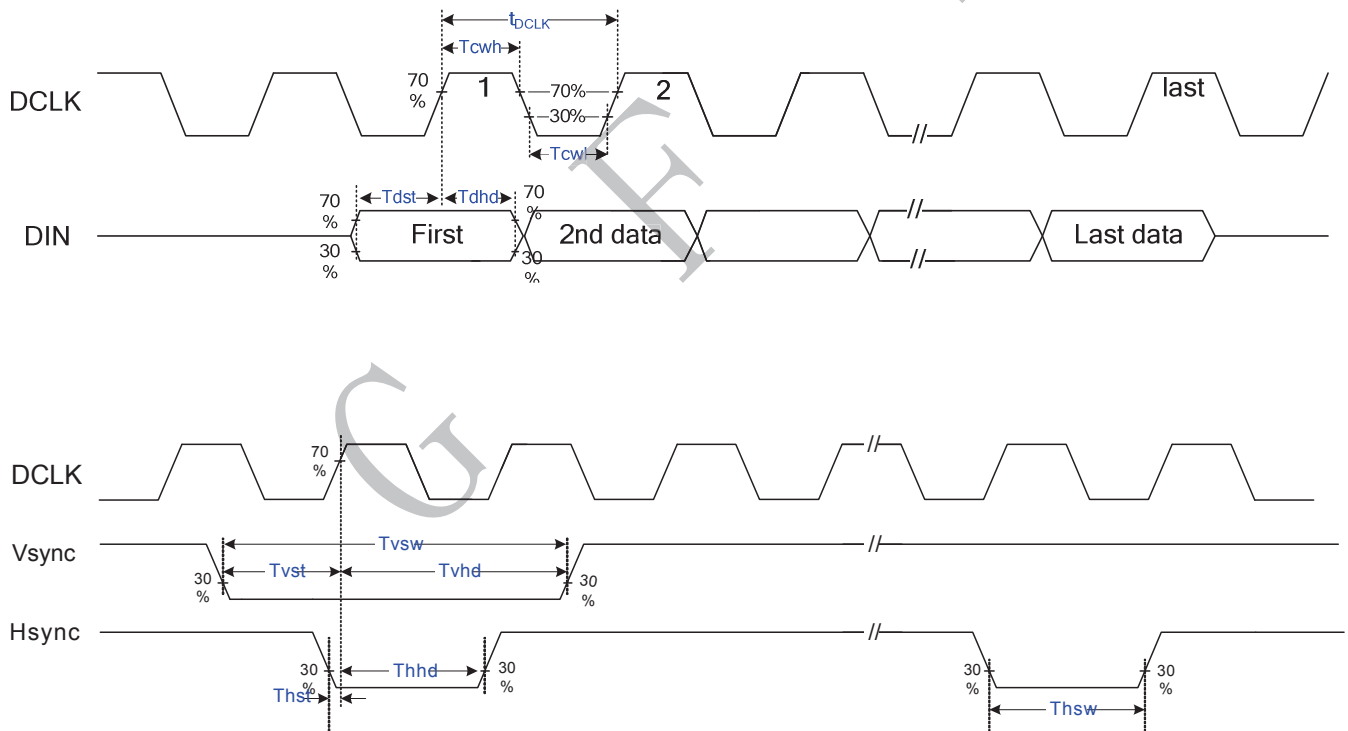
Note2: If using LCD internal LED driver controller the maximum setting should be 25mA. $T_a=25^\circ\text{C}$



4. Input timing AC characteristic

(VDD=3.0 ~3.6V, AGND=GND=0V, TA=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
DCLK duty cycle	Tcw	40	50	60	%	
VSYNC setup time	Tvst	6	-	-	ns	
VSYNC hold time	Tvhd	6	-	-	ns	
HSYNC setup time	Thst	6	-	-	ns	
HSYNC hold time	Thhd	6	-	-	ns	
Data setup time	Tdst	6	-	-	ns	
Data hold time	Tdhd	6	-	-	ns	
HSYNC width	Thsw	1	1	254	t_{DCLK}	
VSYNC width	Tvsw	$1 t_{DCLK}$	$1 t_{DCLK}$	$6t_H$		





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5. Input timing format

5.1 UPS051 timing conditions (Refer to Fig.1 Fig.2 Fig.3)

Parameter		Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency		$1/t_{DCLK}$	13.5	27	27.19	MHz	
HSYNC	Period	t_H	1024	1716	1728	t_{DCLK}	
	Display period	t_{hd}	960			t_{DCLK}	
	Back porch	t_{hbp}	50	70	255	t_{DCLK}	Note 1
	Front porch	t_{hfp}	$t_H - t_{hd} - t_{hbp}$			t_{DCLK}	
	Pulse width	t_{hsw}	1	1	$t_{hbp} - 1$	t_{DCLK}	
VSYNC	Period	Odd	242.5	262.5	450.5	t_H	
		Even					
	Display period	Odd	240	t_H			
		Even					
	Back porch	Odd	1	21	31	t_H	
		Even	1.5	21.5	31.5		
	Front porch	Odd	t_{vfp}	$t_V - t_{vd} - t_{vb}$			
Even							
Pulse width	Odd	t_{vsw}	$1 t_{DCLK}$	$1 t_{DCLK}$	$6 t_H$		
	Even						
1 frame			485	525	901	t_H	

Note 1: The t_{hbp} time is adjustable by setting register HBLK; requirement of minimum blanking time and minimum front porch time must be satisfied.

Note 2: The t_{vbp} time is adjustable by setting register VBLK. UPS051 accepts both interlace and non-interlace vertical input timing.

Fig.1 UPS051 Input Horizontal Timing Chart

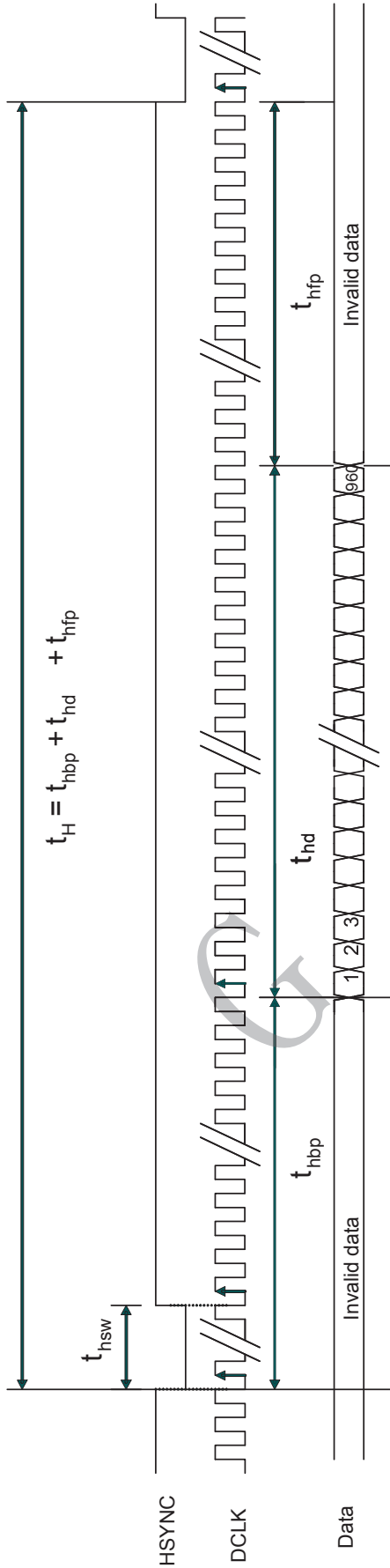


Fig.2 UPS051 Input Horizontal Data Sequence

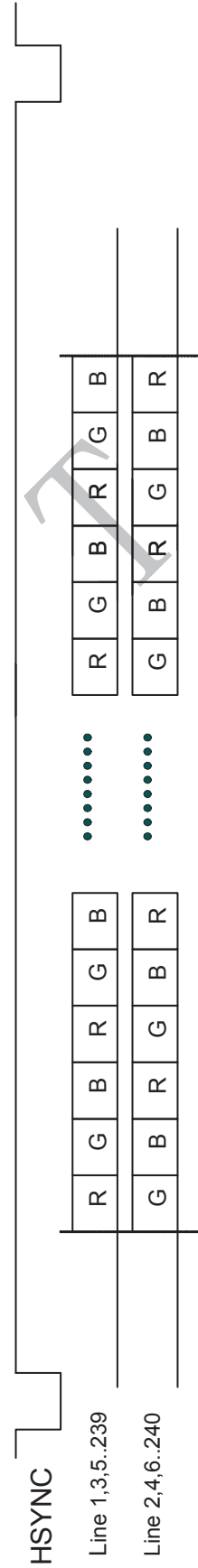
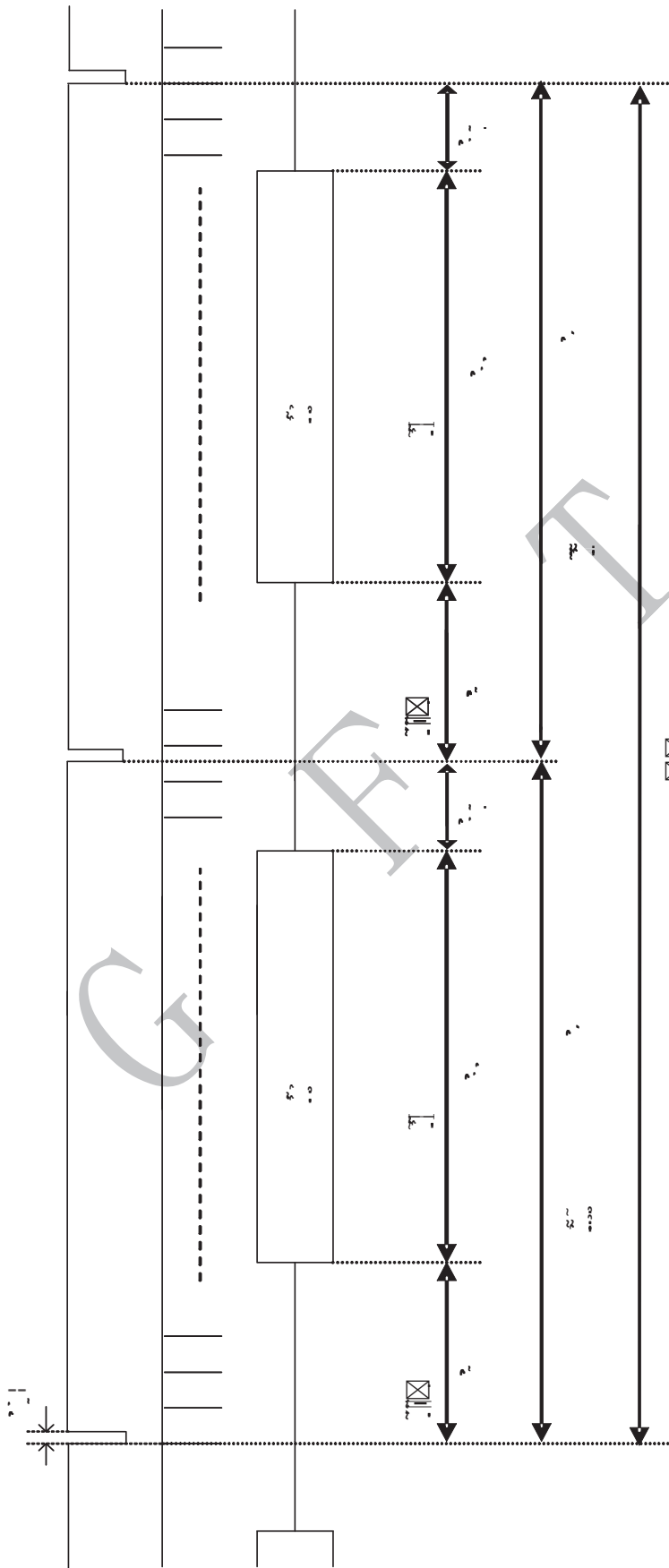


Fig.3 UPS051 Input Vertical Timing Chart





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5.2 UPS052 timing

5.2.1 UPS052 (320 mode/NTSC/24.535MHz) timing specifications. (refer to Fig.4 Fig.5)

Parameter		Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency		$1/t_{DCLK}$	20.54	24.535	30	MHz	
HSYNC	Period	t_H	1306	1560	1907	t_{DCLK}	t_{hbp} must > $15 t_{DCLK}$
	Display period	t_{hd}	1280	1280	1280	t_{DCLK}	
	Back porch	t_{hbp}	15	241	255	t_{DCLK}	
	Front porch	t_{hfp}	$t_H - t_{hd} - t_{hbp}$			t_{DCLK}	
	Pulse width	t_{hsw}	1	1	200	t_{DCLK}	
VSYNC	Period	Odd	t_V	242.5	262.5	450.5	t_H
		Eve					
	Display period	Odd	t_{vd}	240	240	240	t_H
		Eve					
	Back porch	Odd	t_{vbp}	1	21	31	t_H
		Eve		1.5	21.5	31.5	
	Front porch	Odd	t_{vfp}	$t_V - t_{vd} - t_{vb}$			t_H
Eve							
Pulse width	Odd	t_{vsw}	$1 t_{DCLK}$	$1 t_{DCLK}$	$6 t_H$	t_{DCLK}	
	Eve						
1 frame			485	525	901	t_H	

5.2.2 UPS052 (320 mode/PAL/24.375MHz) timing specifications (refer to Fig.4 Fig.5)

Parameter		Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency		$1/t_{DCLK}$	20.4	24.375	30	MHz	
HSYNC	Period	t_H	1306	1560	1920	t_{DCLK}	t_{hbp} must > $15 t_{DCLK}$
	Display period	t_{hd}	1280	1280	1280	t_{DCLK}	
	Back porch	t_{hbp}	15	241	255	t_{DCLK}	
	Front porch	t_{hfp}	$t_H - t_{hd} - t_{hbp}$			t_{DCLK}	
	Pulse width	t_{hsw}	1	1	200	t_{DCLK}	
VSYNC	Period	Odd	t_V	292.5	312.5	450.5	t_H
		Eve					
	Display period	Odd	t_{vd}	288	288	288	t_H
		Eve					
	Back porch	Odd	t_{vbp}	3	24	34	t_H
		Eve		3.5	24.5	34.5	
	Front porch	Odd	t_{vfp}	$t_V - t_{vd} - t_{vb}$			t_H
Eve							
Pulse width	Odd	t_{vsw}	$1 t_{DCLK}$	$1 t_{DCLK}$	$6 t_H$	t_{DCLK}	
	Eve						
1 frame			585	625	901	t_H	



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5.2.3 UPS052 (360 mode/NTSC/27MHz) timing specifications (refer to Fig.4 Fig.5)

Parameter		Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency		$1/t_{DCLK}$	23	27	30	MHz	
HSYNC	Period	t_H	1466	1716	1907	t_{DCLK}	t_{hbp} must > 15 t_{DCLK}
	Display period	t_{hd}	1440	1440	1440	t_{DCLK}	
	Back porch	t_{hbp}	15	241	255	t_{DCLK}	
	Front porch	t_{hfp}	$t_H - t_{hd} - t_{hbp}$			t_{DCLK}	
	Pulse width	t_{hsw}	1	1	200	t_{DCLK}	
VSYNC	Period	Odd	t_v	242.5	262.5	450.5	t_H
		Even					
	Display period	Odd	t_{vd}	240	240	240	t_H
		Even					
	Back porch	Odd	t_{vbp}	1	21	31	t_H
		Even		1.5	21.5	31.5	
	Front porch	Odd	t_{vfp}	$t_v - t_{vd} - t_{vb}$			t_H
		Even					
	Pulse width	Odd	t_{vsw}	$1 t_{DCLK}$	$1 t_{DCLK}$	$6 t_H$	
		Even					
1 frame			485	525	901	t_H	

5.2.4 UPS052 (360 mode/PAL/27MHz) timing specifications (refer to Fig.4 Fig.5)

Parameter		Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency		$1/t_{DCLK}$	23	27	30	MHz	
HSYNC	Period	t_H	1466	1728	1920	t_{DCLK}	t_{hbp} must > 15 t_{DCLK}
	Display period	t_{hd}	1440	1440	1440	t_{DCLK}	
	Back porch	t_{hbp}	15	241	255	t_{DCLK}	
	Front porch	t_{hfp}	$t_H - t_{hd} - t_{hbp}$			t_{DCLK}	
	Pulse width	t_{hsw}	1	1	200	t_{DCLK}	
VSYNC	Period	Odd	t_v	292.5	312.5	450.5	t_H
		Even					
	Display period	Odd	t_{vd}	288	288	288	t_H
		Even					
	Back porch	Odd	t_{vbp}	3	24	34	t_H
		Even		3.5	24.5	34.5	
	Front porch	Odd	t_{vfp}	$t_v - t_{vd} - t_{vb}$			t_H
		Even					
	Pulse width	Odd	t_{vsw}	$1 t_{DCLK}$	$1 t_{DCLK}$	$6 t_H$	
		Even					
1 frame			585	625	901	t_H	

Fig.4 UPS052 Input Horizontal Timing Chart

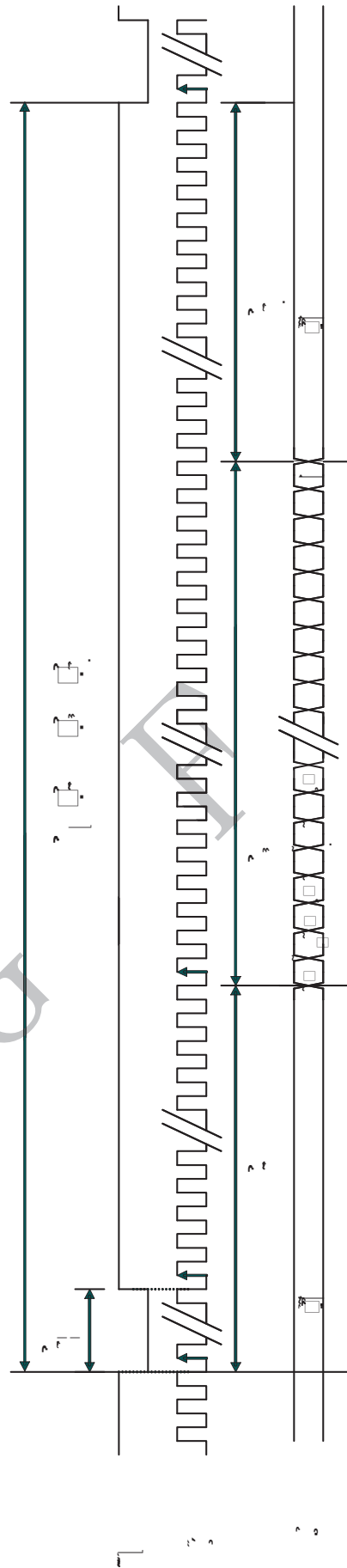
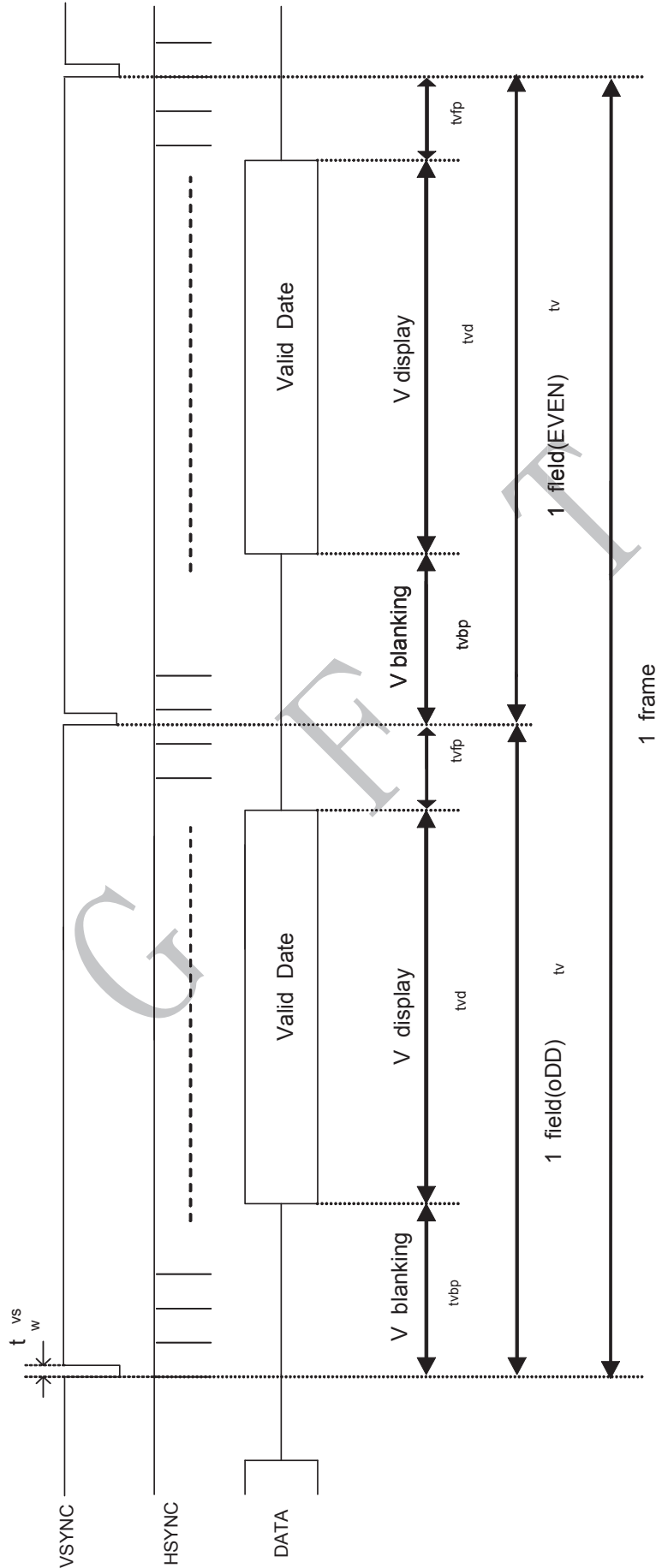


Fig.5 UPS052 Input Vertical Timing Chart



5.3 CCIR656 Timing

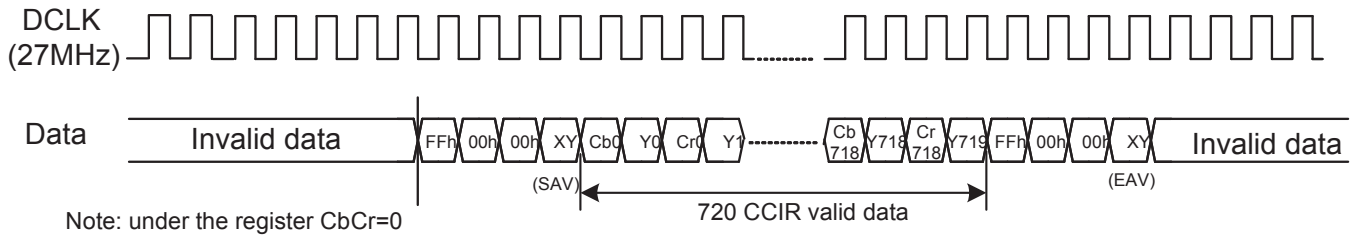


Fig.6 CCIR656 Data input format

5.3.1 CCIR656 decoding

fl FF 00 00 < XY > signals are involved with HSYNC, VSYNC and Field

fl <XY> encode following bits:

F=field select : F=0 for field 1, F=1 for field 2;

V=1 during vertical blanking

H=0 at SAV , H=1 at EAV ,

P3-P0=protection bits :

$P3 = V \oplus H$ $P2 = F \oplus H$ $P1 = F \oplus V$ $P0 = F \oplus V \oplus H$ \oplus : represents the exclusive-OR function

fl Control is provided through “End of Video” (EAV) and “Start of Video” (SAV) timing references.

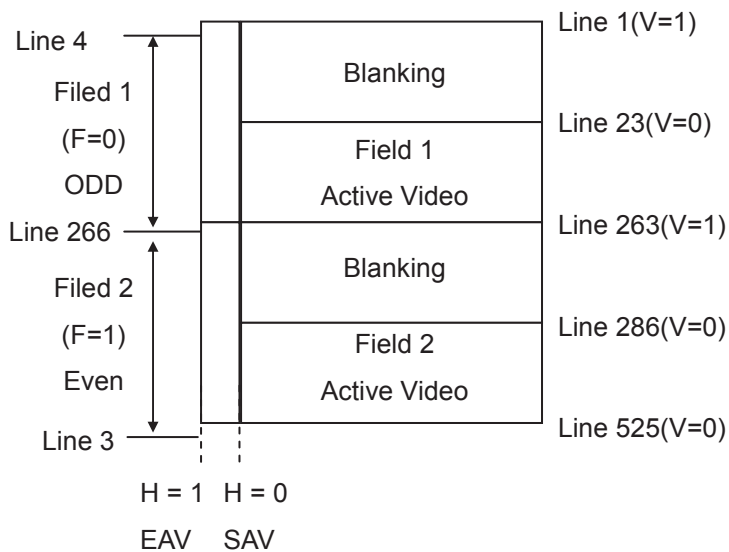
fl Horizontal blanking section consists of repeating pattern 80 10 80 10

XY							
D7(MSB)	D6	D5	D4	D3	D2	D1	D0(LSB)
1	F	V	H	P3	P2	P1	P0



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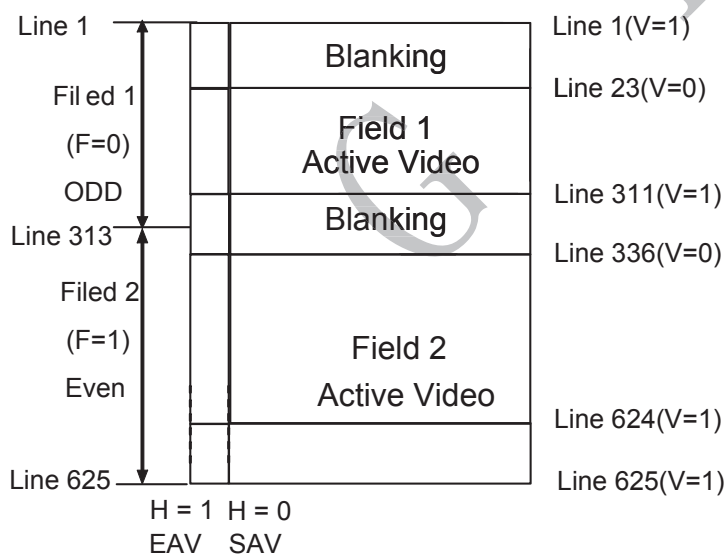
5.3.2 CCIR656 NTSC



Line Number	F	V	H (EAV)	H (SAV)
1-3	1	1	1	0
4-22	0	1	1	0
23-262	0	0	1	0
263-265	0	1	1	0
266-285	1	1	1	0
286-525	1	0	1	0

	F	H	V
1	Even Field	EAV	Blanking
0	Odd Field	SAV	Active Video

5.3.3 CCIR656 PAL



Line Number	F	V	H (EAV)	H (SAV)
1-22	0	1	1	0
23-310	0	0	1	0
311-312	0	1	1	0
313-335	1	1	1	0
335-623	1	0	1	0
624-625	1	1	1	0

	F	H	V
1	Even Field	EAV	Blanking
0	Odd Field	SAV	Active Video



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5.4 YUV 720 and YUV 640 timing

5.4.1 YUV 720 mode/NTSC timing specifications (refer to Fig.7 Fig.9)

Parameter		Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency		$1/t_{DCLK}$	23	27	30	MHz	
HSYNC	Period	t_H	1476	1716	1907	t_{DCLK}	t_{hbp} must > $15 t_{DCLK}$
	Display period	t_{hd}	1440	1440	1440	t_{DCLK}	
	Back porch	t_{hbp}	15	240	255	t_{DCLK}	
	Front porch	t_{hfp}	$t_H - t_{hd} - t_{hbp}$			t_{DCLK}	
	Pulse width	t_{hsw}	1	1	200	t_{DCLK}	
VSYNC	Period	Odd	t_V	242.5	262.5	450.5	t_H
		Even					
	Display period	Odd	t_{vd}	240	240	240	t_H
		Even					
	Back porch	Odd	t_{vbp}	1	21	31	t_H
		Even		1.5	21.5	31.5	
	Front porch	Odd	t_{vfp}	$t_V - t_{vd} - t_{vb}$			t_H
		Even					
	Pulse width	Odd	t_{vsw}	$1 t_{DCLK}$	$1 t_{DCLK}$	$6 t_H$	t_{DCLK}
		Even					
1 frame				525	901	t_H	

5.4.2 YUV 720 mode/PAL timing specifications (refer to Fig.7 Fig.9)

Parameter		Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency		$1/t_{DCLK}$	23	27	30	MHz	
	Period	t_H	1476	1728	1920	t_{DCLK}	t_{hbp} must > $15 t_{DCLK}$
	Display period	t_{hd}	1440	1440	1440	t_{DCLK}	
	Back porch	t_{hbp}	15	240	255	t_{DCLK}	
	Front porch	t_{hfp}	$t_H - t_{hd} - t_{hbp}$			t_{DCLK}	
	Pulse width	t_{hsw}	1	1	200	t_{DCLK}	
VSYNC	Period	Odd	t_V	292.5	312.5	450.5	t_H
		Even					
	Display period	Odd	t_{vd}	288	288	288	t_H
		Even					
	Back porch	Odd	t_{vbp}	3	24	34	t_H
		Even		3.5	24.5	34.5	
	Front porch	Odd	t_{vfp}	$t_V - t_{vd} - t_{vb}$			t_H
		Even					
	Pulse width	Odd	t_{vsw}	$1 t_{DCLK}$	$1 t_{DCLK}$	$6 t_H$	t_{DCLK}
		Even					
1 frame			585	625	901	t_H	



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5.4.3 YUV 640 mode/NTSC timing specifications (refer to Fig.8 Fig.9)

Parameter		Symbol	Min.	Typ.	Max.	Unit.	Remark	
DCLK Frequency		$1/t_{DCLK}$	20.65	24.535	30	MHz		
HSYNC	Period	t_H	1314	1560	1907	t_{DCLK}	t_{hbp} must > 15 t_{DCLK}	
	Display period	t_{hd}	1280	1280	1280	t_{DCLK}		
	Back porch	t_{hbp}	15	240	255	t_{DCLK}		
	Front porch	t_{hfp}	$t_H - t_{hd} - t_{hbp}$			t_{DCLK}		
	Pulse width	t_{hsw}	1	1	200	t_{DCLK}		
VSYNC	Period	Odd	242.5	262.5	450.5	t_H		
		Eve						
	Display period	Odd	240	240	240	t_H		
		Eve						
	Back porch	Odd	1	21	31	t_H		
		Eve	1.5	21.5	31.5			
	Front porch	Odd	t_{vfp}	$t_V - t_{vd} - t_{vb}$				t_H
		Eve						
	Pulse width	Odd	t_{vsw}	$1 t_{DCLK}$	$1 t_{DCLK}$	$6 t_H$		t_{DCLK}
		Eve						
1 frame			485	525	901	t_H		

5.4.4 YUV 640 mode/PAL timing specifications (refer to Fig.8 Fig.9)

Parameter		Symbol	Min.	Typ.	Max.	Unit.	Remark	
DCLK Frequency		$1/t_{DCLK}$	20.5	24.375	30	MHz		
HSYNC	Period	t_H	1314	1560	1920	t_{DCLK}	t_{hbp} must > 15 t_{DCLK}	
	Display period	t_{hd}	1280	1280	1280	t_{DCLK}		
	Back porch	t_{hbp}	15	240	255	t_{DCLK}		
	Front porch	t_{hfp}	$t_H - t_{hd} - t_{hbp}$			t_{DCLK}		
	Pulse width	t_{hsw}	1	1	200	t_{DCLK}		
VSYNC	Period	Odd	292.5	312.5	450.5	t_H		
		Eve						
	Display period	Odd	288	288	288	t_H		
		Eve						
	Back porch	Odd	3	24	34	t_H		
		Eve	3.5	24.5	34.5			
	Front porch	Odd	t_{vfp}	$t_V - t_{vd} - t_{vb}$				t_H
		Eve						
	Pulse width	Odd	t_{vsw}	$1 t_{DCLK}$	$1 t_{DCLK}$	$6 t_H$		t_{DCLK}
		Eve						
1 frame			585	625	901	t_H		

Fig.7 YUV720 Input Horizontal Timing Chart

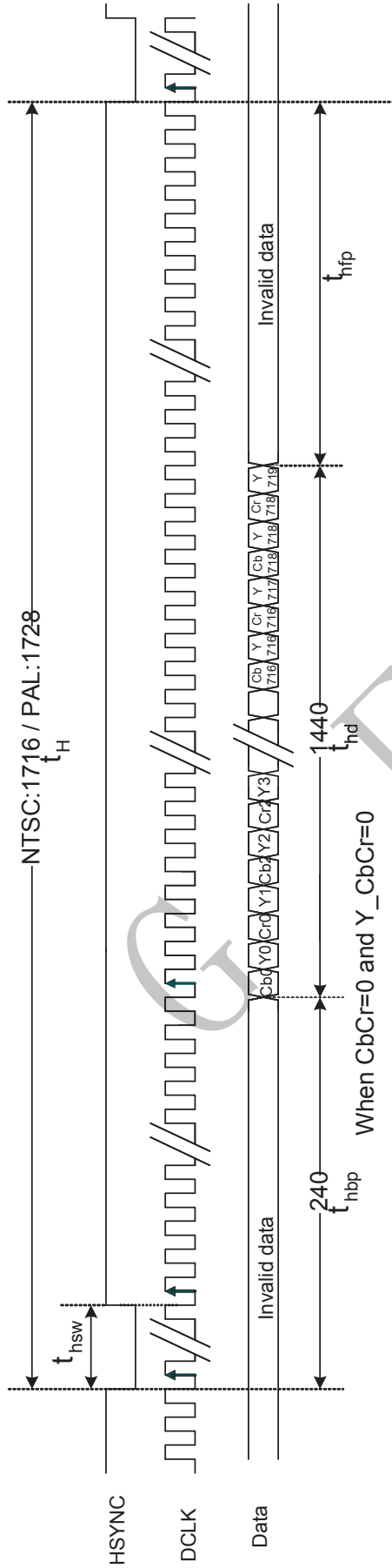


Fig.8 YUV640 Input Horizontal Timing Chart

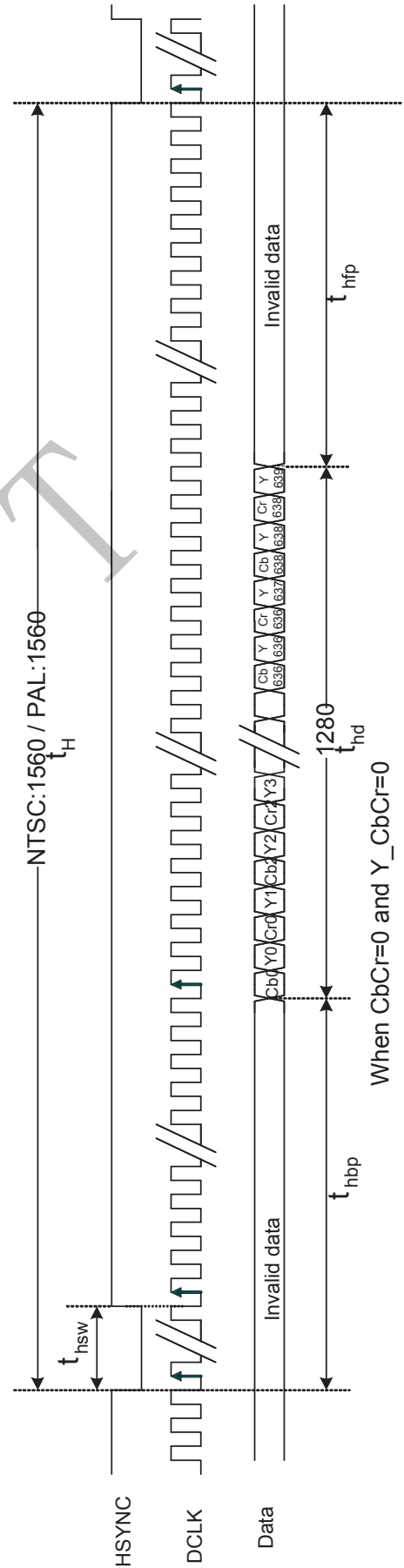
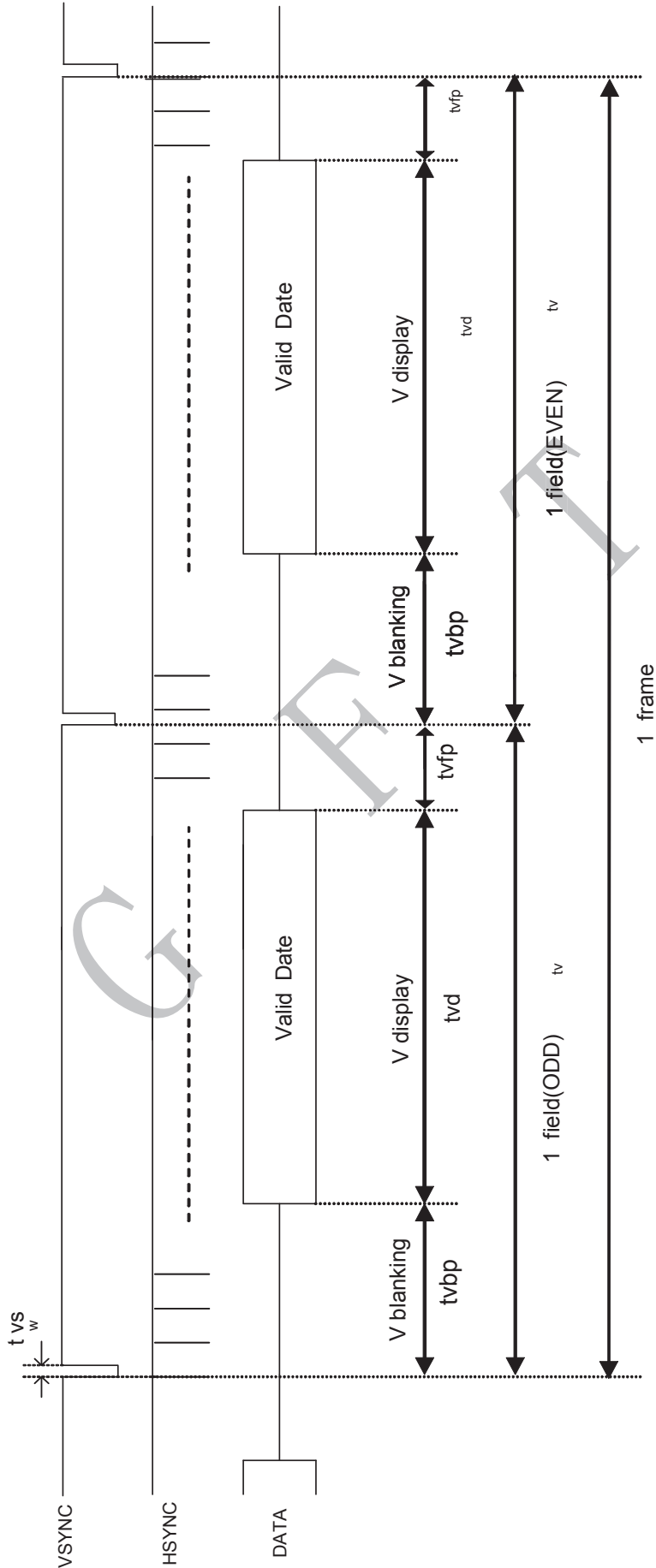


Fig.9 YUV Input Vertical Timing Chart





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5.5 CCIR656/YUV 720/YUV 640 to RGB conversion

$$R_n = 1.164 * [(Y_{2n-1} + Y_{2n}) / 2 - 16] + 1.596 * (C_{rn} - 128)$$

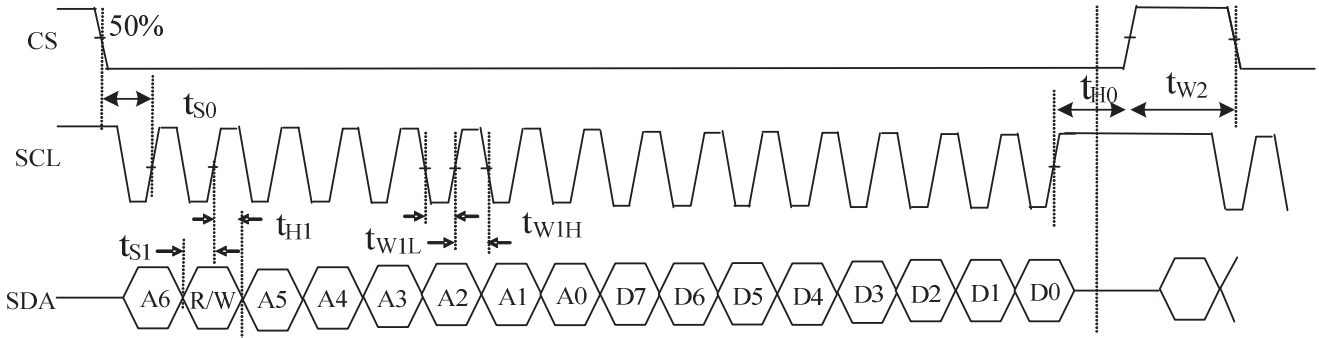
$$G_n = 1.164 * [(Y_{2n-1} + Y_{2n}) / 2 - 16] - 0.813 * (C_{rn} - 128) - 0.392 * (C_{bn} - 128)$$

$$B_n = 1.164 * [(Y_{2n-1} + Y_{2n}) / 2 - 16] + 2.017 * (C_{bn} - 128)$$

Where Y:16~235 C_r:16~240 C_b:16~240

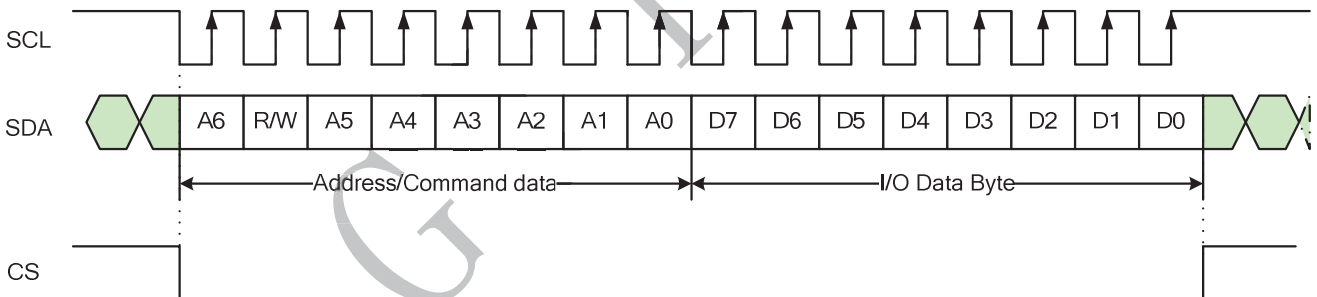
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6. Serial control interface AC characteristic



Item	Symbol	Min	Typical	Max	Unit
CS input setup Time	t_{S0}	50	-	-	ns
Serial data input setup Time	t_{S1}	50	-	--	ns
CS input hold Time	t_{H0}	50	-	-	ns
Serial data input hold Time	t_{H1}	50	-	-	ns
SCL pulse low width	t_{W1L}	50	-	-	ns
SCL pulse high width	t_{W1H}	50	-	-	ns
CS pulse high width	t_{W2}	400	-	-	ns

6.1 Timing chart



- Each serial command consists of 16 bits of data which is loaded one bit a time at the rising edge of serial clock SCL.
- Command loading operation starts from the falling edge of CS and is completed at the next rising edge of CS.
- The serial control block is operational after power on reset, but commands are established by the VSYNC signal. If command is transferred multiple times for the same register, the last command before the VSYNC signal is valid.
- If less than 16 bits of SCL are input while CS is low, the transferred data is ignored.
- If 16 bits or more of SCL are input while CS is low, the previous 16 bits of transferred data after the falling edge of CS pulse are valid data.
- Serial block operates with the SCL clock.
- Serial data can be accepted in the standby (power save) mode.



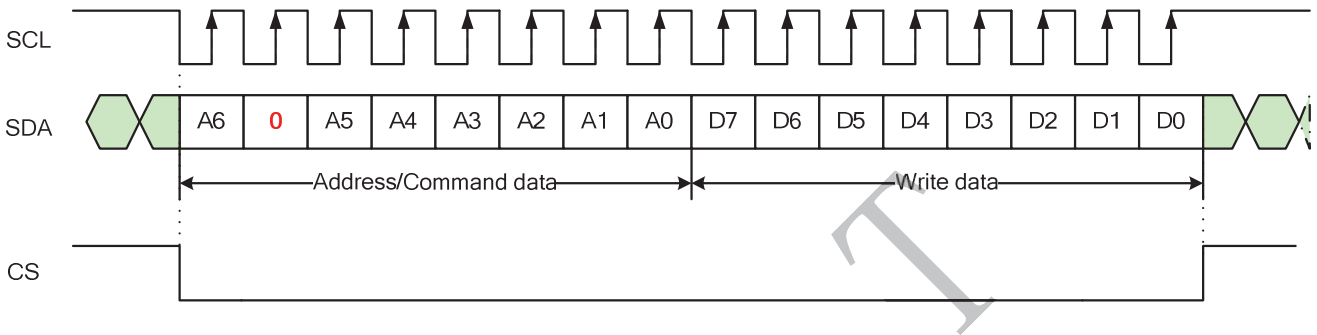
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6.2 The configuration of serial data at SDA terminal is at below

MSB																LSB
A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	
Address		Address						DATA								

R/W: Establishes the Read mode when set to '1', and the Write mode when set to '0'.

Write Mode:





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6.3 Register table

No.	Register address								Register data (default setting)							
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R0	0	0	0	0	0	0	0	0	Y_CbCr (0)	CCIR601 (0)	x	x	VCAC (0)	VCOM_AC (011)		
R1	0	0	0	0	0	0	0	1	VCDCE (1)	x	VCOM_DC (0Ah)					
R3	0	0	0	0	0	0	1	1	Brightness (40h)							
R4	0	0	0	0	0	1	0	0	Narrow (0)	YUV (0)	SEL (00)	NTSC/PAL (10)		VDIR (1)	HDIR (1)	
R5	0	0	0	0	0	1	0	1	DRV_FREQ (0)	GRB (1)	PFM_DUTY (011)		SHDB2 (1)	SHDB1 (1)	STB (0)	
R6	0	0	0	0	0	1	1	0	HBLK_EN (0)	LED_Current (00)	VBLK (15h)					
R7	0	0	0	0	0	1	1	1	HBLK(46h)							
R8	0	0	0	0	1	0	0	0	BL_DRV (00)		x	x	x	x	x	x
R9	0	0	0	0	1	0	0	1	x	x	x	x	x	x	CP1_FREQ (00)	
R10	0	0	0	0	1	0	1	0	x	x	x	x	x	x	CP2_FREQ (00)	
R12	0	0	0	0	1	1	0	0	PAIR (00)	x	CbCr (0)	x	Vdpol (1)	Hdpol (1)	DCLKpol (0)	
R13	0	0	0	0	1	1	0	1	CONTRAST_RGB (40h)							
R14	0	0	0	0	1	1	1	0	x	SUB-CONTRAST_R (40h)						
R15	0	0	0	0	1	1	1	1	x	SUB-BRIGHTNESS_R (40h)						
R16	0	0	0	1	0	0	0	0	x	SUB-CONTRAST_B (40h)						
R17	0	0	0	1	0	0	0	1	x	SUB-BRIGHTNESS_B (40h)						
R21	0	0	0	1	0	1	0	1	LED_ON_CYCLE (0111)				LED_ON_RATIO (1111)			
R48	0	0	1	1	0	0	0	0	x	x	GMA_V0+(100001)					
R49	0	0	1	1	0	0	0	1	x	x	GAM_V3+(101100)					
R50	0	0	1	1	0	0	1	0	x	x	GMA_V6+(110100)					
R51	0	0	1	1	0	0	1	1	x	x	x	GMA_V8+(01101)				
R52	0	0	1	1	0	1	0	0	x	x	x	GMA_V11+(01011)				
R53	0	0	1	1	0	1	0	1	x	x	x	GMA_V15+(10101)				



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R54	0	0	1	1	0	1	1	0	x	x	x	x	GMA_V20+(1111)
R55	0	0	1	1	0	1	1	1	x	x	x	x	GMA_V25+(1011)
R56	0	0	1	1	1	0	0	0	x	x	x	x	GMA_V38+(0000)
R57	0	0	1	1	1	0	0	1	x	x	x	x	GMA_V43+(1000)
R58	0	0	1	1	1	0	1	0	x	x	x		GMA_V48+(00110)
R59	0	0	1	1	1	0	1	1	x	x	x		GMA_V52+(01001)
R60	0	0	1	1	1	1	0	0	x	x	x		GMA_V55+(01011)
R61	0	0	1	1	1	1	0	1	x	x			GMA_V57+(010100)
R62	0	0	1	1	1	1	1	0	x	x			GMA_V60+(001111)
R63	0	0	1	1	1	1	1	1	x	x			GMA_V63+(000001)
R64	1	0	0	0	0	0	0	0	x	x			GMA_V63-(100001)
R65	1	0	0	0	0	0	0	1	x	x			GMA_V60-(110000)
R66	1	0	0	0	0	0	1	0	x	x			GMA_V57-(110100)
R67	1	0	0	0	0	0	1	1	x	x	x		GMA_V55-(01100)
R68	1	0	0	0	0	1	0	0	x	x	x		GMA_V52-(01011)
R69	1	0	0	0	0	1	0	1	x	x	x		GMA_V48-(00111)
R70	1	0	0	0	0	1	1	0	x	x	x	x	GAM_V43-(1000)
R71	1	0	0	0	0	1	1	1	x	x	x	x	GMA_V38-(0000)
R72	1	0	0	0	1	0	0	0	x	x	x	x	GMA_V25-(1010)
R73	1	0	0	0	1	0	0	1	x	x	x	x	GMA_V20-(1111)
R74	1	0	0	0	1	0	1	0	x	x	x		GAM_V15-(10100)
R75	1	0	0	0	1	0	1	1	x	x	x		GMA_V11-(01010)
R76	1	0	0	0	1	1	0	0	x	x	x		GMA_V8-(01100)
R77	1	0	0	0	1	1	0	1	x	x			GMA_V6-(010100)
R78	1	0	0	0	1	1	1	0	x	x			GMA_V3-(001100)
R79	1	0	0	0	1	1	1	1	x	x			GMA_V0-(000001)



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R86	1	0	0	1	0	1	1	0	x	x	x	x	0	1	VGH_SEL(11)	
R97	1	0	1	0	0	0	0	1	X	x	x	X	x	x	x	GAMMA setting (0)

Note: 1. "x" => please set to '0'.

G F T

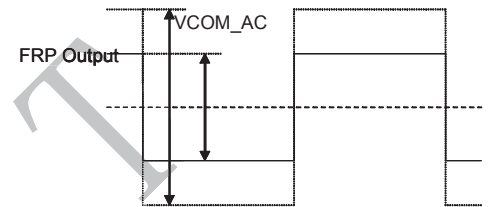
6.4 Register description

R0:

No.	Register address								Register data								MSB		LSB	
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0				
R0	0	0	0	0	0	0	0	0	Y_CbCr(0)	CCIR601 (0)	x	x	VCAC(0)	VCOM_AC(011)						

VCOM_AC: Common voltage AC level selection (deviation $\pm 0.1V$)

VCOM_AC			VCAC	Voltage (V)
D2	D1	D0	D3	
0	0	0	0	3.6
0	0	0	1	3.7
0	0	1	0	3.8
0	0	1	1	3.9
0	1	0	0	4.0
0	1	0	1	4.1
0	1	1	0	4.2(Default)
0	1	1	1	4.3
1	0	0	0	4.4
1	0	0	1	4.5
1	0	1	0	4.6
1	0	1	1	4.7
1	1	X	X	4.8



CCIR601: CCIR601 input timing selection

CCIR601	Function
0(Default)	Disable CCIR601 (Default)
1	Enable CCIR601. (Please refer to the table of R4(SEL) for detail description)

Y_CbCr: Y & CbCr exchange position (only valid for 8-bit input YUV640 / YUV720)

	CbCr(R12[4])='0'	CbCr(R12[4])='1'
Y_CbCr='0' (Default)	Cb0 Y0 Cr0 Y1 Cb2 Y2 Cr2 Y3	Cr0 Y0 Cb0 Y1 Cr2 Y2 Cb2 Y3
Y_CbCr='1'	Y0 Cb0 Y1 Cr0 Y2 Cb2 Y3 Cr2	Y0 Cr0 Y1 Cb0 Y2 Cr2 Y3 Cb2



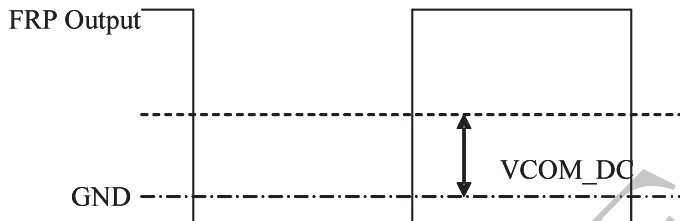
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R1:

No	Register address								Register data							
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R1	0	0	0	0	0	0	0	1	VCDCE (1)	x	VCOM_DC (0Ah)					

VCOM_DC: Common voltage DC level selection (20mV/step)

D5~D0	VCOM DC level (V)
00h	0.10
:	:
0Ah(Default)	0.30(Default)
:	:
3Fh	1.36



VCDCE: VCOM_DC function enable setting

VCDCE	Function
0	VCOM_DC function disable. The COMDC pin is Hi-Z.
1	VCOM_DC function enable. The COMDC voltage follows VCOM_DC setting. (Default)

R3:

No.	Register address								Register data							
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R3	0	0	0	0	0	0	1	1	Brightness (40h)							

BRIGHTNESS: RGB bright level setting, setting accuracy: 1 step / bit

D7 ~ D0	Brightness gain
00h	Dark (-64)
40h(Default)	Center (0) (Default)
FFh	Bright (+191)



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R4:

No.	Register address								Register data							
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R4	0	0	0	0	0	1	0	0	Narrow(0)	YUV(0)	SEL(00)		NTSC/PAL(10)		VDIR(1)	HDIR(1)

HDIR: Horizontal scan direction setting

HDIR	Function
0	Right to left scan
1	Left to right scan (Default)

VDIR: Vertical scan direction setting

VDIR	Function
0	Down to up scan
1	Up to down scan (Default)

NTSC/PAL: NTSC or PAL input mode selection (for UPS052 input timing)

NTSC/PAL		Mode
D3	D2	
0	0	PAL
0	1	NTSC
1	X	Auto detection (Default)

SEL: Input data timing format selection

CCIR601	YUV	SEL		INPUT TIMING FORMAT
		D5	D4	
0	0	0	0	UPS051 (Default)
0	0	0	1	UPS052 320 × 240
0	0	1	X	UPS052 360 × 240
0	1	1	0	CCIR656
1	1	0	X	YUV 640(*)
1	1	1	X	YUV 720(*)

(*)Please refer to YUV640/YUV720 horizontal timing spec for detailed description.

YUV: YUV (CCIR656, YUV640, YUV720) or RGB input selection

YUV	Function
0	RGB input (Default)
1	CCIR656 / YUV640 / YUV720 input.

When this command is sent to driver ic,it will be executed immediately

Narrow: Normal display and Narrow display selection.

Narrow	Function
0	Normal display (Default)
1	Narrow Display



Narrow=0



Narrow=1



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R5:

No	Register address								Register data							MSB	LSB
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1		
R5	0	0	0	0	0	1	0	1	DRV_FREQ(0)	GRB(1)	PFM_DUTY(011)			SHDB2(1)	SHDB1(1)	STB(0)	

STB: Standby (Power saving) mode setting

STB	Function
0	Standby mode (Default)
1	Normal operation

SHDB1: Shut down for back light power converter

SHDB1	Function
0	The back light power converter is off
1	The back light power converter is controlled by power on/off sequence (Default)

SHDB2: Shut down for VGH/VGL charge pump

SHDB2	Function
0	VGH/VGL charge pump is always off
1	VGH/VGL charge pump is controlled by power on/off sequence (Default)

PFM_DUTY: PFM duty cycle selection for back light power converter

PFM_DUTY			Function
D5	D4	D3	PFM duty cycle
0	0	0	50%
0	0	1	60%
0	1	0	65%
0	1	1	70%(Default)
1	0	0	75%
1	0	1	80%
1	1	0	85%
1	1	1	90%

GRB: Register reset setting

GRB	Function
0	Reset all registers to default value
1	Normal operation (Default)

When this command is sent to driver ic, it will be executed immediately

DRV_FREQ: DRV signal frequency setting

DRV_FREQ	DRV frequency
0(Default)	DCLK / 64
1	DCLK / 128



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R6:

No	Register address								Register data							MSB	LSB
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1		
R6	0	0	0	0	0	1	1	0	HBLK_EN(0)	LED_Current(00)	VBLK(15h)						

VBLK: Vertical blanking setting

UPS051, UPS052, YUV640 and YUV720 NTSC mode

D4 ~ D0	VBLK	Unit
01h	1	H (line)
15h	21(Default)	
1Fh	31	

CCIR656 NTSC mode

D4 ~ D0	VBLK	Unit
01h	1	H (line)
16h	22(Default)	
1Fh	31	

UPS052, CCIR656 and YUV640 and YUV720 PAL mode(Vertical blanking + 3)

D4 ~ D0	VBLK	Unit
00h	3	H (line)
15h	24(Default)	
1Fh	34	

Note: V-blanking must be adjusted based on the input data.

LED_CURRENT: adjust LED current

DC-DC feedback voltage

D6	D5	Feedback Threshold voltage
0	0	0.6V(20mA) (default)
0	1	0.75V(25mA)
1	0	0.45V(15mA)
1	1	0.3V(10mA)



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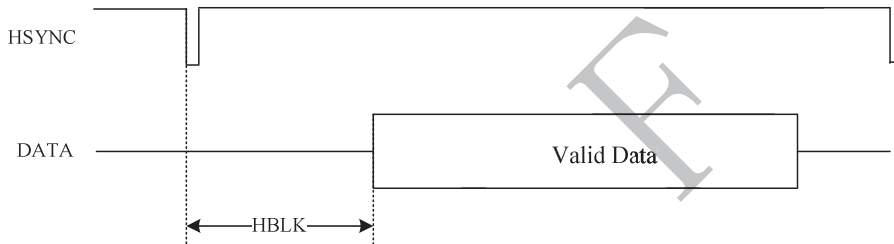
R6 & R7:

No	Register address								Register data							
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R6	0	0	0	0	0	1	1	0	HBLK_EN(0)	LED_Current(00)	VBLK(15h)					
R7	0	0	0	0	0	1	1	1	HBLK(46h)							

HBLK_EN & HBLK: Horizontal blanking setting

HBLK_EN	HBLK(D7~D0)	HBLK	Unit	Remark
x	32h	50	DCLK(*)	UPS051
x	46h	70(Default)		
x	FFh	255		
0	-	241(fixed)	DCLK(*)	UPS052
1	02h~FF	2~255	DCLK(*)	
0	-	240(fixed)	DCLK(*)	YUV640, YUV720
1	02h ~ FFh	2 ~ 255	DCLK(*)	

*The frequency of DCLK is different under different input timing.



R8:

No.	Register address								Register data							
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R8	0	0	0	0	1	0	0	0	BL_DRV(00)		x	x	x	x	x	x

BL_DRV: Backlight driving capability setting

D7	D6	BL_DRV capability
0	0	Normal capability (Default)
0	1	2 times the Normal capability
1	0	4 times the Normal capability
1	1	8 times the Normal capability



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R9 & R10:

No.	Register address								Register data							
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R9	0	0	0	0	1	0	0	1	x	x	x	x	x	x	CP1_FREQ(00)	
R10	0	0	0	0	1	0	1	0	x	x	x	x	x	x	CP2_FREQ(00)	

CP1_FREQ : VINT1 charge pump frequency setting

CP2_FREQ : VINT2/VINT3 charge pump frequency setting

D1	D0	BL_DRV capability
0	0	1/2 * Hsync Freq. (Default)
0	1	1 * Hsync Freq.
1	0	2 * Hsync Freq.
1	1	4 * Hsync Freq.



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R12:

No.	Register address								Register data							
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R12	0	0	0	0	1	1	0	0	PAIR(00)	x	CbCr(0)	x	Vdpol(1)	Hdpol(1)	DCLKpol(0)	

DCLKpol: DCLK polarity selection

DCLKpol	Function
0	Positive polarity (Default)
1	Negative polarity

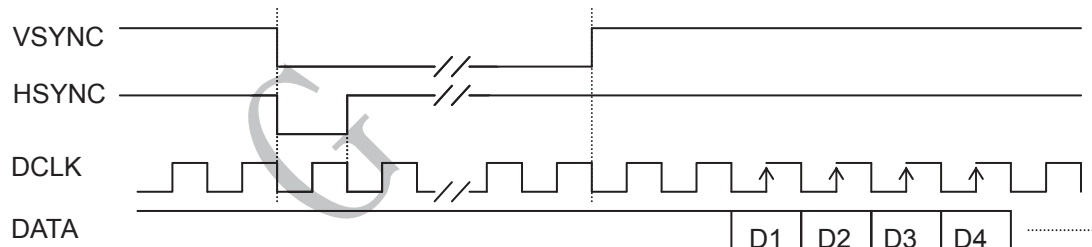
HDpol: HSYNC polarity selection

HDpol	Function
0	Positive polarity
1	Negative polarity (Default)

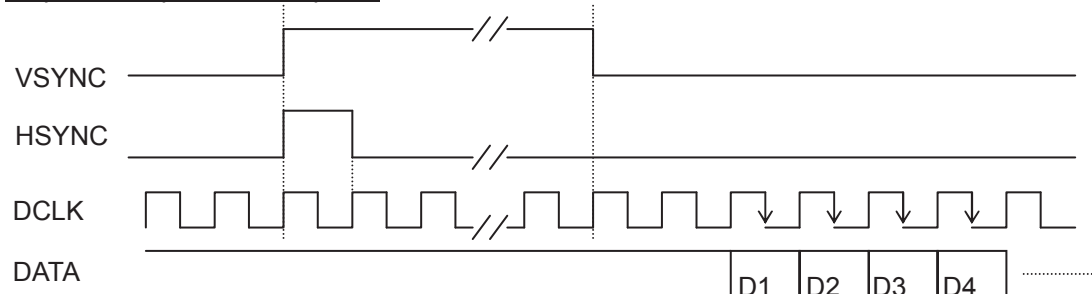
VDpol: VSYNC polarity selection

VDpol	Function
0	Positive polarity
1	Negative polarity (Default)

HDpol=1, VDpol=1, DCLKpol=0



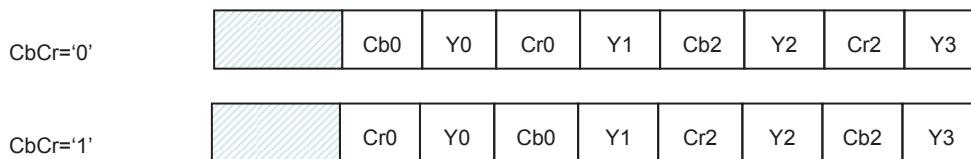
HDpol=0, VDpol=0, DCLKpol=1





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CbCr: Cb & Cr exchange position, (Please refer to the table of R0(Y_CbCr) for detail description)



PAIR: Vertical start time setting for Odd/Even frame

UPS051 / UPS052 NTSC / UPS052 PAL (*)

PAIR		VBLK		Unit
D7	D6	ODD/EVEN		
x	0	21/21(Default)		H (line)
x	1	21/20		

CCIR656/YUV640/YUV720 NTSC/PAL (**)

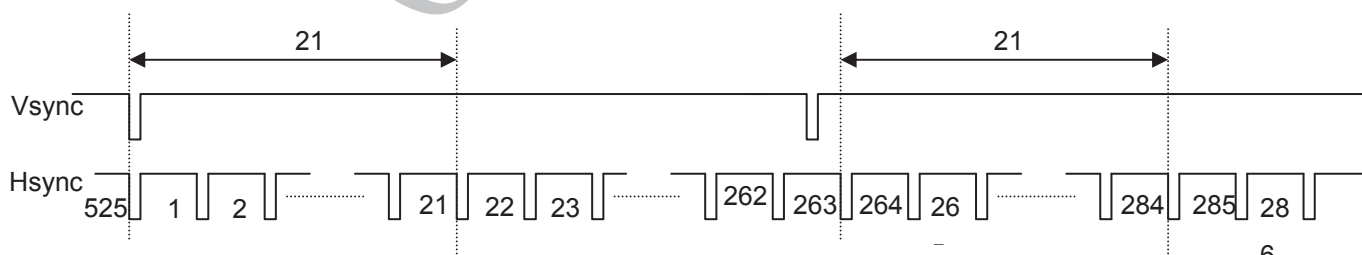
PAIR		VBLK		Unit
D7	D6	ODD/EVEN		
0	0	22/22		H (line)
0	1	22/23		
1	0	23/22		
1	1	23/23		

(*)The typical value of VBLK of UPS052 PAL(24 H) is different than UPS051/UPS052 NTSC(21H).

(**) The typical value of VBLK of CCIR656 PAL(24 H) is different than CCIR656 NTSC(22H).

Note: V-blanking must be adjusted based on the input data.

For example:



		PAIR=0		PAIR=1	
Field	Line	START	END	START	END
	ODD		22	261	22
EVEN		285	524	284	523

This table is based on VBLK=21.



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R13:

No.	Register address								Register data							
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R13	0	0	0	0	1	1	0	1	CONTRAST_RGB(40h)							

CONTRAST_RGB: RGB contrast level setting, the gain changes (1/64) / bit

D7 ~ D0	Contrast gain
00h	0
40h	1(Default)
FFh	3.984

R14~R17:

No.	Register address								Register data							
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R14	0	0	0	0	1	1	1	0	x	SUB-CONTRAST_R(40h)						
R16	0	0	0	1	0	0	0	0	X	SUB-CONTRAST_B(40h)						

SUB-CONTRAST: R/B sub-contrast level setting, the gain changes (1/256) / bit

D6 ~ D0	Brightness gain
00h	0.75
40h	1(Default)
7Fh	1.246

No.	Register address								Register data							
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R15	0	0	0	0	1	1	1	1	X	SUB-BRIGHTNESS_R(40h)						
R17	0	0	0	1	0	0	0	1	X	SUB-BRIGHTNESS_B(40h)						

SUB-BRIGHTNESS: R/B sub-bright level setting, setting accuracy : 1 step / bit

D6 ~ D0	Brightness gain
00h	Dark (-64)
40h	Center (0)(Default)
7Fh	Bright (+63)



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R21:

No.	Register address								Register data							
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R21	0	0	0	1	0	1	0	1	LED_ON_CYCLE (0111)				LED_ON_RATIO (1111)			

LED_ON_RATIO: Set the active ratio of enable signal, and we can use it to adjust brightness of the LEDs.

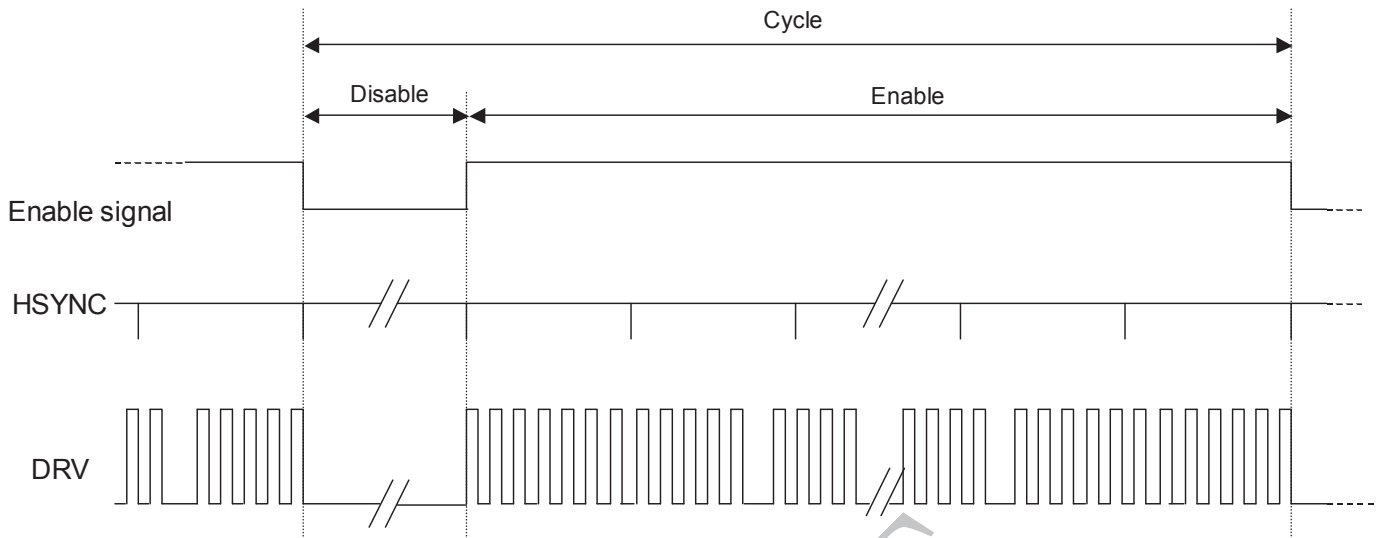
LED_ON_RATIO				Value
D3	D2	D1	D0	
0	0	0	0	1/16
0	0	0	1	2/16
0	0	1	0	3/16
0	0	1	1	4/16
0	1	0	0	5/16
0	1	0	1	6/16
0	1	1	0	7/16
0	1	1	1	8/16
1	0	0	0	9/16
1	0	0	1	10/16
1	0	1	0	11/16
1	0	1	1	12/16
1	1	0	0	13/16
1	1	0	1	14/16
1	1	1	0	15/16
1	1	1	1	16/16(Default)

LED_ON_CYCLE : Set the cycle of enable signal , and we can use it to adjust brightness of the LEDs.

LED_ON_CYCLE				Value
D7	D6	D5	D4	
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
0	0	1	1	4
0	1	0	0	5
0	1	0	1	6
0	1	1	0	7
0	1	1	1	8(Default)
1	0	0	0	9
1	0	0	1	10
1	0	1	0	11
1	0	1	1	12
1	1	0	0	13
1	1	0	1	14
1	1	1	0	15
1	1	1	1	16



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$$16 * \text{LED_ON_CYCLE} = \text{LED_ON_CYCLE} * (\text{LED_ON_RATIO} * 16) + \text{LED_ON_CYCLE} * (16 - \text{LED_ON_RATIO} * 16)$$

(Cycle)
(Enable)
(Disable)

Unit : HSYNC

for example:
 LED_ON_RATIO is "1001", and LED_ON_CYCLE is "0111", then:
 Cycle = 16 * 8 = 128(HSYNC)
 Enable = 8 * ((10/16) * 16) = 80(HSYNC)
 Disable = 8 * (16 - (10/16) * 16) = 48(HSYNC) □ 62.5% on

R48 ~ R79:

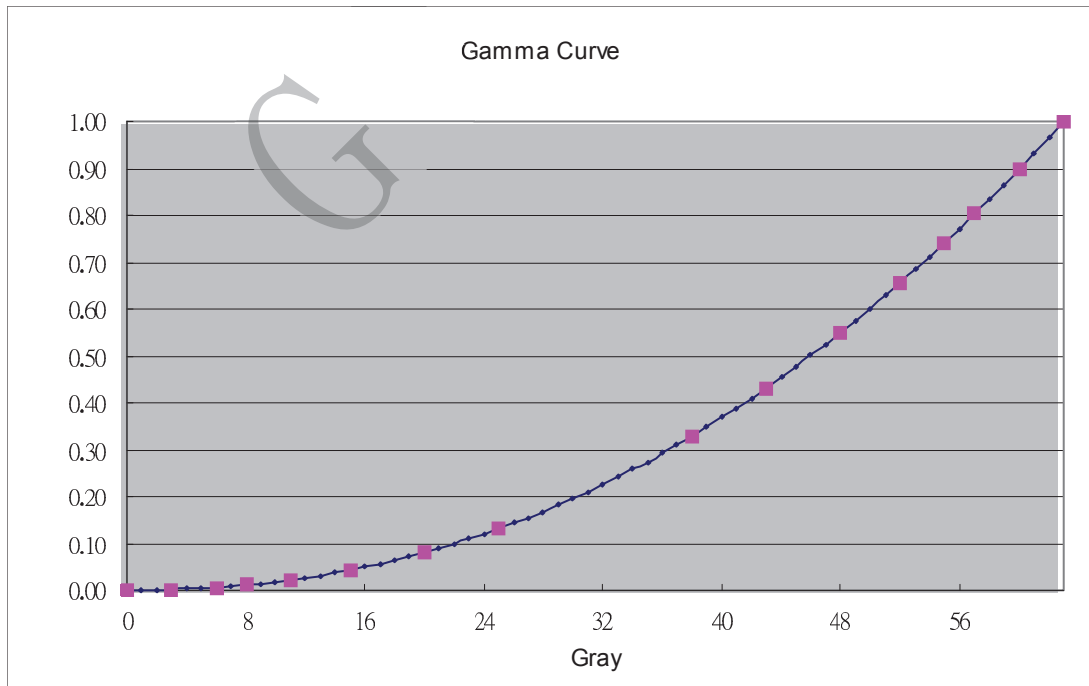
No.	Register address								Register data							LSB
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	
R48	0	0	1	1	0	0	0	0	x	x	GMA_V0+(100001)					
R49	0	0	1	1	0	0	0	1	x	x	GAM_V3+(101100)					
R50	0	0	1	1	0	0	1	0	x	x	GMA_V6+(110100)					
R51	0	0	1	1	0	0	1	1	x	x	x	GMA_V8+(01101)				
R52	0	0	1	1	0	1	0	0	x	x	x	GMA_V11+(01011)				
R53	0	0	1	1	0	1	0	1	x	x	x	GMA_V15+(10101)				
R54	0	0	1	1	0	1	1	0	x	x	x	x	GMA_V20+(1111)			
R55	0	0	1	1	0	1	1	1	x	x	x	x	GMA_V25+(1011)			
R56	0	0	1	1	1	0	0	0	x	x	x	x	GMA_V38+(0000)			
R57	0	0	1	1	1	0	0	1	x	x	x	x	GMA_V43+(1000)			
R58	0	0	1	1	1	0	1	0	x	x	x	GMA_V48+(00110)				
R59	0	0	1	1	1	0	1	1	x	x	x	GMA_V52+(01001)				
R60	0	0	1	1	1	1	0	0	x	x	x	GMA_V55+(01011)				
R61	0	0	1	1	1	1	0	1	x	x	GMA_V57+(010100)					



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R62	0	0	1	1	1	1	1	0	x	x	GMA_V60+(001111)		
R63	0	0	1	1	1	1	1	1	x	x	GMA_V63+(000001)		
R64	1	0	0	0	0	0	0	0	x	x	GMA_V63-(100001)		
R65	1	0	0	0	0	0	0	1	x	x	GMA_V60-(110000)		
R66	1	0	0	0	0	0	1	0	x	x	GMA_V57-(110100)		
R67	1	0	0	0	0	0	1	1	x	x	x	GMA_V55-(01100)	
R68	1	0	0	0	0	1	0	0	x	x	x	GMA_V52-(01011)	
R69	1	0	0	0	0	1	0	1	x	x	x	GMA_V48-(00111)	
R70	1	0	0	0	0	1	1	0	x	x	x	x	GAM_V43-(1000)
R71	1	0	0	0	0	1	1	1	x	x	x	x	GMA_V38-(0000)
R72	1	0	0	0	1	0	0	0	x	x	x	x	GMA_V25-(1010)
R73	1	0	0	0	1	0	0	1	x	x	x	x	GMA_V20-(1111)
R74	1	0	0	0	1	0	1	0	x	x	x		GAM_V15-(10100)
R75	1	0	0	0	1	0	1	1	x	x	x		GMA_V11-(01010)
R76	1	0	0	0	1	1	0	0	x	x	x		GMA_V8-(01100)
R77	1	0	0	0	1	1	0	1	x	x			GMA_V6-(010100)
R78	1	0	0	0	1	1	1	0	x	x			GMA_V3-(001100)
R79	1	0	0	0	1	1	1	1	x	x			GMA_V0-(000001)

16 adjustable points





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R86:

No.	Register address								Register data							
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R86	1	0	0	1	0	1	1	0	x	x	x	x	0	1	VGH_SEL(11)	

VGH_SEL: VGH Voltage selection

VGH_SEL		VGH Voltage (V)
D1	D0	
0	0	12
0	1	13
1	0	14
1	1	15 (Default)

R97:

No.	Register address								Register data							
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R97	1	0	1	0	0	0	0	1	x	x	x	x	x		x	GAMMA2.2(0)

GAMMA2.2 setting : Select auto or manual gamma setting

GAMMA setting	Description
1	Manual set gamma by R48~ R79.
0	Auto set to Default Gamma (Close to 2.2).



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C. Optical specification (Note 1, Note 2, Note 3)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark	
Response time	Rise	$\theta = 0^\circ$	-	10	40	ms	Note 4	
	Fall		-	25	50	ms		
Contrast ratio	CR	At optimized viewing angle	300	400	-		Note 5,6	
Viewing angle	Top	$CR \geq 10$	40	50	-	deg.	Note 7	
	Bottom		Φ_B	50	60			-
	Left		Φ_L	50	60			-
	Right		Φ_R	50	60			-
Brightness	Y_L	$\theta = 0^\circ$	216	270	-	cd/m ²	Note 8	
White chromaticity	x	$\theta = 0^\circ$	(0.26)	(0.31)	(0.36)			
	y	$\theta = 0^\circ$	(0.28)	(0.33)	(0.38)			
	Rx	$\theta = 0^\circ$	TBD	TBD	TBD			
	Ry	$\theta = 0^\circ$	TBD	TBD	TBD			
	Gx	$\theta = 0^\circ$	TBD	TBD	TBD			
	Gy	$\theta = 0^\circ$	TBD	TBD	TBD			
	Bx	$\theta = 0^\circ$	TBD	TBD	TBD			
	By	$\theta = 0^\circ$	TBD	TBD	TBD			
Uniformity	ΔY_L	%	70	75	--	%	Note 10	

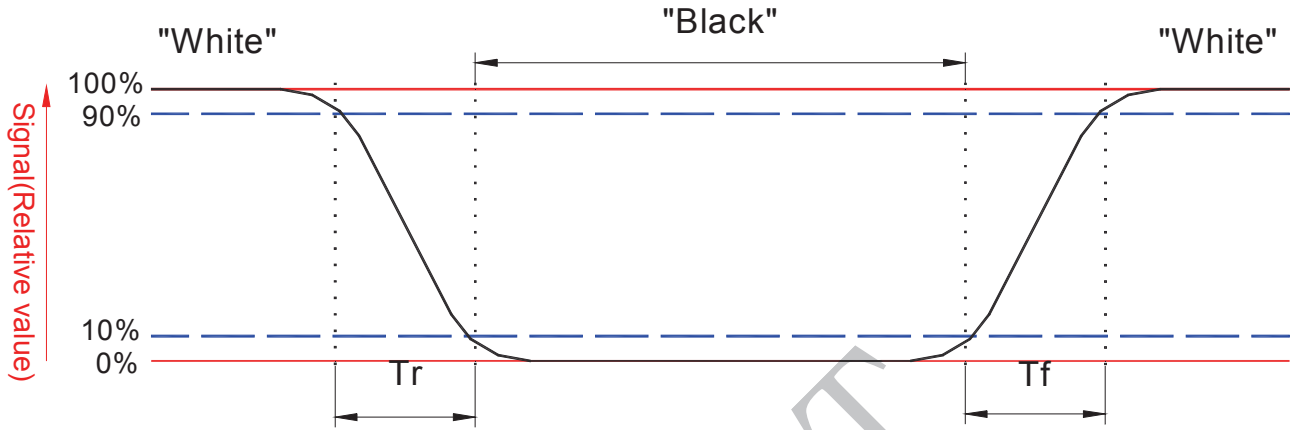
Note 1. Ambient temperature =25°C.

Note 2. To be measured in the dark room.

Note 3. To be measured on the center area of panel with a field angle of 1° by Topcon luminance meter BM-5A, after 10 minutes operation.

Note 4. Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “black” to “white”(falling time) and from “white” to “black”(rising time), respectively. The response time is defined as the time interval between the 10% and 90% of



amplitudes. Refer to figure as below.

Note 5. Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at "White" state}}{\text{Photo detector output when LCD is at "Black" state}}$$

Note 6. White $V_i = V_{i50} \mp 1.5V$

Black $V_i = V_{i50} \pm 2.0V$

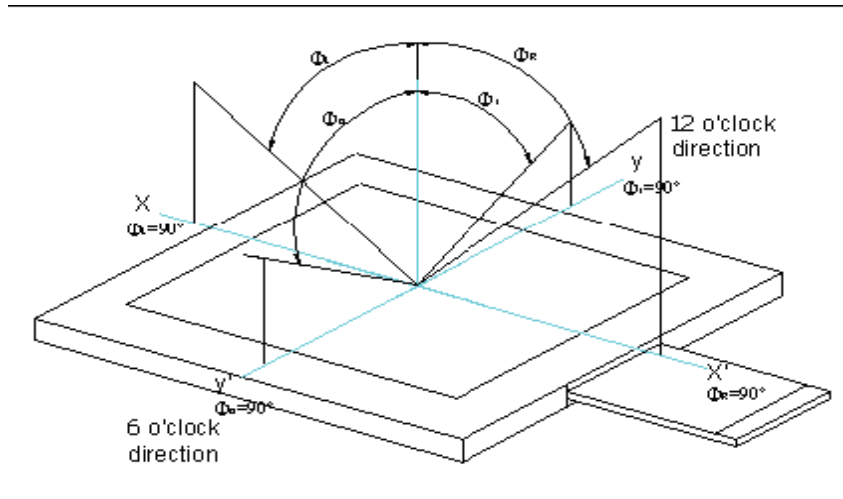
“±” Means that the analog input signal swings in phase with COM signal.

“∓” Means that the analog input signal swings out of phase with COM signal.

V_{i50} : The analog input voltage when transmission is 50%

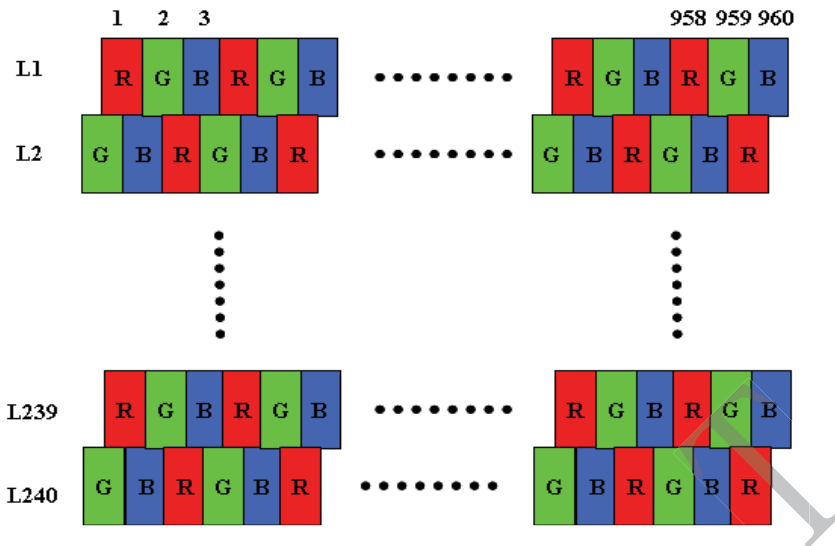
The 100% transmission is defined as the transmission of LCD panel when all the input terminals of module are electrically opened.

Note 7. Definition of viewing angle, Φ , Refer to figure as below.

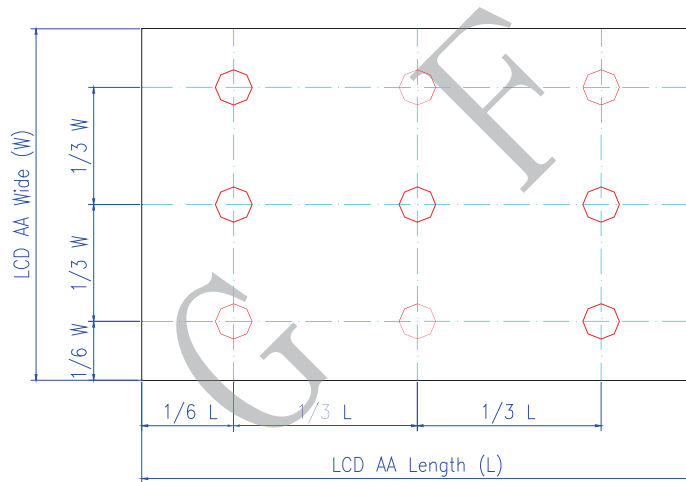


Note 8. Measured at the center area of the panel in gray level 255.

Note 9. Color Filter Arrangement



Note 10 Luminance Uniformity of these 9 points is defined as below:



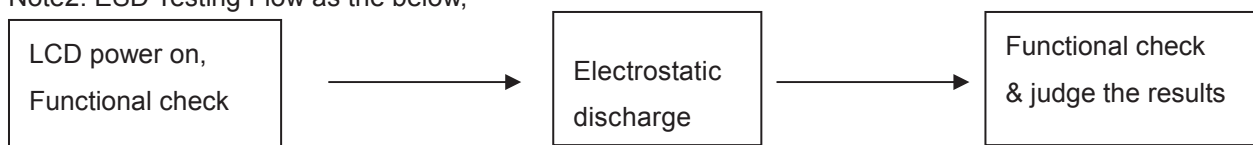
$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points (1-9)}}{\text{maximum luminance in 9 points (1-9)}}$$

D. Reliability test items

No.	Test items	Conditions	Remark
1	High temperature storage	Ta= 70°C 240Hrs	
2	Low temperature storage	Ta= -25°C 240Hrs	
3	High temperature operation	Ta= 60°C 240Hrs	
4	Low temperature operation	Ta= 0°C 240Hrs	
5	High temperature and high humidity	Ta= 60°C. 90% RH 240Hrs	Operation
6	Heat shock	-25°C~80°C/50 cycle 2Hrs/cycle	Non-operation
7	Electrostatic discharge	Air-mode : +/- 8kV Contact-mode : +/- 4kV	Note.2, 3
8	Vibration	Frequency range : 10~55Hz Stoke : 1.5mm Sweep : 10~55Hz~10Hz 2 hours for each direction of X,Y,Z (6 hours for total)	Non-operation JIS C7021, A-10 condition A
9	Mechanical shock	100G . 6ms, ±X,±Y,±Z 3 times for each direction	Non-operation JIS C7021, A-7 condition C
10	Vibration (with carton)	Random vibration: 0.015G ² /Hz from 5~200Hz -6dB/Octave from 200~500Hz	IEC 68-34
11	Drop (with carton)	Height: 60cm 1 corner, 3 edges, 6 surfaces	

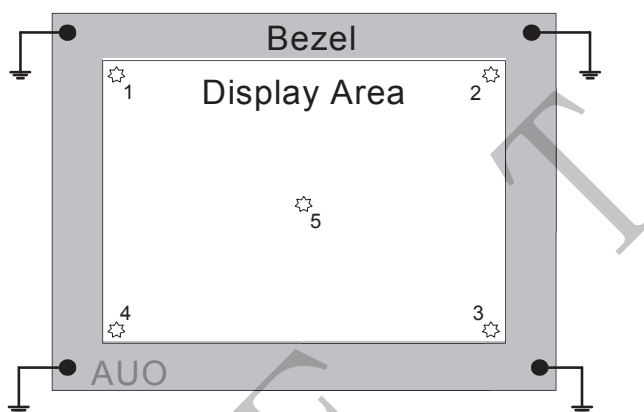
Note1: Ta: Ambient temperature.

Note2: ESD Testing Flow as the below,



Note 3. ESD testing method.

1. Ambient: 24~26°C , 56~65%RH
2. Instruments: Noiseken ESS-2000,
3. Operation System: "CX40FL-B" and adapter "A027DN03 VCT0"
4. Test Mode: Operating mode, test pattern: colorbar+8Gray scale
5. Test Method:
 - a. Contact Discharge: 150pF(330fi) 1sec, 5 points, 10 times/point
 - b. Air Discharge: 150pF(330fi) 1sec, 5 points, 10 times/point
6. Test point:



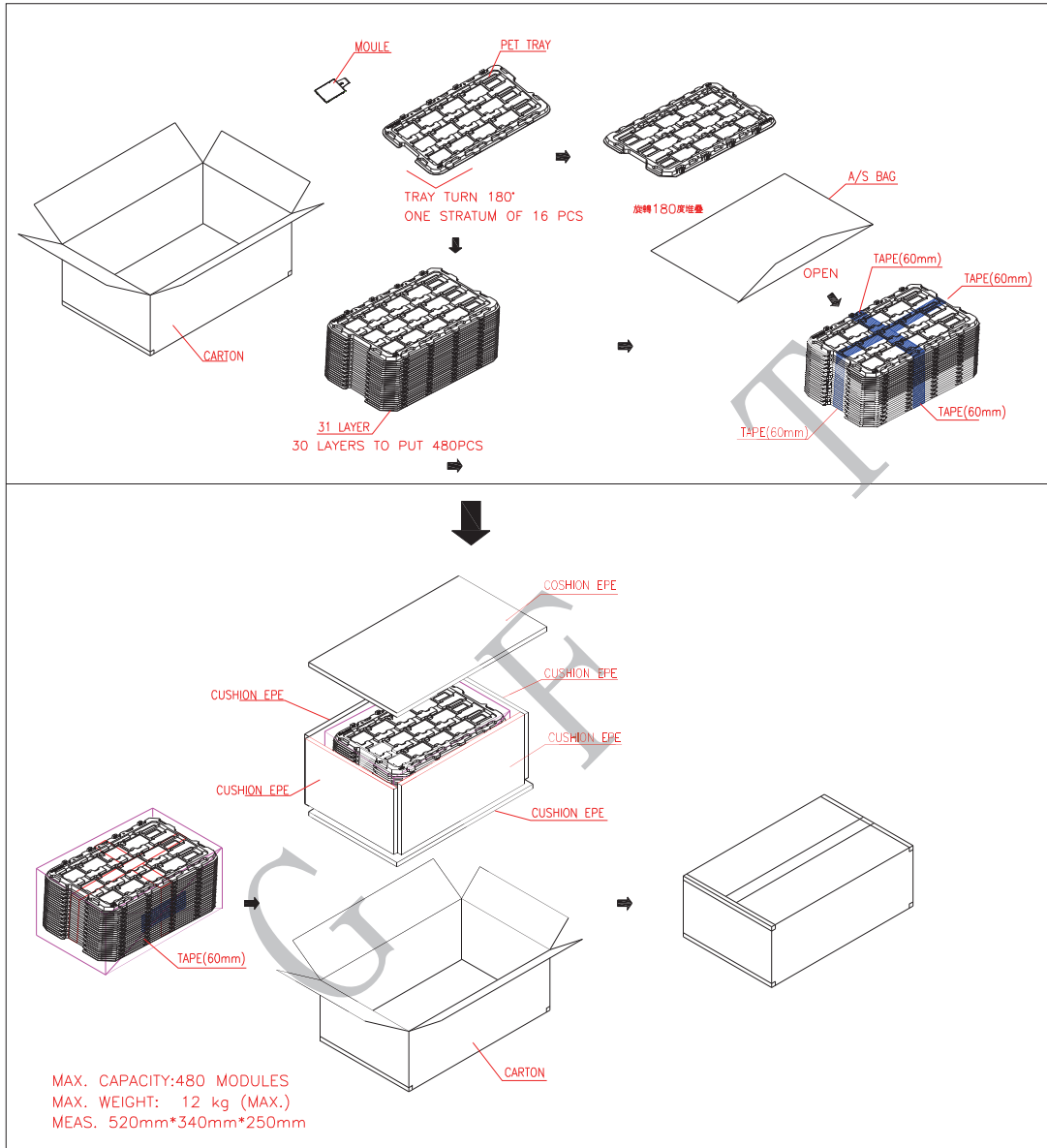
7. The metal casing is connected to power supply ground (0V) at four corners.
8. All register commands are repeating transfer.

G



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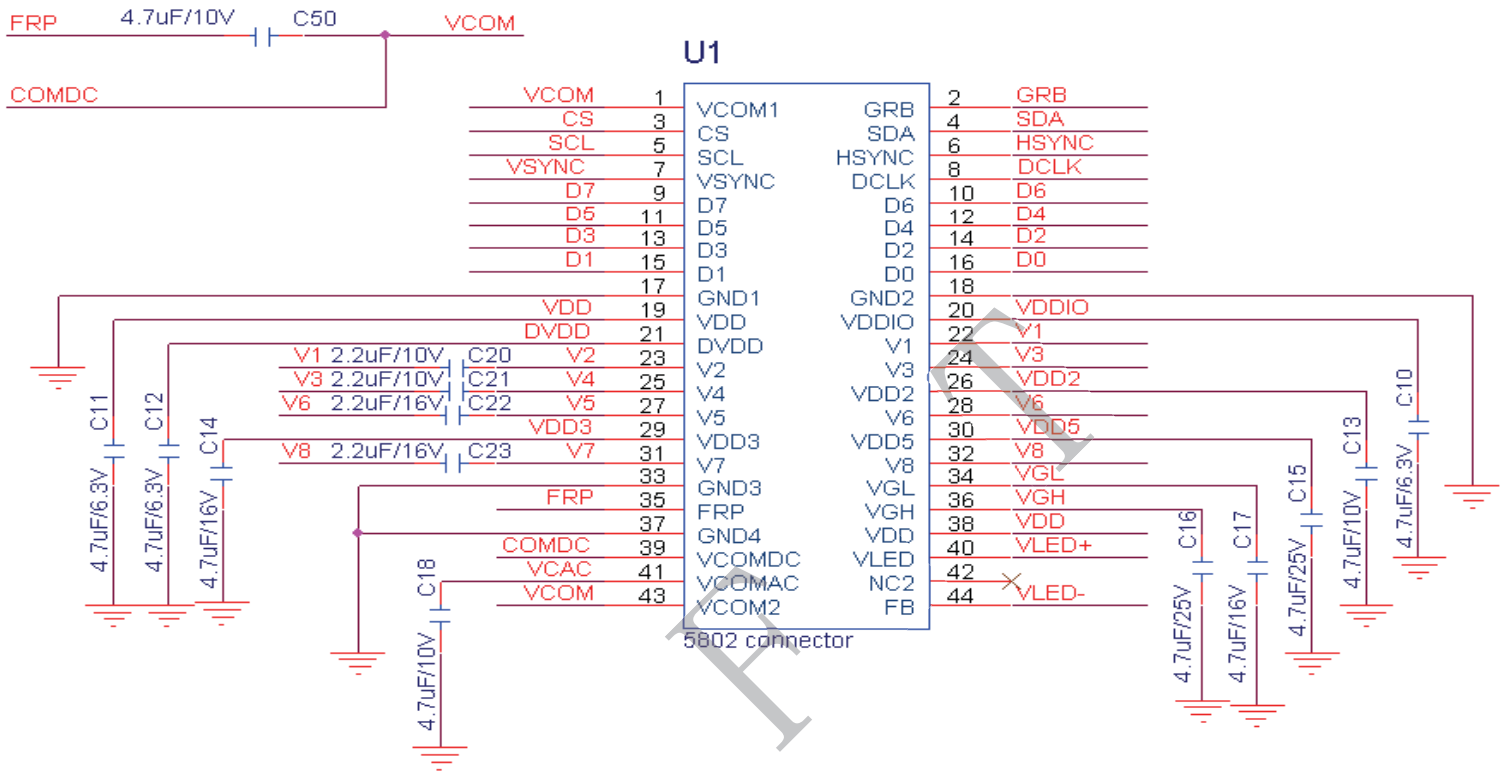
E. Packing form



G. Application note

1. Application circuit

1.1 External LED drive backlight (Internal VcomDC)



Note2: Use external LED driver must set R5[1](SHDB1)= "0".

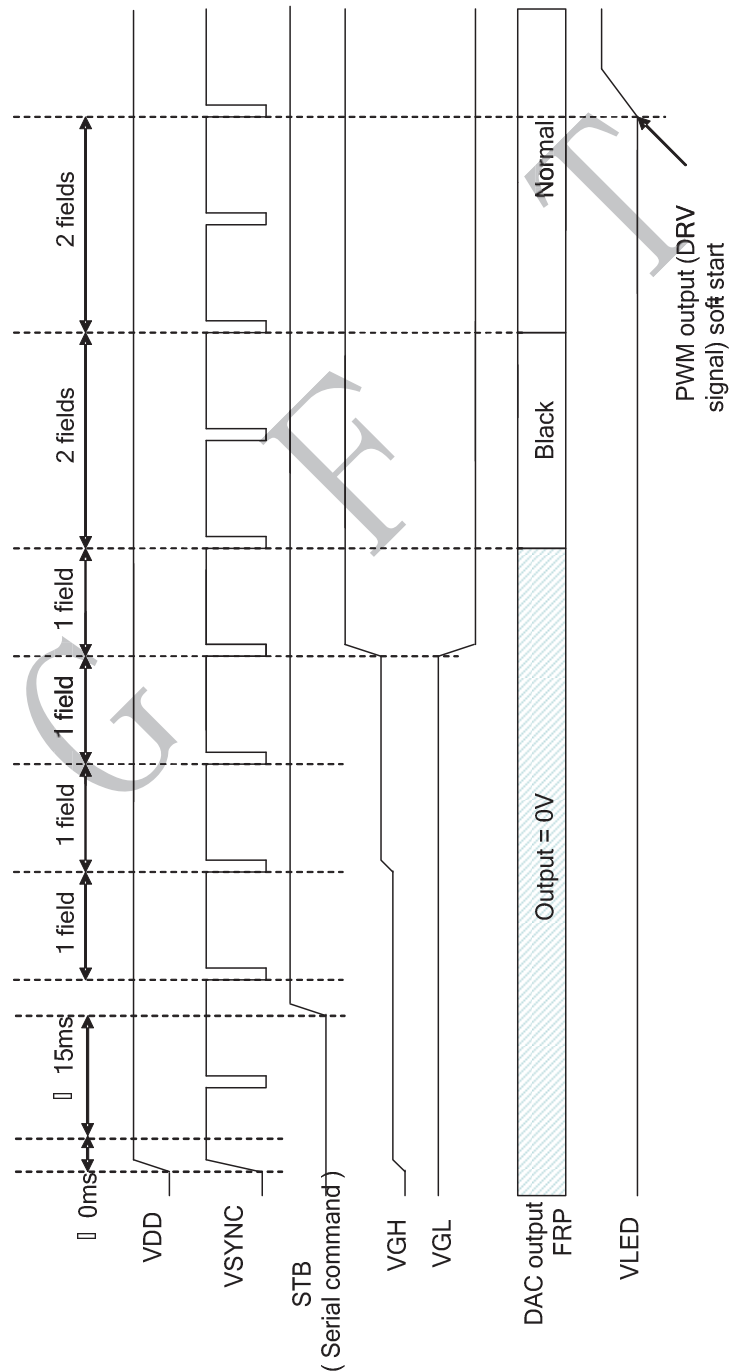
2. Power on/off sequence

The register setting of standby mode disabling / enabling is used to control the build-in power on / off sequence.

2.1 Power on (Standby Disabling)

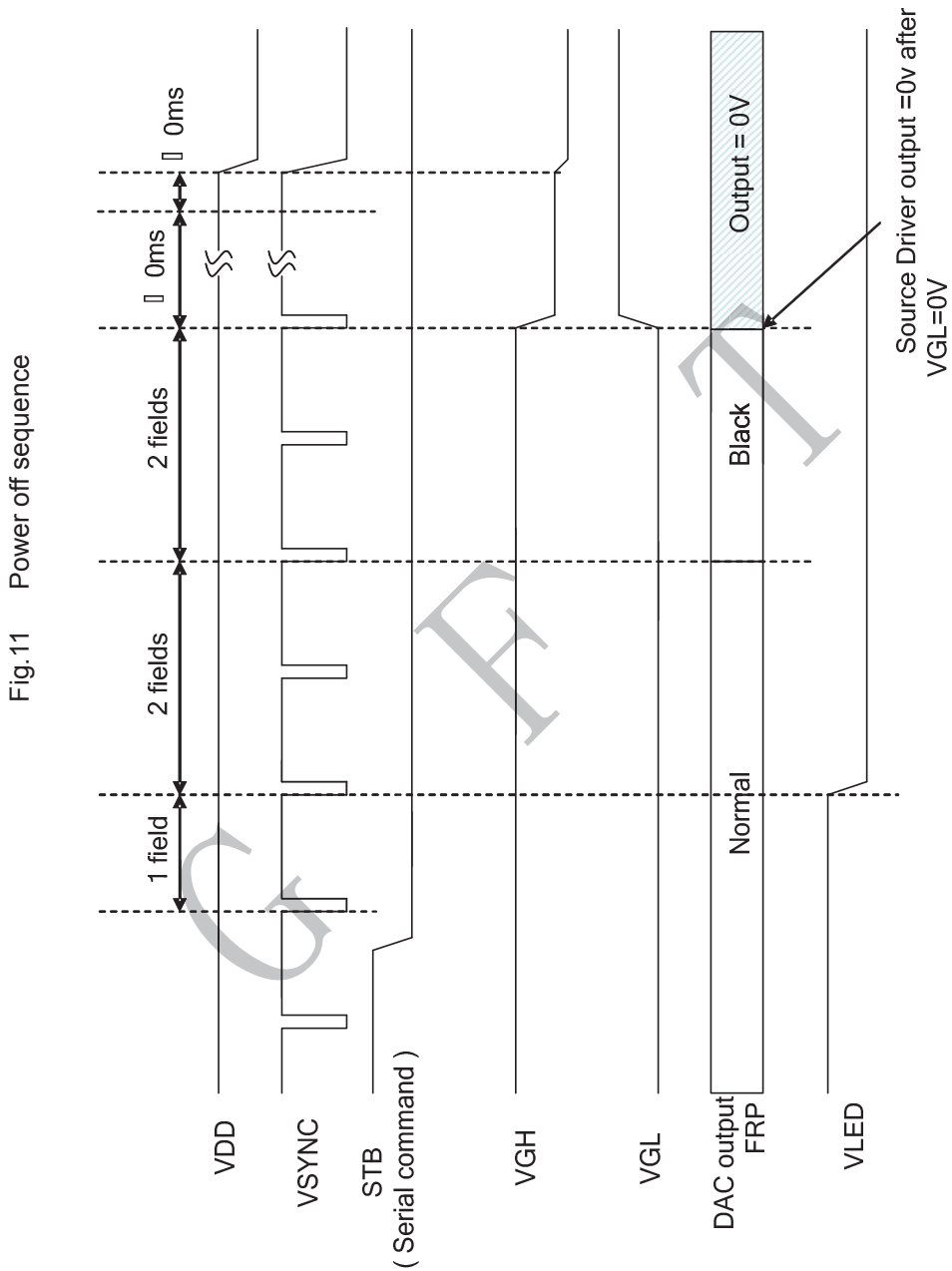
After VDD power on reset, VSYNC/HSYNC/DCLK/DATA can be input, and serial control interface is also operational. The LCD driver is in default standby mode after VDD power-on, and setting register R5: STB to '1' to disable the standby mode is required for normal operation. When the standby mode is disabled, a build-in power on sequence is started. The LCD positive and negative power supplies VGH/VGL are pumped first, and followed by the LED power VLED. Please refer to Fig.10 for the detail timing of power on sequence.

Fig.10 Power on sequence



3.2 Power off (Standby Enabling)

When the register STB is set to '0' to enable standby mode, a build-in power off sequence is started. Please refer to Fig.11 for the detail timing of power off sequence.



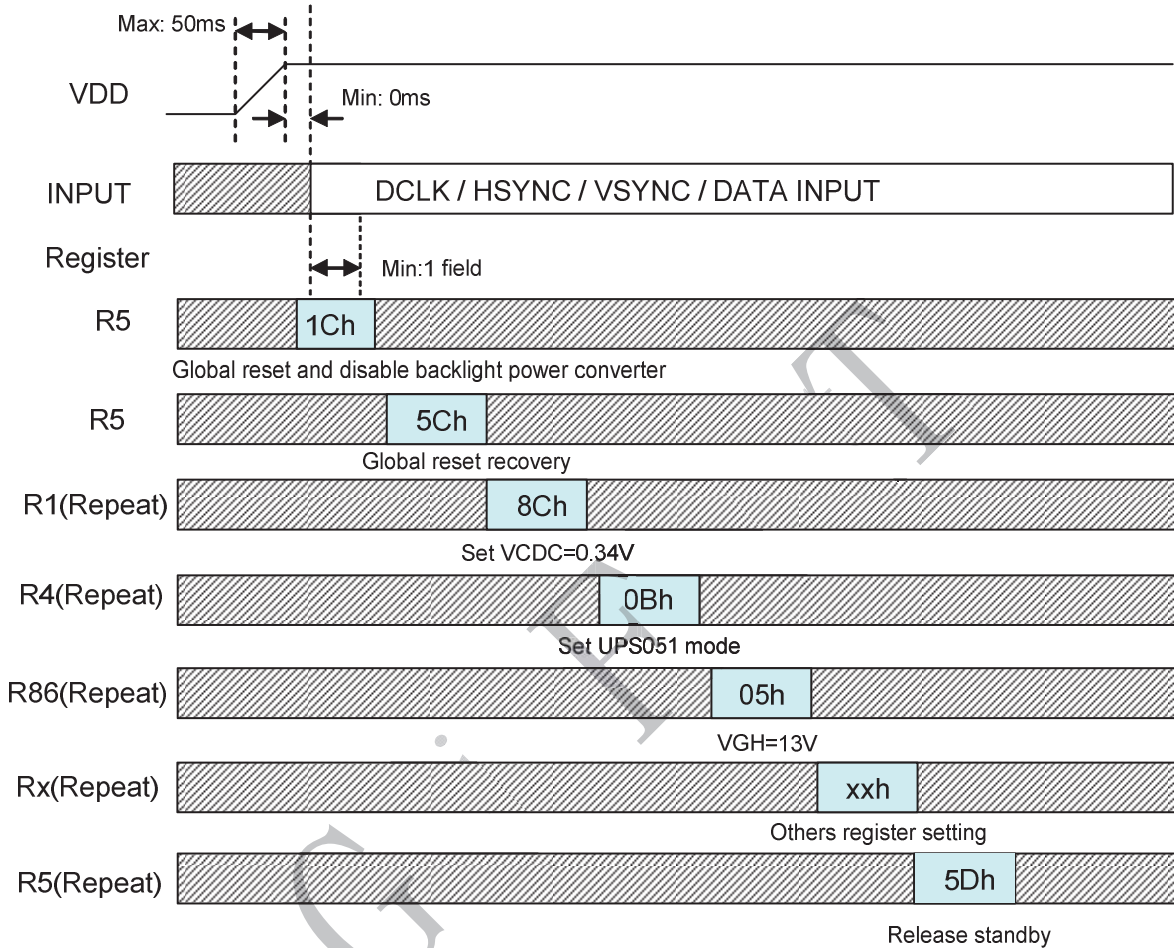


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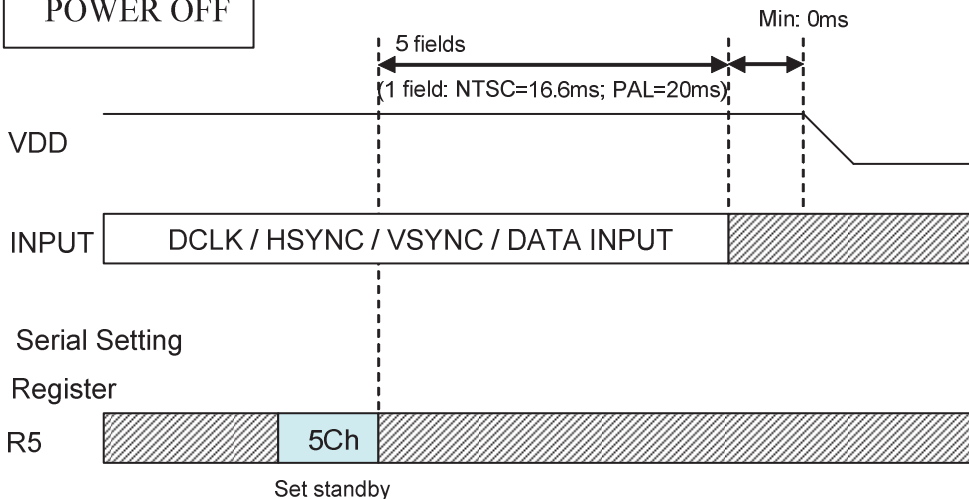
3. Recommended power on/off serial command settings

3.1 UPS051

POWER ON



POWER OFF

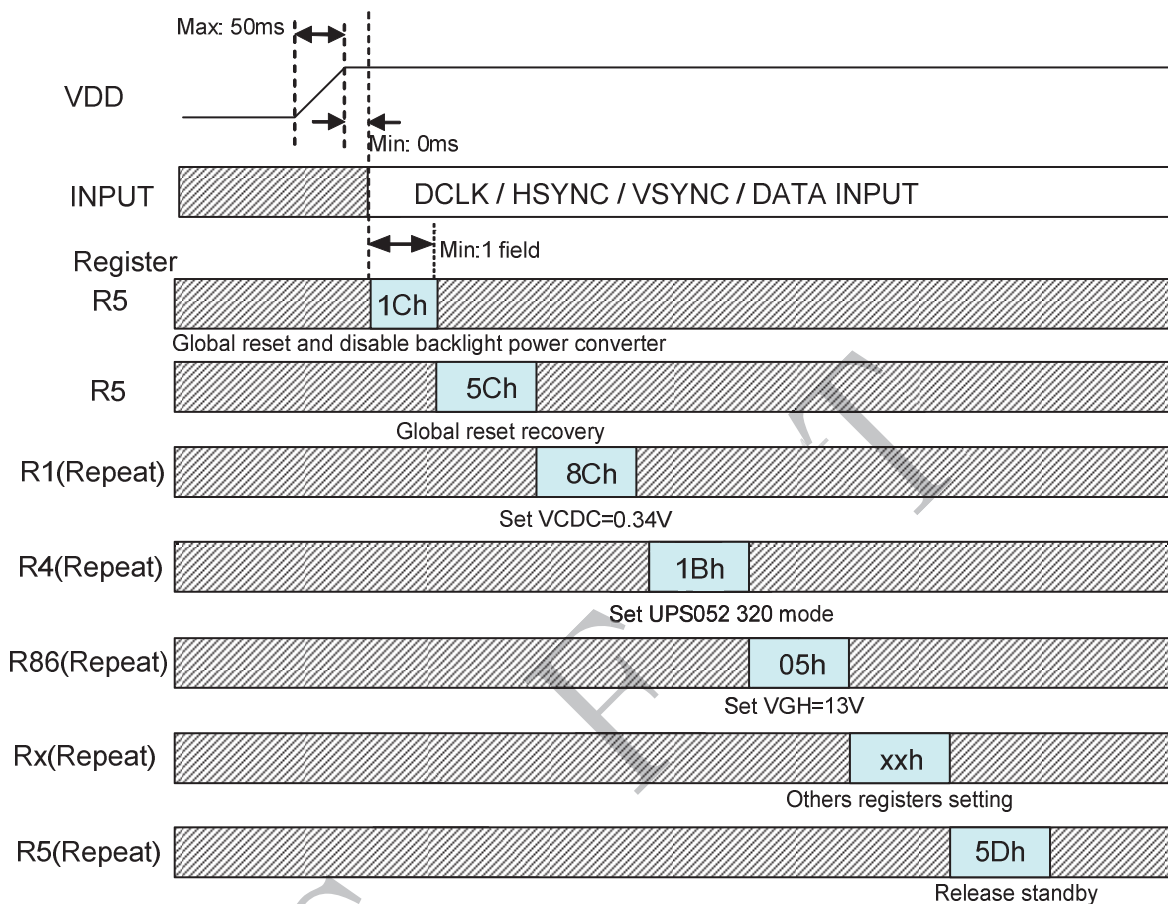




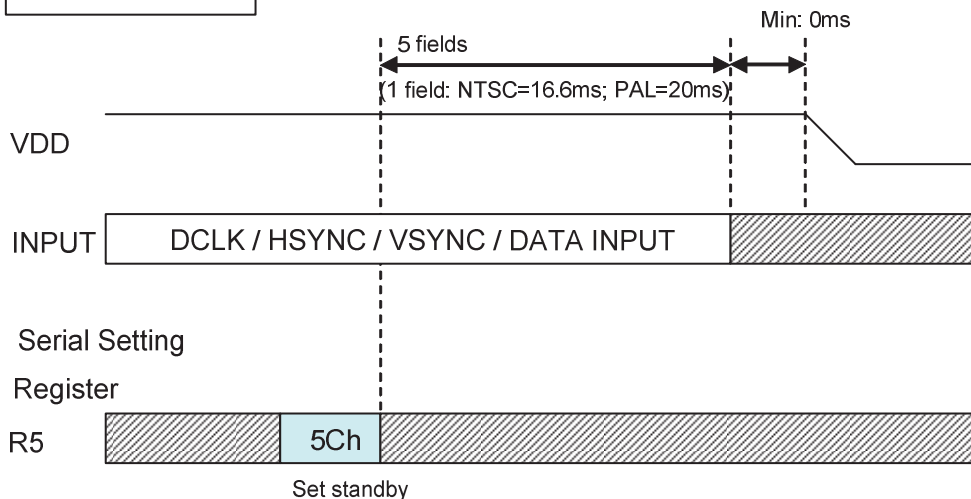
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3.2 UPS052 320 mode

POWER ON



POWER OFF

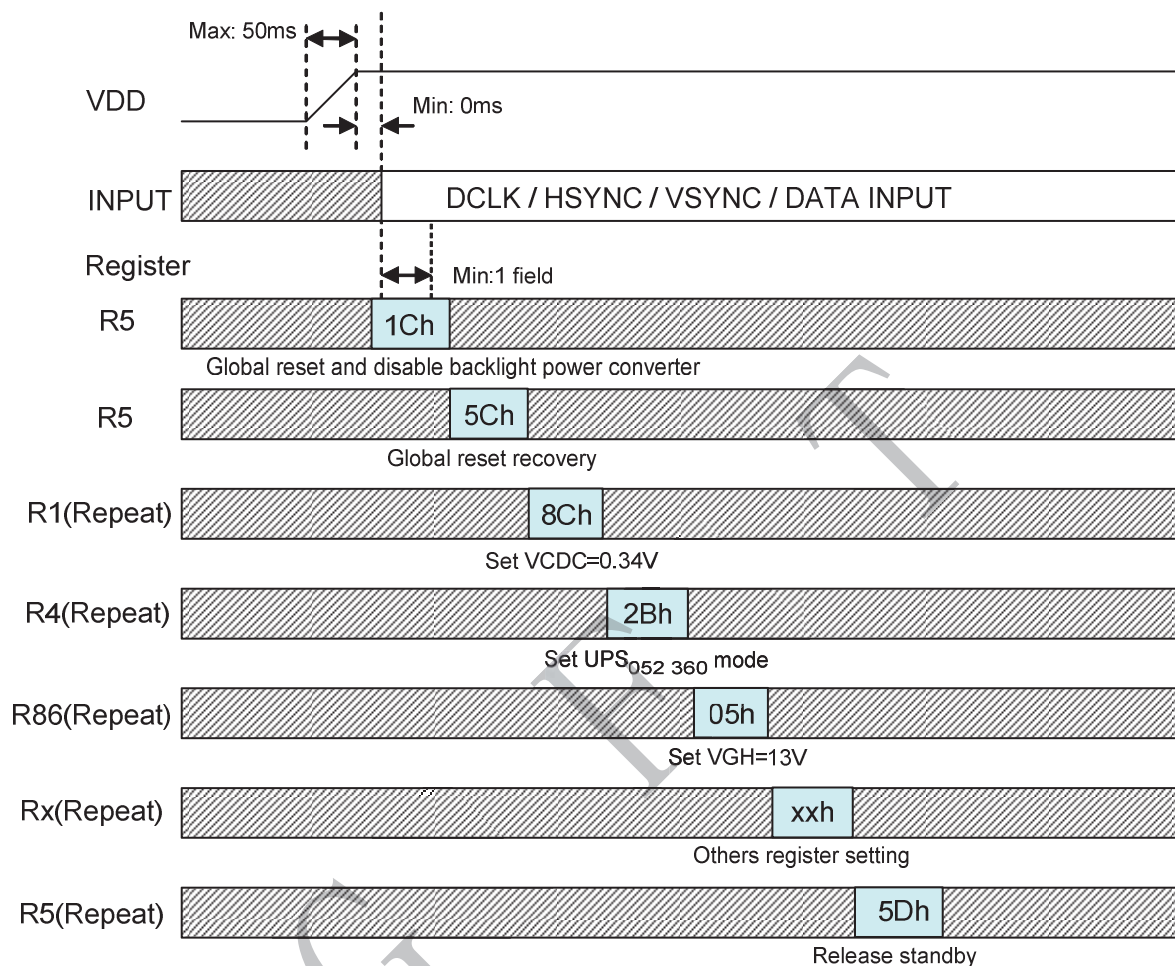




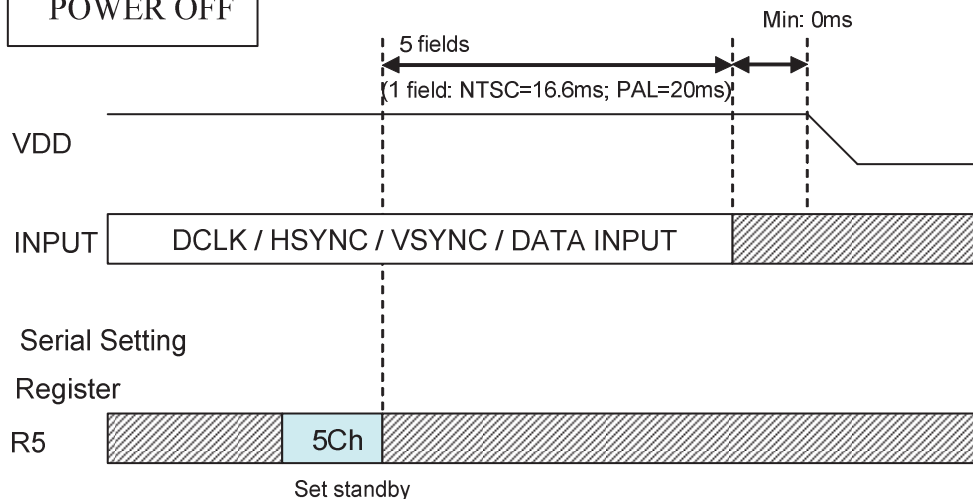
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3.3 UPS052 360 mode

POWER ON



POWER OFF

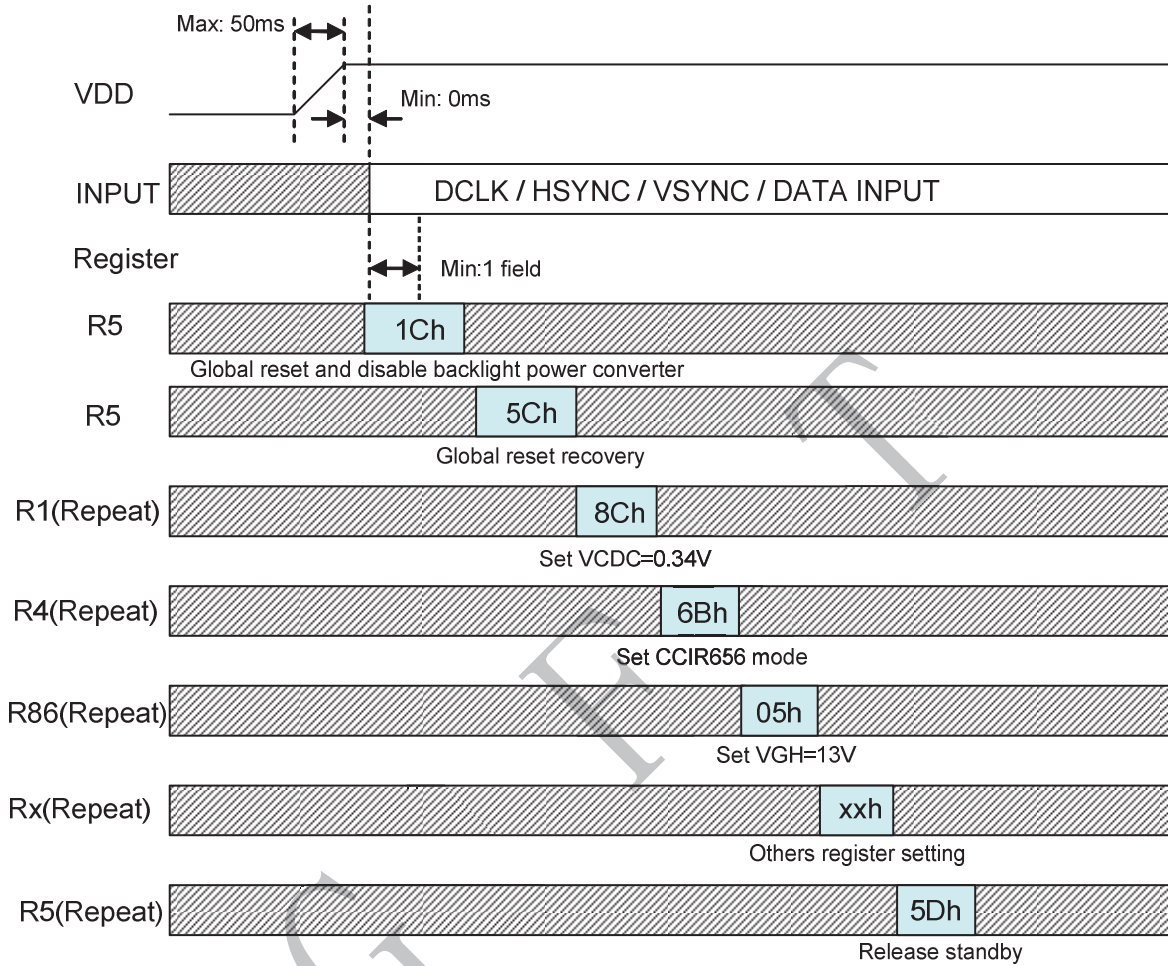




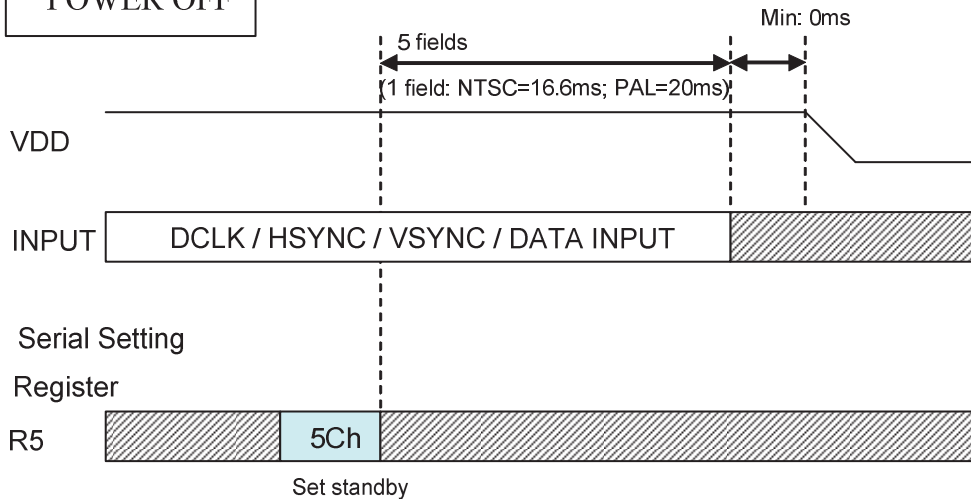
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3.4 CCIR656

POWER ON



POWER OFF

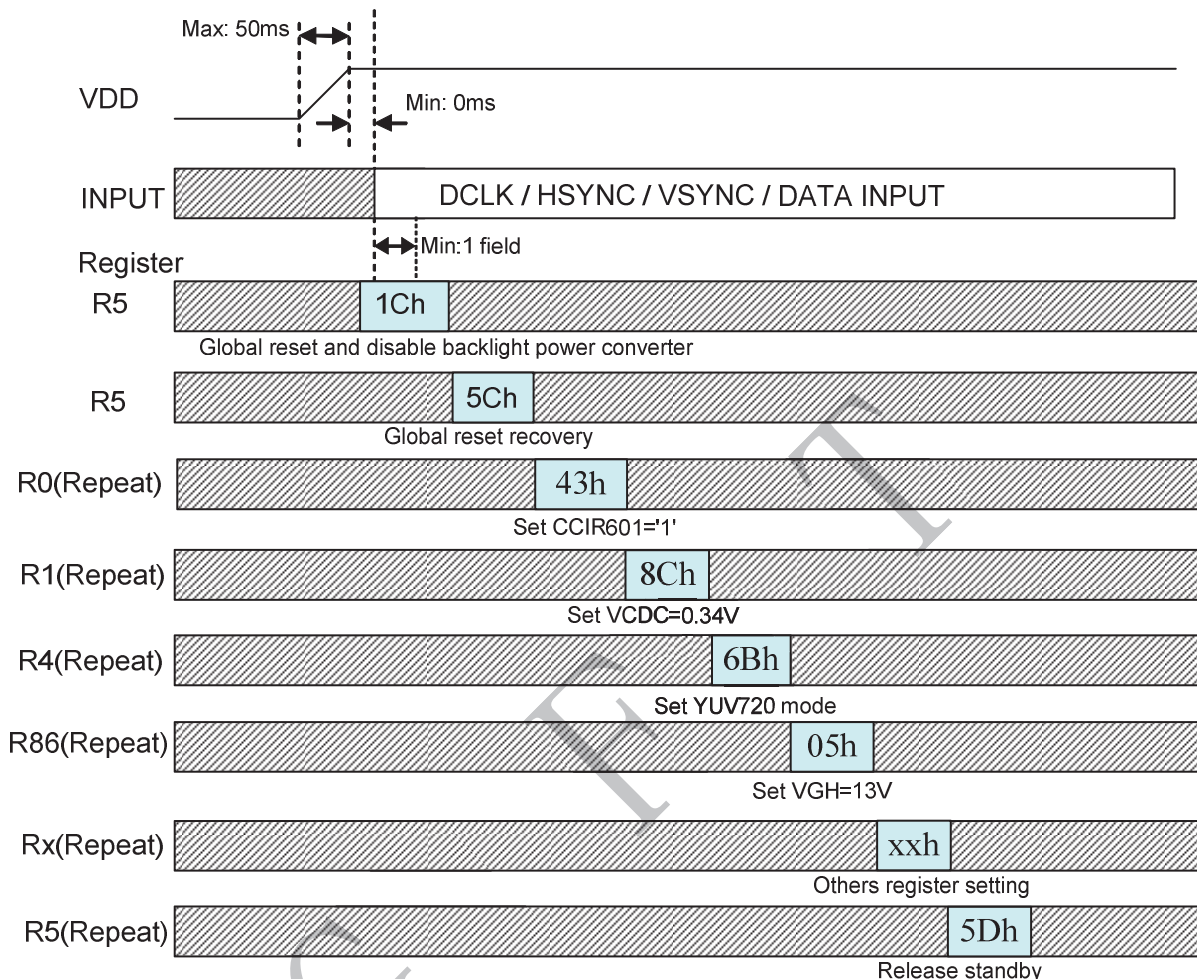




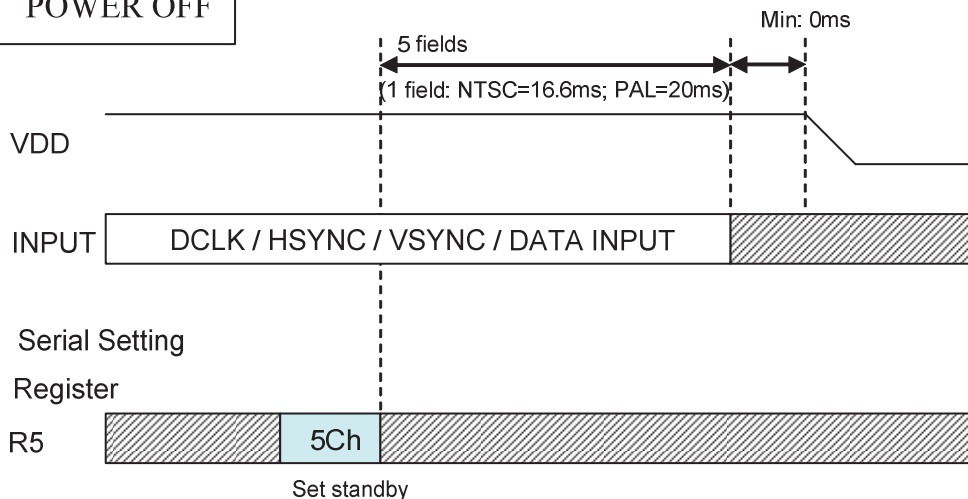
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3.5 YUV 720

POWER ON



POWER OFF

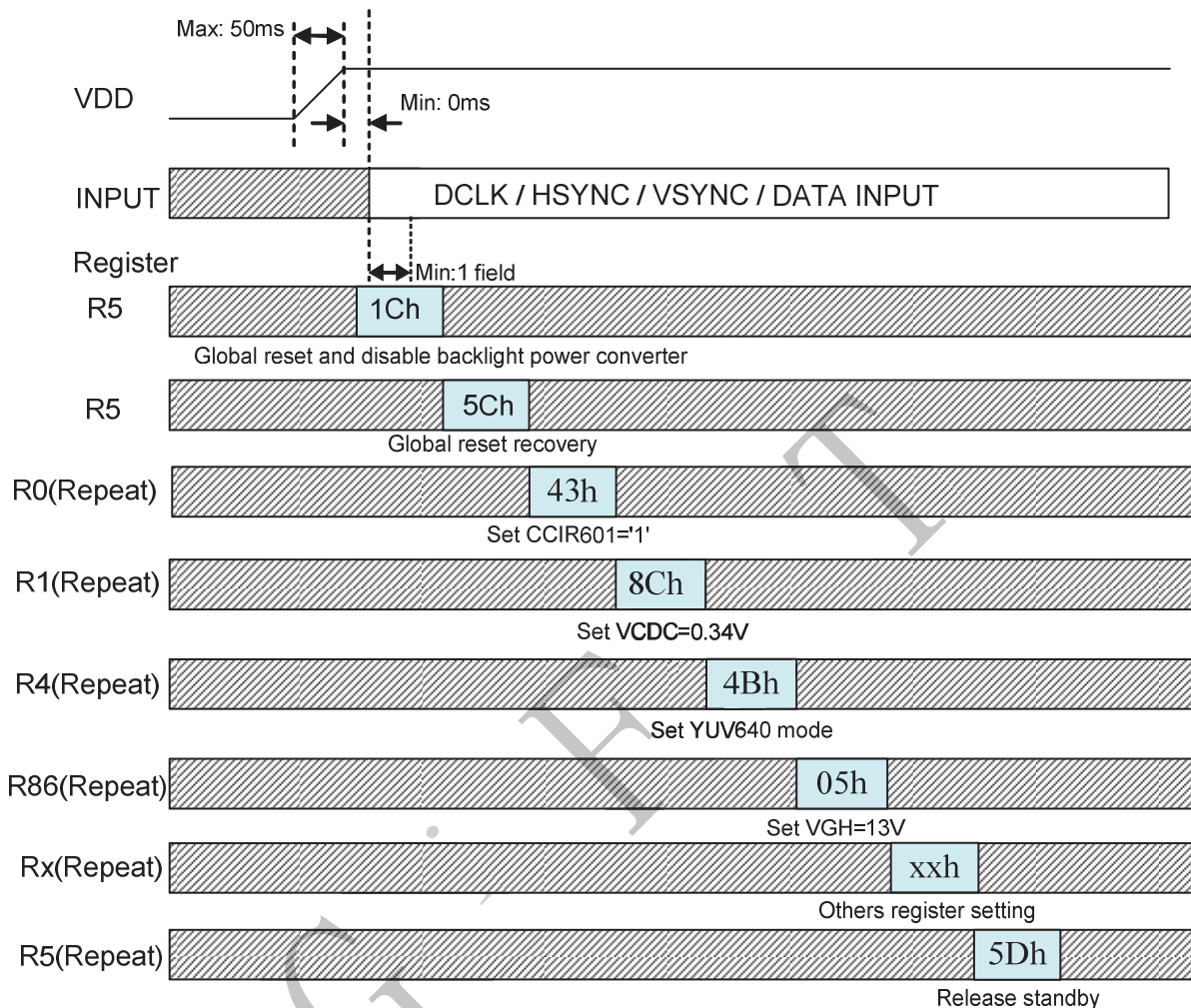




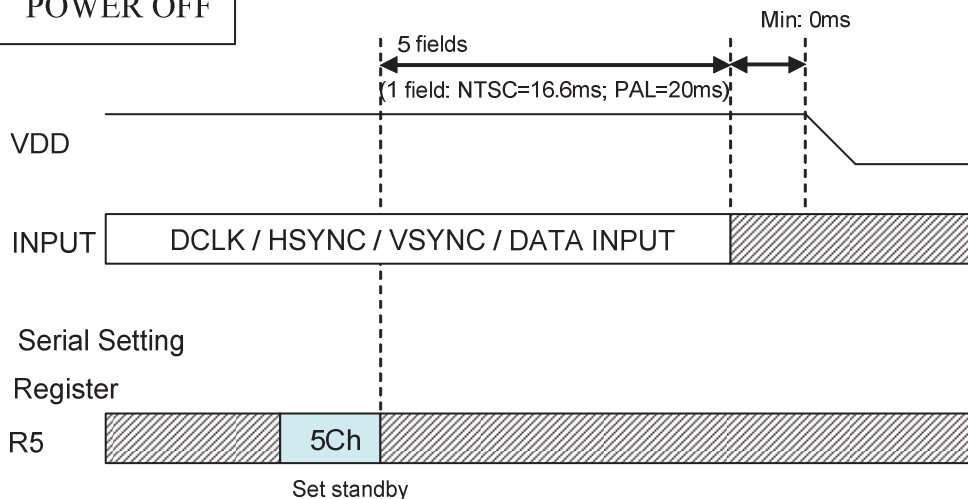
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3.6 YUV 640

POWER ON

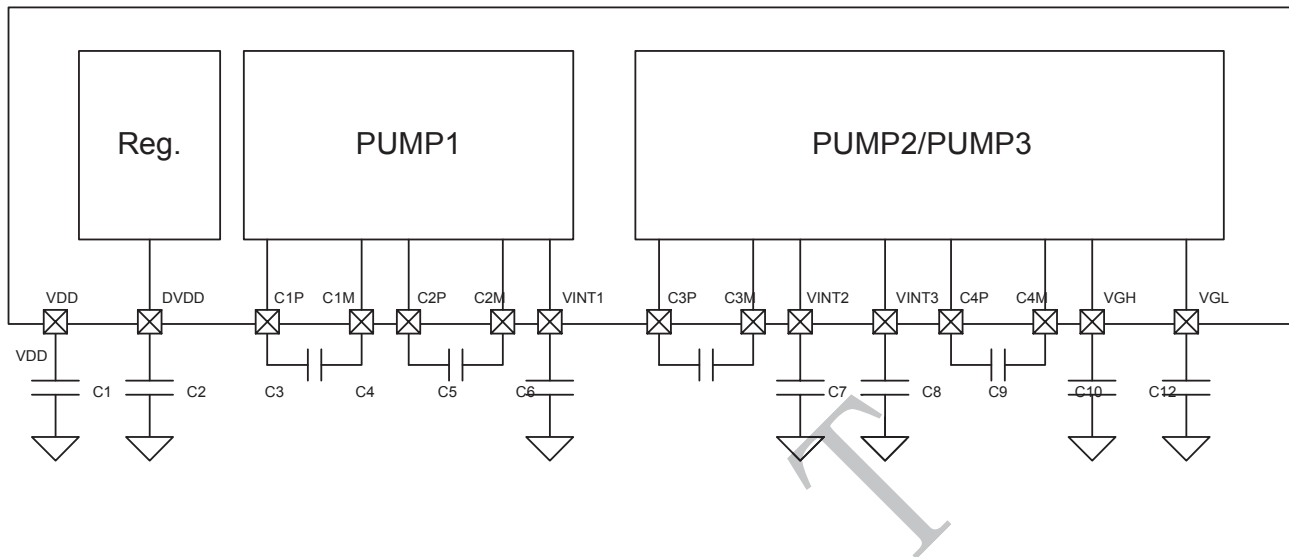


POWER OFF



4. Power generation circuit

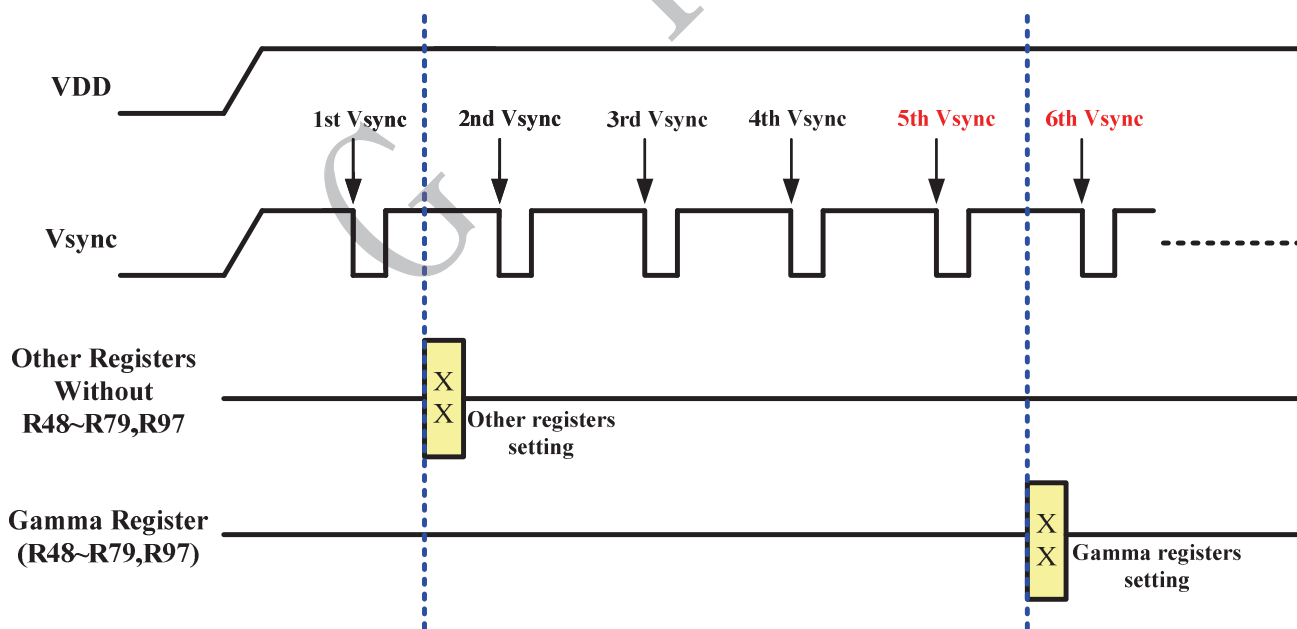
The block diagram of built-in power generation circuit for TFT-LCD supply power is shown as below:



5. Different gamma curve command setting notice

Since the LCD display is non gamma2.2 curve application, others gamma curve application must be follow Fig.12 sequence during power on. Gamma Setting must send after 5th Vsync.

Fig. 12 LCD Different gamma curve serial command setting notice



Note 1: Under different input timing, other registers setting please follow section "Recommended power on/off serial command settings".



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Gamma 2.2 Recommend Command Setting				
Register	Address	Data	Hex	Remark
R97	10100001	00000001	A101	Gamma Enable
R48	00110000	00110010	3032	Gamma+ Setting
R49	00110001	00110101	3135	
R50	00110010	00111111	323F	
R51	00110011	00001101	330D	
R52	00110100	00001100	340C	
R53	00110101	00011001	3519	
R54	00110110	00001111	360F	
R55	00110111	00000111	3707	
R56	00111000	00000010	3802	
R57	00111001	00001001	3909	
R58	00111010	00000011	3A03	
R59	00111011	00010101	3B15	
R60	00111100	00001110	3C0E	
R61	00111101	00011001	3D19	
R62	00111110	00010101	3E15	
R63	00111111	00000101	3F05	
R64	10000000	00011100	801C	Gamma- Setting
R65	10000001	00101100	812C	
R66	10000010	00110011	8233	
R67	10000011	00001110	830E	
R68	10000100	00001010	840A	
R69	10000101	00001000	8508	
R70	10000110	00001010	860A	
R71	10000111	00000011	8703	
R72	10001000	00001001	8809	
R73	10001001	00001101	890D	
R74	10001010	00010011	8A13	
R75	10001011	00001100	8B0C	
R76	10001100	00001101	8C0D	
R77	10001101	00001111	8D0F	
R78	10001110	00000011	8E03	
R79	10001111	00000000	8F00	

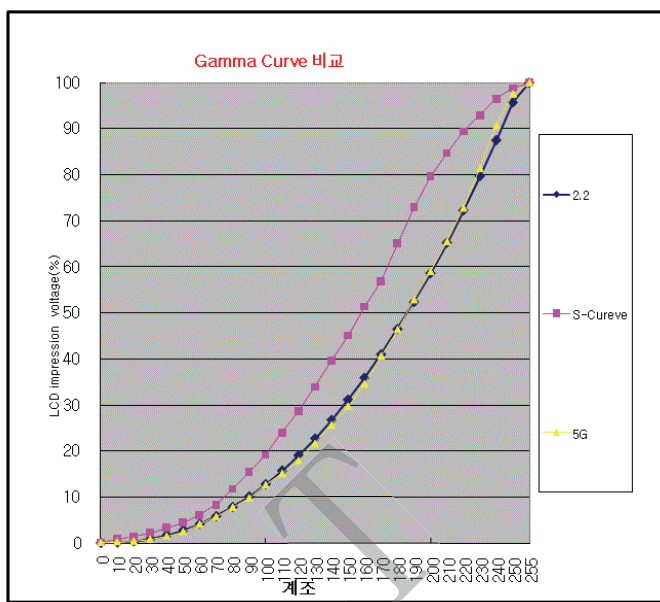


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5.1 S-Gamma setting (only reference)

2. Brightness and Gamma and Contrast Test

Gray Level	휘도		Gamma		
	S-Cureve	5G	S-Cureve	5G	2.2
0	0.30	0.30	0.12	0.12	0.00
10	2.22	0.58	0.87	0.24	0.08
20	3.61	1.01	1.42	0.41	0.37
30	5.67	2.03	2.22	0.83	0.90
40	8.47	3.62	3.32	1.47	1.70
50	11.50	6.00	4.51	2.44	2.78
60	15.60	10.00	6.12	4.07	4.15
70	21.30	14.00	8.35	5.69	5.82
80	30.00	19.00	11.76	7.72	7.81
90	39.30	24.00	15.41	9.76	10.11
100	48.90	31.00	19.18	12.60	12.75
110	61.20	37.00	24.00	15.04	15.73
120	73.00	44.00	28.63	17.89	19.05
130	86.50	53.00	33.92	21.54	22.71
140	101.00	63.00	39.61	25.61	26.74
150	115.00	73.00	45.10	29.67	31.12
160	131.00	85.00	51.37	34.55	35.87
170	145.00	100.00	56.86	40.65	40.98
180	166.00	114.00	65.10	46.34	46.47
190	186.00	130.00	72.94	52.85	52.34
200	203.00	145.00	79.61	58.94	58.60
210	216.00	161.00	84.71	65.45	65.24
220	228.00	173.00	89.41	72.76	72.27
230	237.00	200.00	92.94	81.90	79.69
240	246.00	223.00	96.47	90.65	87.51
250	252.00	240.00	98.82	97.56	95.74
255	255.00	246.00	100.00	100.00	100.00
Contrast	850.0	820.0			



Note : Since S Gamma is out of IC support range, please modify VcomDC = 0.56V setting, before sending S-Gamma command to have better performance.

SEC S-Gamma Recommend Command Setting				
Register	Address	Data	Hex	Remark
R1	00000001	10010111	0193	VcomDC = 0.56V
R97	10100001	00000001	A101	Gamma Enable
R48	00110000	00100010	3022	Gamma+ Setting
R49	00110001	00110100	3134	
R50	00110010	00111110	323E	
R51	00110011	00001111	330F	
R52	00110100	00001110	340E	
R53	00110101	00010110	3516	
R54	00110110	00001101	360D	
R55	00110111	00001000	3708	
R56	00111000	00000010	3802	
R57	00111001	00001010	390A	
R58	00111010	00000110	3A06	
R59	00111011	00010010	3B12	
R60	00111100	00010000	3C10	
R61	00111101	00011000	3D18	
R62	00111110	00010010	3E12	
R63	00111111	00010000	3F10	



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R64	10000000	00010010	8012	Gamma- Setting
R65	10000001	00011010	811A	
R66	10000010	00100010	8222	
R67	10000011	00001011	830B	
R68	10000100	00001010	840A	
R69	10000101	00001010	850A	
R70	10000110	00001011	860B	
R71	10000111	00000100	8704	
R72	10001000	00000110	8806	
R73	10001001	00001101	890D	
R74	10001010	00010000	8A10	
R75	10001011	00001110	8B0E	
R76	10001100	00001111	8C0F	
R77	10001101	00011110	8D1E	
R78	10001110	00010010	8E12	
R79	10001111	00000000	8F00	

F

G