

# FDMC15N06

## N-Channel MOSFET

### 55V, 15A, 0.090Ω

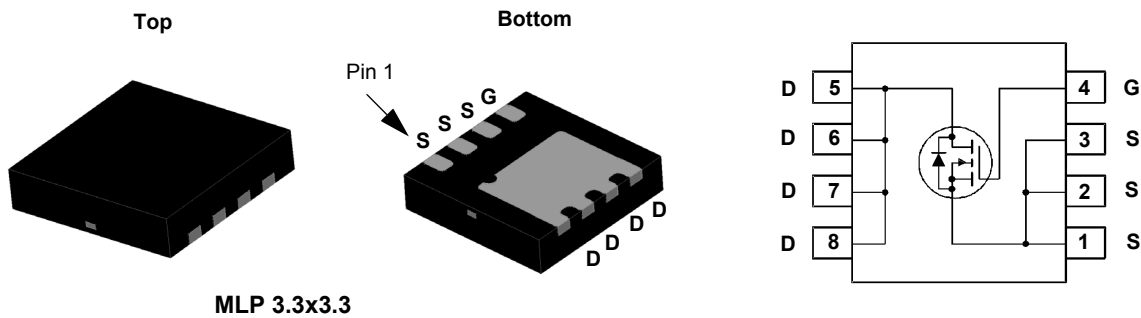
#### Features

- $R_{DS(on)} = 0.075\Omega$  (Typ.) @  $V_{GS} = 10V, I_D = 15A$
- 100% Avalanche Tested
- RoHS Compliant



#### Description

These N-Channel power MOSFETs are manufactured using the innovative UltraFET process. This advanced process technology achieves the lowest possible on-resistance per silicon area, resulting in outstanding performance. This device is capable of withstanding high energy in the avalanche mode and the diode exhibits very low reverse recovery time and stored charge. It was designed for use in applications where power efficiency is important, such as switching regulators, switching converters, motor drivers, relay drivers, low-voltage bus switches, and power management in portable and battery-operated products.



#### MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DSS}$	Drain to Source Voltage	55	V
$V_{GSS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current	-Continuous ( $T_C = 25^\circ\text{C}$ )	15
		-Continuous ( $T_C = 100^\circ\text{C}$ )	9
		-Continuous ( $T_A = 25^\circ\text{C}$ ) (Note 1a)	2.4
$I_{DM}$	Drain Current	- Pulsed (Note 2)	60
$E_{AS}$	Single Pulsed Avalanche Energy	(Note 3)	36
$I_{AR}$	Avalanche Current		15
$E_{AR}$	Repetitive Avalanche Energy		3.5
$P_D$	Power Dissipation	( $T_C = 25^\circ\text{C}$ )	35
		( $T_A = 25^\circ\text{C}$ )	2.3
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

#### Thermal Characteristics

Symbol	Parameter	Ratings	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case	3.5	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	

## Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC15N06	FDMC15N06	Power 33	13"	12mm	3000 units

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}, T_C = 25^\circ\text{C}$	55	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$ , Referenced to $25^\circ\text{C}$	-	70	-	$\text{V}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 50\text{V}, V_{GS} = 0\text{V}$ $V_{DS} = 45\text{V}, T_C = 150^\circ\text{C}$	-	-	1 250	$\mu\text{A}$
$I_{GSS}$	Gate to Body Leakage Current	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$	-	-	$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	2.0	-	4.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{V}, I_D = 15\text{A}$	-	0.75	0.90	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 20\text{V}, I_D = 15\text{A}$	-	5	-	S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{V}, V_{GS} = 0\text{V}$ $f = 1\text{MHz}$	-	265	350	pF
$C_{oss}$	Output Capacitance		-	97	130	pF
$C_{rss}$	Reverse Transfer Capacitance		-	28	42	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 30\text{V}, I_D = 15\text{A}$ $V_{GS} = 10\text{V}$	-	8.8	11.5	nC
$Q_{gs}$	Gate to Source Gate Charge		-	1.7	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge		-	3.6	-	nC

### Switching Characteristics

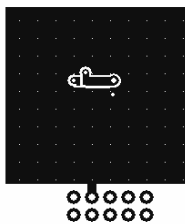
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 30\text{V}, I_D = 15\text{A}$ $R_G = 25\Omega$	-	9.5	29	ns
$t_r$	Turn-On Rise Time		-	36.5	83	ns
$t_{d(off)}$	Turn-Off Delay Time		-	22.5	55	ns
$t_f$	Turn-Off Fall Time		-	22	54	ns

### Drain-Source Diode Characteristics

$I_S$	Maximum Continuous Drain to Source Diode Forward Current	-	-	15	A	
$I_{SM}$	Maximum Pulsed Drain to Source Diode Forward Current	-	-	60	A	
$V_{SD}$	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{V}, I_{SD} = 15\text{A}$	-	-	1.25	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{V}, I_{SD} = 15\text{A}$	-	30	-	ns
$Q_{rr}$	Reverse Recovery Charge	$dI_F/dt = 100\text{A}/\mu\text{s}$	-	35	-	nC

Notes:

1:  $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a. 53 °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b. 125 °C/W when mounted on a minimum pad of 2 oz copper

2: Repetitive Rating: Pulse width limited by maximum junction temperature

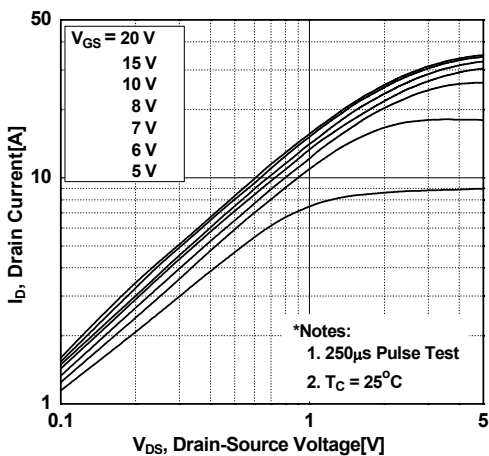
3:  $L = 1\text{mH}, I_{AS} = 8.5\text{A}, R_G = 25\Omega$ , Starting  $T_J = 25^\circ\text{C}$

4: Essentially Independent of Operating Temperature Typical Characteristics

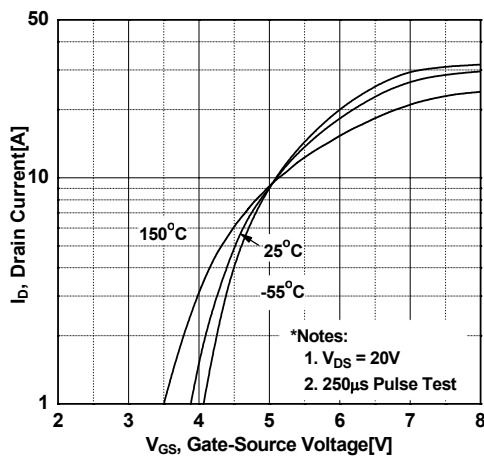
5:  $I_{SD} \leq 15\text{A}, di/dt \leq 200\text{A}/\mu\text{s}, V_{DD} \leq 40\text{V}$ , Starting  $T_J = 25^\circ\text{C}$

## Typical Performance Characteristics

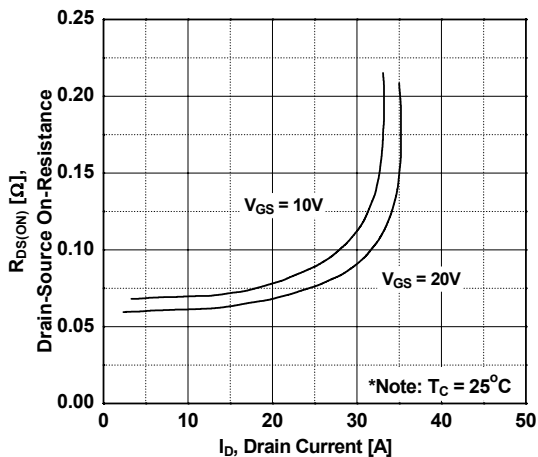
**Figure 1. On-Region Characteristics**



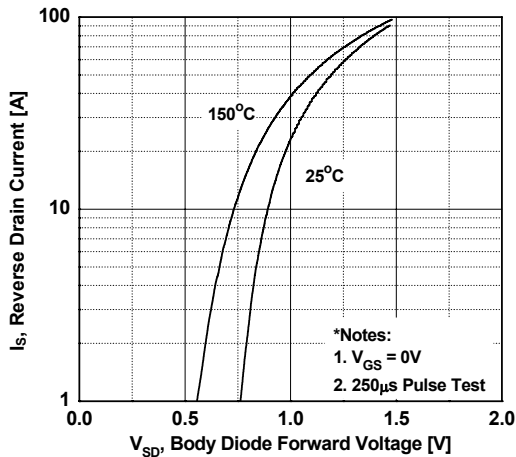
**Figure 2. Transfer Characteristics**



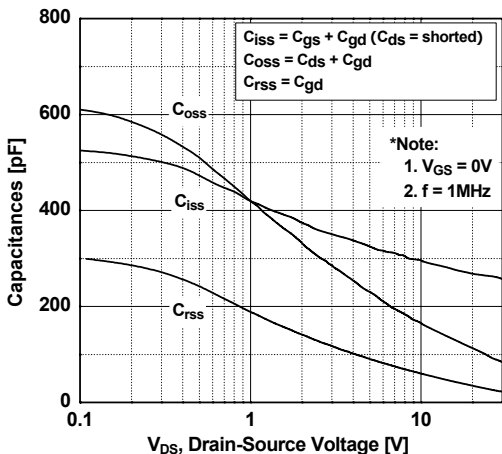
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



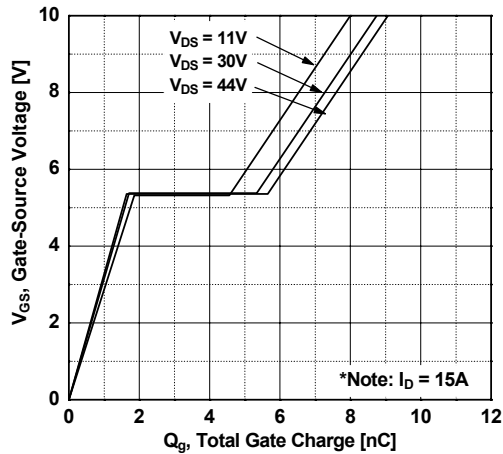
**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**



**Figure 5. Capacitance Characteristics**

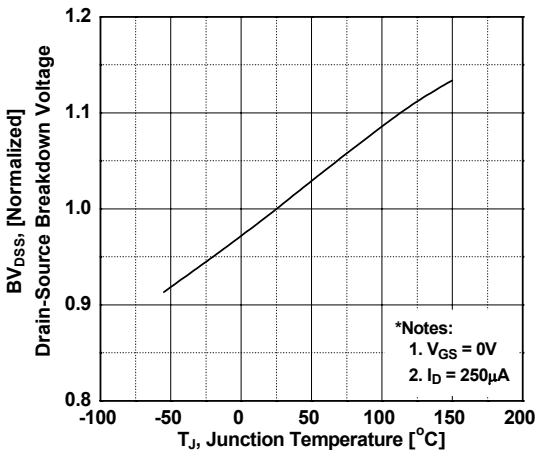


**Figure 6. Gate Charge Characteristics**

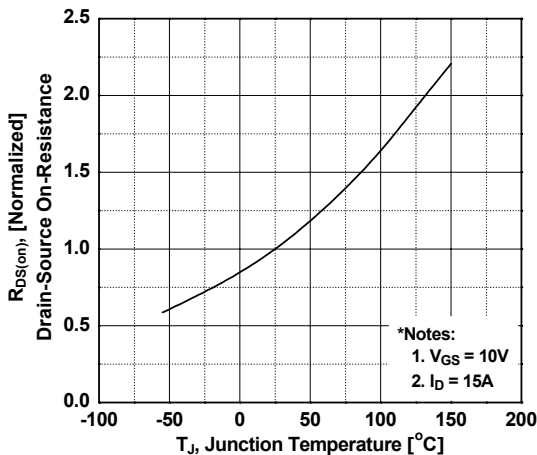


**Typical Performance Characteristics** (Continued)

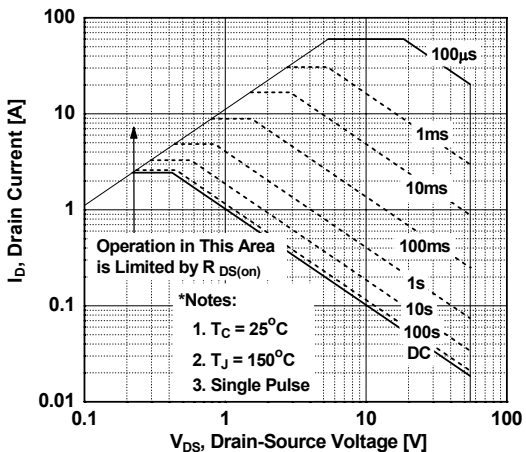
**Figure 7. Breakdown Voltage Variation vs. Temperature**



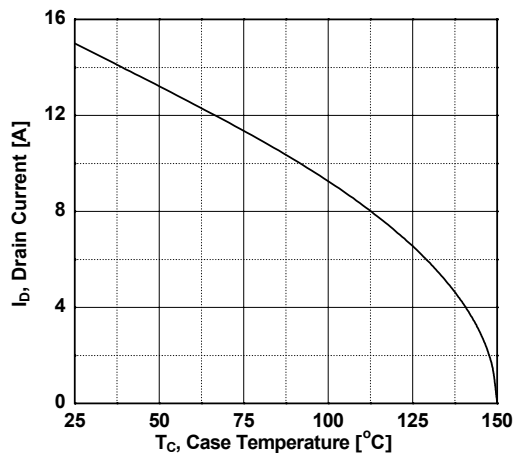
**Figure 8. On-Resistance Variation vs. Temperature**



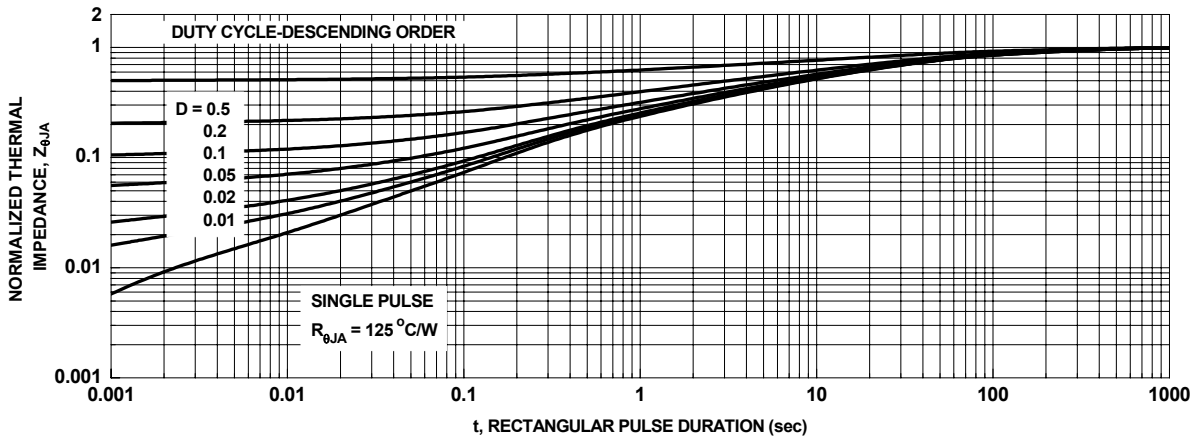
**Figure 9. Maximum Safe Operating Area**



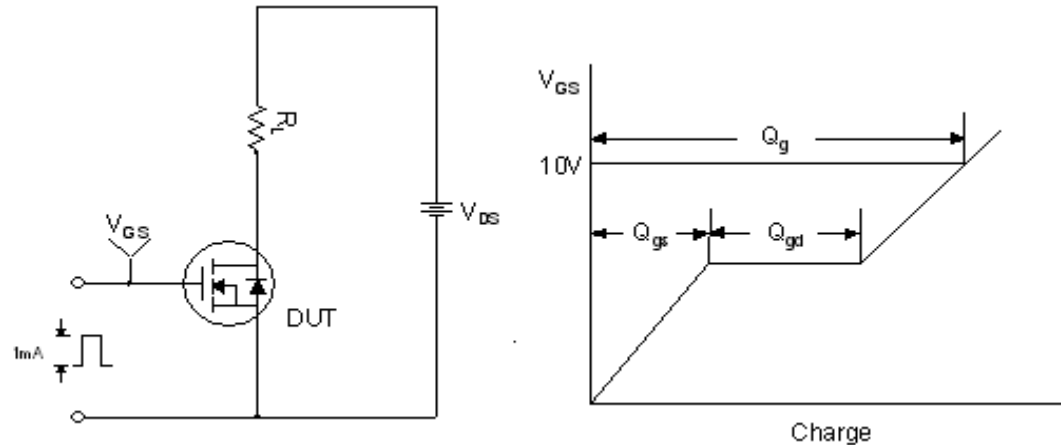
**Figure 10. Maximum Drain Current vs. Case Temperature**



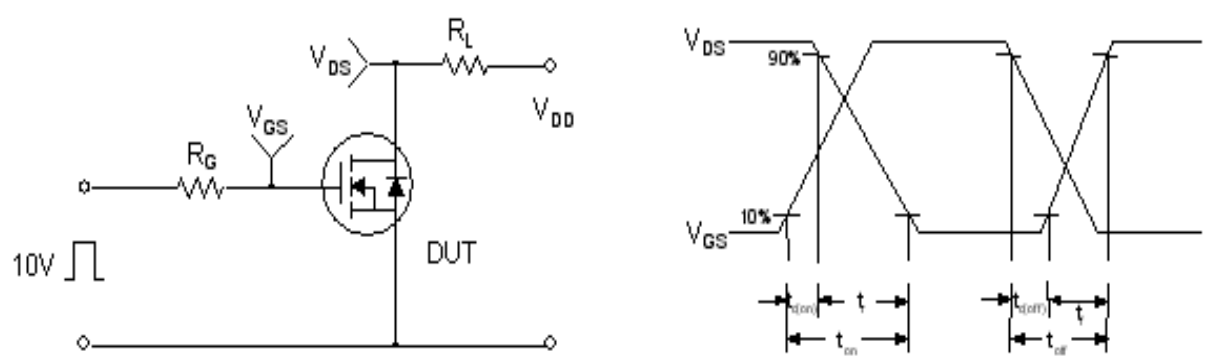
**Figure 11. Transient Thermal Response Curve**



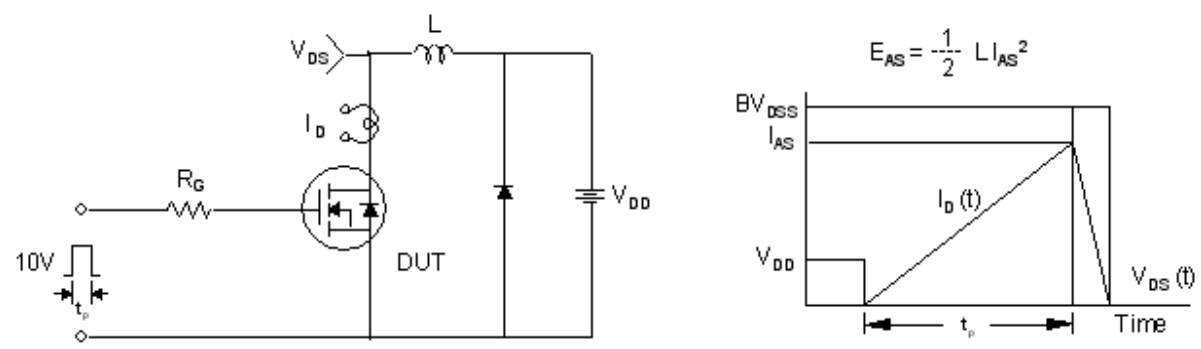
**Gate Charge Test Circuit & Waveform**



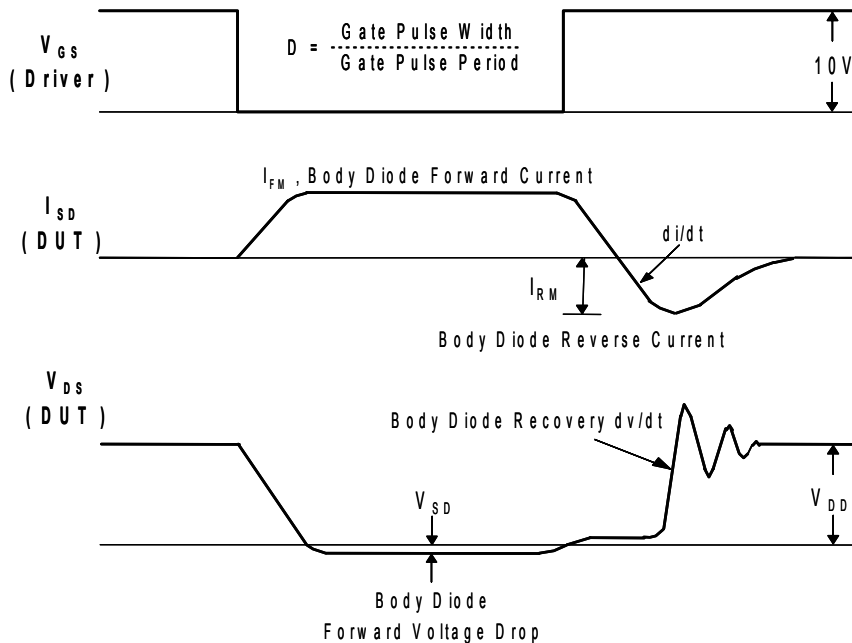
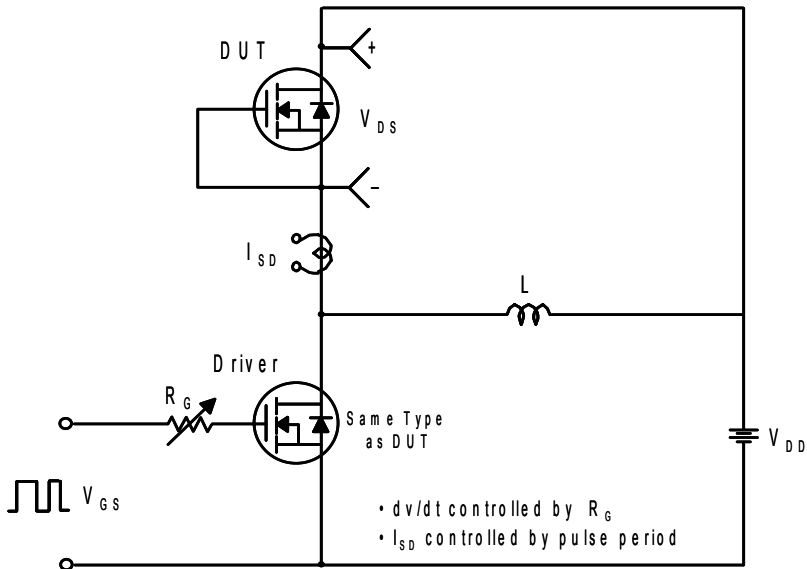
**Resistive Switching Test Circuit & Waveforms**



**Unclamped Inductive Switching Test Circuit & Waveforms**



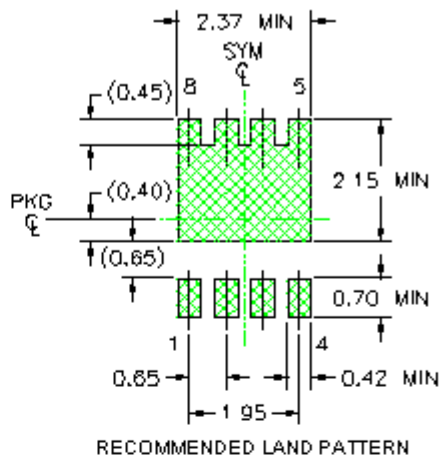
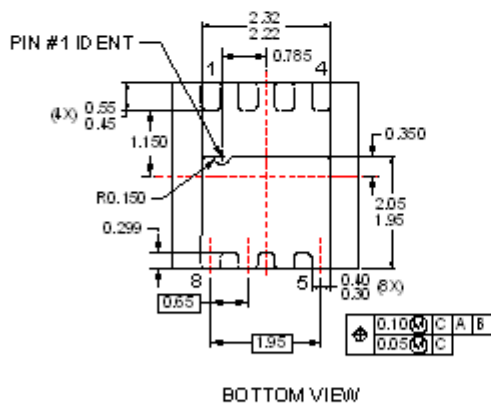
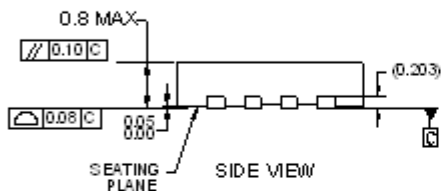
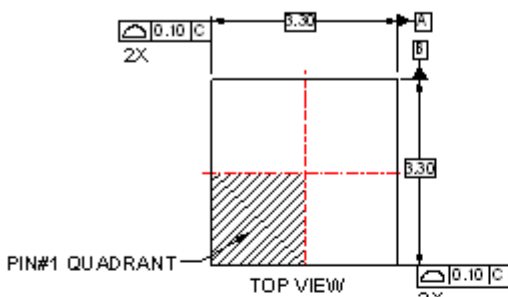
Peak Diode Recovery dv/dt Test Circuit & Waveforms



## Dimensional Outline and Pad Layout

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